



## SRS Circle SurroundII5.1 & Passive Matrix TruSurround HD/HD4XT Decoder

### ■ Package



**NJU26150-19A**

### ■ General Description

The NJU26150-19A is a digital signal processor that provides the function of Circle SurroundII5.1 / TruSurround HD/HD4.

The NJU26150-19A processes the stereo matrix-encoded signal into spacious sound of 5.1 channels by Circle SurroundII5.1. Also non matrix-encoded audio signal can be processed into effective spacious sound.

The NJU26150-19A is also possible surround sound reproduction by Passive Matrix TruSurround HD/HD4 technology, even if it is not only the independent 5.1ch speaker configuration but also the front speaker configuration.

### ■ FEATURES

#### - Software

- 5.1-Channel signal outputs by SRS Circle Surround II 5.1
- Front Multi channel outputs by SRS TruSurround HD/ TruSurround HD4
- Input : Lt/Rt only TruSurround HD(2ch to 3.1ch outputs), TruSurround HD4(4ch to 5.1ch outputs)
- Mono-to-Stereo function
- LFE by SRS TruBass /TruBass-II
- SRS Focus and Dialog Clarity
- SRS Definition
- The sampling rate is fixed with 48KHz.
- Master Volume
- WatchDog Clock Output

#### - Hardware

- 24bit Fixed-point Digital Signal Processing
- Maximum System Clock Frequency : 38MHz Max.
- Digital Audio Interface : 2 Input ports / 3 Output ports
- Digital Audio Format : I<sup>2</sup>S 24bit, Left- justified, Right-justified, Output bit is fixed 16bits. BCK:32/64fs
- Master / Slave Mode : Master Mode MCK 1/2 fclk, 1/3 fclk  
ex. MCK = 384Fs(1/2) or MCK = 256Fs(1/3) at fclk=768Fs
- Power Supply : 2.5V
- Input terminal : 3.3V Input tolerant
- Package : QFP32-R1 (Pb-Free)
- Host interface : I<sup>2</sup>C bus (standard-mode/100kbps)

The detail hardware specification is described in the "NJU26150 Series Hardware Data Sheet".

# NJU26150-19A

## Function Block Diagram

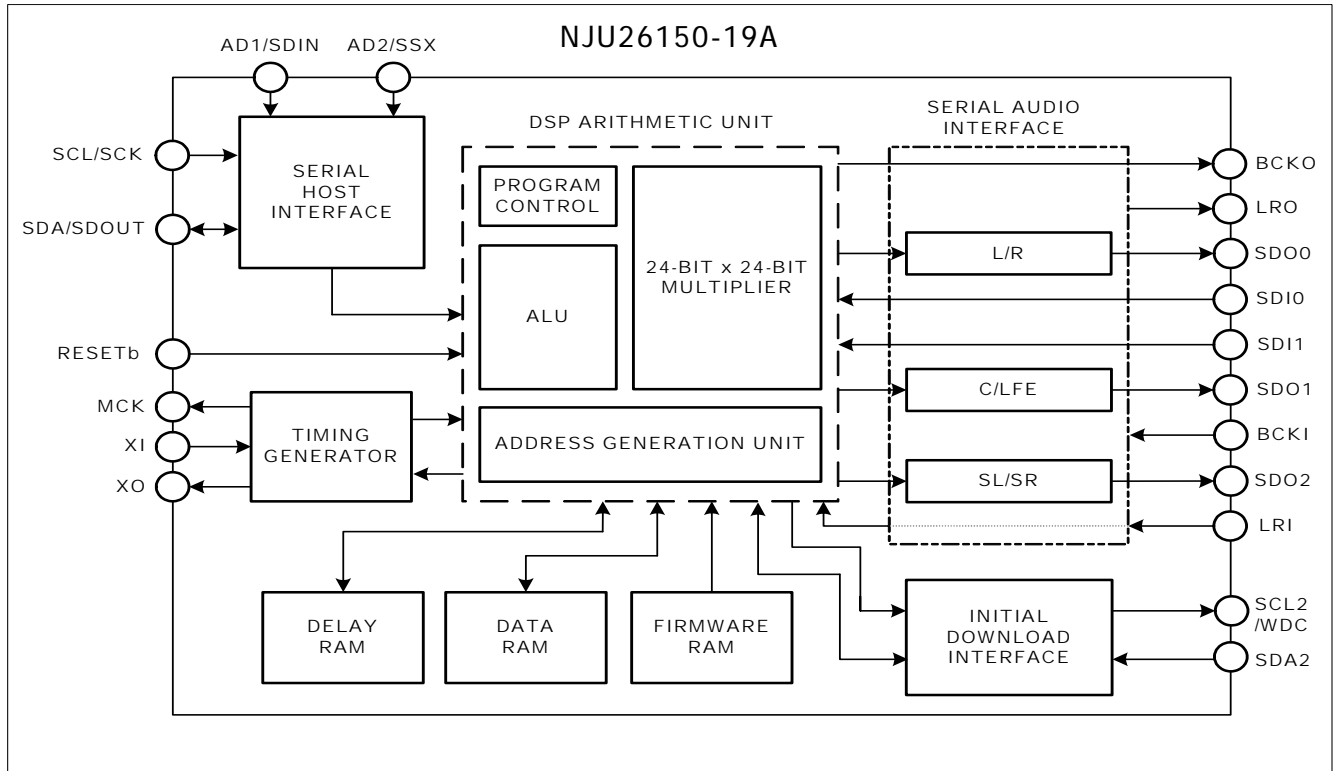


Fig. 1 NJU26150-19A Block Diagram

## DSP Block Diagram

NJU26150-19A Top Level Block Diagram

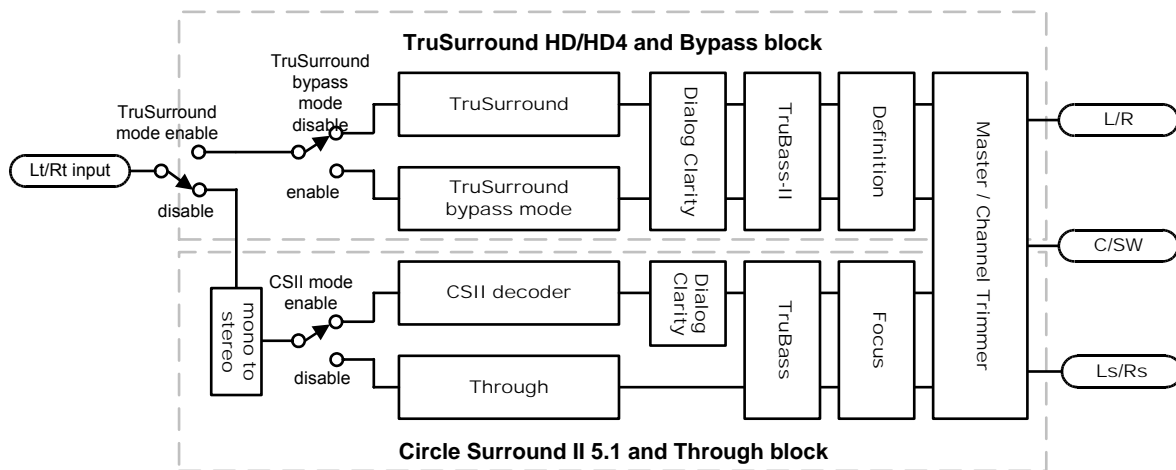


Fig. 2 NJU26150-19A Top Level Function Diagram

TruSurround HD/HD4 and Bypass mode Block Diagram

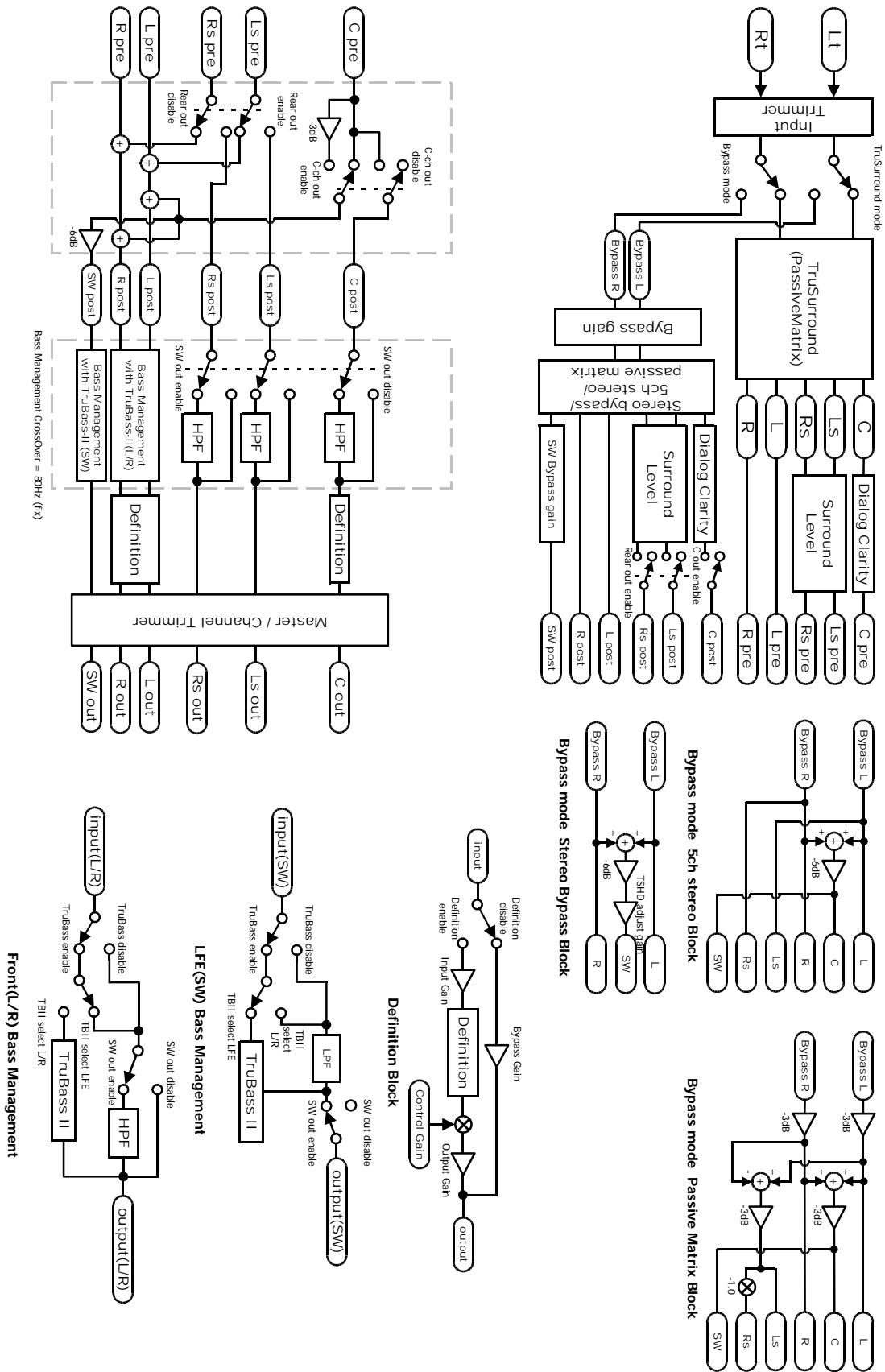


Fig. 3 NJU26150-19A (TruSurround HD/HD4 Mode) Function Diagram

## Circle Surround II 5.1 mode / Through Mode

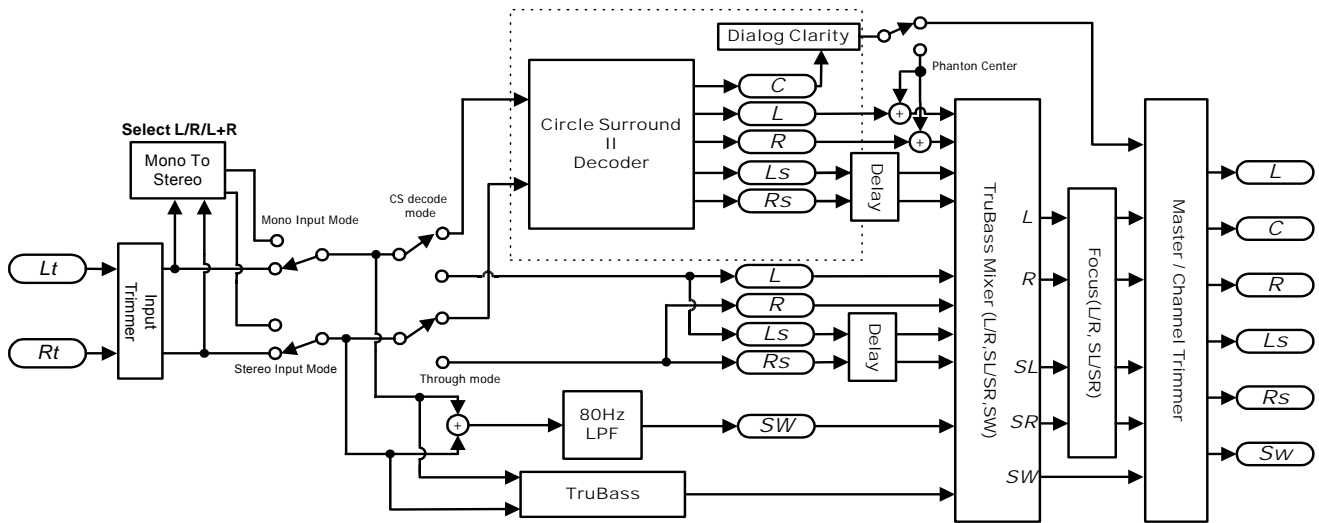


Fig. 4 NJU26150-19A (CSII5.1/Through Mode) Function Diagram

## Pin Configuration

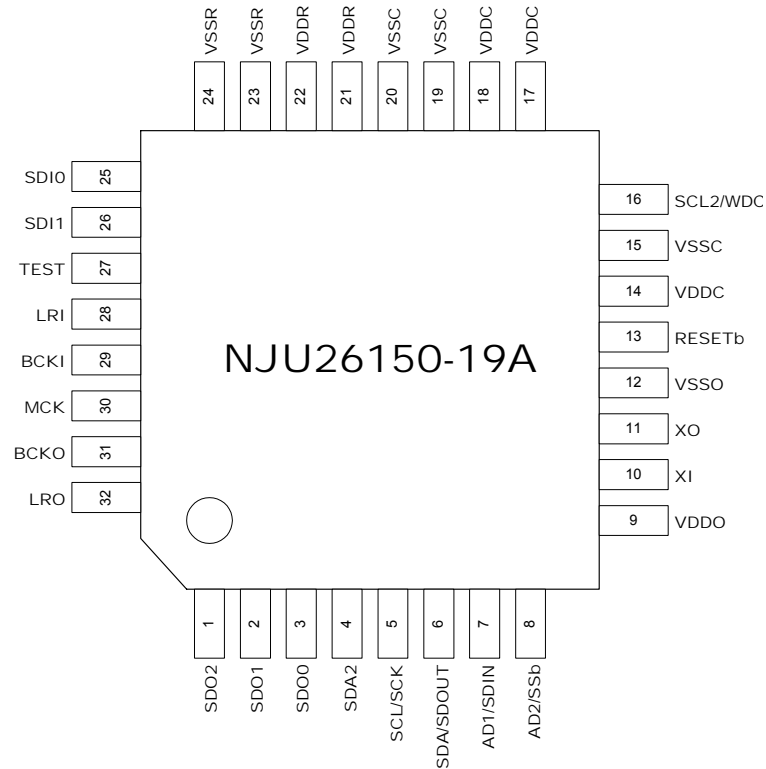


Fig. 5 NJU26150-19A Pin Configuration

## Pin Description

Table 1 Pin Description

No.	Symbol	I/O	Description
1	SDO2	O	Audio Data Output 2
2	SDO1	O	Audio Data Output 1
3	SDO0	O	Audio Data Output 0
4	SDA2	I/O	Select I <sup>2</sup> C (For program down load) This pin requires a pull-up resistance.
5	SCL	I	I <sup>2</sup> C Clock
6	SDA	I/O	I <sup>2</sup> C I/O This pin requires a pull-up resistance.
7	AD1	I	I <sup>2</sup> C Address / Serial Input
8	AD2	I	I <sup>2</sup> C Address / Serial Enable
9	VDDO	--	OSC Power Supply +2.5V
10	XI	I	X'tal Clock Input
11	XO	O	OSC Output
12	VSSO	--	OSC GND
13	RESETb	I	RESET (active Low)
14	VDDC	--	Core Power Supply +2.5V
15	VSSC	--	Core GND
16	SCL2/WDC	O	I <sup>2</sup> C Clock(For program down load) /Clock for Watch Dog Timer

No.	Symbol	I/O	Description
17	VDDC	--	Core Power Supply +2.5V
18	VDDC	--	Core Power Supply +2.5V
19	VSSC	--	Core GND
20	VSSC	--	Core GND
21	VDDR	--	I/O Power Supply +2.5V
22	VDDR	--	I/O Power Supply +2.5V
23	VSSR	--	I/O GND
24	VSSR	--	I/O GND
25	SDI0	I	Audio Data Input 0
26	SDI1	I	Audio Data Input 1
27	TEST	I	Connect to GND
28	LRI	I	LR Clock Input
29	BCKI	I	Bit Clock Input
30	MCK	O	Master Clock Output
31	BCKO	O	Bit Clock Output
32	LRO	O	LR Clock Output

\* I : Input,  
O : Output,  
I/O: Bi-directional

## ■ Digital Audio Interface

The NJU26150-19A audio interface provides industry standard serial data formats of I<sup>2</sup>S, MSB-first left-justified or MSB-first right-justified. The NJU26150-19A audio interface provides two data inputs, SDI0, SDI1 and three data outputs, SDO0, SDO1, SDO1, as shown in table 2, table 3 and Fig.3, Fig.4. An audio interface input and output data format become the same data format.

**Table 2 Serial Audio Input Pin**

Pin No.	Symbol	Description
25	SDI0	Audio Data Input 0
26	SDI1	Audio Data Input 1

**Table 3 Serial Audio Output Pin**

Pin No.	Symbol	Description
3	SDO0	Audio Data Output 0 L / R
2	SDO1	Audio Data Output 1 C /SW
1	SDO2	Audio Data Output 2 Ls/Rs

## ■ Host Interface

The NJU26150-19A can be controlled via Serial Host Interface (SHI) using I<sup>2</sup>C bus. Data transfers are in 8 bit packets (1 byte) when using either format. Serial Host Interface Pin Description.(Table 4)

**Table 4 Serial Host Interface Pin Description**

Pin No.	Symbol	I <sup>2</sup> C bus Format
5	SCL	Serial Clock
6	SDA	Serial Data Input/Output (Open Drain Input/Output)
7	AD1	I <sup>2</sup> C bus address Bit1
8	AD2	I <sup>2</sup> C bus address Bit2

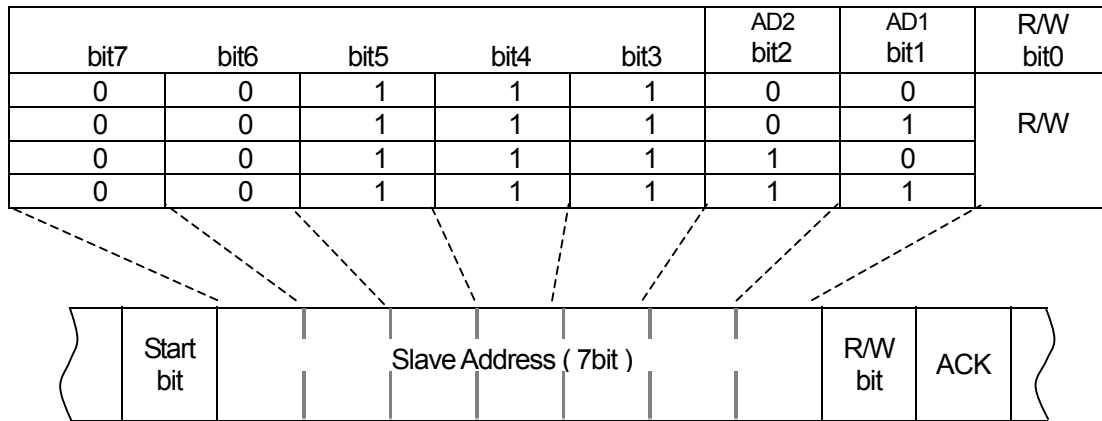
**Note :** SDA pin is a bi-directional open drain. This pin requires a pull-up resistor.

## ■ I<sup>2</sup>C bus

When the NJU26150-19A is configured for I<sup>2</sup>C bus communication during the Reset initialization sequence. I<sup>2</sup>C bus interface transfers data to the SDA pin and clocks data to the SCL pin.

AD1 and AD2 pins are used to configure the seven-bit SLAVE address of the serial host interface. (Table 5) This offers additional flexibility to a system design by four different SLAVE addresses of the NJU26150-19A. An address can be arbitrarily set up by the AD1 and AD2 pins. The I<sup>2</sup>C address of AD1/AD2 is decided by connection of AD1/AD2 pins.

**Table 5 I<sup>2</sup>C bus SLAVE Address**



\* SLAVE address is 0 when AD1/2 is “Low”. SLAVE address is 1 when AD1/2 is “High”.

**Note :** In case of the NJU26150-19A, only single-byte transmission is available. The serial host interface supports “Standard-Mode (100kbps)” I<sup>2</sup>C bus data transfer.

## ■ WatchDog Clock

The NJU26150-19A outputs clock pulse through WDC (No.16) pin during normal operation. The output toggle cycle (Low/High) from a WDC pin changes with sampling frequencies. (Table 6)

**Table 6 WatchDog Clock Output Cycle**

Sampling Frequencies	WDC Output Cycle (Low/High) Time
48 KHz	85ms

The NJU26150-19A generates a clock pulse through the WDC terminal after resetting the NJU26150-19A. The WDC clock is useful to check the status of the NJU26150-19A operation. For example, a microcomputer monitors the WDC clock and checks the status of the NJU26150-19A. When the WDC clock pulse is lost or not normal clock cycle, the NJU26150-19A does not operate correctly. Then reset the NJU26150-19A and set up the NJU26150-19A again.

**Note:** If input and output of a audio signal stop and an audio interface stops, WDC can't output.  
That is because it has controlled based on the signal of an audio interface.

# NJU26150-19A

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## ■ NJU26150-19A Command Table


Table 7 NJU26150-19A Command

No.	Command	No.	Command
1	SET_TASK_CMD	20	SYS_SET_CMD
2	CS_MOD_CMD	21	TB_CTRL_CMD2
3	TB_MOD_CMD	22	TB_CTRL_CMD3
4	TB_CTRL_CMD1	23	FC_CTRL_CMD2
5	FC_MOD_CMD	24	FC_CTRL_CMD3
6	FC_CTRL_CMD1	25	TSHD_CONFIG_CMD
7	MONO_SEL_CMD	26	DF_SELECT_CMD
8	FS_CMD	27	TBII_MODE_CMD
9	REAR_BOOST_CMD	28	TSHD_BYPASS_GAIN_CMD
10	4STREO_CMD	29	TSHD_SRND_LEVEL_CMD
11	DLY_CMD	30	DF_FRONT_BYPASS_CMD
12	MST_VOL_CMD	31	DF_FRONT_INPUT_CMD
13	INPUT_VOL_CMD	32	DF_FRONT_CNTRL_CMD
14	LCH_VOL_CMD	33	DF_FRONT_OUTPUT_CMD
15	RCH_VOL_CMD	34	DF_CENTER_BYPASS_CMD
16	CENT_VOL_CMD	35	DF_CENTER_INPUT_CMD
17	SURR_LEFT_VOL_CMD	36	DF_CENTER_CNTRL_CMD
18	SURR_RIGHT_VOL_CMD	37	DF_CENTER_OUTPUT_CMD
19	SW_VOL_CMD	38	TSHD_BYPASS_SW_CMD

**Notes** : In respect to detail command information, request New Japan Radio Co., Ltd. and permission of a licenser (SRS Labs. Inc.) is required.



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