FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27236-2E

ASSP For Power Supply Applications
(DC/DC Converter for DSC/Camcorder)

4-ch DC/DC Converter IC with Synchronous Rectification

MB39A110

■ DESCRIPTION

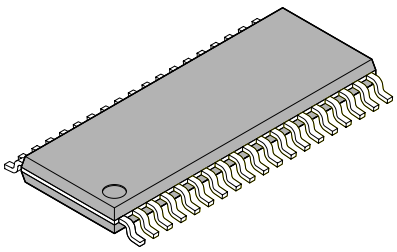
The MB39A110 is a 4-channel DC/DC converter IC using pulse width modulation (PWM). This IC is ideal for up conversion, down conversion, and up/down conversion.
This is built-in 4ch in TSSOP-38P package and operates at 2 MHz Max. Each channel can be controlled, and soft-start.
This is an ideal power supply for high-performance portable devices such as digital still cameras.
This product is covered by US Patent Number 6,147,477.

■ FEATURES

- Supports for down-conversion and up/down Zeta conversion (CH1 to CH3)
- Supports for up-conversion and up/down Sepic conversion (CH4)
- For synchronous rectification (CH1, CH2)
- Power supply voltage range : 2.5 V to 11 V
- Reference voltage : 2.0 V ± 1 %
- Error amplifier threshold voltage : 1.23 V ± 1%
- High-frequency operation capability: 2 MHz (Max)
- Standby current : 0 μA (Typ)
- Built-in soft-start circuit independent of loads
- Built-in totem-pole type output for MOS FET
- Short-circuit detection capability by external signal (–INS terminal)

■ PACKAGE

38-pin plastic TSSOP



(FPT-38P-M03)

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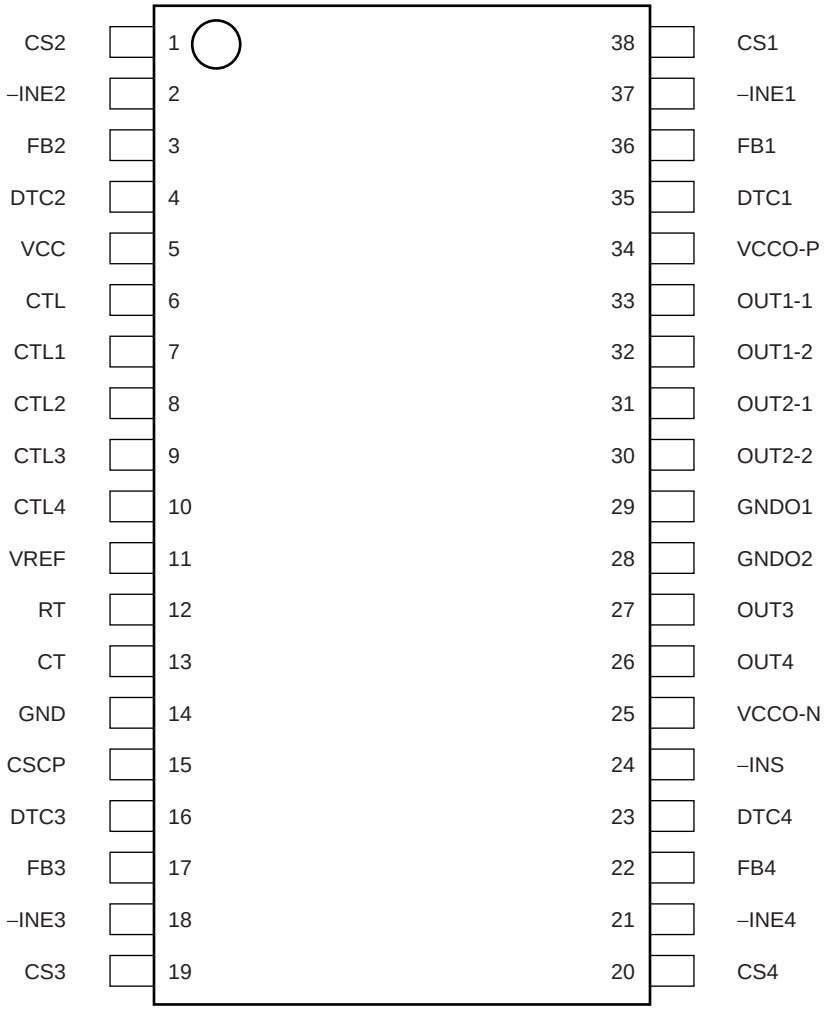
■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-38P-M03)

■ PIN DESCRIPTION

Block	Pin No.	Symbol	I/O	Descriptions
CH1	35	DTC1	I	Dead time control terminal
	36	FB1	O	Error amplifier output terminal
	37	–INE1	I	Error amplifier inverted input terminal
	38	CS1	—	Soft-start setting capacitor connection terminal
	33	OUT1-1	O	Pch drive output block ground terminal (External main side FET gate driving)
	32	OUT1-2	O	Nch drive output block ground terminal (External synchronous rectification side FET gate driving)
CH2	4	DTC2	I	Dead time control terminal
	3	FB2	O	Error amplifier output terminal
	2	–INE2	I	Error amplifier inverted input terminal
	1	CS2	—	Soft-start setting capacitor connection terminal
	31	OUT2-1	O	Pch drive output block ground terminal (External main side FET gate driving)
	30	OUT2-2	O	Nch drive output block ground terminal (External synchronous rectification side FET gate driving)
CH3	16	DTC3	I	Dead time control terminal
	17	FB3	O	Error amplifier output terminal
	18	–INE3	I	Error amplifier inverted input terminal
	19	CS3	—	Soft-start setting capacitor connection terminal
	27	OUT3	O	Pch drive output terminal
CH4	23	DTC4	I	Dead time control terminal
	22	FB4	O	Error amplifier output terminal
	21	–INE4	I	Error amplifier inverted input terminal
	20	CS4	—	Soft-start setting capacitor connection terminal
	26	OUT4	O	Nch drive output terminal
OSC	13	CT	—	Triangular wave frequency setting capacitor connection terminal
	12	RT	—	Triangular wave frequency setting resistor connection terminal

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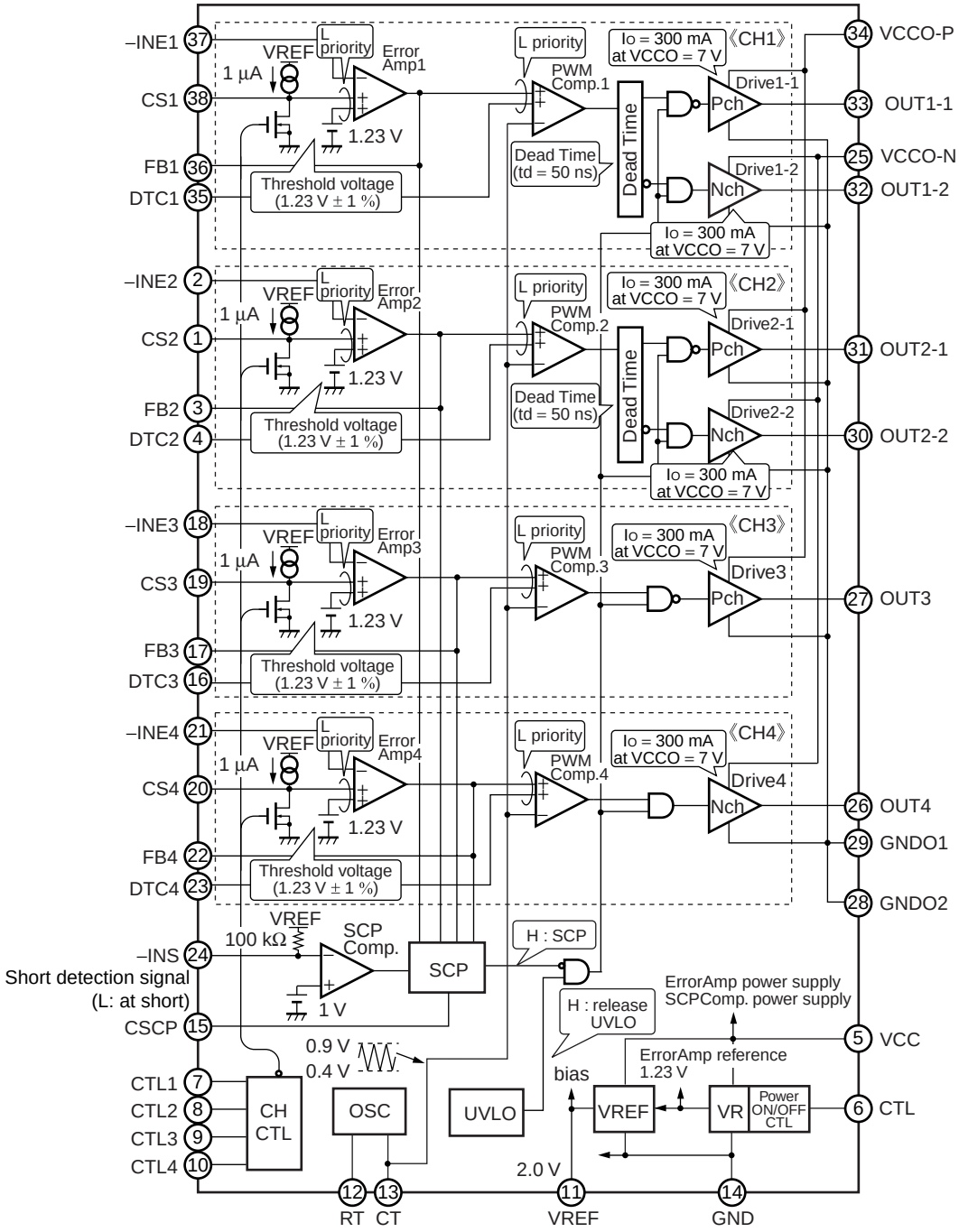
Block	Pin No.	Symbol	I/O	Descriptions
Control	6	CTL	I	Power supply control terminal
	7	CTL1	I	Control terminal
	8	CTL2	I	Control terminal
	9	CTL3	I	Control terminal
	10	CTL4	I	Control terminal
	15	CSCP	—	Short-circuit detection circuit capacitor connection terminal
	24	–INS	I	Short-circuit detection comparator inverted input terminal
Power	34	VCCO-P	—	Pch drive output block power supply terminal
	25	VCCO-N	—	Nch drive output block power supply terminal
	5	VCC	—	Power supply terminal
	11	VREF	O	Reference voltage output terminal
	29	GNDO1	—	Drive output block ground terminal
	28	GNDO2	—	Drive output block ground terminal
	14	GND	—	Ground terminal

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	VCC, VCCO terminal	—	12	V
Output current	I_O	OUT1 to OUT4 terminal	—	20	mA
Peak output current	I_{OP}	OUT1 to OUT4 terminal, Duty ≤ 5% (t = 1 / f_{OSC}×Duty)	—	400	mA
Power dissipation	P_D	Ta ≤ +25 °C	—	1680*	mW
Storage temperature	T_{STG}	—	–55	+125	°C

* : The packages are mounted on the epoxy board (10 cm × 10 cm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	VCC, VCCO terminal	2.5	7	11	V
Reference voltage output current	I_{REF}	VREF terminal	–1	—	0	mA
Input voltage	V_{INE}	–INE1 to –INE4 terminal	0	—	V_{CC} – 0.9	V
		–INS terminal	0	—	V_{REF}	V
	V_{DTC}	DTC1 to DTC4 terminal	0	—	V_{REF}	V
Control input voltage	V_{CTL}	CTL terminal	0	—	11	V
Output current	I_O	OUT1 to OUT4 terminal	–15	—	+15	mA
Oscillation frequency	f_{OSC}	—	0.2	1.02	2.0	kHz
Timing capacitor	C_T	—	27	100	680	pF
Timing resistor	R_T	—	3.0	6.8	39	kΩ
Soft-start capacitor	C_S	CS1 to CS4 terminal	—	0.1	1.0	µF
Short-circuit detection capacitor	C_{SCP}	—	—	0.1	1.0	µF
Reference voltage output capacitor	C_{REF}	—	—	0.1	1.0	µF
Operating ambient temperature	Ta	—	–30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = VCCO = 7 V, Ta = +25 °C)

Parameter		Sym-bol	Pin No	Conditions	Value			Unit
					Min	Typ	Max	
1. Reference voltage block [VREF]	Output voltage	V_{REF1}	11	VREF = 0 mA	1.98	2.00	2.02	V
		V_{REF2}	11	VCC = 2.5 V to 11 V	1.975	2.000	2.025	V
		V_{REF3}	11	VREF = 0 mA to –1 mA	1.975	2.000	2.025	V
	Input stability	Line	11	VCC = 2.5 V to 11 V	—	2*	—	mV
	Load stability	Load	11	VREF = 0 mA to –1 mA	—	2*	—	mV
	Temperature stability	ΔV_{REF} /V_{REF}	11	Ta = 0 °C to +85 °C	—	0.20*	—	%
	Output current at short-circuit	I_{OS}	11	VREF = 0 V	—	–300*	—	mA
2. Under voltage lockout protection circuit block [UVLO]	Threshold voltage	V_{TH}	33	VCC = ↗	1.7	1.8	1.9	V
	Hysteresis width	V_H	33	—	0.05	0.1	—	V
	Reset voltage	V_{RST}	33	VREF = ↘	1.5	1.7	1.85	V
3. Short-circuit detection block [SCP]	Threshold voltage	V_{TH}	15	—	0.65	0.70	0.75	V
	Input source current	I_{CSCP}	15	—	–1.4	–1.0	–0.6	µA
4. Triangular wave oscillator block [OSC]	Oscillation frequency	f_{OSC1}	26, 27, 30 to 33	CT = 100 pF, RT = 6.8 kΩ	0.97	1.02	1.07	MHz
		f_{OSC2}	26, 27, 30 to 33	CT = 100 pF, RT = 6.8 kΩ, VCC = 2.5 V to 11 V	0.964	1.02	1.076	MHz
	Frequency input stability	Δf_{OSC}/ f_{OSC}	26, 27, 30 to 33	CT = 100 pF, RT = 6.8 kΩ, VCC = 2.5 V to 11 V	—	1.0*	—	%
	Frequency temperature stability	Δf_{OSC}/ f_{OSC}	26, 27, 30 to 33	CT = 100 pF, RT = 6.8 kΩ, Ta = 0 °C to +85 °C	—	1.0*	—	%
5. Soft-start block [CS1 to CS4]	Charge current	I_{CS}	1, 19, 20, 38	CS1 to CS4 = 0 V	–1.4	–1.0	–0.6	µA

* : Standard design value

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(VCC = VCCO = 7 V, Ta = +25 °C)

Parameter		Sym-bol	Pin No	Conditions	Value			Unit
					Min	Typ	Max	
6. Error amplifier block [Error Amp1 to Error Amp4]	Threshold voltage	V_{TH1}	2, 18, 21, 37	VCC = 2.5 V to 11 V, Ta = +25 °C	1.217	1.230	1.243	V
		V_{TH2}	2, 18, 21, 37	VCC = 2.5 V to 11 V, Ta = 0 °C to +85 °C	1.215	1.230	1.245	V
	Temperature stability	$\Delta V_{TH}/V_{TH}$	2, 18, 21, 37	Ta = 0 °C to +85 °C	—	0.1*	—	%
	Input bias current	I_B	2, 18, 21, 37	–INE1 to –INE4 = 0 V	–120	–30	—	nA
	Voltage gain	A_V	3, 17, 22, 36	DC	—	100*	—	dB
	Frequency bandwidth	BW	3, 17, 22, 36	A_V = 0 dB	—	1.4*	—	MHz
	Output voltage	V_{OH}	3, 17, 22, 36	—	1.7	1.9	—	V
		V_{OL}	3, 17, 22, 36	—	—	40	200	mV
	Output source current	I_{SOURCE}	3, 17, 22, 36	FB1 to FB4 = 0.65 V	—	–2	–1	mA
	Output sink current	I_{SINK}	3, 17, 22, 36	FB1 to FB4 = 0.65 V	150	200	—	µA
7. PWM comparator block [PWM Comp.1 to PWM Comp.4]	Threshold voltage	V_{T0}	26, 27, 30 to 33	Duty cycle = 0%	0.3	0.4	—	V
		V_{T100}	26, 27, 30 to 33	Duty cycle = 100%	0.85	0.90	0.95	V
	Input current	I_{DTC}	4, 16, 23, 35	DTC = 0.4 V	–2.0	–0.6	—	µA
8. Output block [Drive1 to Drive4]	Output source current	I_{SOURCE}	26, 27, 30 to 33	Duty ≤ 5% ($t = 1 / f_{OSC} \times$ Duty), OUT1 to OUT4 = 0 V	—	–300*	—	mA
	Output sink current	I_{SINK}	26, 27, 30 to 33	Duty ≤ 5% ($t = 1 / f_{OSC} \times$ Duty), OUT1 to OUT4 = 7 V	—	300*	—	mA
	Output ON resistor	R_{OH}	26, 27, 30 to 33	OUT1 to OUT4 = –15 mA	—	9	14	Ω
		R_{OL}	26, 27, 30 to 33	OUT1 to OUT4 = 15 mA	—	9	14	Ω
	Dead time	t_{D1}	30 to 33	OUT2 ↓ –OUT1 ↓	—	50*	—	ns
		t_{D2}	30 to 33	OUT1 ↑ –OUT2 ↑	—	50*	—	ns
9. Short-circuit detection comparator block [SCP Comp.]	Threshold voltage	V_{TH}	33	—	0.97	1.00	1.03	V
	Input bias current	I_B	24	–INS = 0 V	–25	–20	–17	µA

*: Standard design value

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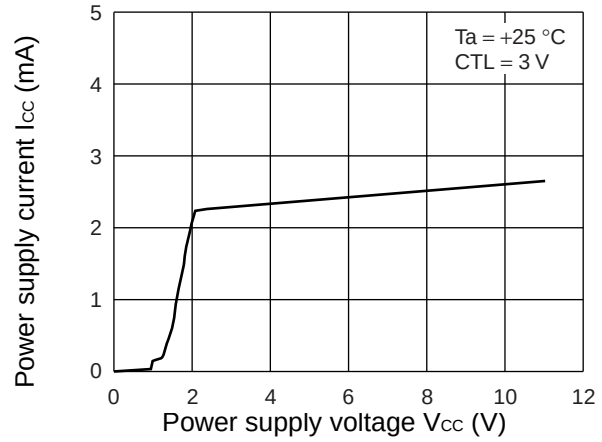
(VCC = VCCO = 7 V, Ta = +25 °C)

Parameter		Sym-bol	Pin No	Conditions	Value			Unit
					Min	Typ	Max	
10. Control block [CTL, CHCTL]	Output ON conditions	V_{IH}	6, 7 to 10	CTL, CTL1 to CTL4	2	—	11	V
	Output OFF conditions	V_{IL}	6, 7 to 10	CTL, CTL1 to CTL4	0	—	0.8	V
	Input current	I_{CTLH}	6, 7 to 10	CTL, CTL1 to CTL4 = 3 V	—	30	60	µA
		I_{CTLL}	6, 7 to 10	CTL, CTL1 to CTL4 = 0 V	—	—	1	µA
11. General	Standby current	I_{CCS}	5	CTL, CTL1 to CTL4 = 0 V	—	0	2	µA
		I_{CCSO}	25, 34	CTL = 0 V	—	0	1	µA
	Power supply current	I_{CC}	5	CTL = 3 V	—	3	4.5	mA

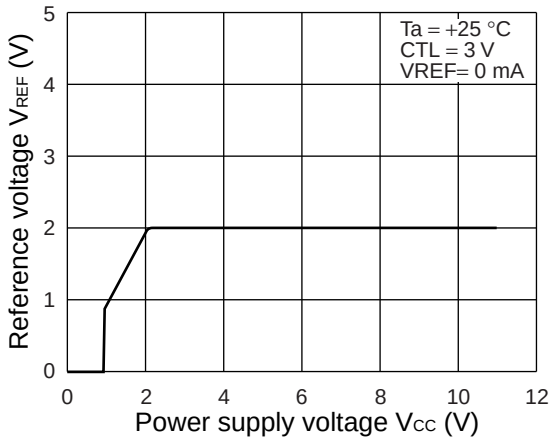
*: Standard design value

■ TYPICAL CHARACTERISTICS

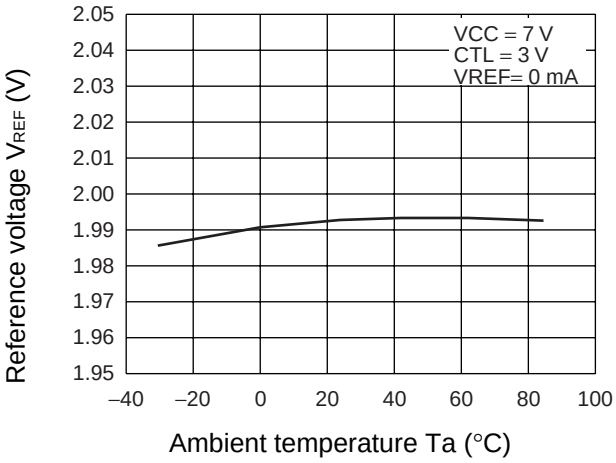
Power Supply Current vs. Power Supply Voltage



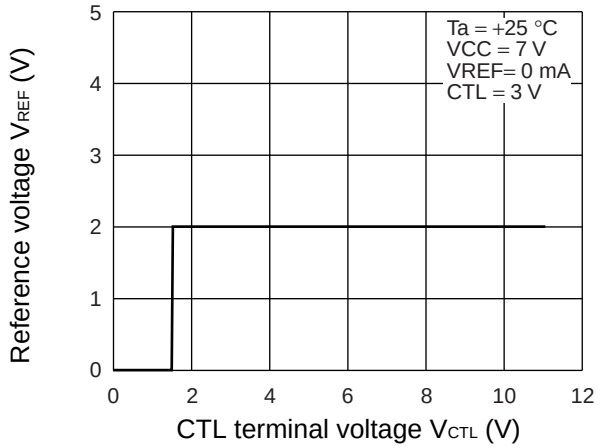
Reference Voltage vs. Power Supply Voltage



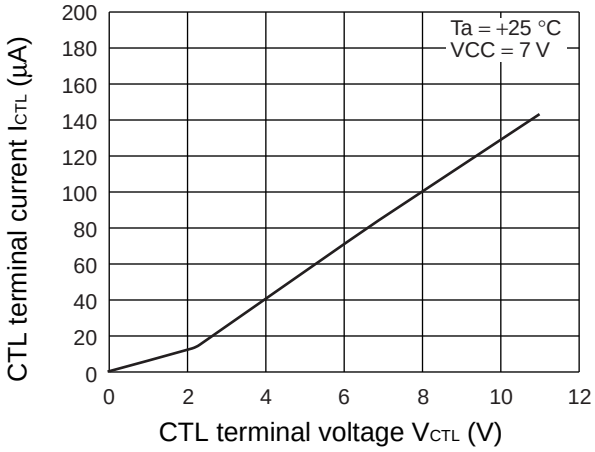
Reference Voltage vs. Ambient Temperature



Reference Voltage vs. CTL terminal Voltage



CTL terminal Current vs. CTL terminal Voltage



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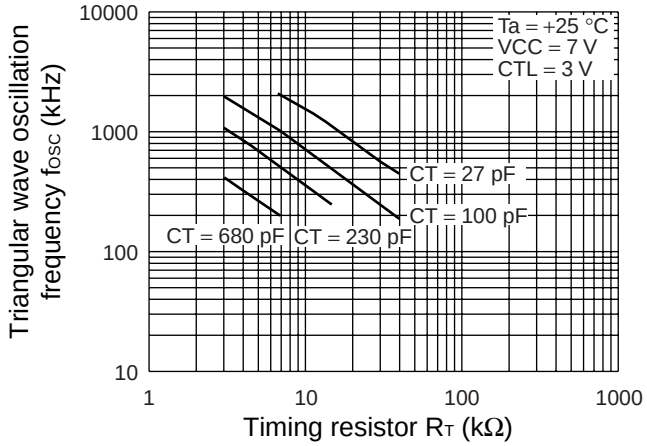
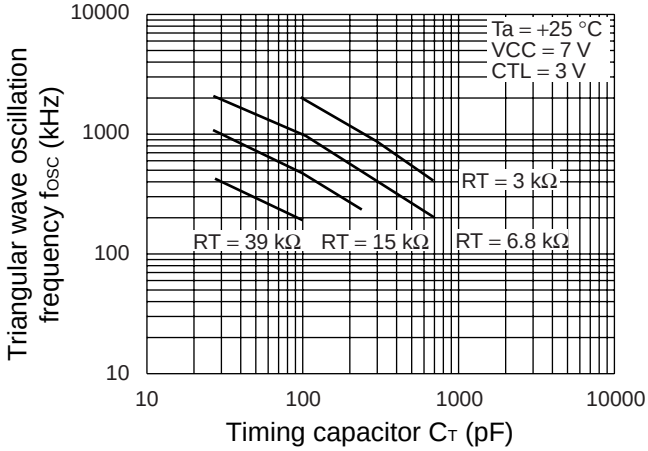
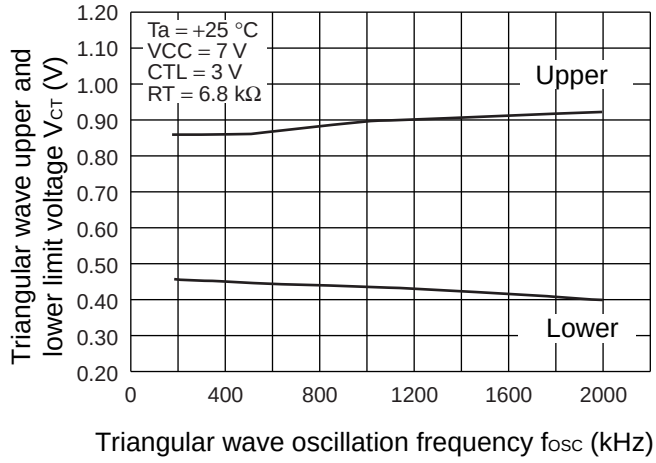
Triangular Wave Oscillation Frequency vs. Timing Resistor



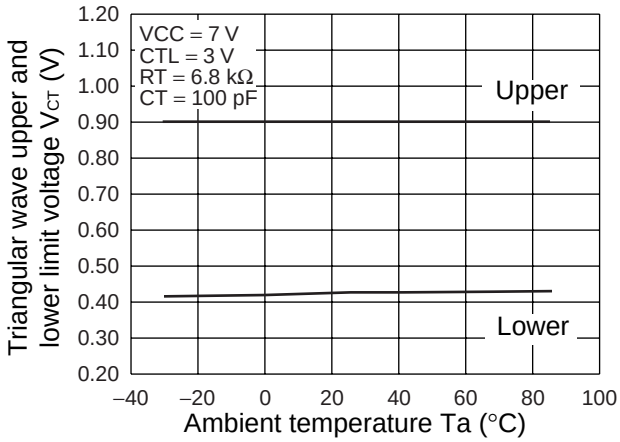
Triangular Wave Oscillation Frequency vs. Timing Capacitor



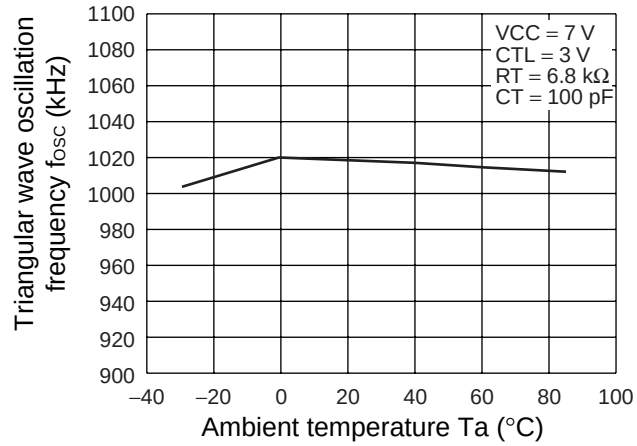
Triangular Wave Upper and Lower Limit Voltage vs. Triangular Wave Oscillation Frequency



Triangular Wave Upper and Lower Limit Voltage vs. Ambient Temperature



Triangular Wave Oscillation Frequency vs. Ambient Temperature



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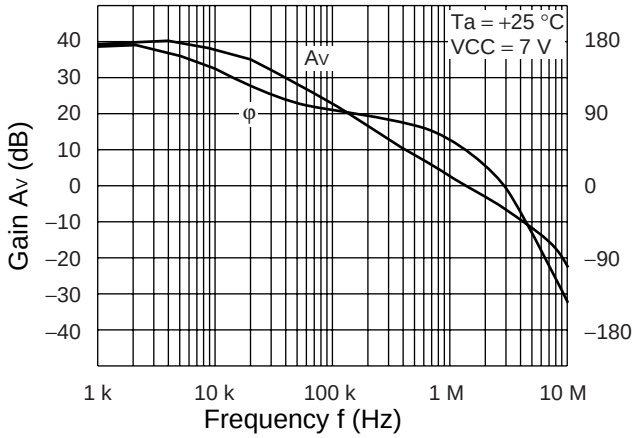
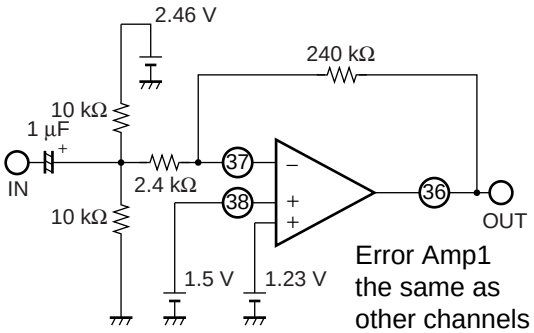
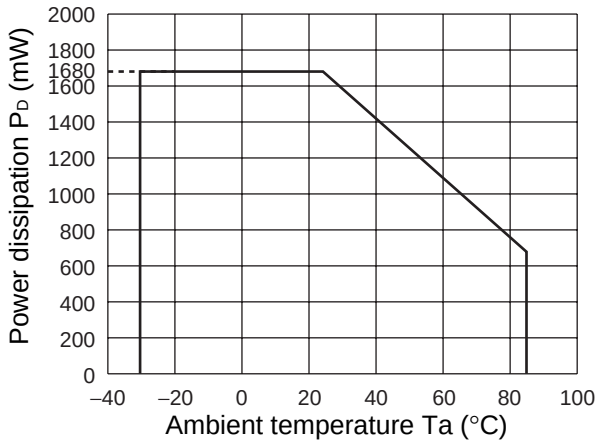
Error Amplifier Gain, Phase vs. Frequency





Power Dissipation vs. Ambient Temperature



■ FUNCTION DESCRIPTION

1. DC/DC Converter Functions

(1) Reference Voltage Block (VREF)

The reference voltage circuit generates a temperature-compensated reference voltage (2.0 V Typ) from the voltage supplied from the power supply terminal (pin 5). The voltage is used as the reference voltage for the IC's internal circuit.
The reference voltage can supply a load current of up to 1 mA to an external device through the VREF terminal (pin 11).

(2) Triangular-wave Oscillator Block (OSC)

The triangular wave oscillator incorporates a timing capacitor and a timing resistor connected respectively to the CT terminal (pin 13) and RT terminal (pin 12) to generate triangular oscillation waveform amplitude of 0.4 V to 0.9 V.
The triangular waveforms are input to the PWM comparator in the IC.

(3) Error Amplifier Block (Error Amp1 to Error Amp4)

The error amplifier detects the DC/DC converter output voltage and outputs PWM control signals. In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the output terminal to inverted input terminal of the error amplifier, enabling stable phase compensation to the system.
Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor with the CS1 terminal (pin 38) to CS4 terminal (pin 20) which are the non-inverted input terminal for Error Amp. The use of Error Amp for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load on the DC/DC converter.

(4) PWM Comparator Block (PWM Comp.1 to PWM Comp.4)

The PWM comparator is a voltage-to-pulse width modulator that controls the output duty depending on the input/output voltage.
The output transistor turns on while the error amplifier output voltage and DTC voltage remain higher than the triangular wave voltage.

(5) Output Block (Drive1 to Drive 4)

The output block is in the totem pole type, capable of driving an external P-channel MOS FET (channel 1 and 2 main side and channel 3), and N-channel MOS FET (channel 1 and 2 synchronous rectification side and channel 4).

2. Channel Control Function

The main or each channel is turned on and off depending on the voltage levels at the CTL terminal (pin 6), CS1 terminal (pin 38), CS2 terminal (pin 1), CS3 terminal (pin 19), and CS4 terminal (pin 20).

Channel On/Off Setting Conditions

CTL	CTL1	CTL2	CTL3	CTL4	Power	CH1	CH2	CH3	CH4
L	—*	—*	—*	—*	OFF	OFF	OFF	OFF	OFF
H	L	L	L	L	ON	OFF	OFF	OFF	OFF
H	H	L	L	L	ON	ON	OFF	OFF	OFF
H	L	H	L	L	ON	OFF	ON	OFF	OFF
H	L	L	H	L	ON	OFF	OFF	ON	OFF
H	L	L	L	H	ON	OFF	OFF	OFF	ON
H	H	H	H	H	ON	ON	ON	ON	ON

* : Undifined

Note : Note that current over stand-by current flows into VCC terminal when the CTL terminal is in “L” level and one of terminals between CTL1 and CTL4 is set to “H” level.
(Refer to “■ I/O EQUIVALENT CIRCUIT”)

3. Protective Functions

(1) Timer-latch short-circuit protection circuit (SCP, SCP Comp.)

The short-circuit detection comparator (SCP) detects the output voltage level of each channel, and if any channel output voltage becomes the short-circuit detection voltage or less, the timer circuits are actuated to start charging the external capacitor C_{SCP} connected to the CSCP terminal (pin 15).
When the capacitor (C_{SCP}) voltage reaches about 0.7 V, the circuit is turned off the output transistor and sets the dead time to 100 %.
In addition, the short-circuit detection from external input is capable by using –INS terminal (pin 24) on short-circuit detection comparator (SCP Comp.) .
To release the actuated protection circuit, either turn the power supply off and on again or set the CTL terminal (pin 6) to the “L” level to lower the VREF terminal (pin 11) voltage to 1.5 V (Min) or less. (See “■SETTING TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT”.)

(2) Under voltage lockout protection circuit (UVLO)

The transient state or a momentary decrease in supply voltage, which occurs when the power supply is turned on, may cause the IC to malfunction, resulting in breakdown or degradation of the system. To prevent such malfunctions, under voltage lockout protection circuit detects a decrease in internal reference voltage with respect to the power supply voltage, turn off the output transistor, and set the dead time to 100% while holding the CSCP terminal (pin 15) at the “L” level.
The circuit restores the output transistor to normal when the supply voltage reaches the threshold voltage of the undervoltage lockout protection circuit.

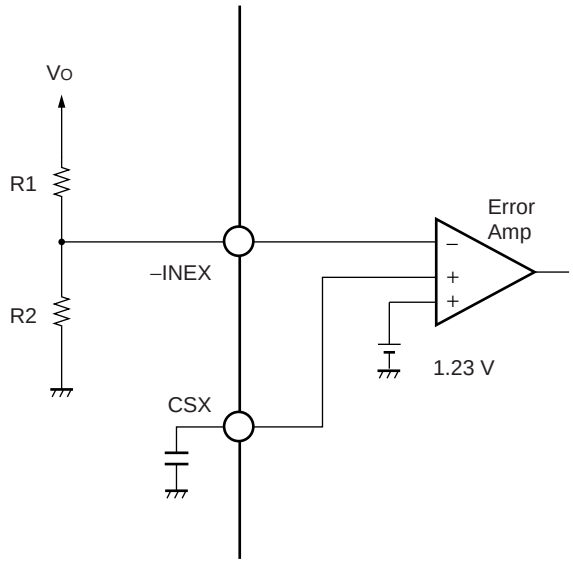
■ PROTECTION CIRCUIT OPERATING FUNCTION TABLE

This table refers to output condition when protection circuit is operating.

Operating circuit	OUT1-1	OUT1-2	OUT2-1	OUT2-2	OUT3	OUT4
Short-circuit protection circuit	H	L	H	L	H	L
Under voltage lockout protection circuit	H	L	H	L	H	L

■ SETTING THE OUTPUT VOLTAGE

• CH1 to CH4



$$V_O\ (V) = \frac{1.23}{R2}\ (R1 + R2)$$

X: Each channel No.

■ SETTING THE TRIANGULAR OSCILLATION FREQUENCY

The triangular oscillation frequency is determined by the timing resistor (R_T) connected to the RT terminal (pin 12), and the timing capacitor (C_T) connected to the CT terminal (pin 13).

Triangular oscillation frequency : f_{OSC}

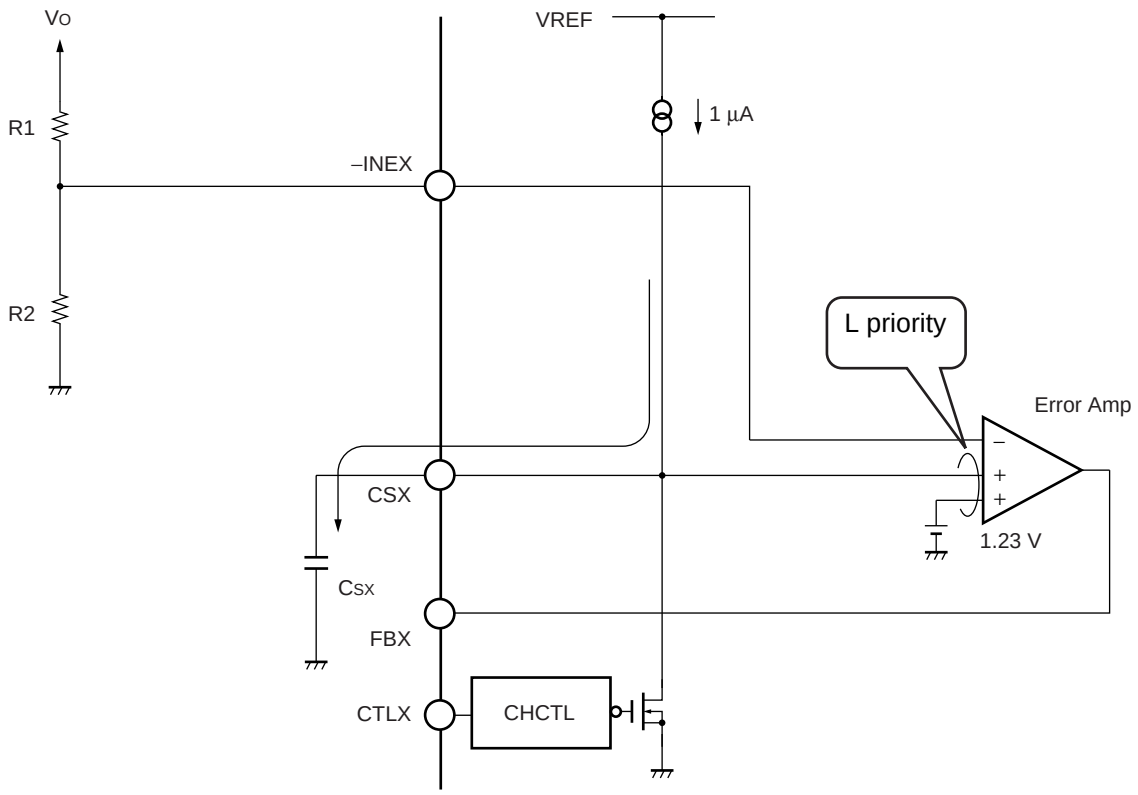
$$f_{OSC}\ (kHz) \fallingdotseq \frac{693600}{C_T\ (pF) \bullet R_T\ (k\Omega)}$$

■ SETTING THE SOFT-START TIME

To prevent rush currents when the IC is turned on, you can set a soft-start by connecting soft-start capacitors (C_{S1} to C_{S4}) to the CS1 terminal (pin 38) to the CS4 terminal (pin 20), respectively.
Setting each CTLX from “L” to “H” switches to charge the external soft-start capacitors (C_{S1} to C_{S4}) connected to the CS1 to CS4 terminals at 1 μA.
The error amplifier output (FB1 to FB4) is determined by comparison between the lower one of the potentials at two non-inverted input terminals (1.23 V, CS terminal voltages) and the inverted input terminal voltage (–INE1 to –INE4).
The FB terminal voltage during the soft-start period (CS terminal voltage < 1.23 V) is therefore determined by comparison between the –INE terminal and CS terminal voltages. The DC/DC converter output voltage rises in proportion to the CS terminal voltage as the soft-start capacitor connected to the CS terminal is charged.
The soft-start time is obtained from the following formula:

Soft-start time: ts (time to output 100%)
ts (s) ≒ 1.23 × C_{SX} (μF)

• Soft-Start Circuit

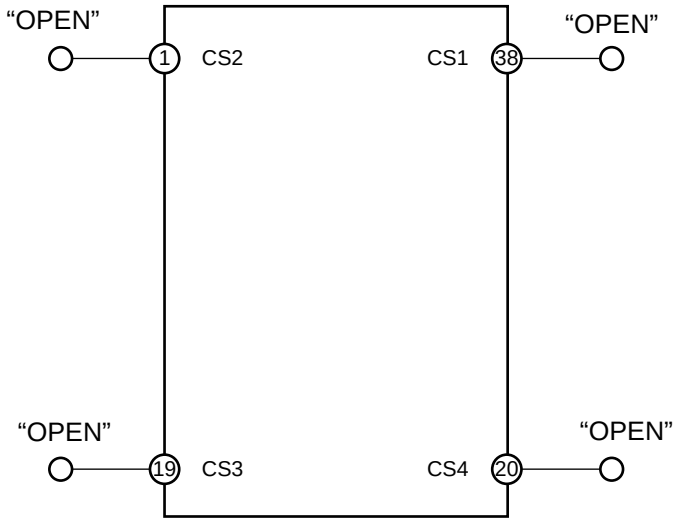


X: Each channel No.

■ TREATMENT WITHOUT USING CS TERMINAL

When not using the soft-start function, open the CS1 terminal (pin 38), the CS2 terminal (pin 1), the CS3 terminal (pin 19), the CS4 terminal (pin 20).

• **Without Setting Soft-Start Time**



■ SETTING TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT

Each channel uses the short-circuit detection comparator (SCP) to always compare the error amplifier's output level to the reference voltage.

While DC/DC converter load conditions are stable on all channels, the short-circuit detection comparator output remains at "L" level, and the CSCP terminal (pin 15) is held at "L" level.

If the load condition on a channel changes rapidly due to a short-circuit of the load, causing the output voltage to drop, the output of the short-circuit detection comparator on that channel goes to "H" level. This causes the external short-circuit protection capacitor C_{SCP} connected to the CSCP terminal to be charged at 1 µA.

Short-circuit detection time : t_{CSCP}

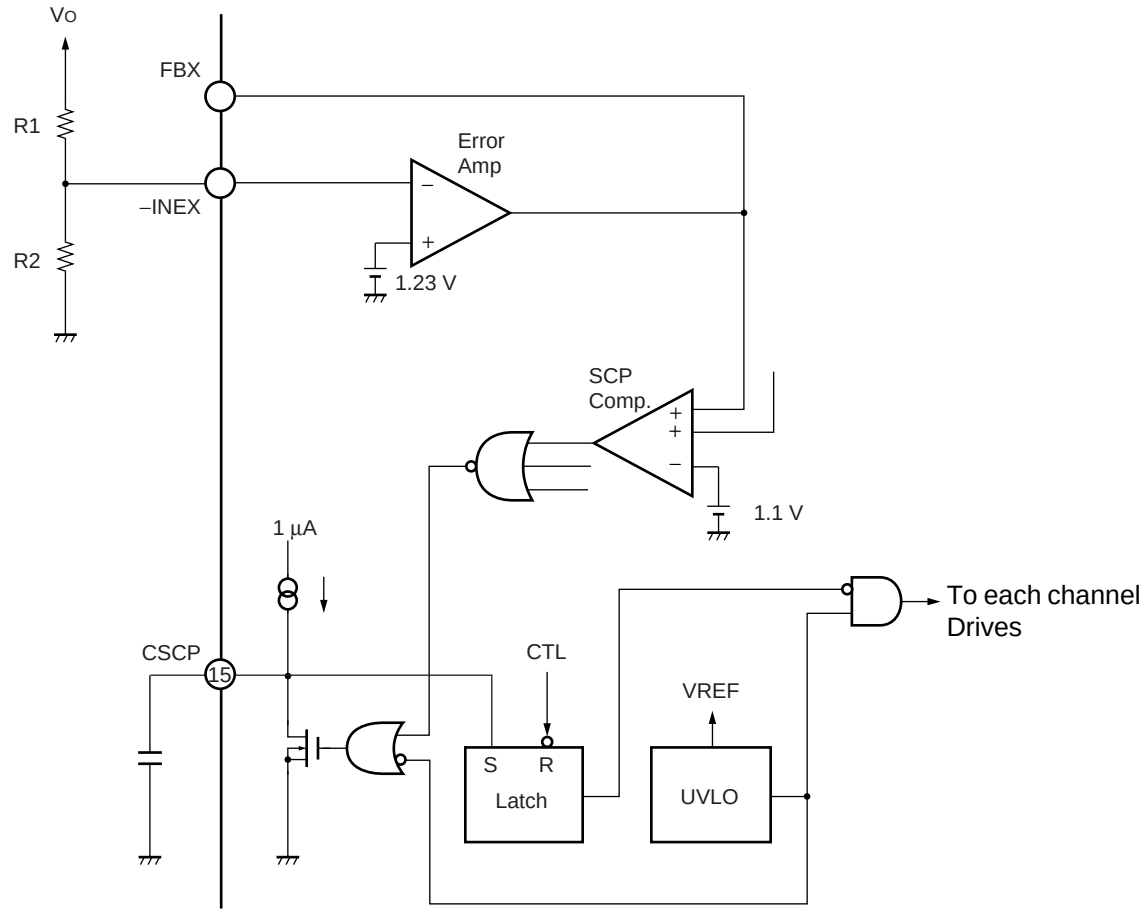
t_{CSCP} (s) ≒ 0.70 × C_{SCP} (µF)

When the capacitor C_{SCP} is charged to the threshold voltage (V_{TH} ≒ 0.70 V), the latch is set and the external FET is turned off (dead time is set to 100%). At this time, the latch input is closed and the CSCP terminal (pin 15) is held at "L" level.

In addition, the short-circuit detection from external input is capable by using –INS terminal (pin 24) on the short-circuit detection comparator (SCP Comp.). The short-circuit detection operation starts when –INS terminal voltage is less than threshold voltage (V_{TH} ≒ 1 V).

When the power supply is turn off and on again or VREF terminal (pin 11) voltage is less than 1.5 V (Min) by setting CTL terminal (pin 6) to "L" level, the latch is released.

• Timer-latch short-circuit protection circuit

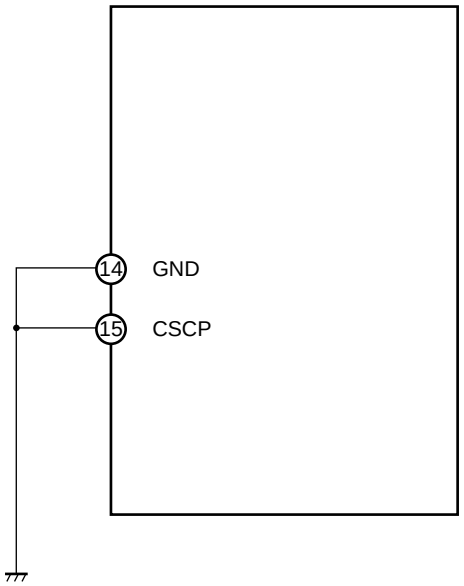


X: Each channel No.

■ TREATMENT WITHOUT USING CSCP TERMINAL

When not using the timer-latch short-circuit protection circuit, connect the CSCP terminal (pin 15) to GND with the shortest distance.

• **Treatment without using CSCP terminal**



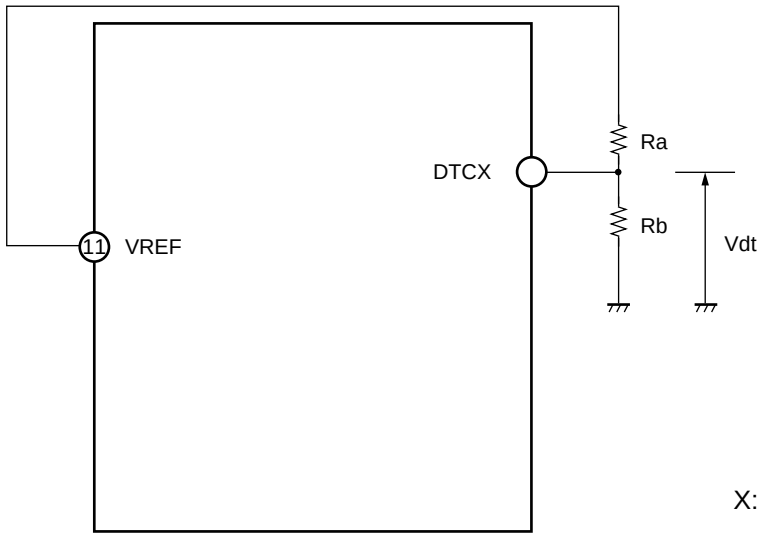
■ SETTING THE DEAD TIME

When the device is set for step-up or inverted output based on the step-up or step-up/down Zeta conversion, step-up/down Sepic conversion or flyback conversion, the FB terminal voltage may reach and exceed the triangular wave voltage due to load fluctuation. If this case happens, the output transistor is fixed to a full-ON state (ON duty = 100 %). To prevent this, set the maximum duty of the output transistor. To set it, set the voltage at the DTC terminal by applying a resistive voltage divider to the VREF voltage as shown below.
When the DTC terminal voltage is higher than the triangular wave voltage, the output transistor is turned on. The maximum duty calculation formula assuming that triangular wave amplitude ≒ 0.5 V and triangular wave lower voltage ≒ 0.4 V is given below.

$$\text{DUTY (ON) Max} \fallingdotseq \frac{\text{Vdt} - 0.4\ \text{V}}{0.5\ \text{V}} \times 100\ (\%)\ ,\ \text{Vdt} = \frac{\text{Rb}}{\text{Ra} + \text{Rb}} \times \text{VREF}$$

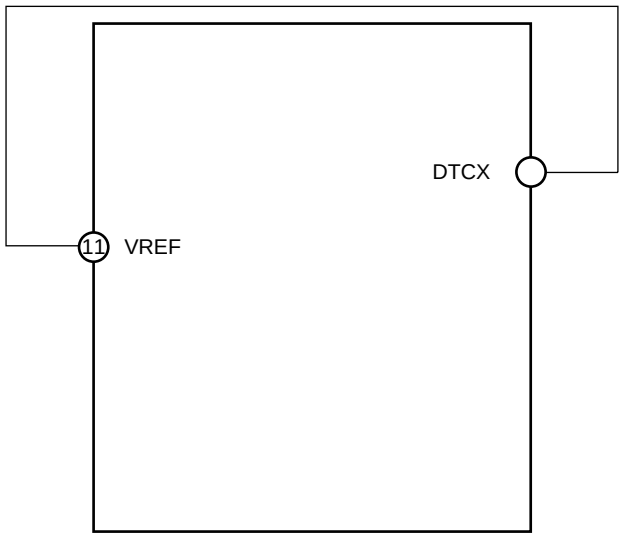
When the DTC terminal is not used, connect it directly to the VREF terminal (pin 11) as shown below (when no dead time is set).

• **When using DTC to set dead time**



X: Each channel No.

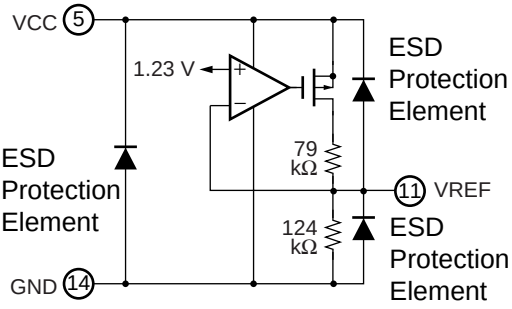
• **When no dead time is set**



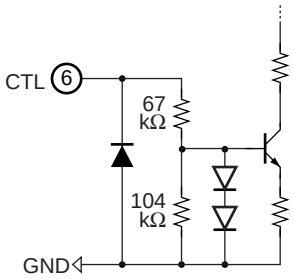
X: Each channel No.

■ I/O EQUIVALENT CIRCUIT

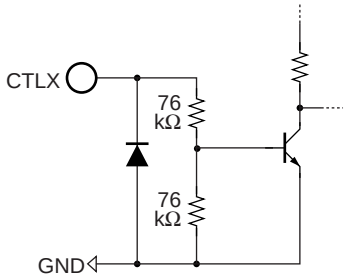
⟨⟨Reference voltage block⟩⟩



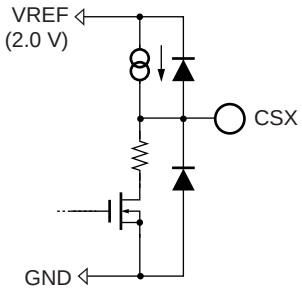
⟨⟨Control block⟩⟩



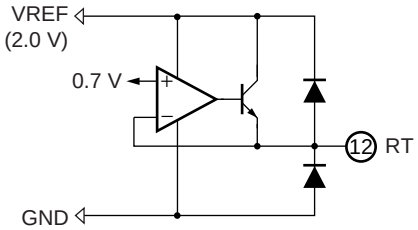
⟨⟨Channel control block⟩⟩



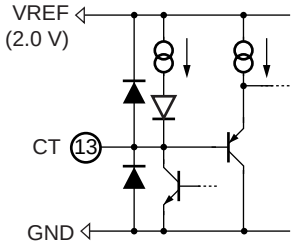
⟨⟨Short-start block⟩⟩



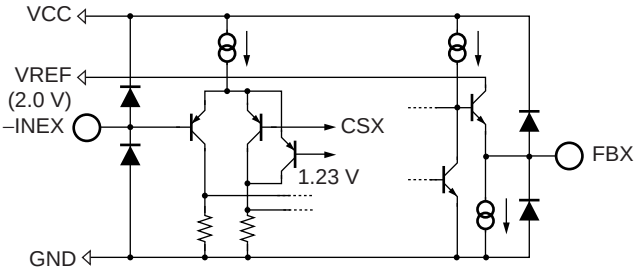
⟨⟨Triangular wave oscillator block (RT) ⟩⟩



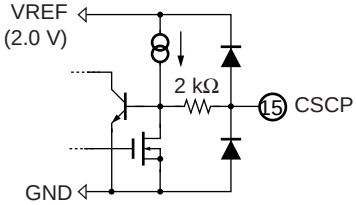
⟨⟨Triangular wave oscillator block (CT)⟩⟩



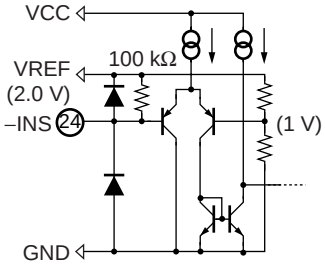
⟨⟨Error amplifier block (CH1 to CH4) ⟩⟩



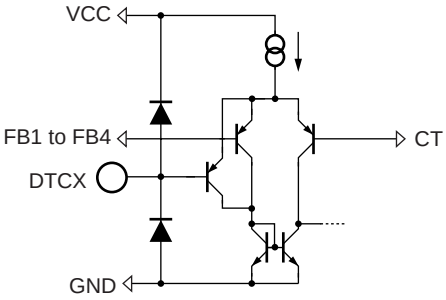
⟨⟨Short-circuit detection block⟩⟩



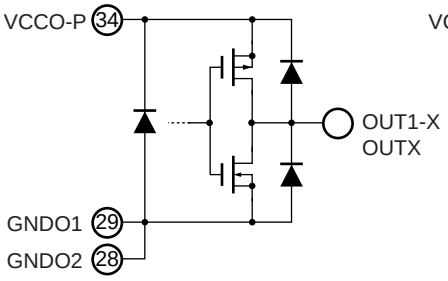
⟨⟨Short-circuit detection comparator block⟩⟩



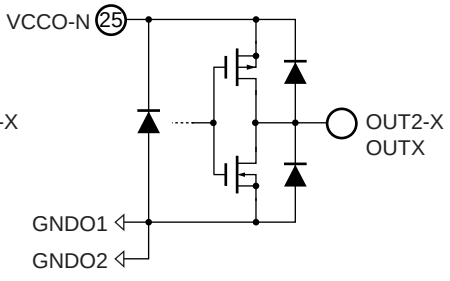
⟨⟨PWM comparator block⟩⟩



⟨⟨Output block Pch (CH1 to CH3) ⟩⟩

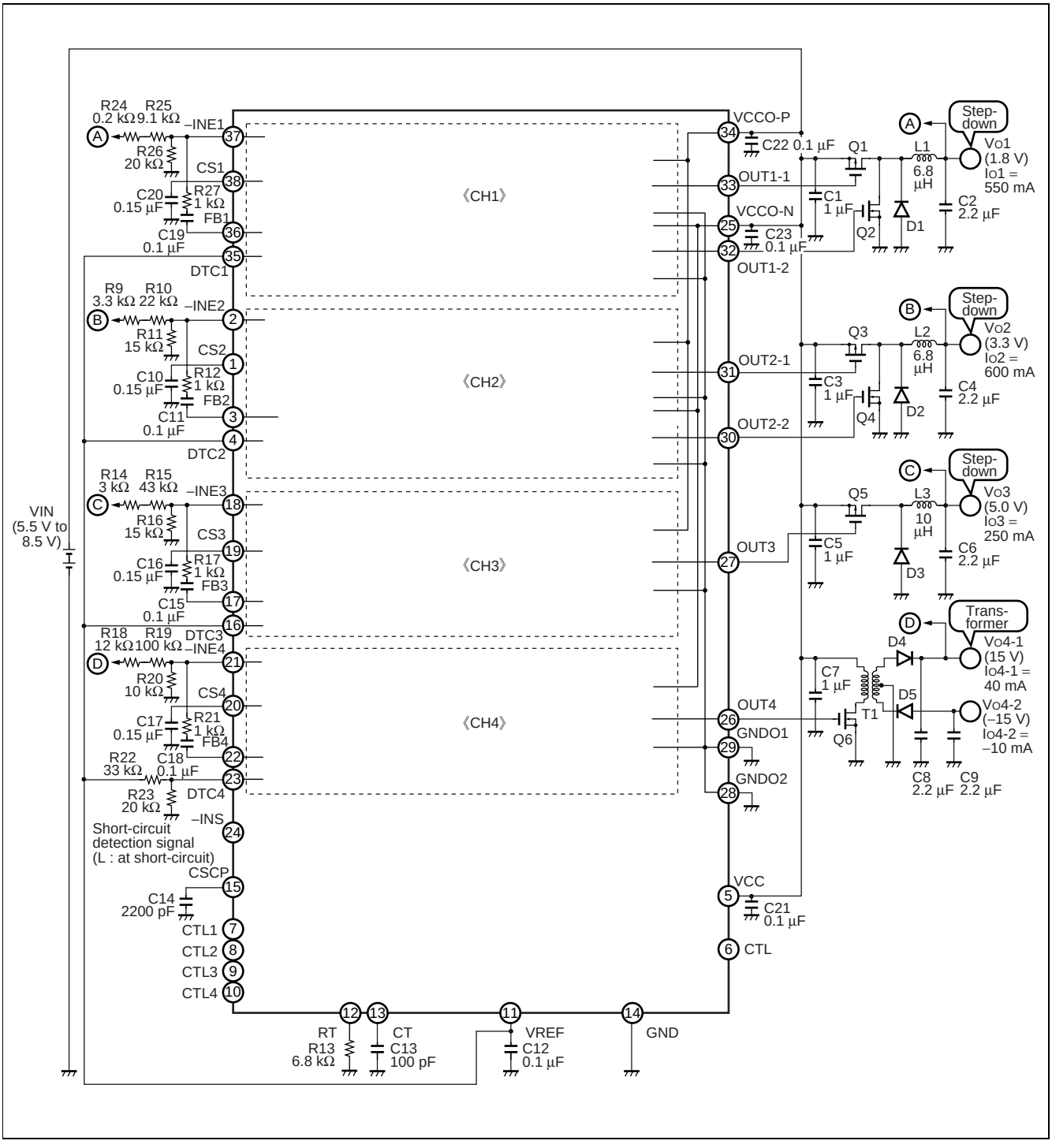


⟨⟨Output block Nch (CH1, CH2, CH4) ⟩⟩



X: Each channel No.

■ APPLICATION EXAMPLE



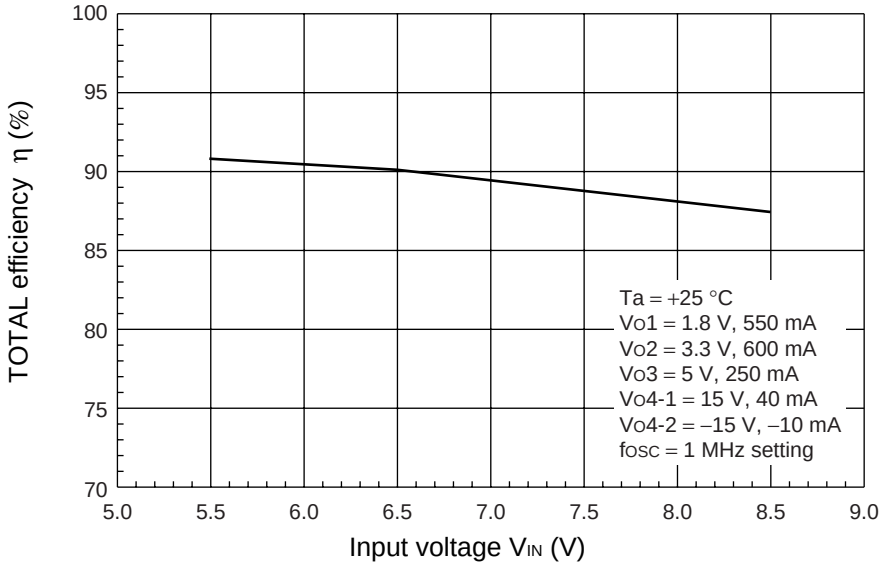
■ PARTS LIST

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1, Q3, Q5	Pch FET	VDS = –20 V, ID = –1.0 A		SANYO	MCH3307
Q2, Q4	Nch FET	VDS = 20 V, ID = 1.8 A		SANYO	MCH3405
Q6	Nch FET	VDS = 30 V, ID = 1.4 A		SANYO	MCH3408
D1 to D3	Diode	VF = 0.4 V (Max) , IF = 1 A		SANYO	SBS004
D4, D5	Diode	VF = 0.55 V (Max) , IF = 0.5 A		SANYO	SB05-05CP
L1, L2	Inductor	6.8 µH	1.1 A, 47 mΩ	TDK	RLF5018T-6R8M1R1
L3	Inductor	10 µH	0.94 A, 56 mΩ	TDK	RLF5018T-100MR94
T1	Transformer	—	—	SUMIDA	CLQ52 5388-T139
C1, C3, C5, C7	Ceramics Condenser	1 µF	25 V	TDK	C3216JB1E105K
C2, C4, C6, C8	Ceramics Condenser	2.2 µF	25 V	TDK	C3216JB1E225K
C9, C11	Ceramics Condenser	2.2 µF	25 V	TDK	C3216JB1E225K
C10, C16, C17	Ceramics Condenser	0.15 µF	16 V	TDK	C1608JB1C154M
C11, C12, C15	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C13	Ceramics Condenser	100 pF	50 V	TDK	C1608CH1H101J
C14	Ceramics Condenser	2200 pF	50 V	TDK	C1608JB1H222K
C18, C19	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C20	Ceramics Condenser	0.15 µF	16 V	TDK	C1608JB1C154M
C21 to C23	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
R9	Resistor	3.3 kΩ	0.5%	ssm	RR0816P-332-D
R10	Resistor	22 kΩ	0.5%	ssm	RR0816P-223-D
R11, R16	Resistor	15 kΩ	0.5%	ssm	RR0816P-153-D
R12, R17, R21	Resistor	1 kΩ	0.5%	ssm	RR0816P-102-D
R13	Resistor	6.8 kΩ	0.5%	ssm	RR0816P-682-D
R14	Resistor	3 kΩ	0.5%	ssm	RR0816P-302-D
R15	Resistor	43 kΩ	0.5%	ssm	RR0816P-433-D
R18	Resistor	12 kΩ	0.5%	ssm	RR0816P-123-D
R19	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R20	Resistor	10 kΩ	0.5%	ssm	RR0816P-103-D
R22	Resistor	33 kΩ	0.5%	ssm	RR0816P-333-D
R23, R26	Resistor	20 kΩ	0.5%	ssm	RR0816P-203-D
R24	Resistor	200 Ω	0.5%	ssm	RR0816P-201-D
R25	Resistor	9.1 kΩ	0.5%	ssm	RR0816P-912-D
R27	Resistor	1 kΩ	0.5%	ssm	RR0816P-102-D

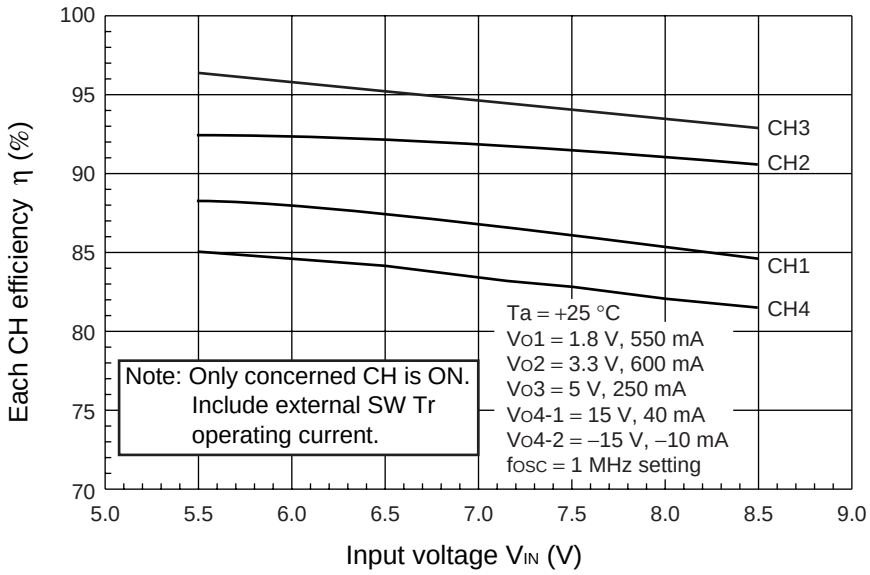
Note : SANYO : SANYO Electric Co., Ltd.
TDK : TDK Corporation
SUMIDA : SUMIDA Electric Co., Ltd.
ssm : SUSUMU Co., Ltd.

■ REFERENCE DATA

TOTAL Efficiency vs. Input Voltage



Each CH Efficiency vs. Input Voltage



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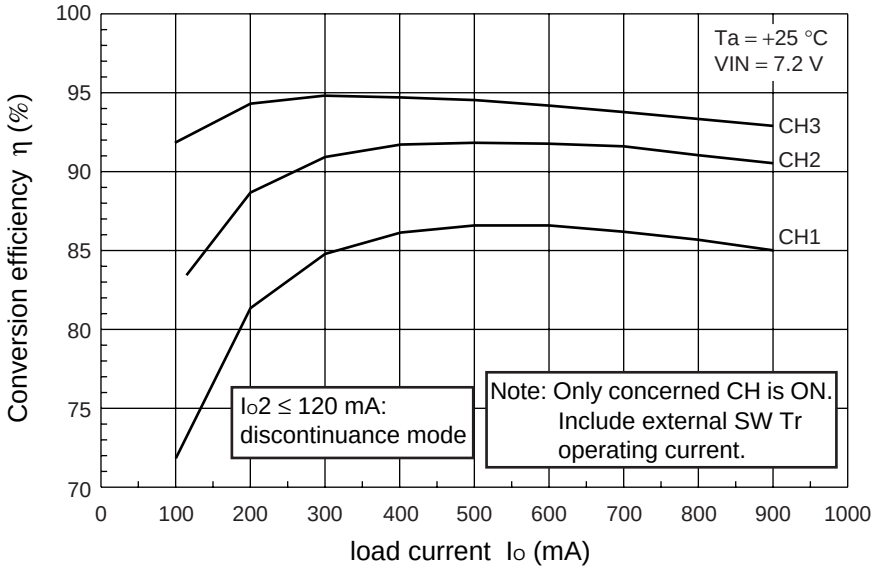
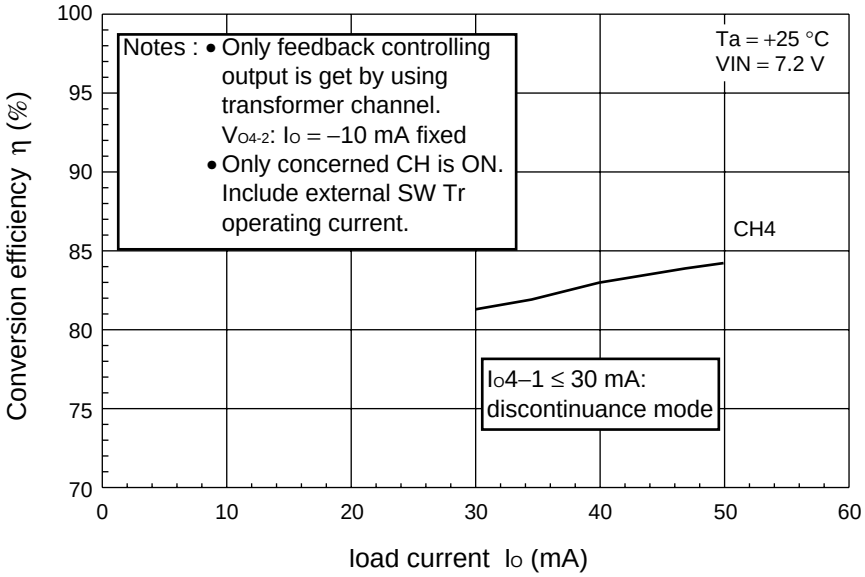
Conversion Efficiency vs. Load Current (CH1, CH2, CH3)



Conversion Efficiency vs. Load Current (CH4)



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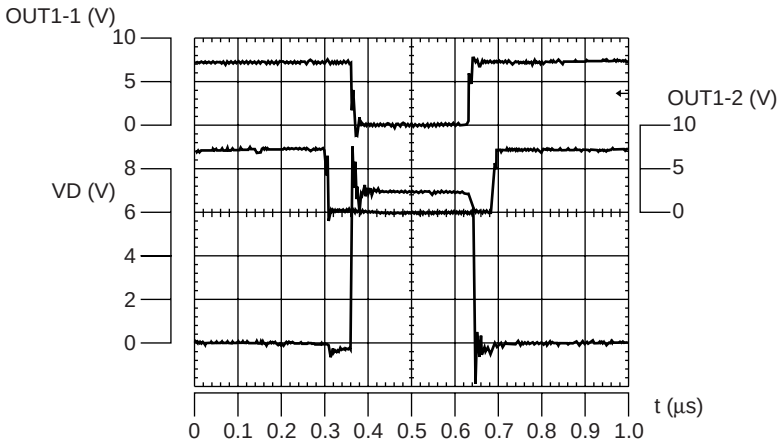
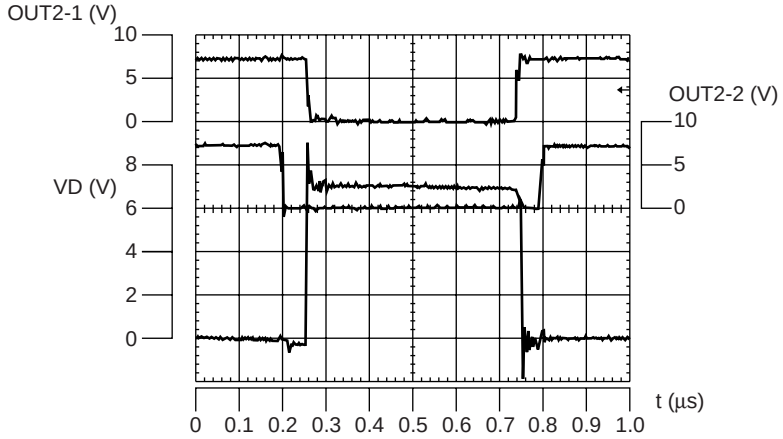
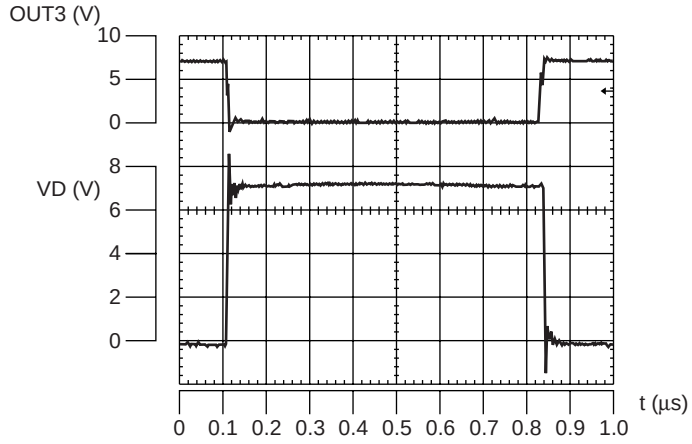
Switching Wave Form



CH1
VIN = 7.2 V
Vo1 = 1.8 V
Io1 = 550 mA



CH2
VIN = 7.2 V
Vo2 = 3.3 V
Io2 = 600 mA



CH3
VIN = 7.2 V
Vo3 = 5 V
Io3 = 250 mA

(Continued)

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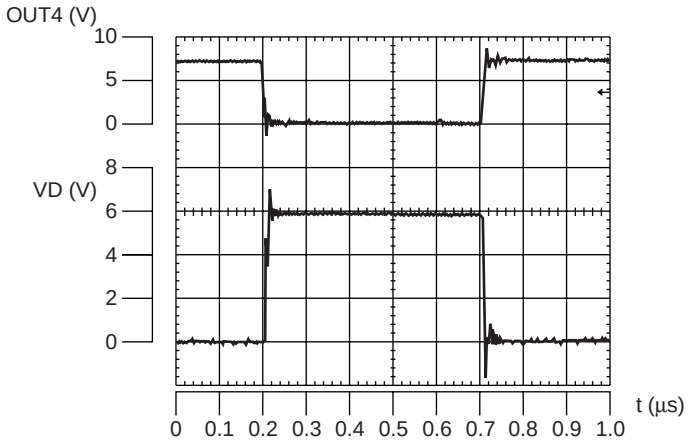


CH4
VIN = 7.2 V
$V_{O4\text{-}1}$ = 15 V
$I_{O4\text{-}1}$ = 40 mA
$V_{O4\text{-}2}$ = –15 V
$I_{O4\text{-}1}$ = –10 mA

■ USAGE PRECAUTION

• Printed circuit board ground lines should be set up with consideration for common impedance.

• Take appropriate static electricity measures.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

• Do not apply negative voltages.

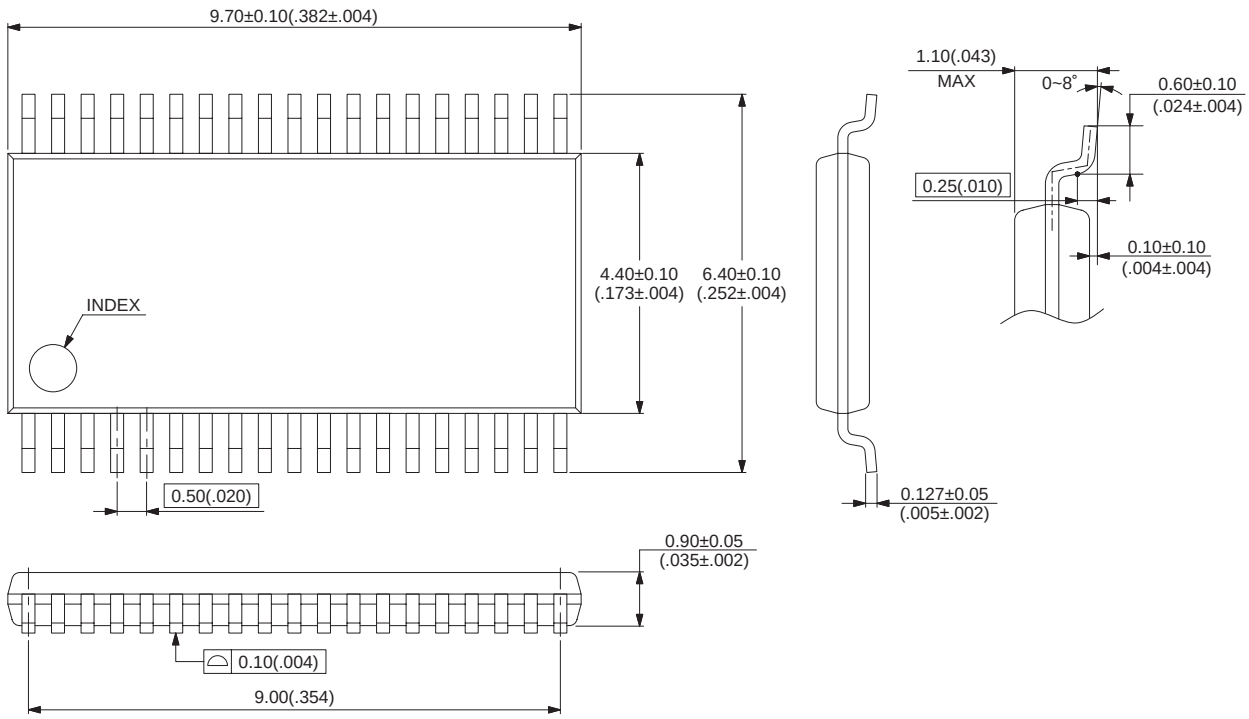
The use of negative voltages below –0.3 V may create parasitic transistors on LSI lines, which can cause abnormal operation.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB39A110PFT	38-pin plastic TSSOP (FPT-38P-M03)	

■ PACKAGE DIMENSION

38-pin plastic TSSOP
(FPT-38P-M03)



Dimensions in mm (inches)

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F0303