# M5L8289P

T-52-33-55

**BUS ARBITER**

## DESCRIPTION

The M5L8289P is a system bus (®MULTIBUS) arbiter for the MELPS 86, 88 16-bit microprocessors. When a request for access to the system bus is made by any of these microprocessors, the M5L8289P prevents simultaneous access by two or more processors by allowing only the first processor which requests access to access the system, preventing all others from accessing the system bus. It generates the required signals for bus access. (®MULTIBUS is a registered trademark of Intel Corporation.)

## FEATURES

- ®MULTIBUS compatible
- Usable in multiprocessing systems using the MELPS 86, 88 microprocessors
- Four modes of request and bus surrender are possible
- Low power dissipation

## APPLICATION

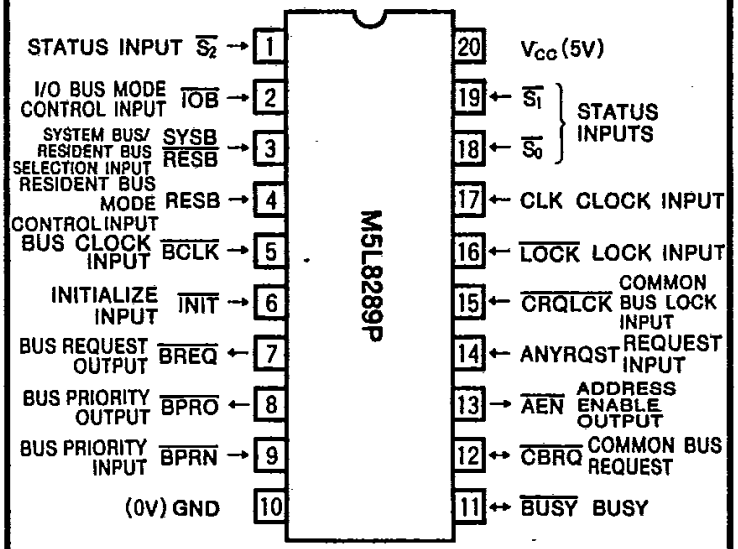
Bus arbitration for MULTIBUS boards using the MELPS 86, 88 or 8089

## FUNCTION

The M5L8289P is a bus arbiter for ®MULTIBUS boards using the MELPS 86, 88 microprocessors. When several processors are connected to the system bus (®MULTIBUS), it is necessary to prevent two or more processors from attempting to access the system bus simultaneously.

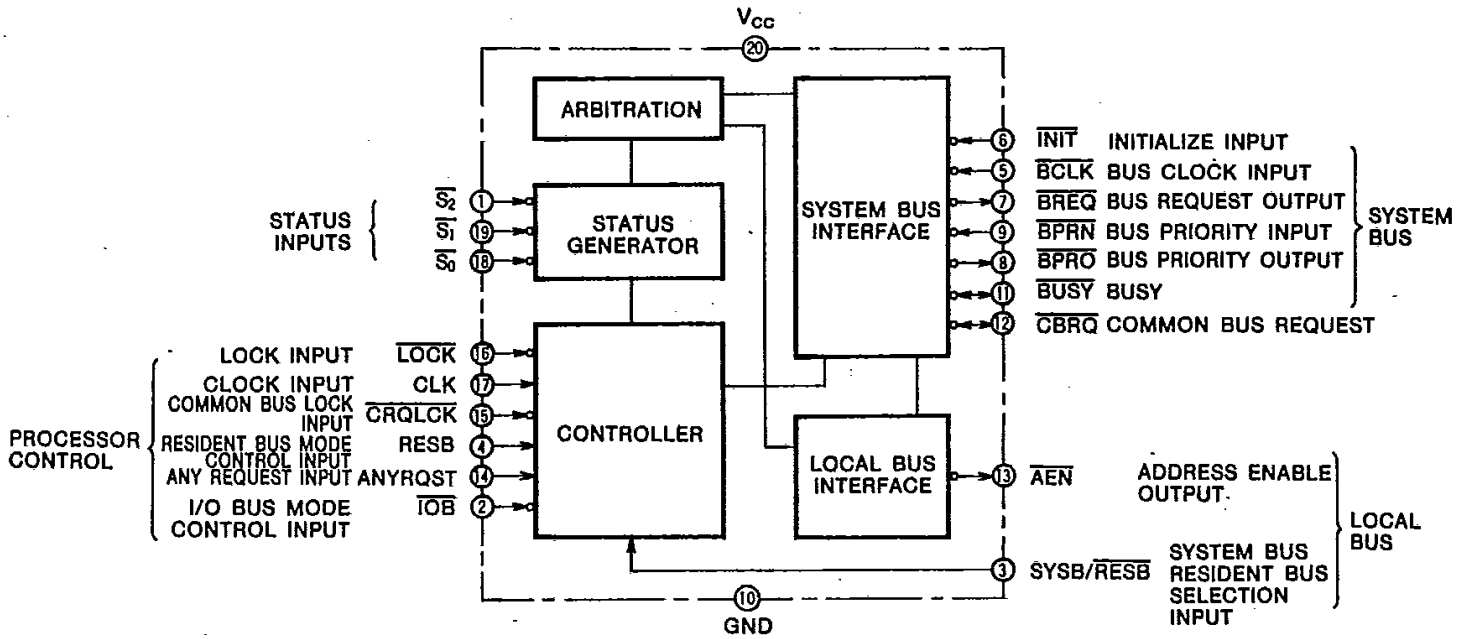
This function is performed by the M5L8289P, which decodes the processor status, and if access to the system bus is required, prevents other processors from attempting system bus access by generating the required control signals.

## PIN CONFIGURATION (TOP VIEW)




Outline 20P4

## BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

The M5L8289P decodes the status signals $\overline{S_0} \sim \overline{S_2}$ from the processor, and requests system bus privileges or surrenders them. The conditions for such operation are shown in Table 1. As shown in the Table 1, the following four modes are possible for use with boards of various types.

### (1) Single Bus Mode

In this mode there is neither memory nor I/O ports on the board, and the processor accesses only the system bus.

### (2) I/O Bus Mode

In this mode I/O ports exist on the board, and the processor accesses only these. For this mode the M5L8289P outputs a system bus request signal only for memory access.

### (3) Resident Bus Mode

In this mode both memory and/or I/O port(s) exist on the board and the processor can access both on the system bus. In this mode the chip select signal (active low) for I/O ports and memory on the system bus is input to SYSB/$\overline{\text{RESB}}$. By doing this, when the I/O port(s) and memory on the board are accessed, the M5L8289P does not output a request signal to the system bus.

### (4) I/O Bus Mode Resident Bus Mode

In this mode both I/O ports and memory are existent on the board, and only the I/O port on the board is accessed.

In this mode the chip select signal (active low) for memory on the board is input to SYSB/$\overline{\text{RESB}}$. By doing this, the M5L8289P outputs a request signal to the system bus when system memory is accessed.

In addition, the M5L8289P has the following control inputs.

- $\overline{\text{LOCK}}$

  This signal locks the bus arbitrate function when it is low, the M5L8289P continues to output a request signal to the system bus, and once acquired, setting $\overline{\text{LOCK}}$ to a high level retains bus privileges until the conditions listed in Table 1 are satisfied. Normally, this input is connected to th $\overline{\text{LOCK}}$ output of the processor.

- $\overline{\text{CRQLCK}}$

  This signal locks the arbitrate function by CBRQ. When set to low, the bus privilege surrender conditions listed in Table 1 in which CBRQ are input, are ignored. This input is set to low level when it is desired to prevent low-priority arbiters from acquiring bus privileges.

- ANYRQST

  Even after one bus access has been completed, the M5L8289P does not surrender bus privileges until the surrender conditions listed in Table 1 are satisfied. However, by setting the ANYRQST input to high, the bus can be freed after each single access, thereby facilitating the acquisition of bus privileges by low-priority arbiters.

## Table 1 M5M8289P Modes and Bus Request and surrender Conditions

| Status | | | | I/O Bus mode only | Resident bus mode only | | I/O Bus mode resident bus mode | | Single bus mode |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $\overline{IOB}$=L RESB=L | $\overline{IOB}$=H RESB=H | | $\overline{IOB}$=L RESB=H | | $\overline{IOB}$=H RESB=L |
| Command | $\overline{S_2}$ | $\overline{S_1}$ | $\overline{S_0}$ | | SYSB/$\overline{RESB}$=H | SYSB/$\overline{RESB}$=H | SYSB/$\overline{RESB}$=H | SYSB/$\overline{RESB}$=L | |
| Interrupt acknowledge | 0 | 0 | 0 | × | ○ | × | × | × | ○ |
| I/O Port read | 0 | 0 | 1 | × | ○ | × | × | × | ○ |
| I/O Write | 0 | 1 | 0 | × | ○ | × | × | × | ○ |
| Halt | 0 | 1 | 1 | × | × | × | × | × | × |
| Instruction fetch | 1 | 0 | 0 | ○ | ○ | × | ○ | × | ○ |
| Memory read | 1 | 0 | 1 | ○ | ○ | × | ○ | × | ○ |
| Memory write | 1 | 1 | 0 | ○ | ○ | × | ○ | × | ○ |
| Passive cycle | 1 | 1 | 1 | × | × | × | × | × | × |

○ ····· A request signal is output by the system bus.
× ····· The system bus privileges are surrendered.

| Mode | Input | | Bus request condition (excluding halt and passive cycles) | Bus surrender condition (Note 1) |
|---|---|---|---|---|
| | $\overline{IOB}$ | RESB | | |
| Single bus mode | H | L | All bus access states | HLT+(TI·$\overline{CBRQ}$)+HPBRQ |
| Resident bus mode only | H | H | (SYSB/$\overline{RESB}$=high)·(Bus access state) | ((SYSB/$\overline{RESB}$=L+T1)·CBRQ) +HLT+HPBRQ |
| I/O Bus mode only | L | L | All memory access states | (I/O Access state+T1)·CBRQ)+HLT +HPERQ |
| I/O Bus mode resident bus mode | L | H | (SYSB/$\overline{RESB}$=high)·(Memory access states) | ((I/O Access state +(SYSB/$\overline{RESB}$=low))· CBRQ + HPBRQ HLT +HPBRQ |

Note 1 : When $\overline{LOCK}$=low, the bus is not released under any circumstances.
When $\overline{CRQLCK}$=low, the bus is not released even when low-priority arbiters request it.
2 : HLT·····Halt state
TI·····Idle (passive) state
CBRQ·····$\overline{CBRQ}$=low
HPBRQ ·····Indicates that a high-priority arbiter is requesting the bus ($\overline{BPRN}$=high)

## PIN DESCRIPTION

| Pin | Name | Input or output | Function |
|---|---|---|---|
| $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ | Status input | In | Status input from the processor. The M5L8289P decodes this signal and based on it, requests or surrenders bus privileges. |
| CLK | Clock input | In | This is the same clock input as used on the processor, and used for decoding of the status. It receives the clock from the M5L8284AP. |
| $\overline{LOCK}$ | Lock input | In | This is the lock input signal from the processor. When $\overline{LOCK}$=low, the M5L8289P will, in no circumstances, surrender bus privileges. |
| $\overline{CRQLCK}$ | Common bus request lock input | In | This is the lock signal for arbitration from a common bus request. When $\overline{CRQLCK}$=low, the M5L8289P ignores bus surrendering conditions by signal CBRQ. |
| RESB | Resident bus mode control input | In | This is the M5L8289P mode setting input. When RESB=high, the M5L8289P is in the resident bus mode. |
| $\overline{IOB}$ | I/O Bus mode control input | In | This is an M5L8289P mode setting input. When $\overline{IOB}$=low, the M5L8289P is in the I/O bus mode. |
| ANYRQST | Any request input | In | This controls the bus surrendering conditions for the M5L8289P. When ANYRQST=low, the M5L8289P releases the bus under the conditions listed in Table 1. When ANYRQST=high, as soon as $\overline{CBRQ}$ goes low, the bus is released. Therefore, by setting ANYRQST to high and $\overline{CBRQ}$ to low, the M5L8289P can be made to release the bus after a single access. |
| SYSB/$\overline{RESB}$ | System bus/resident bus selection input | In | This input is valid when the M5L8289P is in the resident bus mode. When SYSB/$\overline{RESB}$=low, this means that the processor is accessing the bus on the board, and the M5L8289P does not output a request to the system bus. When SYSB/$\overline{RESB}$=high, this indicates that the processor is accessing the system bus, and the M5L8289P outputs the request signal to the system bus. |
| $\overline{BCLK}$ | Bus lock input | In | This is the clock for arbitration of other boards. The M5L8289P performs arbitration in synchronous with this clock. It is fed from the system bus $\overline{BCLK}$ signal. |
| $\overline{INIT}$ | Initialize input | In | This line resets the arbitration circuit. Immediately after resetting, none of the arbiters have system bus privileges. This input is fed from the system bus $\overline{INIT}$ signal. |
| $\overline{BREQ}$ | Bus request output | Out | This signal requests system bus privileges. It is used as the system bus $\overline{BREQ}$ signal. |
| $\overline{BPRN}$ | Bus priority input | In | This signal indicates whether a high-priority arbiter has requested privileges or not. When $\overline{BPRN}$=low, a high-priority arbiter has not requested privileges and when $\overline{BPRN}$=high, this indicates that a high-priority arbiter has requested privileges. This input is fed from the system bus $\overline{BPRN}$ signal. |
| $\overline{BPRO}$ | Bus priority output | Out | This signal indicates whether the M5L8289P or high-order arbiter has requested the bus. When $\overline{BPRO}$=low, there was a bus request and when $\overline{BPRO}$=high, there was no bus request. This signal is used as the system bus $\overline{BPRO}$ signal. |
| $\overline{BUSY}$ | Busy | In/Out | This signal indicates that the system bus has been acquired. When $\overline{BUSY}$=low, the bus is busy and when $\overline{BUSY}$=high, it indicates that no arbiter has acquired the bus privileges. When the M5L8289P has acquired bus privileges, a low-level output (open collector) is made. This signal is used as the system bus $\overline{BUSY}$ signal. |
| $\overline{CBRQ}$ | Common bus request | In/Out | This signal indicates when any arbiter has requested the system bus. When $\overline{CBRQ}$=low, the M5L8289P releases the bus according to the conditions listed in Table1. When making a request of the system bus, $\overline{CBRQ}$ is output as low (open collector). This signal is used as the system bus $\overline{CBRQ}$ signal. |
| $\overline{AEN}$ | Address enable input | Out | This signal informs the bus buffer on the board that the system bus has been acquired. It is connected to the address and data buffer outputs, and the output enable line on the board as well as the M5L8288P $\overline{AEN}$ line. |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5～7 | V |
| $V_I$ | Input voltage | | −1～5.5 | V |
| $V_O$ | Output voltage | | −0.5～7 | V |
| $T_{opr}$ | Operating temperature | | 0～75 | ℃ |
| $T_{stg}$ | Storage temperature | | −65～150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS ($T_a$=0～75℃, unless otherwise noted)

| Symbol | Parameter | | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | | | 4.5 | 5 | 5.5 | V |
| $I_{OH}$ | High-level output current | $\overline{BUSY}$, $\overline{CBRQ}$, | $V_{OH}$≧2.4V | Open collector | | | μA |
| | | Other output, | $V_{OH}$≧2.4V | 0 | | 400 | |
| $I_{OL}$ | Low-level output current | $\overline{BUSY}$, $\overline{CBRQ}$, | $V_{OL}$≦0.45V | 0 | | 20 | mA |
| | | $\overline{AEN}$ | $V_{OL}$≦0.45V | 0 | | 16 | |
| | | $\overline{BPRO}$, $\overline{BREQ}$, | $V_{OL}$≦0.45V | 0 | | 10 | |

## ELECTRICAL CHARACTERISTICS ($T_a$=0～75℃, $V_{CC}$=5V±10%, unless otherwise noted)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | | | 2.0 | | | V |
| $V_{OL}$ | Low-level output voltage | $\overline{BUSY}$, $\overline{CBRQ}$ | $I_{OL}$=20mA | | | 0.45 | V |
| | | $\overline{AEN}$ | $I_{OL}$=16mA | | | 0.45 | |
| | | $\overline{BPRO}$, $\overline{BREQ}$ | $I_{OL}$=10mA | | | 0.45 | |
| $V_{OH}$ | High-level output voltage | $\overline{BUSY}$, $\overline{CBRQ}$ | | Open collector | | | V |
| | | $\overline{AEN}$, $\overline{BPRO}$, $\overline{BREQ}$ | $I_{OH}$=400μA | 2.4 | | | |
| $V_{IC}$ | Input clamp voltage | | $V_{CC}$=4.50V, $I_C$=−5mA | | | −1 | V |
| $I_{IL}$ | Low-level input current | | $V_{CC}$=5.50V, $V_F$=0.45V | | | −0.5 | mA |
| $I_{IH}$ | High-level input current | | $V_{CC}$=5.50V, $V_R$=5.50V | | | 60 | μA |
| $I_{CC}$ | Supply current | | | | | 120 | mA |
| $C_{IN}$ | Input capcitance | Status | f=1MHz, $V_{B2AS}$=2.5V | | | 25 | pF |
| | | Others | | | | 12 | |

## TIMING REQUIREMENT ($T_a$=0~75℃, $V_{CC}$=5V±10%, unless otherwise noted)

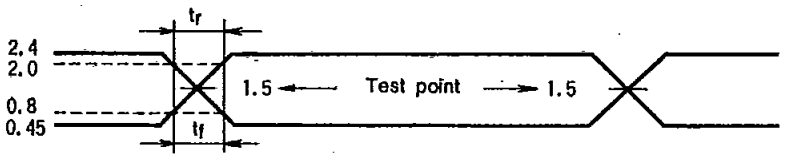
| Symbol | Parameter | Alternate symbol | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $t_{C(CLK)}$ | CLK cycle period | $t_{CLCL}$ | | 125 | | | ns |
| $t_{W(CLKL)}$ | CLK"L" pulse width | $t_{CLCH}$ | | 65 | | | ns |
| $t_{W(CLKH)}$ | CLK"H" pulse width | $t_{CHCL}$ | | 35 | | | ns |
| $t_{su(\overline{S0}\sim\overline{S2})}$ | Status active setup time | $t_{SVCH}$ | | 65 | | $t_{CLCL}$-10 | ns |
| $t_{h(\overline{S0}\sim\overline{S2})}$ | Status active hold time | $t_{CHSV}$ | | 10 | | $t_{CLCL}$-10 | ns |
| $t_{su(\overline{S0}\sim\overline{S2})}$ | Status inactive setup time | $t_{SHCL}$ | | 50 | | | ns |
| $t_{h(\overline{S0}\sim\overline{S2})}$ | Status inactive hold time | $t_{CLSH}$ | | 10 | | | ns |
| $t_{h(\overline{LOCK})}$ | $\overline{LOCK}$ inactive hold time | $t_{CLLL1}$ | | 10 | | | ns |
| $t_{su(LOCK)}$ | LOCK active setup time | $t_{CLLL2}$ | | 40 | | | ns |
| $t_{su(SYSB/\overline{RESB})}$ | SYSB/$\overline{RESB}$ setup time | $t_{CLSR1}$ | | 0 | | | ns |
| $t_{h(SYSB/\overline{RESB})}$ | SYSB/$\overline{RESB}$ hold time | $t_{CLSR2}$ | | 20 | | | ns |
| $t_{C(\overline{BCLK})}$ | $\overline{BCLK}$ cycle time | $t_{BLBL}$ | | 100 | | | ns |
| $t_{W(\overline{BCLKH})}$ | $\overline{BCLK}$"H" pulse width | $t_{BHBL}$ | | 30 | | | ns |
| $t_{su(\overline{BPRU})}$ | $\overline{BPRN}$ ↑ ↓ to $\overline{BCLK}$ setup time | $t_{PNSBL}$ | | 15 | | | ns |
| $t_{su(\overline{BUSY})}$ | $\overline{BUSY}$ ↑ ↓ to $\overline{BCLK}$ ↓ setup time | $t_{BYSBL}$ | | 20 | | | ns |
| $t_{su(\overline{CBRQ})}$ | $\overline{CBRQ}$ ↑ ↓ to $\overline{BCLK}$ ↓ setup time | $t_{CBSBL}$ | | 20 | | | ns |
| $t_{W(INIT)}$ | INIT pulse width | $t_{IVIH}$ | | $3t_{BLBL}+3t_{CLCL}$ | | | ns |
| $t_r$ | Input rise time | $t_{ILIH}$ | 0.8~2V | | | 20 | ns |
| $t_f$ | Input fall time | $t_{IHIL}$ | 2~0.8V | | | 12 | ns |

## SWITCHING CHARACTERISTICS ($T_a$=0~75℃, $V_{CC}$±5V±5%, unless otherwise noted)

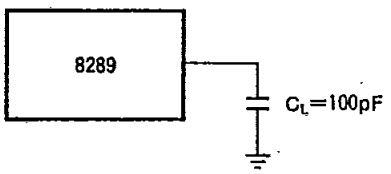
| Symbol | Parameter | Alternate symbol | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $t_{PHL(\overline{BREQ})}$ | $\overline{BCLK}$→$\overline{BREQ}$ ↑; ↓ Delay time | $t_{BLBRL}$ | | | | 35 | ns |
| $t_{PLH(\overline{BPRO})}$ | $\overline{BCLK}$→$\overline{BPRO}$ ↑, ↓ Delay time (See note 2) | $t_{BLPOH}$ | | | | 40 | ns |
| $t_{PHL(\overline{BPRO})}$ | $\overline{BPRN}$ ↑, ↓→$\overline{BPRO}$ ↑ ↓ Delay time (See note 2) | $t_{PNPO}$ | | | | 25 | ns |
| $t_{PHL(\overline{BUSY})}$ | $\overline{BCLK}$→$\overline{BUSY}$ ↓ Delay time | $t_{BLBYL}$ | | | | 60 | ns |
| $t_{PLZ(\overline{BUSY})}$ | $\overline{BCLK}$→$\overline{BUSY}$ Float time (See note 3) | $t_{BLBYH}$ | | | | 35 | ns |
| $t_{PLH(\overline{AEN})}$ | CLK→$\overline{AEN}$, ↑ Delay time | $t_{CLAEH}$ | | | | 65 | ns |
| $t_{PHL(\overline{AEN})}$ | $\overline{BCLK}$→$\overline{AEN}$, ↓ Delay time | $t_{BLAEL}$ | | | | 40 | ns |
| $t_{PHL(\overline{CBRQ})}$ | $\overline{BCLK}$→$\overline{CBRQ}$, ↓ Delay time | $t_{BLCBL}$ | | | | 60 | ns |
| $t_{PLZ(\overline{CBRQ})}$ | $\overline{BCLK}$→$\overline{CBRQ}$ Delay time (See note 3) | $t_{BLCBH}$ | | | | 35 | ns |
| $t_r$ | Output rise time | $t_{OLOH}$ | 0.8V~2.0V | | | 20 | ns |
| $t_f$ | Output fall time (See note 4, 5) | $t_{OHOL}$ | 2.0V~0.8V | | | 12 | ns |

Note 1 : Symbol ↑, ↓ means rise signal and fall signal.
2 : $\overline{BCLK}$ generate the first $\overline{BPRO}$ and then BPRO changes lower in the chain are generated through BPRN.
3 : Measured at 0.5V above GND

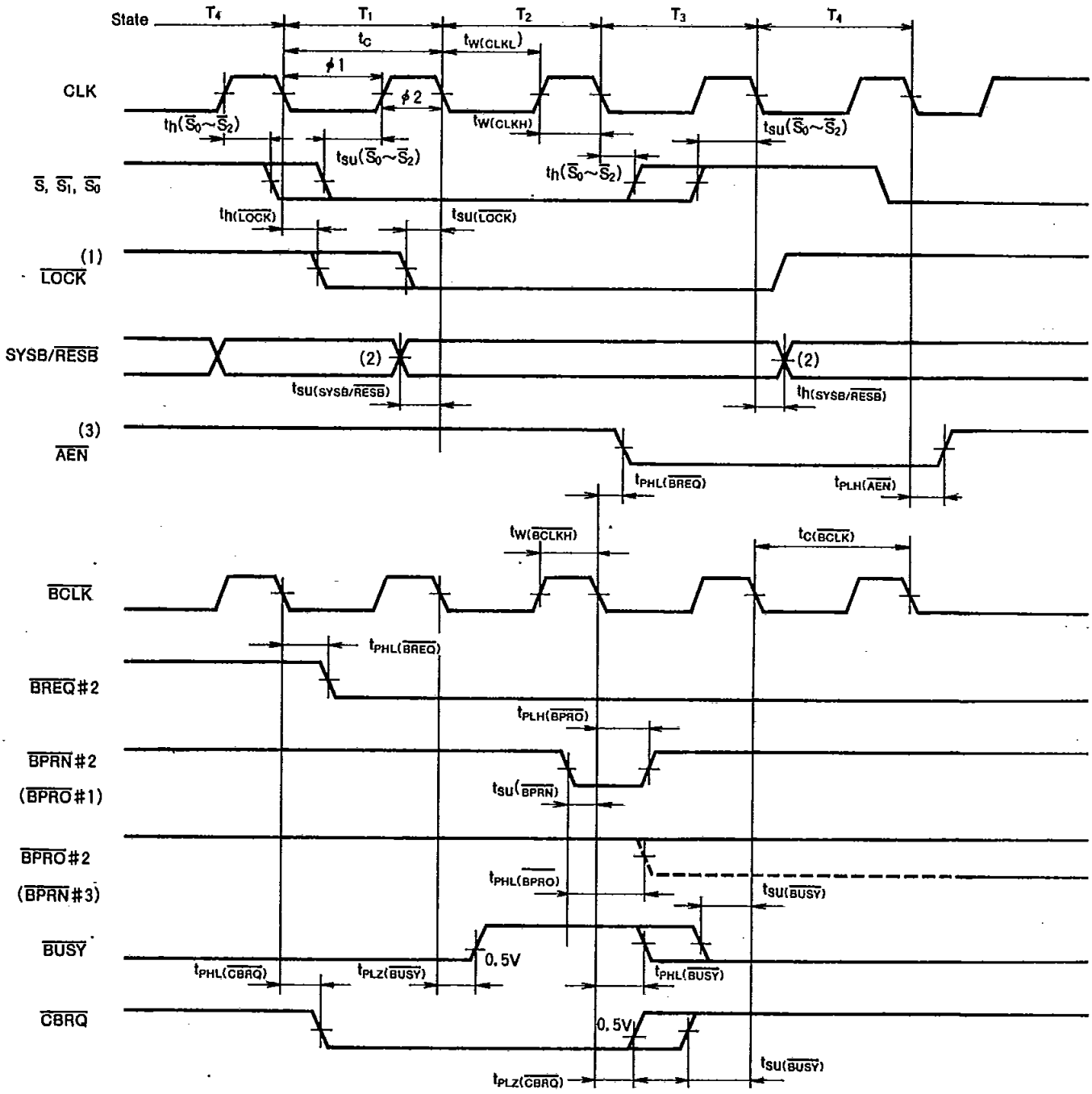
Note 4 : A.C. test wave form.




Note 5 : Load circuit



## TIMING DIAGRAM




Note 1 : LOCK can be active during any state as long as the relation ships shown above with the respect to CLK are maintained.
LOCK can be inactive asynchronously.
CRQLCK is an asynchronous input signal.

2 : Noise is permitted during this time. After φ2 of T1 and before φ1 of T4 should be stable.

3 : AEN negative-edge is related to CLK, positive-edge to CLK.
ANE positive-edge is generated after as ricrity is lost.