

# MOS FIELD EFFECT TRANSISTOR 2SK2411, 2SK2411-Z

## SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

### DESCRIPTION

The 2SK2411 is N-Channel MOS Field Effect Transistor designed for high speed switching applications.

### FEATURES

- Low On-Resistance  
 $R_{DS(on)1} = 40 \text{ m}\Omega \text{ MAX. (@ } V_{GS} = 10 \text{ V, } I_D = 15 \text{ A)}$   
 $R_{DS(on)2} = 60 \text{ m}\Omega \text{ MAX. (@ } V_{GS} = 4 \text{ V, } I_D = 15 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 1500 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

### QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

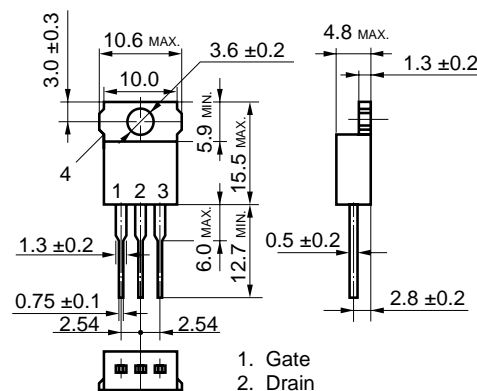
### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25 \text{ }^\circ\text{C}$ )

Drain to Source Voltage	$V_{DS}$	60	V
Gate to Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 30$	A
Drain Current (pulse)*	$I_{D(pulse)}$	$\pm 120$	A
Total Power Dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ )	$P_{T1}$	75	W
Total Power Dissipation ( $T_A = 25 \text{ }^\circ\text{C}$ )	$P_{T2}$	1.5	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current**	$I_{AS}$	30	A
Single Avalanche Energy**	$E_{AS}$	90	mJ

\*  $PW \leq 10 \text{ } \mu\text{s}$ , Duty Cycle  $\leq 1 \%$

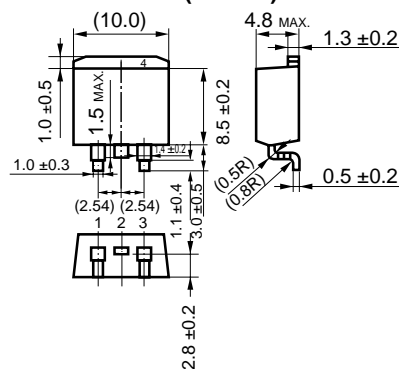
\*\* Starting  $T_{ch} = 25 \text{ }^\circ\text{C}$ ,  $R_G = 25 \text{ } \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$

### PACKAGE DIMENSIONS (in millimeter)

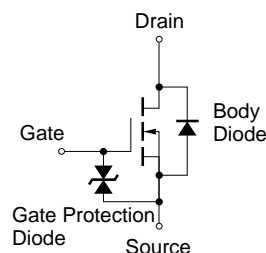


1. Gate
  2. Drain
  3. Source
  4. Fin (Drain)
- JEDEC: TO-220AB

### MP-25 (TO-220)



### MP-25Z (SURFACE MOUNT TYPE)

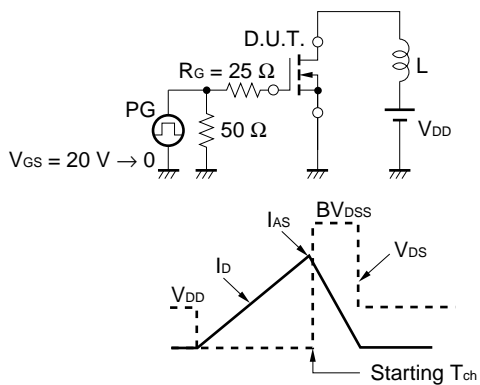


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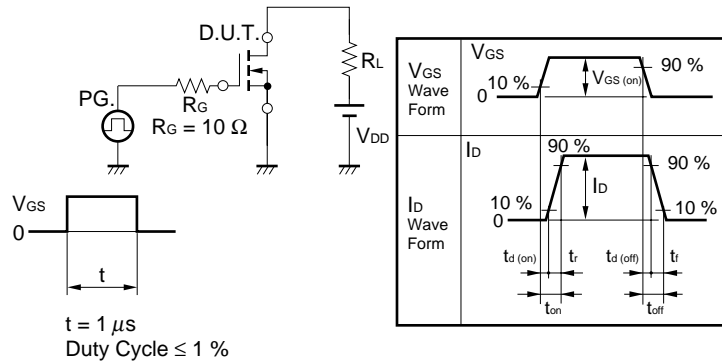
**ELECTRICAL CHARACTERISTICS (TA = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	$R_{DS(on)1}$		31	40	mΩ	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$
Drain to Source On-Resistance	$R_{DS(on)2}$		40	60	mΩ	$V_{GS} = 4\text{ V}, I_D = 15\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0	1.5	2.0	V	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	15	27		S	$V_{DS} = 10\text{ V}, I_D = 15\text{ A}$
Drain Leakage Current	$I_{DSS}$			10	μA	$V_{DS} = 60\text{ V}, V_{GS} = 0$
Gate to Source Leakage Current	$I_{GSS}$			±10	μA	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0$
Input Capacitance	$C_{iss}$		1500		pF	$V_{DS} = 10\text{ V}$
Output Capacitance	$C_{oss}$		720		pF	$V_{GS} = 0$
Reverse Transfer Capacitance	$C_{rss}$		190		pF	$f = 1\text{ MHz}$
Turn-On Delay Time	$t_{d(on)}$		20		ns	$I_D = 15\text{ A}$
Rise Time	$t_r$		260		ns	$V_{GS(on)} = 10\text{ V}$
Turn-Off Delay Time	$t_{d(off)}$		130		ns	$V_{DD} = 30\text{ V}$
Fall Time	$t_f$		150		ns	$R_G = 10\ \Omega$
Total Gate Charge	$Q_G$		50		nC	$I_D = 30\text{ A}$
Gate to Source Charge	$Q_{GS}$		5.0		nC	$V_{DD} = 48\text{ V}$
Gate to Drain Charge	$Q_{GD}$		15		nC	$V_{GS} = 10\text{ V}$
Body Diode Forward Voltage	$V_{F(S-D)}$		1.1		V	$I_F = 30\text{ A}, V_{GS} = 0$
Reverse Recovery Time	$t_{rr}$		110		ns	$I_F = 30\text{ A}, V_{GS} = 0$
Reverse Recovery Charge	$Q_{rr}$		320		nC	$di/dt = 100\text{ A}/\mu\text{s}$

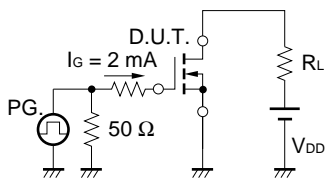
**Test Circuit 1 Avalanche Capability**



**Test Circuit 2 Switching Time**

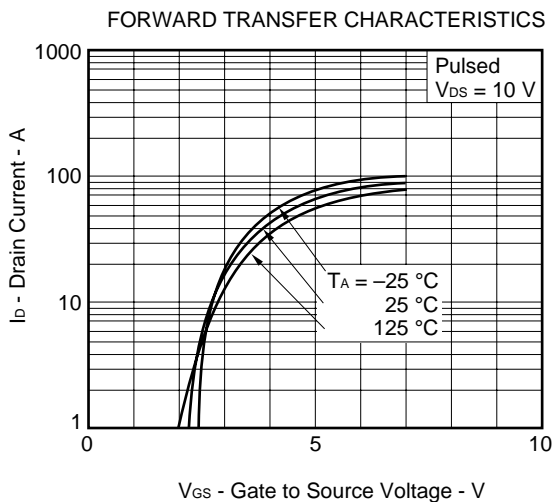
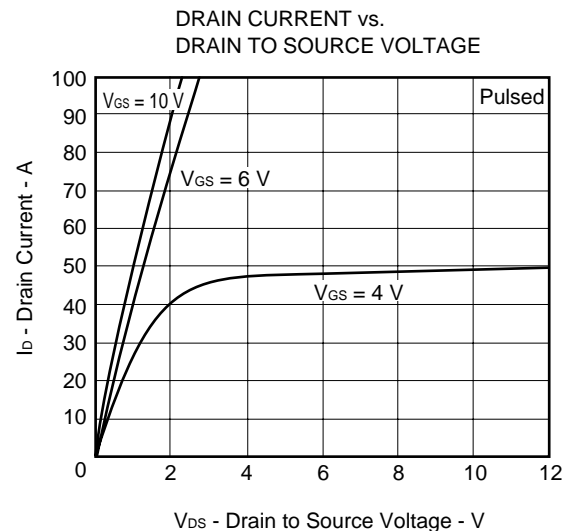
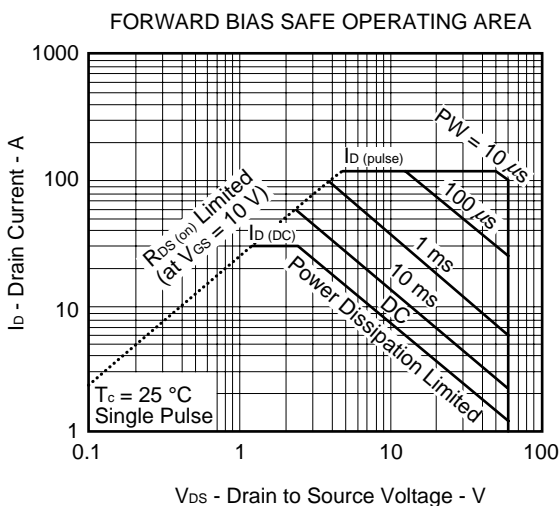
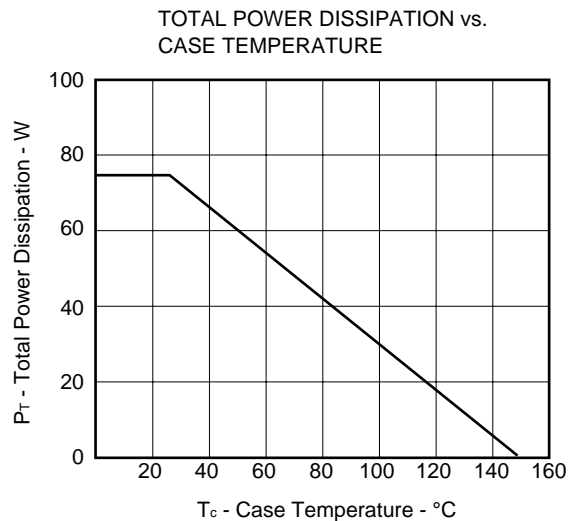
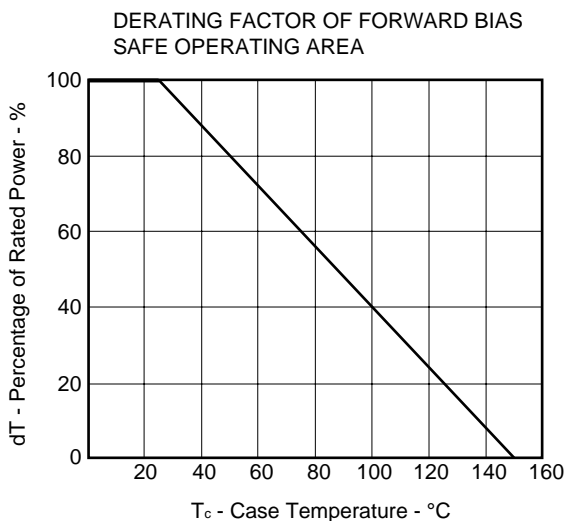


**Test Circuit 3 Gate Charge**

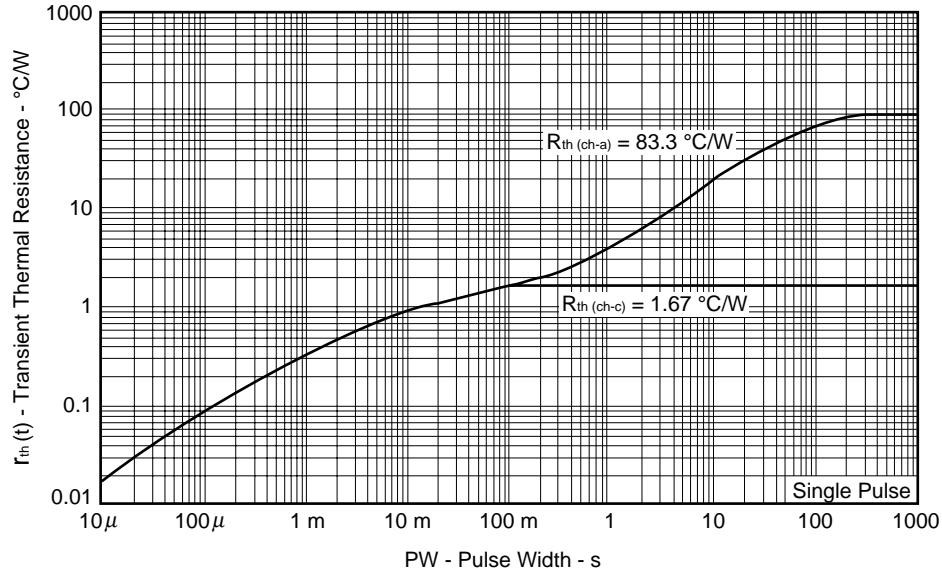


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

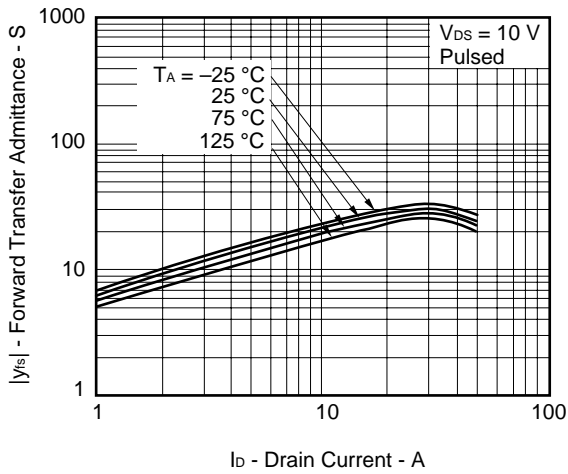
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)



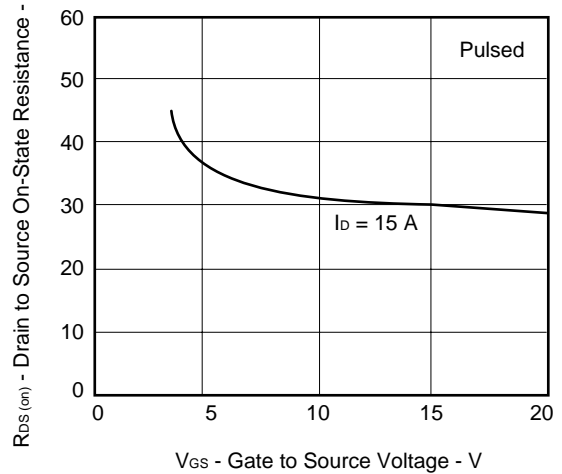
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



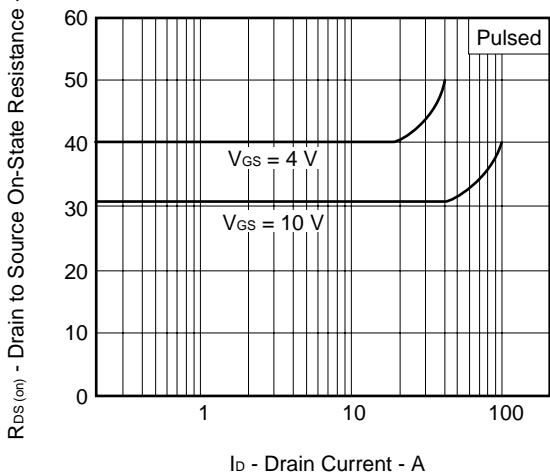
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



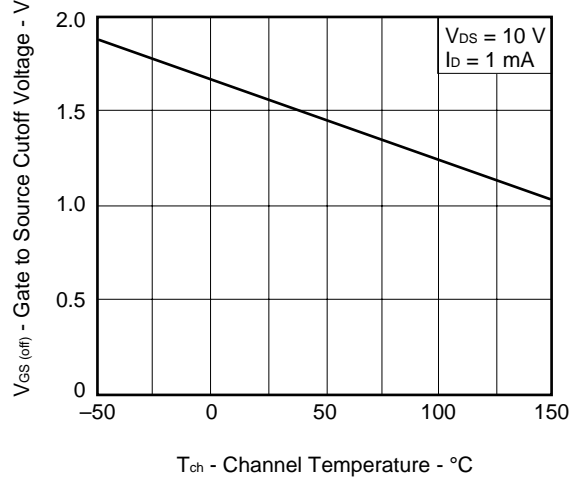
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

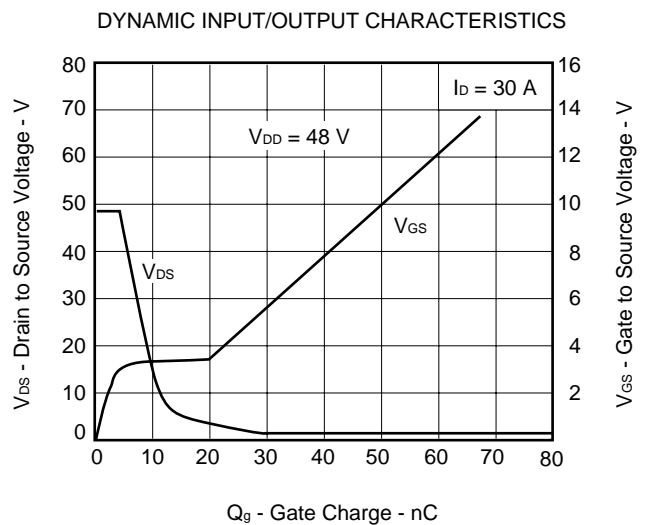
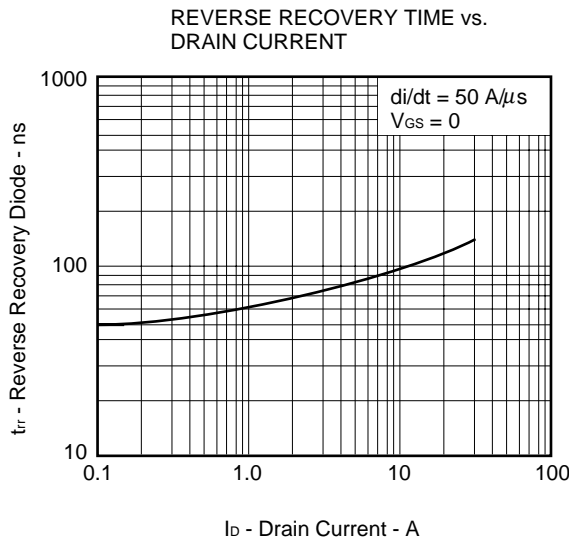
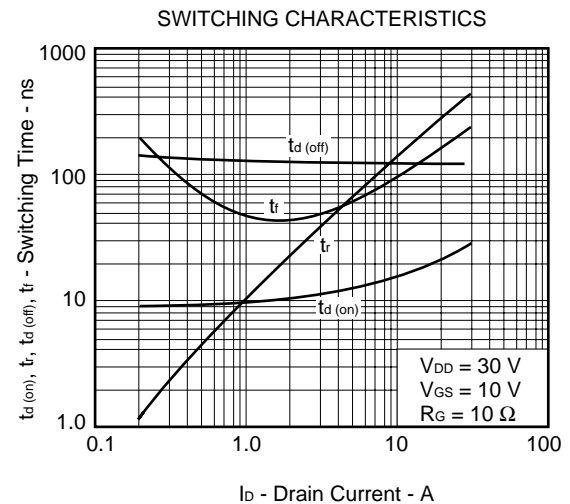
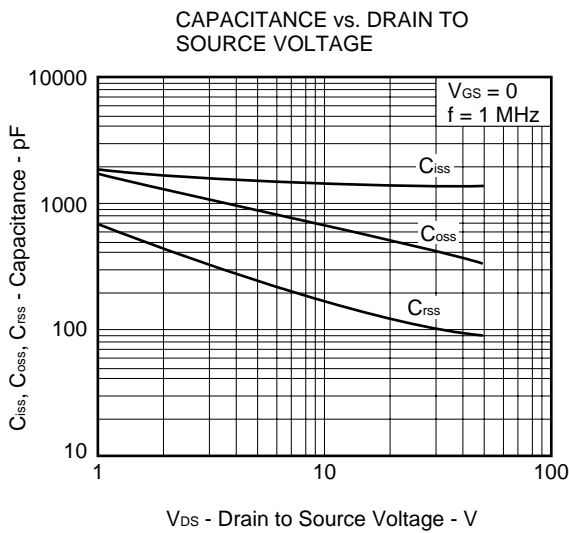
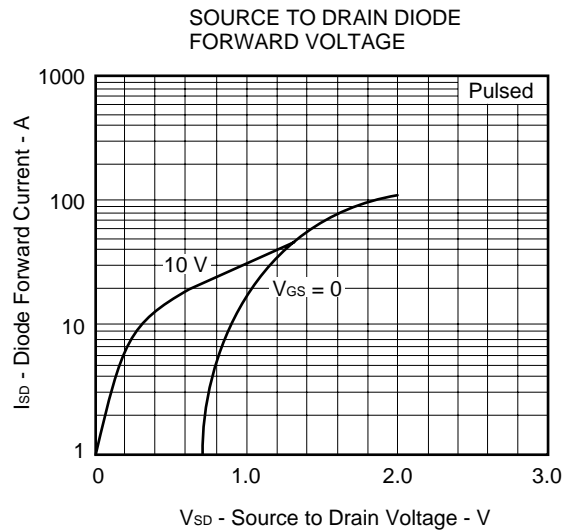
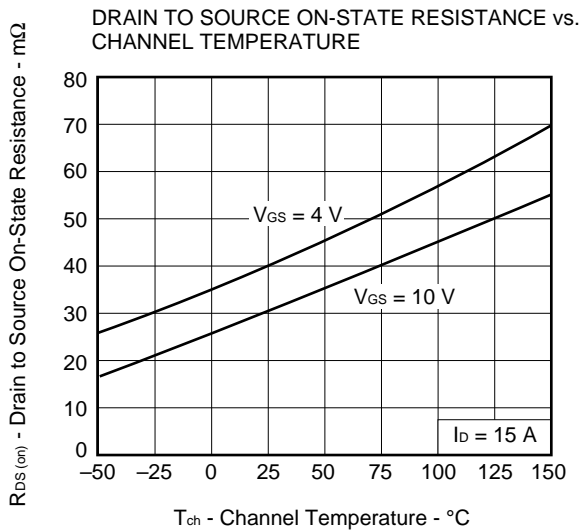


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

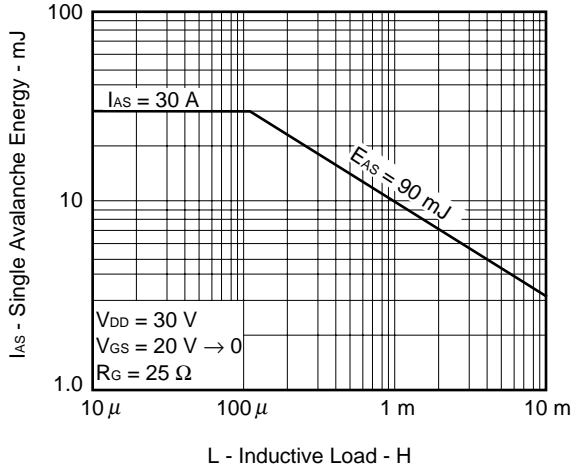


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

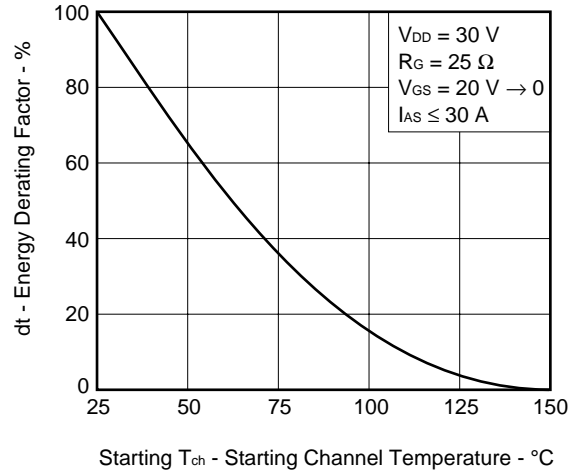




SINGLE AVALANCHE ENERGY vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



## REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	C11745E
Quality grade on NEC semiconductor devices.	C11531E
Semiconductor device mounting technology manual.	C10535E
IC package manual.	C10943X
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	X10679E
Power MOS FET features and application switching power supply.	D12971E
Application circuits using Power MOS FET.	D12972E
Safe operating area of Power MOS FET.	D13085E

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Anti-radioactive design is not implemented in this product.