CX2002

0.5µm CMOS ASIC Production Family

Introduction

The CX2002 is a 0.5µm CMOS triple-metal module array product used for high-volume cost reduction, production. CX2002 provides a migration path from the prototyping and production phase that is typically done with the 0.6µm CX2001 product family.

The decrease in die size from 0.6µm to the 0.5µm technology allows for reduced production prices. In addition, the CX2002 features 25% lower power consumption and 20% higher core utilization than the comparable CX2001 device. The no-risk migration from the CX2001 family to the CX2002 technology is achieved by using the same synthesized netlist, test vectors, and package type.

Sixteen-week lead-time is available for high-volume production.

Features

- 0.5µm CMOS TLM process
- 3.3V or 5V operation with mixed mode I/O
- 5V tolerance with reference voltage
- PCI compliant outputs (3.3V / 5V)
- Power dissipation:
  - 2.1µW / MHz / Gate @ 5V
  - 0.86µW / MHz / Gate @ 3.3V
- 800 MHz maximum flip-flop toggle rate
- Analog PLL operating frequency up to 250 MHz
- Embedded memory
  - Configurable as single-port RAM, dual-port RAM or ROM
  - Worst-case cycle performance: 200 MHz @ 5V; 150 MHz @ 3.3V
  - Fully static, synchronized RAM

CX2002 Product

Master Slice	Estimated Usable Gates	Embedded Memory Bits	Max Memory Instantiations	APLL	Max I/O
CX2022	10k	2k	1	3	120
CX2052	25k	32k	8	2	208

Cell Library

- Synopsys DC and DesignWare support
- Low power flip-flops
- Built-in scan MUX in flip-flops
- 26 simple gates; 36 complex gates
- 31 flip-flops
- 24 latches
- Multiplexers, decoders
- Tristate / drive cells
- 1280 input / output buffers

Power Pin Assignment

All I/O cells are programmable as VDD, VSS, input, output, or bi-directional. This flexibility allows the user to properly ratio power pins with output drive requirements or match specific pin-out when replacing existing devices.

Input & Output Bi-Directional Cells

The CX2002 library contains a large selection of input, output, and bi-directional cells that enable a wide range of designs. Input cells can be personalized with internal pull-up or pull-down resistors and with or without hysteresis. Output cells include slew rate control, current drive capability from 2mA to 12mA, as well as N channel and P channel open drains. If required, outputs can be used in parallel to enable increased drive capability. Each I/O can be programmed independently for 3.3V or 5V.

Recommended Operating Conditions

Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
V_{DD}	Supply voltage	0	7.0	V
V_{DDIO}	I/O supply voltage	0	5.5	V
V_{IN}	DC input voltage	-0.3	VDD+0.3	V
T_J	Junction temperature	--	150	°C
T_{STG}	Storage temperature	-65	150	°C
T_{SOL}	Soldering lead temperature (10 seconds)	--	210	°C

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{DD}	Supply voltage	Commercial (0°C ≤ T_J ≤ 100°C)	4.75	5.25	V
		Industrial (-40°C ≤ T_J ≤ 115°C)	4.75	5.25	V
		Military (-55°C ≤ T_J ≤ 125°C)	4.75	5.25	V
V_{IH}	Input high voltage	TTL inputs	2.0	VDD	V
		CMOS inputs	0.7 VDD	VDD	V
V_{IL}	Input low voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	0.3 VDD	V
T_{IN}	Input signal transition time		--	10	nS

DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	Output high voltage	TTL outputs	3.5	--	V
		CMOS outputs	3.5	--	V
V_{OL}	Output low voltage	TTL outputs	--	0.45	V
		CMOS outputs	--	0.45	V
I_{IN}	Input leakage current		-10	10	µA
C_{IN}	Input capacitance	QFP packages	--	--	Note 1
		BGA packages	--	--	Note 1

Note 1:
Please refer to current packaging information on our website (www.chipexpress.com / design).

For More Info

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