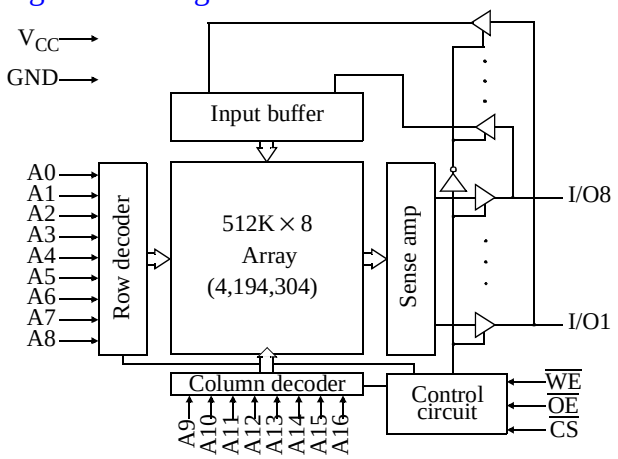
2.7V to 3.3V 512K × 8 Intelliwatt™ low-power CMOS SRAM

Features

- AS6VA5128
- Intelliwatt™ active power circuitry
- Industrial and commercial temperature ranges available
- Organization: 524,288 words × 8 bits
- 2.7V to 3.3V at 55 ns
- Low power consumption: ACTIVE
  - 132 mW at 3.3V and 55 ns
- Low power consumption: STANDBY
  - 66 µW max at 3.3V
- 1.2V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CS}$, $\overline{OE}$ inputs
- Smallest footprint packages
  - 36(48)-ball FBGA
  - 32-pin TSOP I and TSOP II packages are available on Alliance AS6UB5128 product family (available January 2001)
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



48-CSP BGA Package (shading indicates no ball)

	1	2	3	4	5	6
A	A_0	A_1	NC	A_3	A_6	A_8
B	I/O_5	A_2	$\overline{WE}$	A_4	A_7	I/O_1
C	I/O_6		NC	A_5		I/O_2
D	V_{SS}					V_{CC}
E	V_{CC}					V_{SS}
F	I/O_7		A_{18}	A_{17}		I/O_3
G	I/O_8	$\overline{OE}$	$\overline{CS}$	A_{16}	A_{15}	I/O_4
H	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}

Selection guide

Product	V_{CC} Range Min (V)	V_{CC} Range Typ[2] (V)	V_{CC} Range Max (V)	Speed (ns)	Power Dissipation Operating (I_{CC}) Max (mA)	Power Dissipation Standby (I_{SB1}) Max (µA)
AS6VA5128	2.7	3.0	3.3	55	2	20

Functional description

The AS6VA5128 is a low-power CMOS 4,194,304-bit Static Random Access Memory (SRAM) device organized as 524,288 words × 8 bits. It is designed for memory applications where slow data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 55 ns are ideal for low-power applications. Active high and low chip selects ($\overline{CS}$) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CS}$ is high, the device enters standby mode: the AS6VA5128 is guaranteed not to exceed 66 µW power consumption at 3.3V and 55ns. The device also returns data when V_{CC} is reduced to 1.5V for even lower power consumption.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip select ($\overline{CS}$) low. Data on the input pins I/O1–I/O8 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CS}$ (write cycle 2).To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$), chip select ($\overline{CS}$), with write enable ($\overline{WE}$) High. The chip drives I/O pins with the data word referenced by the input address. When either chip select or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are CMOS-compatible, and operation is from a single 2.7V to 3.3V supply. The device is available in the JEDEC standard 36(48)-ball FBGA package.

Absolute maximum ratings

Parameter	Device	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to V_{SS}		V_{tIN}	–0.5	V_{CC} + 0.5	V
Voltage on any I/O pin relative to GND		$V_{tI/O}$	–0.5		V
Power dissipation		P_D	–	1.0	W
Storage temperature (plastic)		T_{stg}	–65	+150	°C
Temperature with V_{CC} applied		T_{bias}	–55	+125	°C
DC output current (low)		I_{OUT}	–	20	mA

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Supply Current	I/O1–I/O8	Mode
H	X	X	I_{SB}	High Z	Standby (I_{SB})
L	X	X	I_{SB}	High Z	Standby (I_{SB})
L	H	H	I_{CC}	High Z	Output disable (I_{CC})
L	H	L	I_{CC}	D_{OUT}	Read (I_{CC})
L	L	X	I_{CC}	D_{IN}	Write (I_{CC})

Key: X = Don’t care, L = Low, H = High.

Recommended operating condition (over the operating range)

Parameter	Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.1mA	V_{CC} = 2.7V	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1mA	V_{CC} = 2.7V		0.4	V
V_{IH}	Input HIGH Voltage		V_{CC} = 2.7V	2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		V_{CC} = 2.7V	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output Load Current	GND ≤ V_O ≤ V_{CC}; Outputs High Z		–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA, f = 0, V_{IN} = V_{IL} or V_{IH}	V_{CC} = 3.3V		2	mA
I_{CC1} @ 1 MHz	Average V_{CC} Operating Supply Current at 1 MHz	$\overline{CS}$ ≤ 0.2V, V_{IN} ≤ 0.2V, or V_{IN} ≥ V_{CC} – 0.2V, f = 1 mS	V_{CC} = 3.3V		5	mA
I_{CC2}	Average V_{CC} Operating Supply Current	$\overline{CS}$ ≠ V_{IL}, V_{IN} = V_{IL} or V_{IH}, f = f_{Max}	V_{CC} = 3.3V (55 ns)		40	mA
I_{SB}	$\overline{CS}$ Power Down Current; TTL Inputs	$\overline{CS}$ ≥ V_{IH}, other inputs = 0V – V_{CC}	V_{CC} = 3.3V		100	µA
I_{SB1}	$\overline{CS}$ Power Down Current; CMOS Inputs	$\overline{CS}$ ≥ V_{CC} – 0.2V, other inputs = 0V – V_{CC}, f = f_{Max}	V_{CC} = 3.3V		20	µA
I_{SBDR}	Data Retention	$\overline{CS}$ ≥ V_{CC} – 0.1V, f = 0	V_{CC} = 1.2V		2	µA

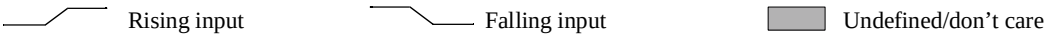
Capacitance (f = 1 MHz, T_a = Room temperature, V_{CC} = NOMINAL)[2]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$	V_{IN} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0V	7	pF

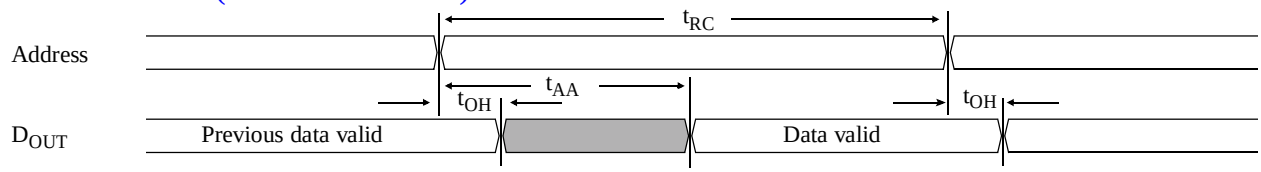
Read cycle (over the operating range)[3,9]

Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time	t_{RC}	55	–	ns	
Address access time	t_{AA}	–	55	ns	3
Chip select ($\overline{CS}$) access time	t_{ACS}	–	55	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	25	ns	
Output hold from address change	t_{OH}	10	–	ns	5
$\overline{CS}$ low to output in low Z	t_{CLZ}	10	–	ns	4, 5
$\overline{CS}$ high to output in high Z	t_{CHZ}	0	20	ns	4, 5
$\overline{OE}$ low to output in low Z	t_{OLZ}	5	–	ns	4, 5
$\overline{OE}$ high to output in high Z	t_{OHZ}	0	20	ns	4, 5
Power up time	t_{PU}	0	–	ns	4, 5
Power down time	t_{PD}	–	55	ns	4, 5

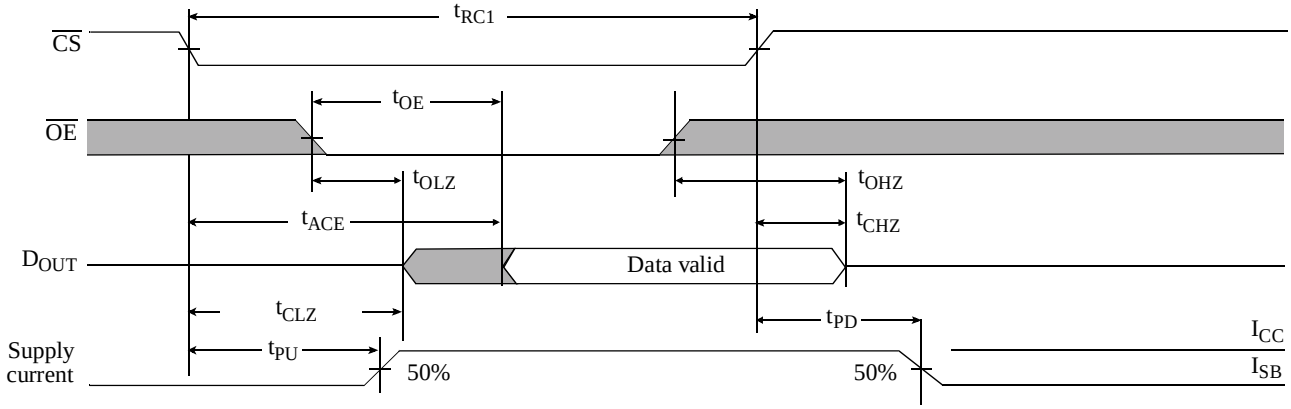
Key to switching waveforms



Read waveform 1 (address controlled)[3,6,7,9]



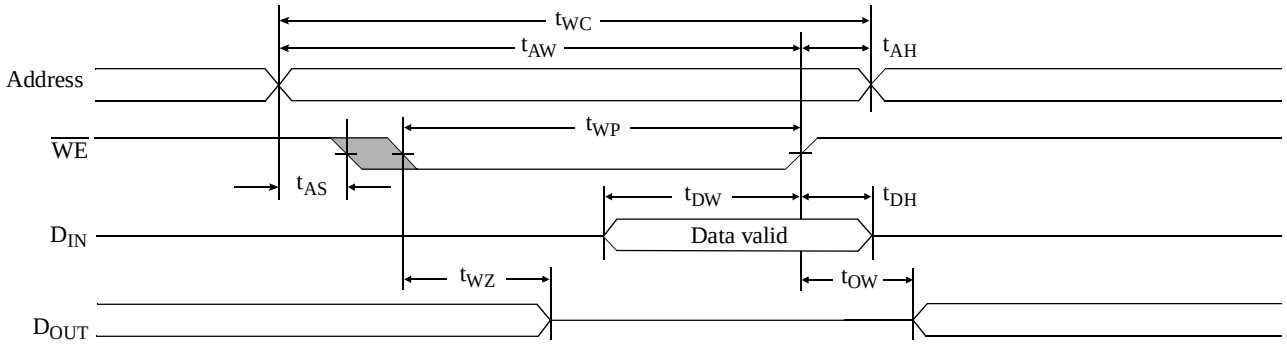
Read waveform 2 ($\overline{CS}$, $\overline{OE}$ controlled)[3,6,8,9]



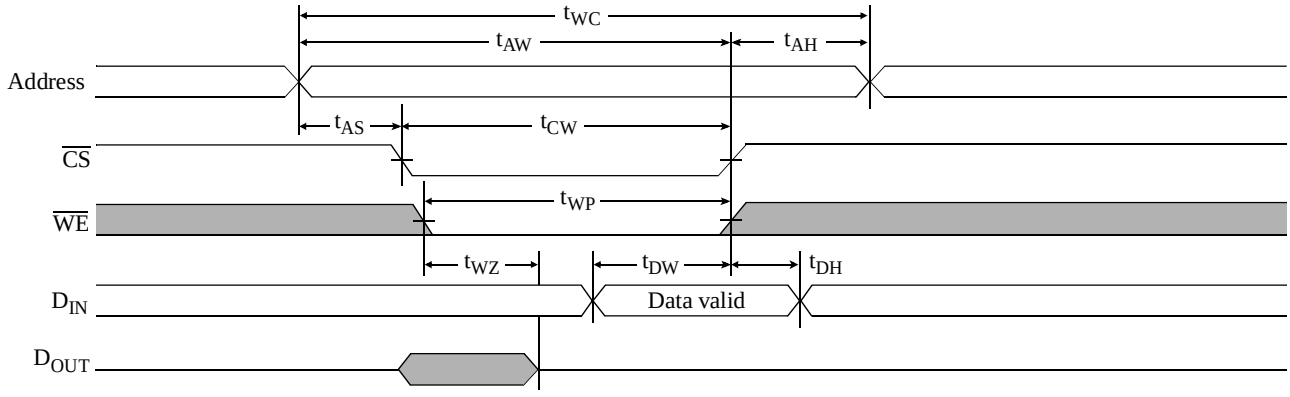
Write cycle (over the operating range)[11]

Parameter	Symbol	Min	Max	Unit	Notes
Write cycle time	t_{WC}	55	–	ns	
Chip select to write end	t_{CW}	40	–	ns	12
Address setup to write end	t_{AW}	40	–	ns	
Address setup time	t_{AS}	0	–	ns	12
Write pulse width	t_{WP}	35	–	ns	
Address hold from end of write	t_{AH}	0	–	ns	
Data valid to write end	t_{DW}	25	–	ns	
Data hold time	t_{DH}	0	–	ns	4, 5
Write enable to output in high Z	t_{WZ}	0	20	ns	4, 5
Output active from write end	t_{OW}	5	–	ns	4, 5

Write waveform 1 ($\overline{WE}$ controlled)[10,11]



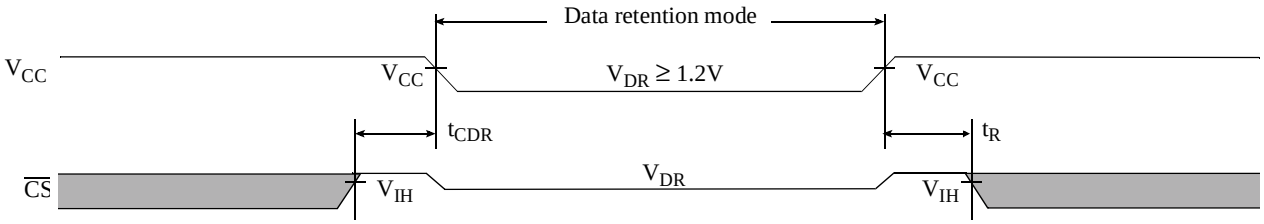
Write waveform 2 ($\overline{CS}$ controlled)[10,11]



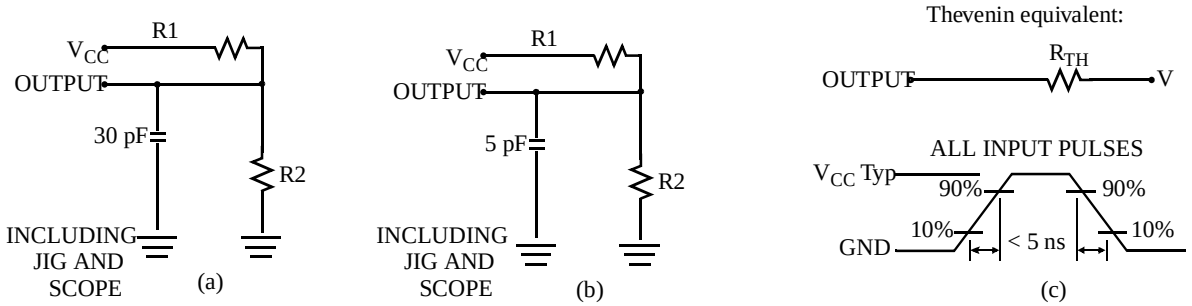
Data retention characteristics (over the operating range)[13,5]

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 1.2V $\overline{CS} \geq V_{CC} - 0.1V$ or $V_{IN} \geq V_{CC} - 0.1V$ or $V_{IN} \leq 0.1V$	1.2V	3.3	V
Data retention current	I_{CCDR}		–	4	µA
Chip deselect to data retention time	t_{CDR}		0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns

Data retention waveform



AC test loads and waveforms



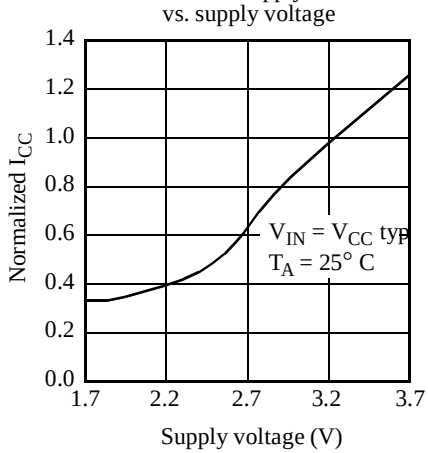
Parameters	V_{CC} = 3.0V	V_{CC} = 2.5V	V_{CC} = 2.0V	Unit
R1	1105	16670	15294	Ohms
R2	1550	15380	11300	Ohms
R_{TH}	645	8000	6500	Ohms
V_{TH}	1.75V	1.2V	0.85V	Volts

Notes

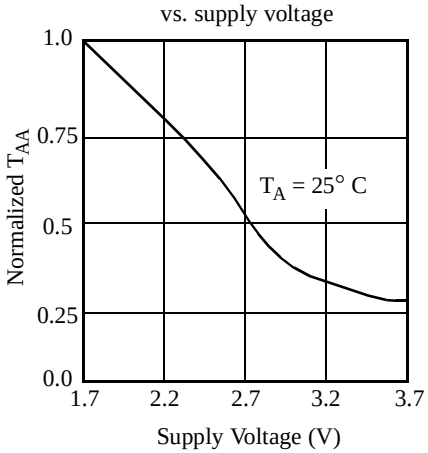
1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CS}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*.
4 t_{CLZ} and t_{CHZ} are specified with C_L = 5pF as in Figure C. Transition is measured ±500 mV from steady-state voltage.
5 This parameter is guaranteed, but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CS}$ and $\overline{OE}$ are LOW for read cycle.
8 Address valid prior to or coincident with $\overline{CS}$ transition LOW.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CS}$ or $\overline{WE}$ must be HIGH during address transitions. Either $\overline{CS}$ or $\overline{WE}$ asserting high terminates a write cycle.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 N/A.
13 1.2V data retention applies to commercial and industrial temperature range operations.
14 C = 30pF, except at high Z and low Z parameters, where C = 5pF.

Typical DC and AC characteristics

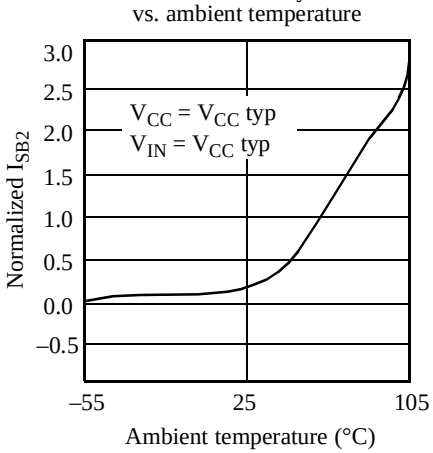
Normalized supply current vs. supply voltage



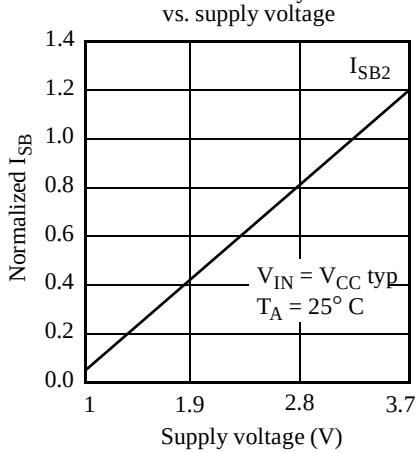
Normalized access time vs. supply voltage



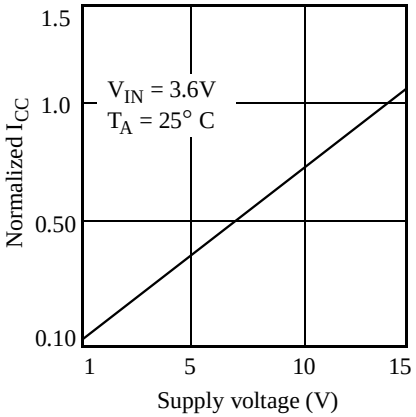
Normalized standby current vs. ambient temperature



Normalized standby current vs. supply voltage

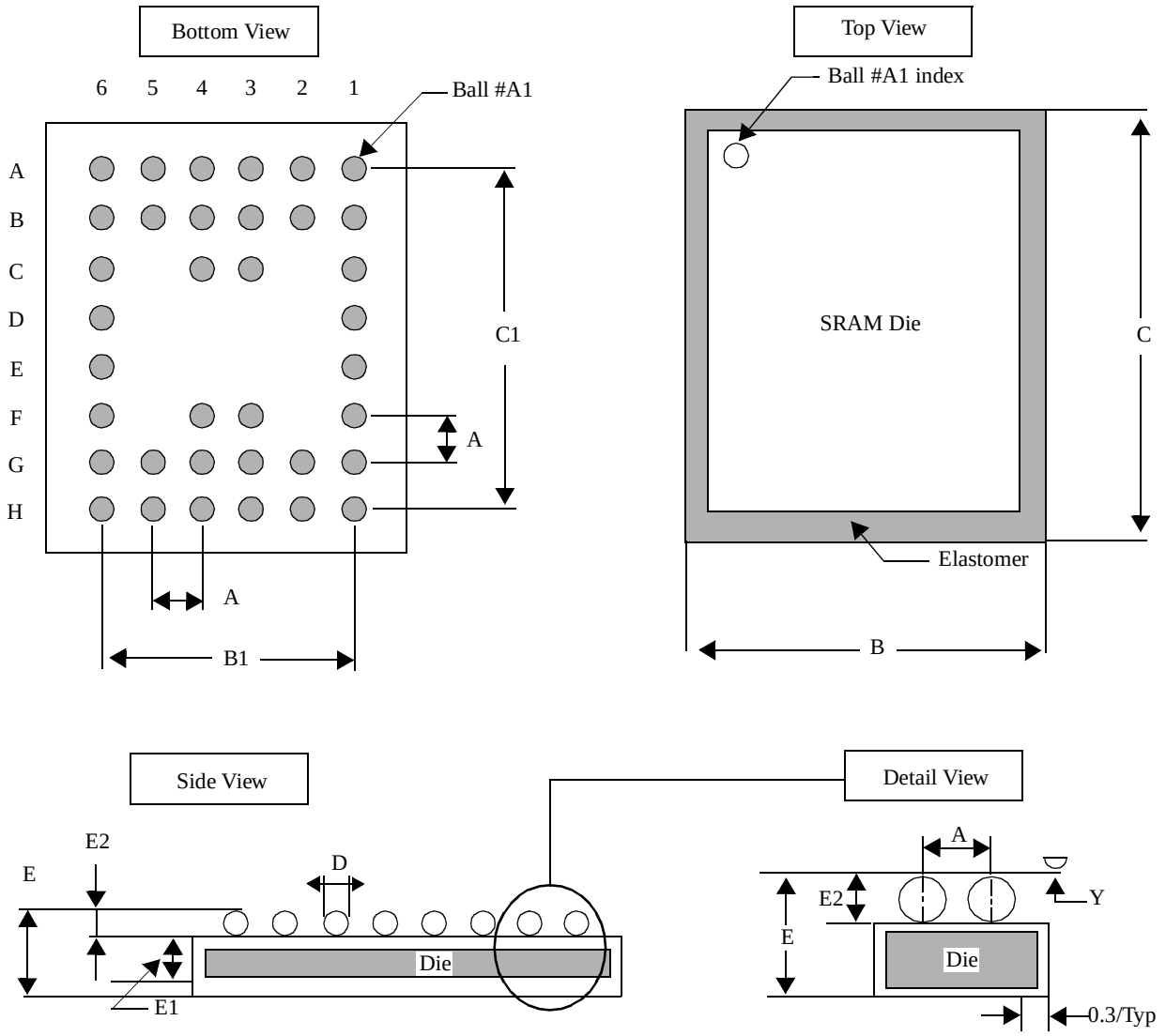


Normalized I_{CC} vs. Cycle Time



Package diagrams and dimensions

36(48)-ball FBGA



	Minimum	Typical	Maximum
A	–	0.75	–
B	6.90	7.00	7.10
B1	–	3.75	–
C	10.90	11.00	11.10
C1	–	5.25	–
D	0.30	0.35	0.40
E	–	–	1.20
E1	–	0.68	–
E2	0.22	0.25	0.27
Y	–	–	0.08

Notes

1. Bump counts: 36(48) (8 row × 6 column).
2. Pitch: (x,y) = 0.75 mm × 0.75 mm (typ).
3. Units: millimeters.
4. All tolerances are ±0.050, unless otherwise specified.
5. Typ: typical.
6. Y is coplanarity: 0.08 (max).

Ordering codes

Speed (ns)	Ordering Code	Package Type	Operating Range
55	AS6VA5128-BC	48-ball fine pitch BGA	Commercial
55	AS6VA5128-BI	48-ball fine pitch BGA	Industrial

Part numbering system

AS6VA	5128	T, ST, HF, HR, B	C, I
SRAM Intelliwatt™ prefix	Device number	Package: B: CSP BGA	Temperature range: C: Commercial: 0° C to 70° C I: Industrial: –40°C to 85° C