128-DOT LCD DRIVER WITH TIMER AND CLOCK FUNCTIONS

Table of Contents-

GENERAL DESCRIPTION

This chip is an LCD driver for a telephone dialer number display or other equipment. A maximum of 16 digits or 128 dots can be displayed, with 1/3 bias, 1/4 duty, and 32 segments.

In normal mode, a maximum of 128 dots (programmed by μP transceiver function) can be displayed on the LCD panel. In clock mode, the LCD panel can display a built-in clock that can also be programmed through the μP transceiver function. In timer mode, the LCD panel can display the conversation time. The timer mode cannot be programmed by the μP.

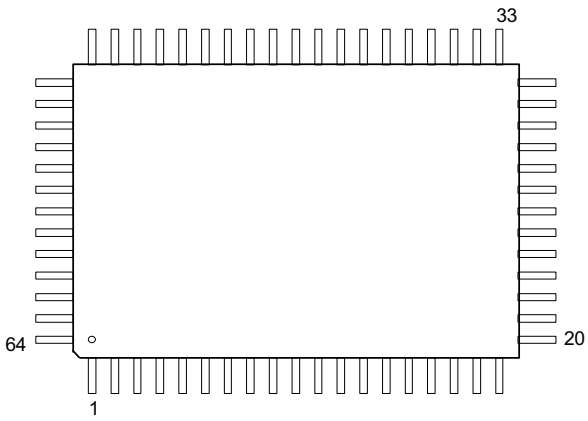
A $V_{DD}1$ pin is used in different voltage system applications to implement a voltage level shift function to guarantee the transceiver data.

This chip is fabricated using Winbond's high performance CMOS technology.

FEATURES

- Supply voltage: 1.5V or 3V by mask option
- Operating frequency: 32.768 KHz
- Built-in crystal oscillator circuit
- RC/Crystal mode selected by mask option
- Voltage level shift with a μP
- Three operating modes
  - Normal mode (can be programmed by μP)
  - Clock mode (can be programmed by μP)
  - Timer mode. (can not be programmed by μP)
- Max. 16 (128 dots) digits with 8 dots/digit displayed in normal mode
- LCD (128 dots) can be programmed by μP from any address between 0 and 127
- Clock display include leap-year, month, date, hour, and minute
- Clock adjustable through MODE, SET pins or μP
- Conversation time max. 11 hours 59 min 59 sec
- Clock 12 or 24 format by pin select
- 16, or 32 Hz LCD frequency select by mask option
- 1/3 bias, 1/4 duty 32-segment LCD panel
- Built-in $V_{DD}1$ for different voltage system data transceiver application
- Built-in $\overline{ATS}$ pin to enable/disable timer mode
- Packaged in 64-pin PQFP

PIN CONFIGURATION



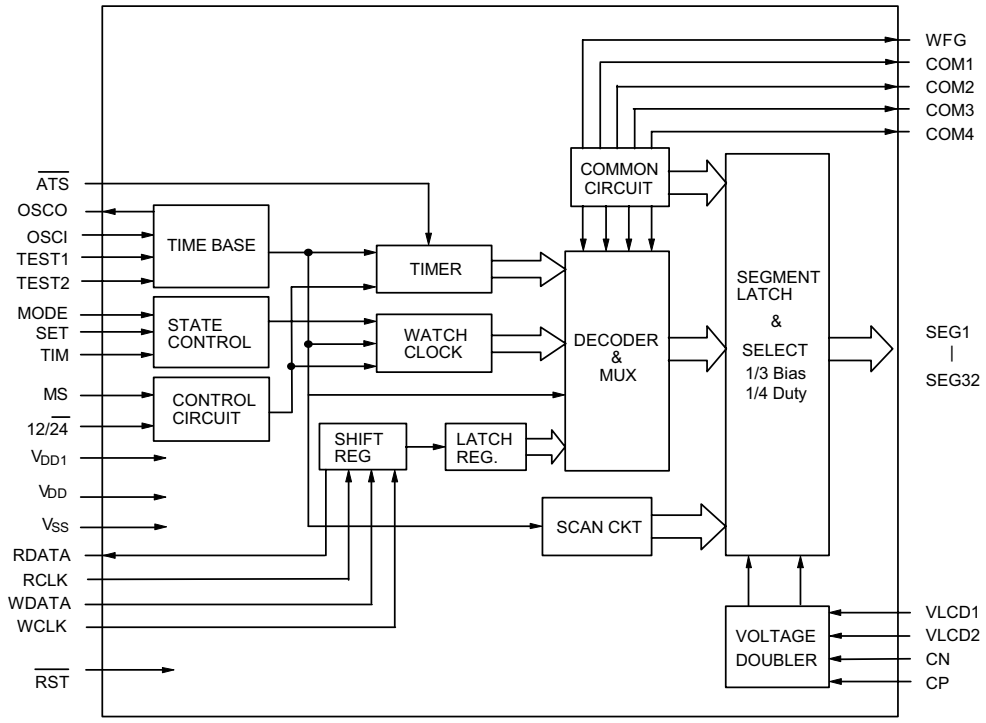
PIN DESCRIPTION

SYMBOL	PIN	I/O	FUNCTION
OSCI	38	I	Oscillator input pin. Connect to a 32.768 KHz crystal. An external capacitor is needed. In RC mode an internal resistor must be added in circuit between the OSCI and OSCO pins.
OSCO	37	O	Oscillator output pin with internal capacitor.
V_{DD}	35	I	Positive power supply.
V_{DD1}	46	I	For voltage level shift during data transceiver.
V_{SS}	40	I	Negative power supply.
V_{LCD1}, V_{LCD2}	51, 50	I	LCD voltage pins.
CN, CP	54, 55	I	CP is the voltage control capacitor positive pin. CN is the voltage control capacitor negative pin. A 0.1 µF capacitor should be connected between these two pins.
TEST1 TEST2	36, 29	I	Test pins with pull-low resistor. Not used.
$\overline{RST}$	34	I	Chip reset input pin. Active low with internal pull-high resistor.

Pin Description, continued

SYMBOL	PIN	I/O	FUNCTION
COM1– COM4	56–59	O	LCD panel common pins. (1/3 bias, 1/4 duty)
SEG1– SEG32	60–64, 2–28	O	LCD panel segment pins. (1/3 bias, 1/4 duty)
RDATA	44	O	Serial data output pin. It is H-Z when not active. Power source: V_{DD1}
RCLK	42	I	Synchronous read clock input pin. Power source: V_{DD1}
WDATA	45	I	Serial data/address input pin. Power source: V_{DD1}
WCLK	41	I	Synchronous write clock input pin. Power source: V_{DD1}
MS	43	I	Mode select input pin with floating status. Normal mode is active high or low by mask option. MS pin is high as normal mode through all the SPEC. Power source: V_{DD1} (Refer to functional description for more details)
12 / $\overline{24}$	47	I	12-hour (high) or 24-hour (low) clock select pin with floating status. Power source: V_{DD1}
WFG	48	O	Waveform generator output pin. When $\overline{RST}$ = 0, 1 Hz or 1024 Hz (selected by mask option) will output from this pin. When $\overline{RST}$ = 1, the control bits (248, 249, 250) will output the square-wave from this pin. Power source: V_{DD1}.
TIM	39	I	Timer start/stop control pin with floating status.
MODE	30	I	Clock mode-adjust pin with internal pull-low resistor.
SET	31	I	Clock digit-adjust pin with internal pull-low resistor.
$\overline{ATS}$	49	I	Auto Timer Select pin with floating status. $\overline{ATS}$ = 1, Auto timer disable. $\overline{ATS}$ = 0, Auto timer enable. (Refer to functional description for more details)

BLOCK DIAGRAM



W33D _ _ _ 1

supply voltage:
1 --- 1.5V, oscllate by crystal
2 --- 1.5V, oscllate by RC
3 --- 3V, oscllate by crystal
4 --- 3V, oscllate by RC

COM. frequency / calibration frequency:
2 --- 16 Hz/1024 Hz
4 --- 32 Hz/1024 Hz

0: MS = low active, return to last state after 15 sec.
"0" will not be shown in decimal digit of hour and min.

1: MS = high active, return to last state after 15 sec.
"0" will not be shown in decimal digit of hour and min.

3: MS = high active, return to last state after 15 sec.
"0" will be shown in decimal digit of hour and min.

FUNCTIONAL DESCRIPTION

1. Operating Mode

The W33D0001 provides three operating modes: Normal mode, Clock mode, and Timer mode.

Only the normal mode and clock mode can be programmed by the μP. The address data corresponding to the mode is shown in Figure 1.

In Figure 1 the address 0–127 range works as a working-loop. This means that the programmed address located in the 0-127 range will return to zero when the 127 address location is exceeded. The 128–255 range has the same function as the 0–127 range.

Data in the 0–127 range are known as normal mode data. Data in the 192–227 range are known as clock mode data, and data in the 248–255 are known as function control bits.

The following description shows the control functions, including the 8 control bits (248–255), the transceiver function controlled by a μP in normal mode (0–127), and clock mode (192–227).

1.1 The Function Control Bits

<table>
<tr><th>BIT</th><th>FUNCTION</th></tr>
<tr><td>0–127</td><td>These addresses are for normal mode data display. This section functions as a working-loop. When you program data over address 127, the data will automatically start from the 0 address again.</td></tr>
<tr><td>128–191,
228–247</td><td>Reserved section area.</td></tr>
<tr><td>192–227</td><td>Clock data area.</td></tr>
<tr><td>248</td><td>Waveform Disable bit
0: Disable the waveform output from the WFG pin and keep the output to high. (Default value)
1: Enable the waveform output from the WFG pin.</td></tr>
<tr><td>249, 250</td><td>Determine which waveform will be generated on the WFG pin.
The waveform can be determined by the following table:
<table>
<tr><th>249</th><th>250</th><th>Divid Time</th></tr>
<tr><td>0</td><td>0</td><td>1S (default)</td></tr>
<tr><td>0</td><td>1</td><td>1/2</td></tr>
<tr><td>1</td><td>0</td><td>1/16</td></tr>
<tr><td>1</td><td>1</td><td>1/256</td></tr>
</table></td></tr>
<tr><td>251</td><td>LCD panel ON/OFF control bit.
(This bit will not affect the normal data in the chip, it just affects the LCD panel)
0: LCD panel light on. (Default value)
1: LCD panel light off.</td></tr>
</table>

1.1 The Function Control Bits, continued

BIT	FUNCTION
252	Normal mode data reset control bit. (This bit will cause the 128 dots' data reset to "0"). 0: Non-reset the 128 dots' data. (Default value) 1: Resets the 128 dots' data to "0". (It is a level active signal)
253	RDATA pin output status control bit 0: RDATA pin with high impedance. 1: RDATA pin work as output pin in the read mode but H-Z in write mode.
254	Timer bit. (This bit can disable or enable the Timer mode) 0: Timer mode can be shown on the LCD panel. (Default value) 1: Timer mode cannot be shown on the LCD panel.
255	Clock bit. (This bit can disable or enable the Clock mode) 0: Clock mode can be shown on the LCD panel. (Default value) 1: Clock mode cannot be shown on the LCD panel.

1.2 The transceiver function controlled by a µP:

The W33D0001 can display the data on the LCD panel. These data are inputted by a serial transmission function from an external device such as a microprocessor. In normal mode and clock mode, the data can be read or written by a µP with a transceiver function at the rising edge of RCLK or WCLK pin. The RCLK pin and WCLK pin must normally be set to a high state if there is no data reception and transmission.

1.2.1 Switch Read or Write Function

If the W33D0001 is in write function mode, the first falling edge of RCLK will switch the write function to read function and the µP can read data from the RCLK pin and RDATA pin, and vice versa. Refer to Figure 2. When the write function is reactivated (function changed from read to write or power on reset), the first 8 bits sent by the µP sends through the WCLK pin and WDATA pin indicate the starting address of the desired read or write data. Refer to Figure 3 and Figure 4.

1.2.2 Serial Data Written by µP

A µP can send serial data and clock to the W33D0001 through the WDATA pin and WCLK pin, respectively. When the µP writes data to the W33D0001 in normal mode or clock mode, the µP first does a dummy read before sending a serial starting address to the W33D0001 through the WDATA pin and WCLK pin.

The serial starting address includes 8 bits which, from the first bit to the 8th bit, represent the LSB to the MSB of the starting address, respectively. Lastly, the µP sends the serial data to the W33D0001 through the WDATA and WCLK pins. The serial data address stored in the W33D0001 is increased by one when the WCLK pin receives one clock form µP. Refer to Figure 3.

1.2.3 Serial Data Read by μP

The μP can read data from the W33D0001 in normal mode or clock mode. First, the μP sends the starting address to the W33D0001. This addressing method is the same as the addressing method used in write functions. When the μP sends a clock through the RCLK pin and the first falling edge on RCLK pin changes the write function to the read function, the W33D0001 can output the serial data from the RDATA pin when each rising edge of RCLK clock is input. Refer to Figure 4. Please note that the address 253 (RDATA status control bit) must be programmed to "1" before the read function is performed.

The function of the three operating modes are described in the following section.

1.3 Normal mode:

As shown in Table 1, the normal mode can be programmed only when the MS pin is high. If the Timer bit and Clock bit are both "1" (indicating a disabled clock mode and timer mode) the normal mode data can always be displayed on the LCD panel.

In normal mode, the 128 dots (16 digits) are addressed from 0−127. The first digit is shown in the left most place in the LCD panel. When the μP reads or writes data to or from the W33D0001 in normal mode, the μP first arbitrarily sets any address between 0 to 127 as the starting address. The μP will then read or write one bit to or from the W33D0001 while the RCLK or WCLK pin receives one clock from the μP and the address is increased by one after every read or write clock input. The next address is reset to 0 when the 127 address is reached.

If more than 128 dots are written by the μP to the W33D0001 at a time, the 129th dot will replace the first dot, the 130th dot will replace the second dot, and so on until all the dots are written. Refer to Figure 1.

The active operating mode is selected through the MS pin, Timer bit and Clock bit, where the Timer bit and Clock bit can be programmed through the μP and stored in the 254 and 255 addresses, respectively.

The default values of the two bits are both "0". Table 1 indicates the relationship between operating mode and the MS pin, Timer bit and the Clock bit.

1.3.1 Cascade function:

More than two W33D0001 chips can be cascaded to expand the normal mode display data from 128 dots to 256 dots, 384 dots, ..etc. Only one MS pin in these chips can be pulled high to indicate the active chip. The data can then be written to the active W33D0001 chip. The application circuits are shown as Figure 14.

When the cascade function is performed, the exact data in the timer bit and clock bit (254, 255) must be programmed. In most cases, both bits must be programmed to "0".

1.4 Clock mode:

As shown in Table 2 the clock mode can display leap-year, month, date, hour, and minute. In this active clock mode, two LCD bars can flash every second. Refer to Figure 8.

There are two methods for adjusting the data for clock mode.

One method uses the transceiver function of the μP to program the clock data.

Another method is through the manual adjustment of the MODE and SET pins.

1.4.1 Using the transceiver function of µP to program the clock data

Programming the clock data through the transceiver function of the µP is similar to programming in normal mode. Unlike normal mode, the programming addresses use the 192–227 range.

When the MS pin is high and the clock bit is zero, the clock can be programmed by the µP. When the clock setting is adjusted by the µP, the clock function is stopped. After the clock's data is set, the clock time resets using the new data setting.

However, the clock will not stop while the µP is reading the clock data. In clock mode, the µP can read or write the clock data with the addressing function. 192 is the starting address of clock mode.

Moreover, the digit is displayed by means of an internal decoder in clock mode. Therefore, it needs only 4 bits to store a digit. The address of the digit corresponding to Month is 192–199. The address range for Date is 200–207.

The µP only reads or writes clock data in 24-hour format, however, the W33D0001 will automatically display the clock time in 12-hour format if the $12/\overline{24}$ pin is set high. The "P" symbol in the LCD panel is not programmed through the µP. The appearance of the "P" symbol depends on the data in the Hour reg. (address = 208–215).

The data in the 224–227 address indicate the leap-year. When the dot beside the symbol "P" is lighted, the data in the 224–227 will be (0000) in the leap-year. The data (0001) means the 1st year after the leap-year and the data (0010) means the 2nd year after the leap-year and so on.

Refer to Figure 1, and the address mapping show in table 2.

Any data not listed on Table 2 cannot be programmed in the clock mode. During programming (writing) of the data in clock mode, the clock is stopped. It is restarted when the read clock is input to the RCLK pin (or a dummy read is performed). This means that the built-in clock starts to work after the write function of the clock mode has ended.

The built-in clock will not stop when clock mode data is being read.

1.4.2 Manual adjusting method through the MODE and SET pins.

When clock mode is entered, the current time is displayed. Keeping the MODE pin depressed will cause the month digits to begin to flash. The SET pin can used to adjust the month setting; the setting will increase by one with each trigger. When the MODE pin is released, the month digits will continue the flash. At this time, a new input on the MODE pin will cause the date digits to begin flashing, and the date can be set.

Successive inputs on the MODE pin will cause the hour, minute, and leap-year digits to flash, allowing the hour, minute, and leap-year to be adjusted. While the leap-year digits are flashing, a trigger on the MODE pin will return the system to clock mode. If there is no signal on the MODE pin for more than 15 seconds (or 30 seconds, by mask option), it will return to clock mode automatically.

If the SET pin is depressed and held down for over 2 seconds, the clock setting will speed the µP at an interval of 125 mS.

When the SET pin is depressed during the clock adjusting mode, the clock will be restarted from the new data setting. The clock mode will automatically return to normal status from flash status if the flash status flashes for over 15 sec and no key is depressed.

The MODE and SET pins are both high active. Refer to Figure 7.

1.5 Timer mode:

The timer mode is controlled by the $\overline{ATS}$ pin with first priority. When the $\overline{ATS}$ pin is high, the timer function is inhibited meaning the timer data cannot display on the LCD panel. This timer function exists only when $\overline{ATS}$ pin is low, the MS pin is high, and Timer bit is equal to zero. Refer to Figure 9.

In timer mode, the elapsed conversation time since the beginning of the call is displayed on the LCD panel. When the MS pin goes from low to high and the no data is transmitted, the LCD panel will show a flashing first digit (3 bars).

When the MS pin is high, and no data transmission occur for more than 6 seconds, the timer will automatically start to count until the MS pin returns to a low state (in this case, the timer data will be kept for 5 sec. Befor being transferned to clock data). The maximum counting time is 11-59-59, and cycles to 00-00-00 to start again.

The other method of starting and stopping the timer is by triggering the TIM pin. A high trigger input on the TIM pin will reverse the current condition of the timer; thus if the timer is counting, a high trigger on TIM will stop the counter, and vice versa. When the timer is in the initial state and the first trigger on the TIM pin occurs before the normal mode transmission data, the timer will display the previous counting number.

Detailed flow charts depicting the above three operating modes are shown in Figure 5 and Figure 6.

2. Reset Function

There are two methods for initializing the chip: one is power-on reset, the other is pulling the $\overline{RST}$ pin low (low active).

2.1. Power-on reset

At power on reset , the power-on reset circuit will generate a pulse to reset the chip. All LCD segments will flash momentarily for about 2 seconds and the built-in clock will start from 1–1 00–00 and the normal mode data of 128 dots will be reset to "0".

2.2. $\overline{RST}$ Pin function

Pulling $\overline{RST}$ low will reset all of the chip's functions except for the clock. All LCD segments will flash momentarily for about 2 seconds and the 128 dots will be reset to "0".

3. LCD Format

The LCD panel is 1/3 bias, 1/4 duty. Refer to Figure 10 and Figure 11. The LCD format is shown in Figure 12.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	120	mW
Ambient Operating Temperature	-20 to +70	°C
Storage temperature	-55 to +155	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

ELECTRICAL CHARACTERISTICS

DCharacteristics

V_{DD}–V_{SS} = 1.5V, F_{OSC} = 32.768 KHz, T_A = 25° C

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage1	V_{DD1}	-	1.2	1.5	1.7	V
Op. Voltage2	V_{DD2}	-	2.4	3.0	3.4	V
Op. Current1	I_{DD1}	No load, V_{DD} = 1.5V (Crystal mode)	-	5	10	µA
Op. Current2	I_{DD2}	No load, V_{DD} = 3.0V (Crystal mode)	-	20	40	µA
Op. Current3	I_{DD3}	No load, V_{DD} = 1.5V (RC Mode)	-	30	40	µA
Op. Current4	I_{DD4}	No load V_{DD} = 3.0V (RC Mode)	-	60	80	µA
SEG1 to SEG32 Source Current	I_{SH}	V_{OH} = 1.2V	-0.4	-	-	µA
SEG1 to SEG32 Sink Current	I_{SH}	V_{OL} = 0.3V	0.4	-	-	µA
COM1 to COM4 Source Current	I_{CH1}	V_{OH} = 1.2V	-4	-	-	µA
COM1 to COM4 Sink Current	I_{CL1}	V_{OL} = 0.3V	4	-	-	µA
WFG Source Current	I_{CH2}	V_{OH} = 1.2V	-	500	-	µA

DC Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
WFG Sink Current	I_{CL2}	V_{OL} = 0.3V	-	500	-	μA
Pull-high Resistor	RH	$\overline{RST}$	-	1.0	2.0	MΩ
Pull-low Resistor	R_L	MODE, SET	-	1.0	2.0	MΩ
Input Low Voltage	V_{IL}	-	0	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V
Oscillator Resistor	R_{OSC}	RC Mode	-	510	-	KΩ
RDATA Drive Current WDATA Sink Current	I_{RDD}	V_{DD} = 3.0V V_{OH} = 2.7V	-	0.4	-	mA

AC Characteristics

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Frequency	F_{OSC}	Crystal, V_{DD} = 1.5V	-	32.768	-	KHz
Op. Frequency	F_{OSC1}	RC mode, V_{DD} = 1.5V	-	32.768	-	KHz
LCD Frequency	F_{LCD}	Mask Option	-	16	-	Hz
			-	32	-	Hz
Rising Debounce Time	T_{RD}	MODE, SET, TIM (Crystal Mode)	35	-	-	mS
Falling Debounce Time	T_{FD}	MODE, SET, TIM (Crystal Mode)	35	-	-	mS
Rising Debounce Time	T_{RD}	MODE, SET, TIM (RC Mode)	$\frac{35 * 32768}{F_{OSC1}}$	-	-	mS
Falling Debounce Time	T_{FD}	MODE, SET, TIM (RC Mode)	$\frac{35 * 32768}{F_{OSC1}}$	-	-	mS
Mode to Set Effect Time	T_{MS}	-	1	-	-	mS
Slow Adjust Effect Period	T_{SPD}	-	1	-	1999	mS
Quick Set Data Time	T_{QD}	-	-	125	-	mS
Quick Set-up Time	T_{QS}	-	2	-	-	S
$\overline{RST}$ Active Low Width	TRWD	-	-	1	-	μS
Serial Transmit Data Setup Time	T_{DS}	-	50	-	-	nS
Serial Transmit Data Hold Time	T_{DH}	-	50	-	-	nS

AC Characteristics, Continued

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial Receive Data Access Time	TAS	-	50	-	-	nS
RCLK Period	TRCLK	-	200	-	-	nS
WCLK Period	TWCLK	-	150	-	-	nS
Transmit/Receive Time	TTRN	-	-	3	-	mS
Oscillator Start Up Time	TSTD	-	2	-	-	S
WFG Duty Cycle	TDCYL	-	-	50	-	%

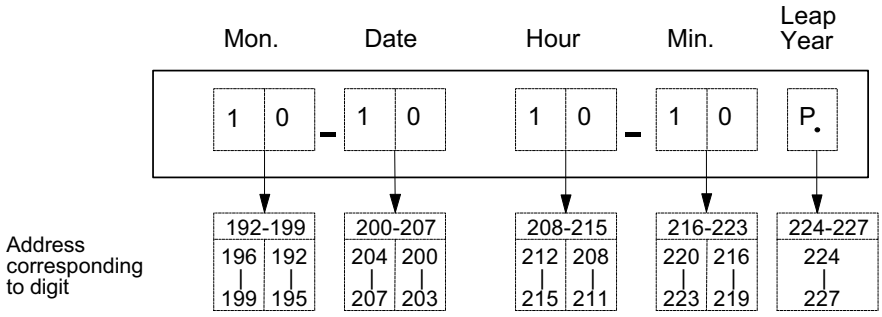
Table 1: Clock, Timer, and Normal Mode Function Table

MS	TIMER	CLOCK	CLOCK MODE		TIMER MODE	NORMAL MODE	
Pin	Bit	Bit	Progra-mmable	Display-ed	Displayed	Programable	Display-ed
0	×	0	×	√	×	×	×
0	0	1	×	×	≡	×	×
0	1	1	×	×	×	×	√
1	0	0	√	×	√	√	√
1	1	0	√	×	×	√	√
1	0	1	×	×	√	√	√
1	1	1	×	×	×	√	√

Notes:

1. "×" represent "don't care".
2. "√" represent "function existed".
3. "×" represent "function not existed".
4. "≡" represent "initial state displayed".

Table 2: Clock Mode Address Mapping



The address corresponding to the first displayed digit of Min./Hour/Date/Mon.

Address 199–196 / 207–204/ 215–212 / 223–220	Displayed Digit
0 0 0 0	None (M/D), ∗ (H/Mi)
0 0 0 1	1 (M/D/H/Mi)
0 0 1 0	2 (D/Mi/H)
0 0 1 1	3 (D/Mi)
0 1 0 0	4 (Mi)
0 1 0 1	5 (Mi)
Others	✶ (M/D/H/Mi)

The address corresponding to the 2nd displayed digit of Min./Hour/Date/Mon.

Address 195–192 / 203–200/ 211–208 / 219–216	Displayed Digit
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
Others	✶

227–224	H Dot of 16th Digit
0 0 0 0	•
0 0 0 1	None
0 0 1 0	None
0 0 1 1	None
Others	✶

Notes:

1. (M/D/H/Mi) means "for Mon. or Date or Hour or Min.".
2. "∗": Displays "0" or none by mask option.
3. "✶": Represent an illegal programming data.
4. "•" : Represent a leap year.

TIMING WAVEFORMS

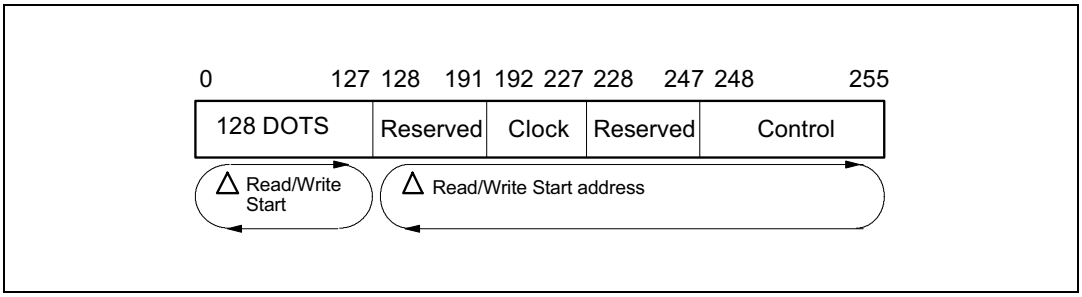


Figure 1. Address Format

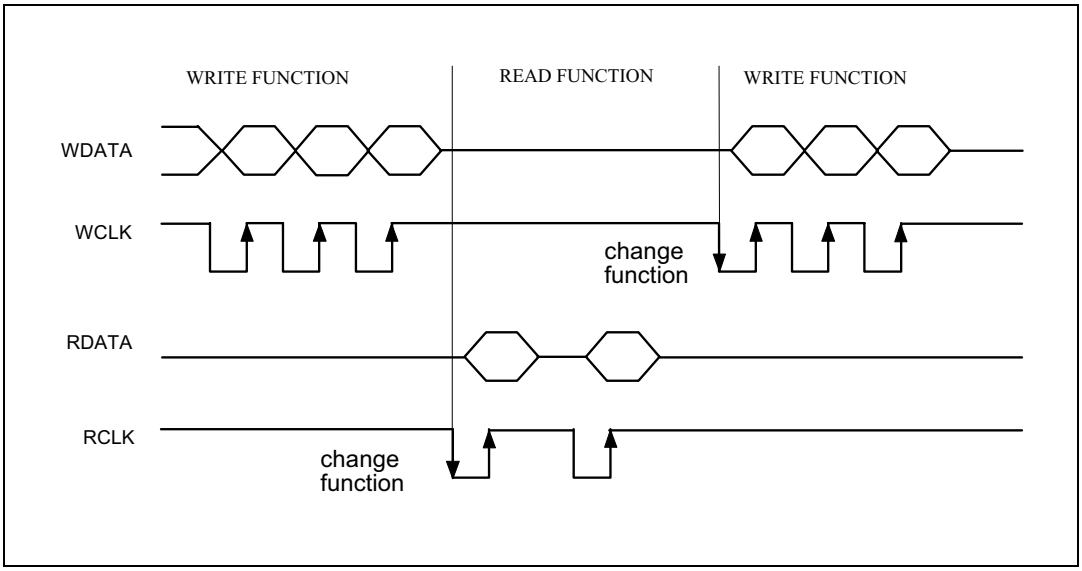


Figure 2. Read/Write Change Function

Timing Waveforms, continued

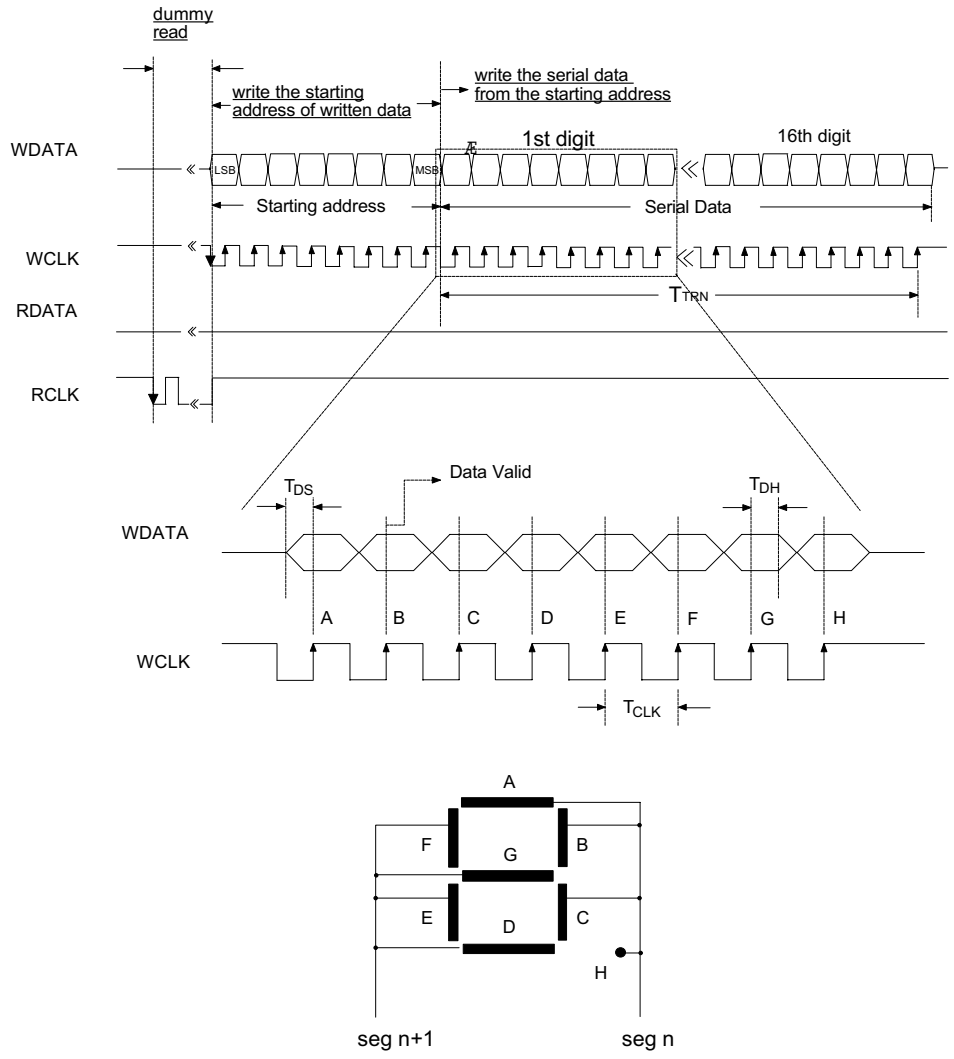


Figure 3. Write Function Controlled By μP

Timing Waveforms, continued

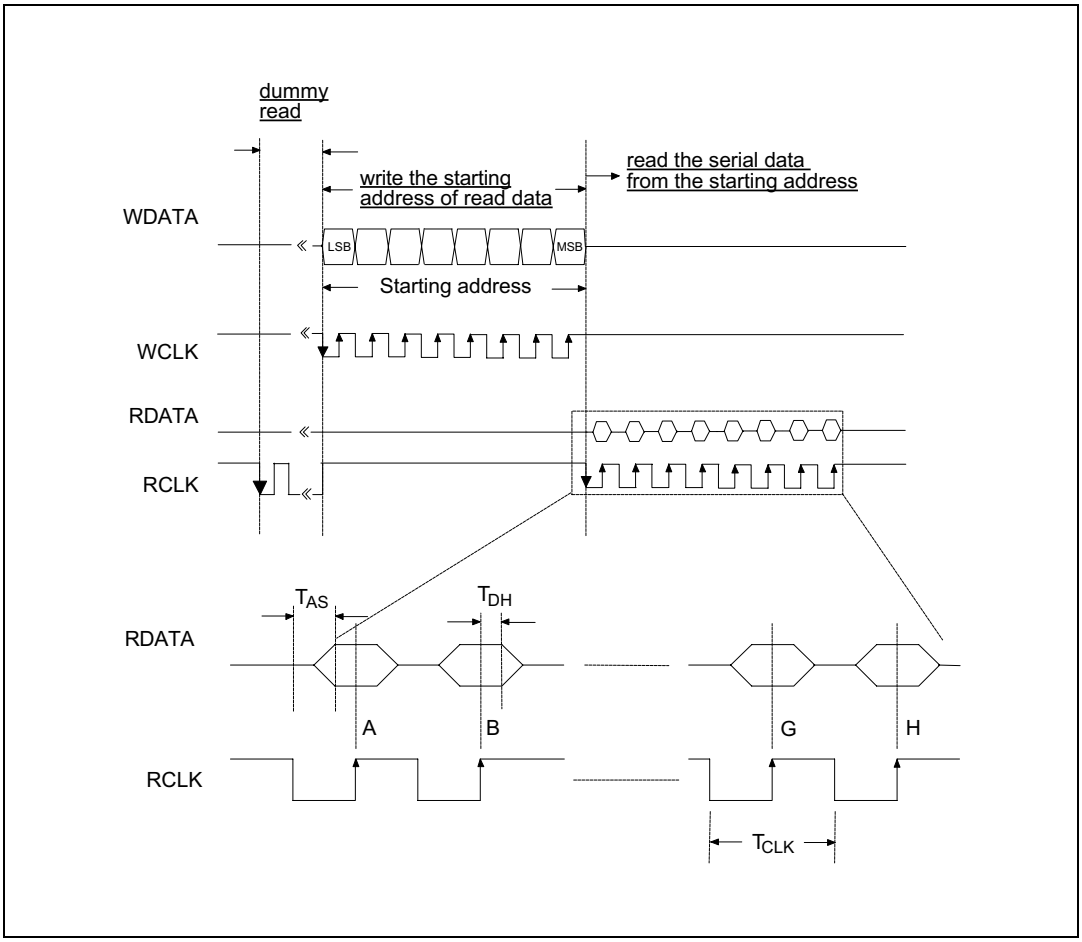


Figure 4. Read Function Controlled By μP

Timing Waveforms, continued

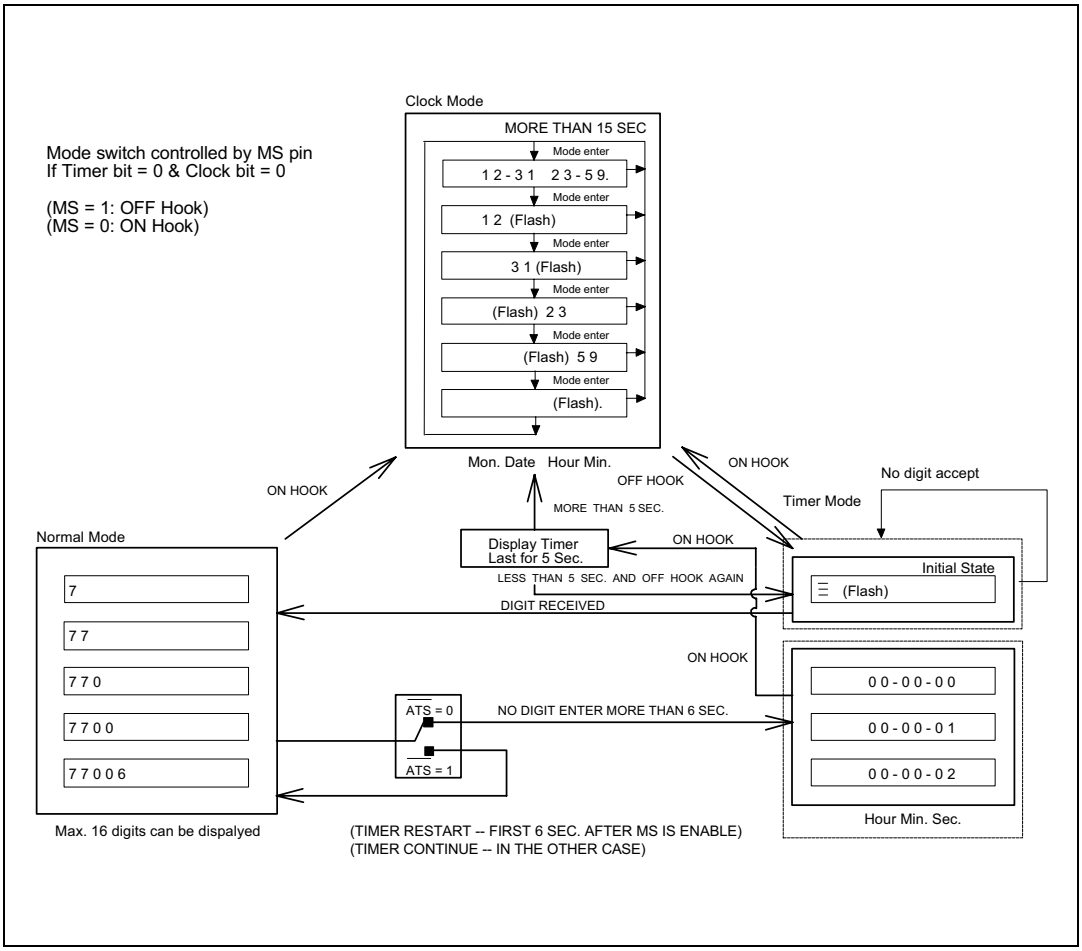


Figure 5. Mode Chart

Timing Waveforms, continued

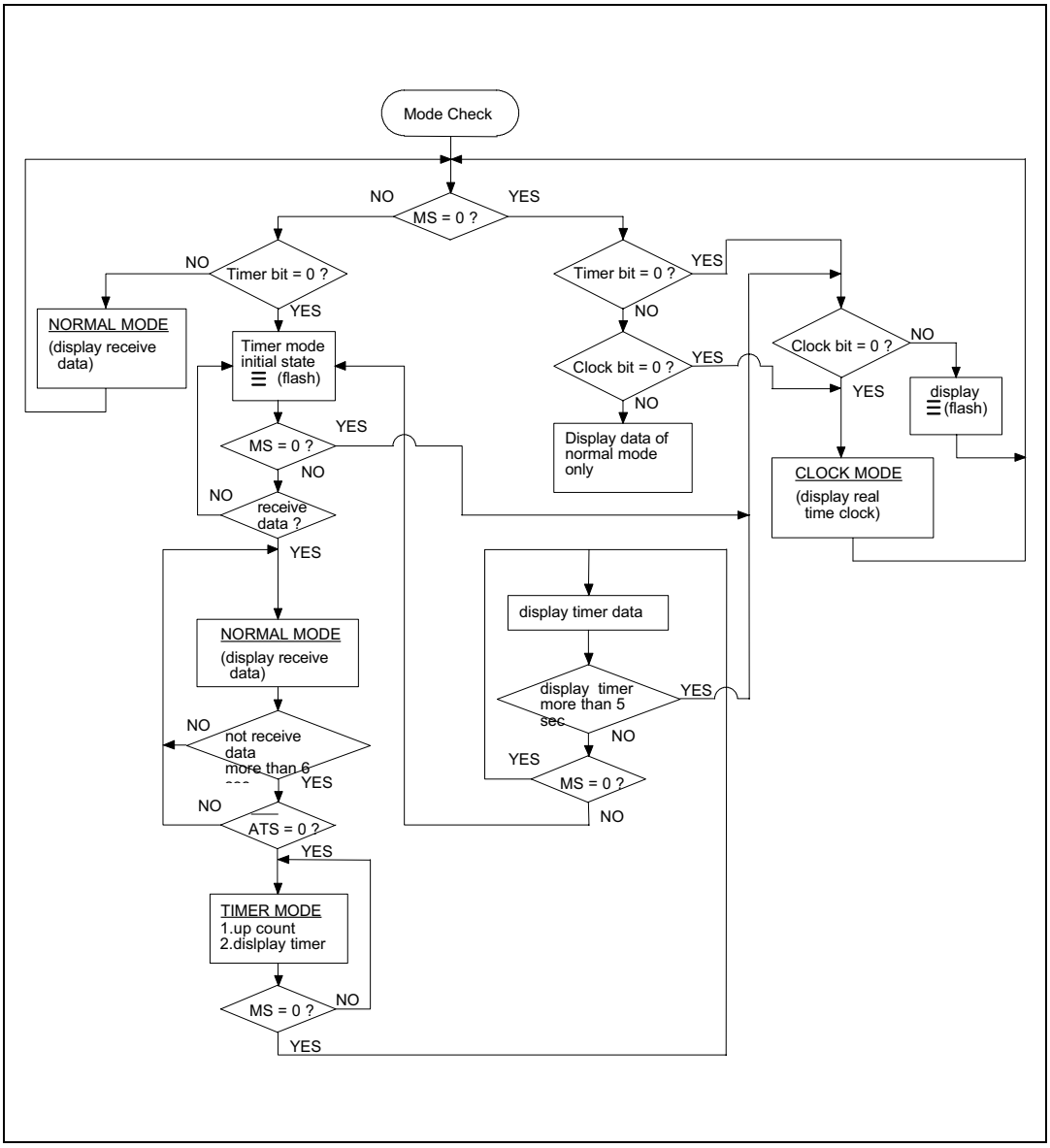


Figure 6. Flow Chart

Timing Waveforms, continued

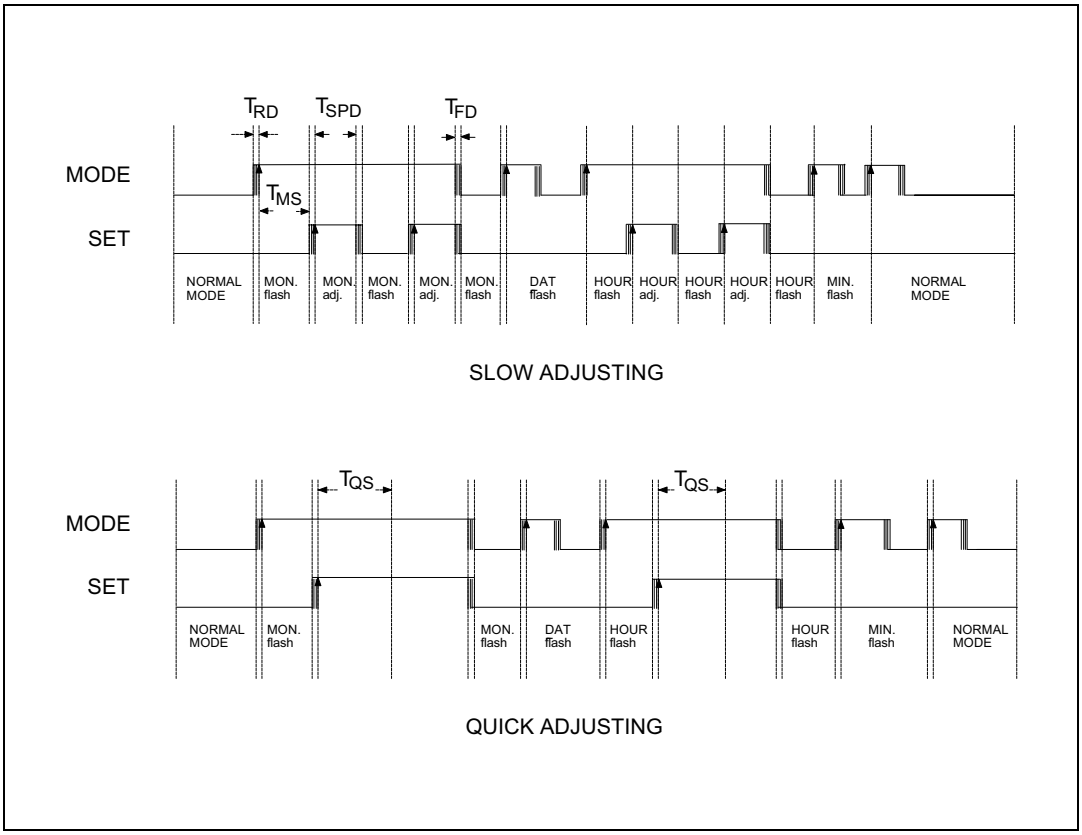


Figure 7. Clock Adjusting

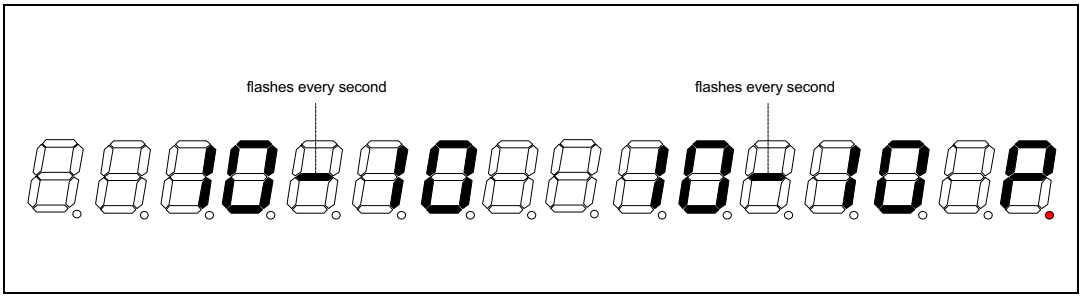


Figure 8. LCD Clock Format

Timing Waveforms, continued

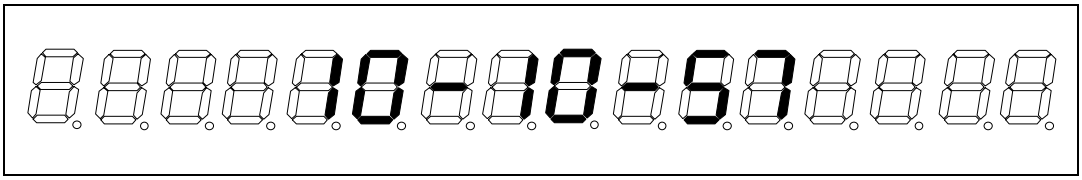


Figure 9. LCD Timer Format

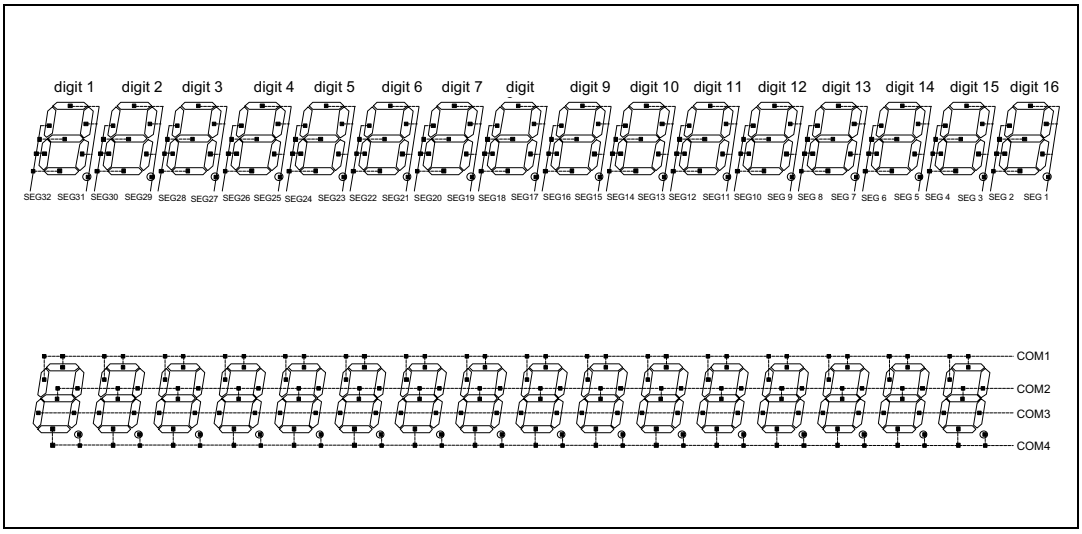


Figure 10. LCD Layout

Timing Waveforms, continued

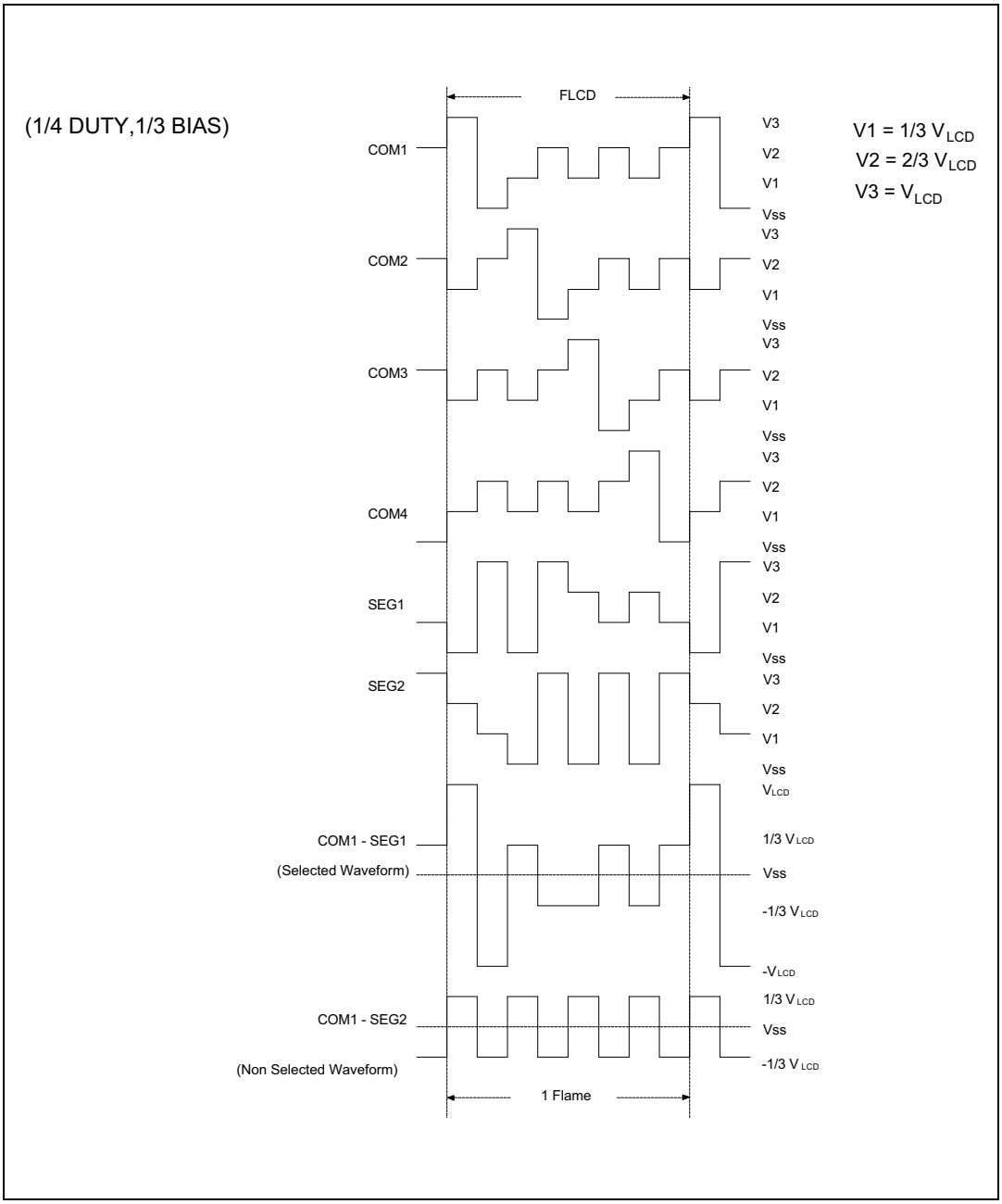


Figure 11. LCD Waveform

Timing Waveforms, continued

SEG	Digit 1		Digit 2		Digit 3		Digit 4		Digit 5		Digit 6		Digit 7		Digit 8	
COM	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
1	F	A	F	A	F	A	F	A	F	A	F	A	F	A	F	A
2	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
3	E	C	E	C	E	C	E	C	E	C	E	C	E	C	E	C
4	D	H	D	H	D	H	D	H	D	H	D	H	D	H	D	H

SEG	Digit 9		Digit 10		Digit 11		Digit 12		Digit 13		Digit 14		Digit 15		Digit 16	
COM	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	F	A	F	A	F	A	F	A	F	A	F	A	F	A	F	A
2	G	B	G	B	G	B	G	B	G	B	G	B	G	B	G	B
3	E	C	E	C	E	C	E	C	E	C	E	C	E	C	E	C
4	D	H	D	H	D	H	D	H	D	H	D	H	D	H	D	H

Figure 12. LCD Panel Format

The diagram for the W33D0001 control is shown in Figure 13.

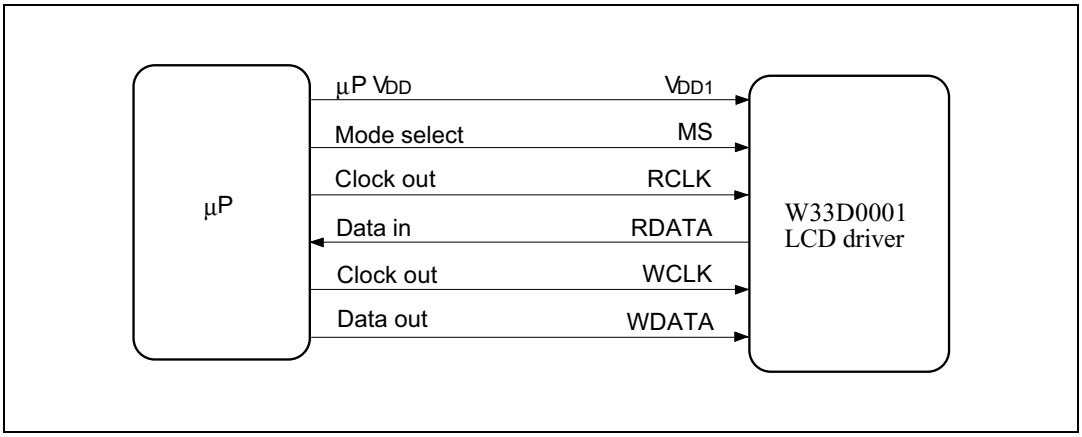


Figure 13. Application Suggestion

Note: The condition, where normal mode is enabled by setting the MS pin high or low, is a mask option. Normal mode is enabled when the MS pin is high.

Timing Waveforms, continued

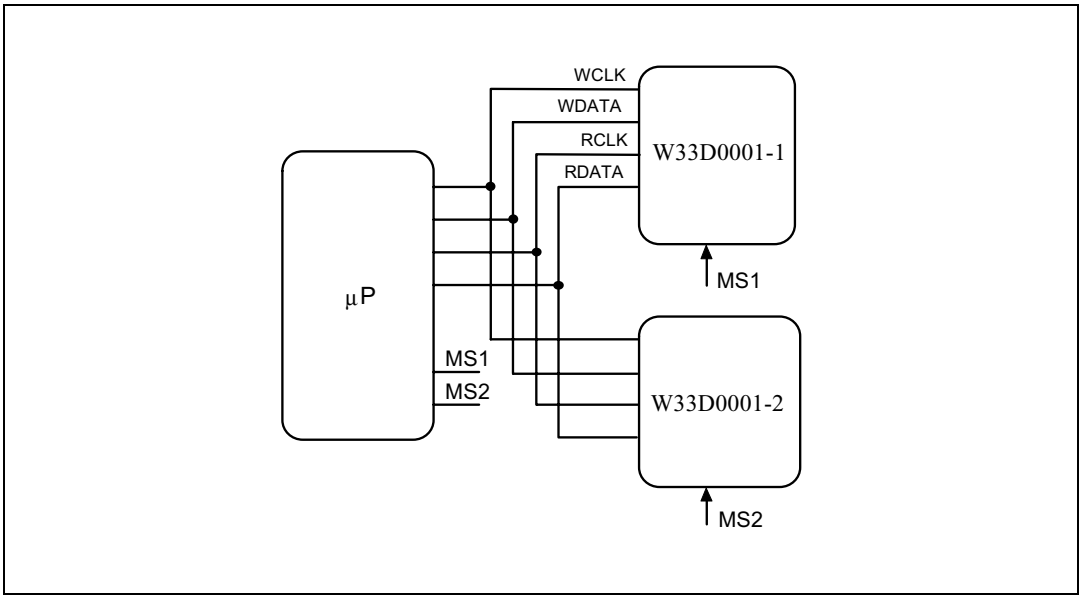


Figure 14. Normal Mode Cascade Application Circuit

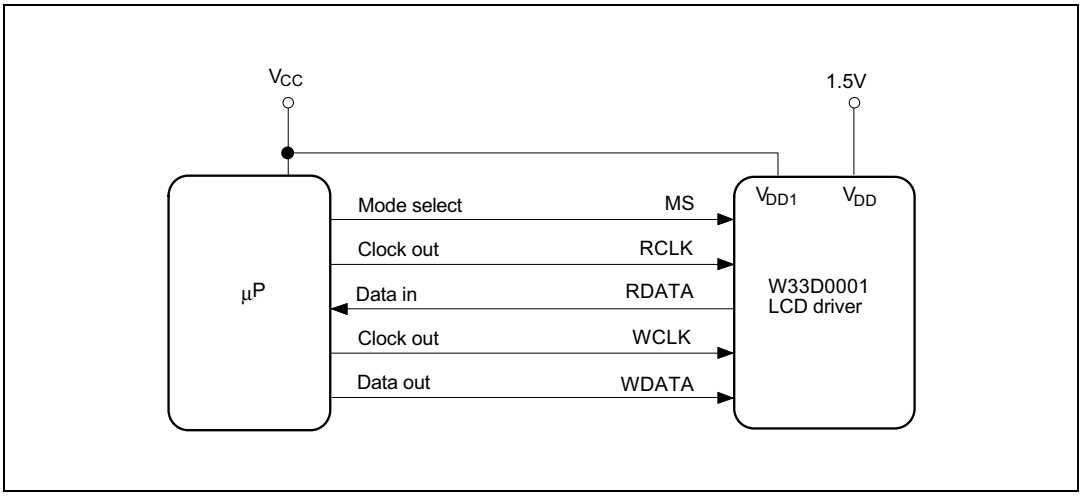


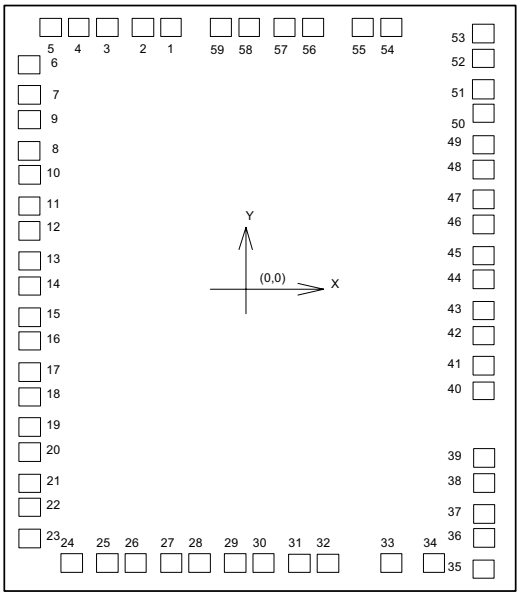
Figure 15. Application Circuit

Notes:

1. V_{DD}: W33D0001 SERIES Main power

2. $V_{DD}1$: Voltage source come from μP for level shift

BONDING PAD DIAGRAM



PAD LIST

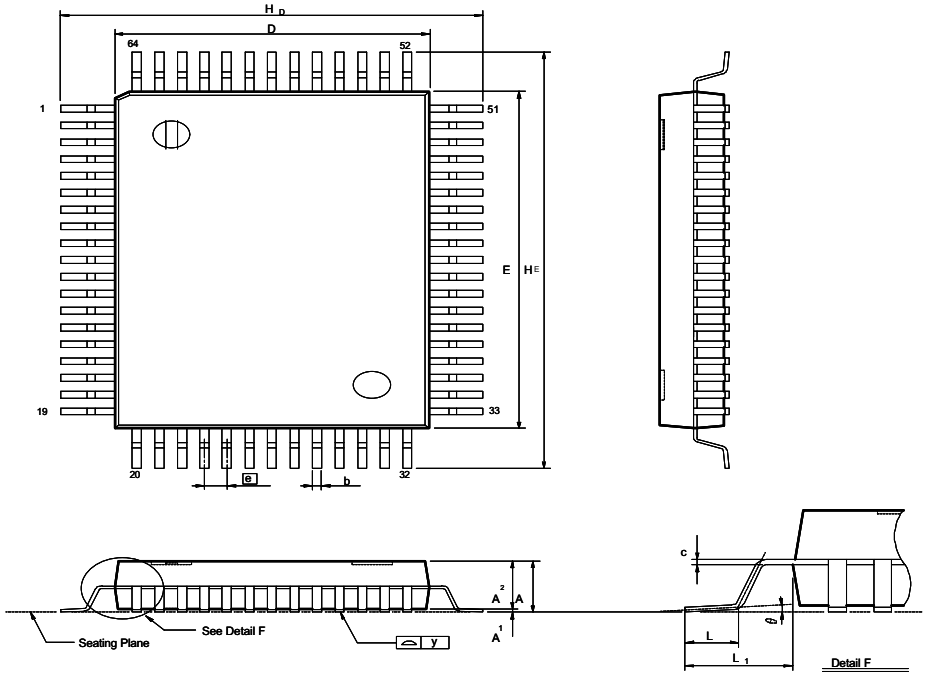
PAD NO.	PAD NAME	PIN#	X	Y	PAD NO.	PAD NAME	PIN#	X	Y
1	SEG 1	60	-406.8	1507.80	31	SEG 31	27	155.30	-1542.80
2	SEG 2	61	-546.80	1507.80	32	SEG 32	28	295.30	-1542.80
3	SEG 3	62	-715.80	1507.80	33	TEST2	29	648.45	-1542.80
4	SEG 4	63	-855.60	1507.80	34	MODE	30	883.20	-1542.80
5	SEG 5	64	-1024.80	1507.80	35	SET	31	1164.40	-1350.10
6	SEG 6	2	-1172.30	1246.20	36	$\overline{RST}$	34	1164.40	-1381.10
7	SEG 7	3	-1172.30	1077.20	37	V_{DD}	35	1164.40	-1241.10
8	SEG 8	4	-1172.30	937.20	38	TEST1	36	1164.40	-107810
9	SEG 9	5	-1172.30	768.20	39	OSCO	37	1164.40	-927.10
10	SEG 10	6	-1172.30	628.20	40	OSCI	38	1164.40	-321.00
11	SEG 11	7	-1172.30	459.20	41	TIM	39	1164.40	-379.80
12	SEG 12	8	-1172.30	319.20	42	V_{SS}	40	1164.40	-221.50
13	SEG 13	9	-1172.30	150.20	43	WCLK	41	1164.40	-63.50
14	SEG 14	10	-1172.30	10.20	44	RCLK	42	1164.40	78.40

Pad List, continued

PAD NO.	PAD NAME	PIN#	X	Y	PAD NO.	PAD NAME	PIN#	X	Y
15	SEG 15	11	-1172.30	-158.80	45	MS	43	1164.40	243.00
16	SEG 16	12	-1172.30	-298.80	46	RDATA	44	1164.40	421.70
17	SEG 17	13	-1172.30	-467.80	47	WDATA	45	1164.40	561.70
18	SEG 18	14	-1172.30	-607.80	48	$V_{DD}1$	46	1164.40	716.20
19	SEG 19	15	-1172.30	-776.00	49	$12 / \overline{24}$	47	1164.40	885.20
20	SEG 20	16	-1172.30	-916.80	50	WFG	48	1164.40	1039.70
21	SEG 21	17	-1172.30	-1085.80	51	$\overline{ATS}$	49	1164.40	1179.70
22	SEG 22	18	-1172.30	-1225.80	52	VLCD2	50	1164.40	1358.10
23	SEG 23	19	-1173.30	-1394.80	53	VLCD1	51	1164.40	1498.10
24	SEG 24	20	-940.70	-1542.30	54	CN	54	788.40	1507.80
25	SEG 25	21	-771.70	-1542.30	55	CP	55	619.40	1507.80
26	SEG 26	22	-631.70	-1542.30	56	COM1	56	302.90	1507.80
27	SEG 27	23	-462.70	-1542.30	57	COM2	57	162.90	1507.80
28	SEG 28	24	-322.70	-1542.30	58	COM3	58	-37.40	1507.80
29	SEG 29	25	-153.70	-1542.30	59	COM4	59	-177.40	1507.80
30	SEG 30	26	-13.70	-1542.30					

PACKAGE DIMENSIONS

64-pin PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.130	—	—	3.30
A_1	0.004	—	—	0.10	—	—
A_2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.014	0.016	0.020	0.35	0.40	0.50
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.546	0.551	0.556	13.87	14.00	14.13
E	0.782	0.787	0.792	19.87	20.00	20.13
e	0.033	0.039	0.045	0.85	1.00	1.15
H_D	0.728	0.740	0.752	18.49	18.80	19.10
H_E	0.964	0.976	0.988	24.49	24.80	25.10
L	0.039	0.047	0.055	1.00	1.20	1.40
L_1	0.087	0.094	0.103	2.21	2.40	2.62
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

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