Monolithic N-Channel JFET Duals

SST5198NL U5196NL U5198NL
SST5199NL U5197NL U5199NL

PRODUCT SUMMARY					
Part Number	**$V_{GS(off)}$ (V)**	**$V_{(BR)GSS}$ Min (V)**	**g_{fs} Min (mS)**	**I_G Max (pA)**	**$\|V_{GS1} - V_{GS2}\|$ Max (mV)**
U5196NL	-0.7 to -4	-50	1	-15	5
U5197NL	-0.7 to -4	-50	1	-15	5
SST/U5198NL	-0.7 to -4	-50	1	-15	10
SST/U5199NL	-0.7 to -4	-50	1	-15	15

FEATURES

- Anti Latchup Capability
- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 5 pA
- Low Noise
- High CMRR: 100 dB

BENEFITS

- External Substrate Bias—Avoids Latchup
- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

APPLICATIONS

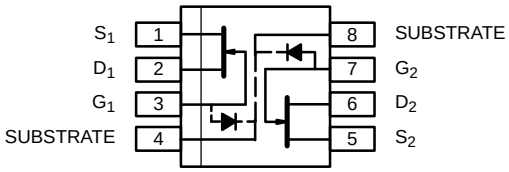
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

DESCRIPTION

The SST/U5196NL series of JFET duals are designed for high-performance differential amplification for a wide range of precision test instrumentation applications. This series features tightly matched specs, low gate leakage for accuracy, and wide dynamic range with I_G guaranteed at V_{DG} = 20 V.

Pins 4 and 8 of the SST series and pin 4 on the U series part numbers enable the substrate to be connected to a positive, external bias (V_{DD}) to avoid latchup.

Narrow Body SOIC



Top View

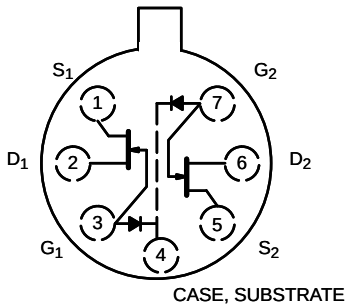
Marking Codes:

SST5198NL - 5198NL
SST5199NL - 5199NL

The U series in the hermetically-sealed TO-78 package is available with full military processing. The SST series SO-8 package provides ease of manufacturing and the symmetrical pinout prevents improper orientation. The SO-8 package is available with tape-and-reel options for compatibility with automatic assembly methods.

For similar products see the low-noise SST/U401NL series and the low-leakage U421NL/423NL data sheets.

TO-78



Top View
U5196NL, U5198NL
U5197NL, U5199NL

ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage . . . . . -50 V
Gate Current . . . . . 50 mA
Lead Temperature ($^1/_{16}$" from case for 10 sec.) . . . . . 300 °C
Storage Temperature . . . . . -65 to 200°C
Operating Junction Temperature . . . . . -55 to 150°C

Power Dissipation :
Per Side[a] . . . . . 250 mW
Total[b] . . . . . 500 mW

Notes
a. Derate 2 mW/°C above 85°C
b. Derate 4 mW/°C above 85°C

SPECIFICATIONS FOR U5196NL AND U5197NL (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Typ[a]	Limits U5196NL Min	Limits U5196NL Max	Limits U5197NL Min	Limits U5197NL Max	Unit
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 μA, V_{DS} = 0 V	-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 20 V, I_D = 1 nA	-2	-0.7	-4	-0.7	-4	V
Saturation Drain Current[b]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	3	0.7	7	0.7	7	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-10		-25		-25	pA
		T_A = 150°C	-20		-50		-50	nA
Gate Operating Current	I_G	V_{DG} = 20 V, I_D = 200 μA	-5		-15		-15	pA
		T_A = 125°C	-0.8		-15		-15	nA
Gate-Source Voltage	V_{GS}	V_{DG} = 20 V, I_D = 200 μA	-1.5	-0.2	-3.8	-0.2	-3.8	V
Dynamic								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V f = 1 kHz	3.0	1	4	1	4	mS
Common-Source Output Conductance	g_{os}		8		50		50	μS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, I_D = 200 μA f = 1 kHz	0.8	0.7	1.6	0.7	1.6	mS
Common-Source Output Conductance	g_{os}		1		4		4	μS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V f = 1 MHz	3		6		6	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		2		2	
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	11		20		20	$\frac{nV}{\sqrt{Hz}}$
Noise Figure	NF	V_{DS} = 20 V, V_{GS} = 0 V f = 100 Hz, R_G = 10 MΩ			0.5		0.5	dB
Matching								
Differential Gate-Source Voltage	$\lvert V_{GS1}–V_{GS2}\rvert$	V_{DG} = 20 V, I_D = 200 μA			5		5	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}–V_{GS2}\rvert}{\Delta T}$	V_{DG} = 20 V, I_D = 200 μA T_A = -55 to 125°C			5		10	μV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 20 V, V_{GS} = 0 V	0.98	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DS} = 20 V, I_D = 200 μA f = 1 kHz	0.99	0.97	1	0.97	1	
Differential Output Conductance	$\lvert g_{os1}–g_{os2}\rvert$		0.1		1		1	μS
Differential Gate Current	$\lvert I_{G1} – I_{G2}\rvert$	V_{DG} = 20 V, I_D = 200 μA , T_A = 125°C	0.1		5		5	nA
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 200 μA	100					dB

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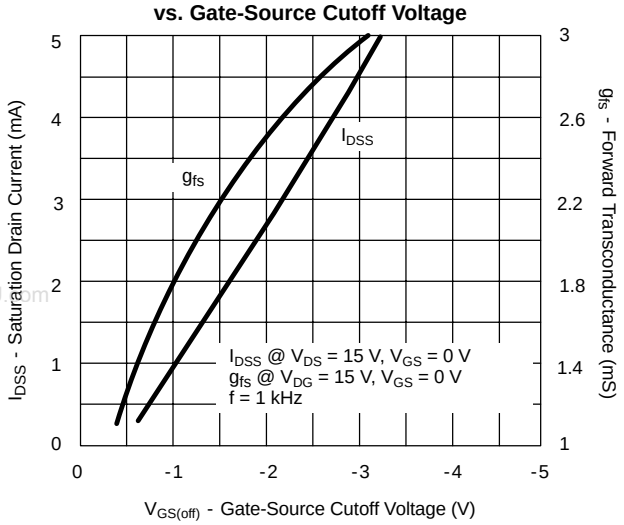
SPECIFICATIONS FOR SST/U5198NL AND SST/U5199NL (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions		Typ[a]	Limits SST/U5198NL Min	Limits SST/U5198NL Max	Limits SST/U5199NL Min	Limits SST/U5199NL Max	Unit
Static									
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V		-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 20 V, I_D = 1 nA		-2	-0.7	-4	-0.7	-4	V
Saturation Drain Current[b]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		3	0.7	7	0.7	7	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V		-10		-25		-25	pA
			T_A = 150°C	-20		-50		-50	nA
Gate Operating Current	I_G	V_{DG} = 20 V, I_D = 200 µA		-5		-15		-15	pA
			T_A =125°C	-0.8		-15		-15	nA
Gate-Source Voltage	V_{GS}	V_{DG} = 20 V, I_D = 200 µA		-1.5	-0.2	-3.8	-0.2	-3.8	V
Dynamic									
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz		3.0	1	4	1	4	mS
Common-Source Output Conductance	g_{os}			8		50		50	µS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, I_D = 200 µA f = 1 kHz		0.8	0.7	1.6	0.7	1.6	mS
Common-Source Output Conductance	g_{os}			1		4		4	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		3		6		6	pF
Common-Source Reverse Transfer Capacitance	C_{rss}			1		2		2	
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz		11					$\frac{nV}{\sqrt{Hz}}$
Noise Figure	NF	V_{DS} = 20 V, V_{GS} = 0 V f = 100 Hz, R_G = 10 MΩ (U Only)		0.5					dB
Matching									
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 20 V, I_D = 200 µA				10		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 20 V, I_D = 200 µA T_A = -55 to 125°C	SST5198NL	15					µV/°C
			SST5199NL	30					
			U Only			20		40	
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 20 V, V_{GS} = 0 V	SST Only	0.97					µS
			U Only		0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DS} = 20 V, I_D = 200 µA f = 1 kHz	SST Only	0.97					
			U Only		0.95	1	0.95	1	
Differential Output Conductance	$\lvert g_{os1}-g_{os2}\rvert$		SST Only	0.2					
			U Only			1		1	
Differential Gate Current	$\lvert I_{G1} - I_{G2}\rvert$	V_{DG} = 20 V, I_D = 200 µA, T_A = 125°C	SST Only	0.1					nA
			U Only			5		5	
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 200 µA		97					dB

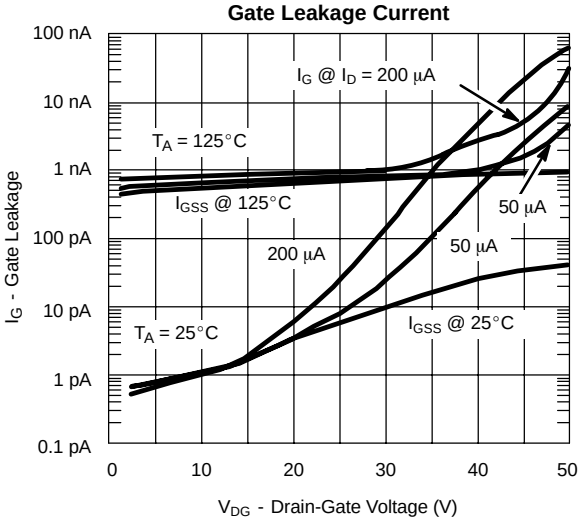
Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. NQP
b. Pulse test: PW ≤ 300 µs duty cycle ≤ 3%.

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

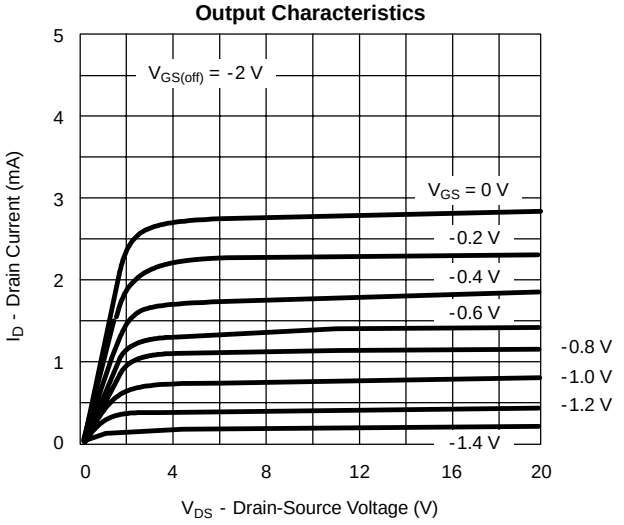
Drain Current and Transconductance vs. Gate-Source Cutoff Voltage



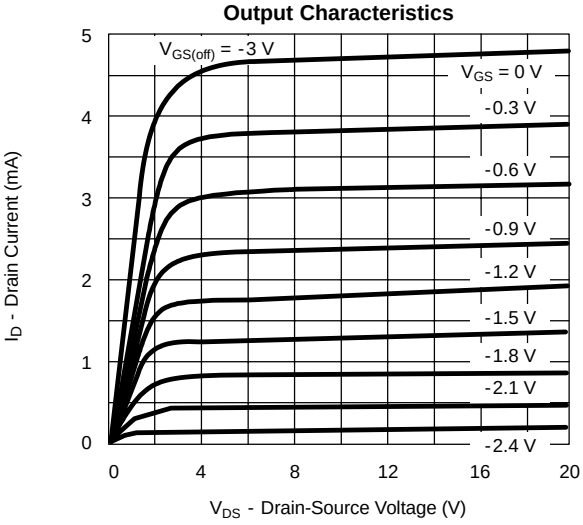
Gate Leakage Current



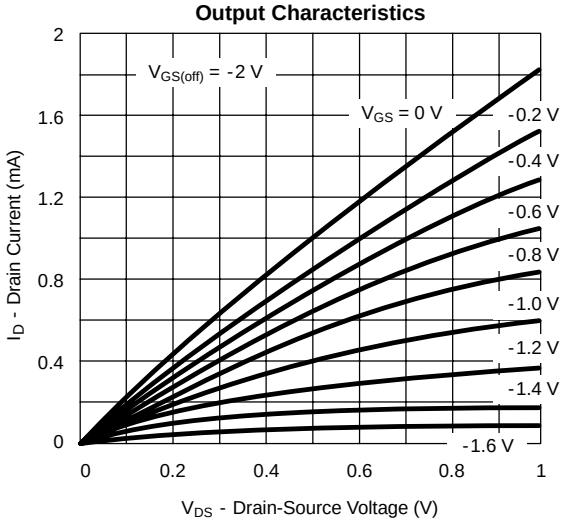
Output Characteristics



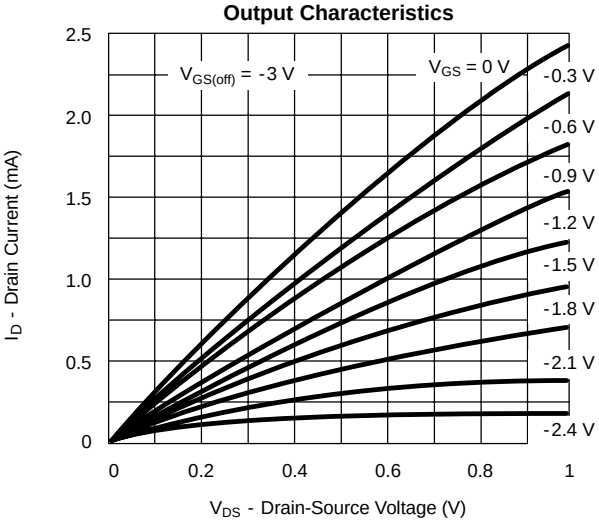
Output Characteristics



Output Characteristics



Output Characteristics



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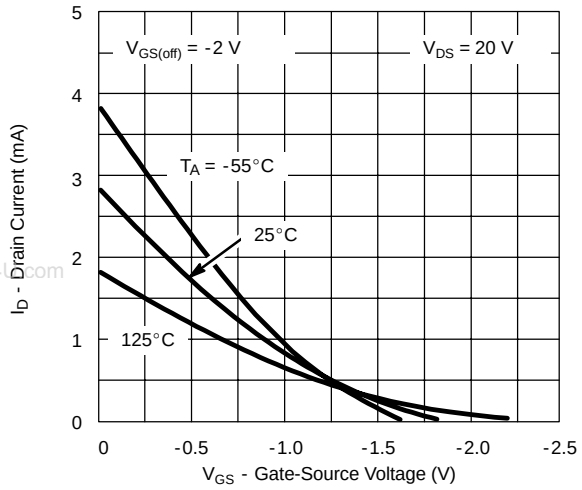
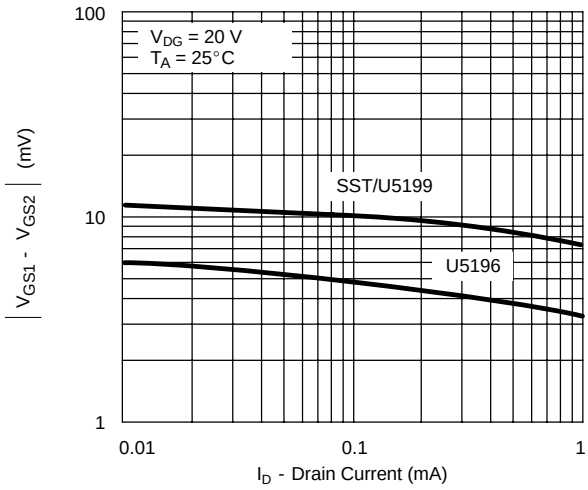
TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

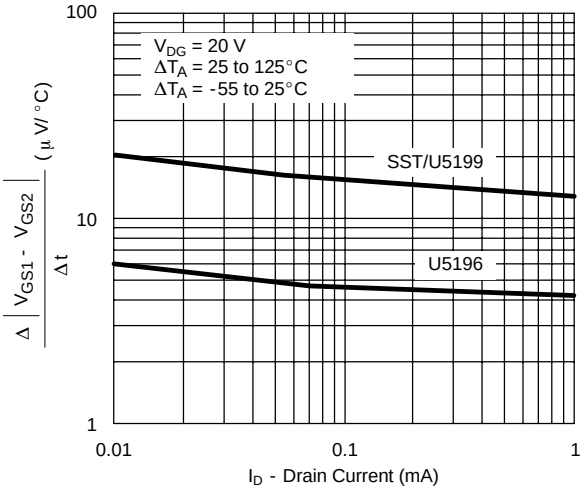
Transfer Characteristics



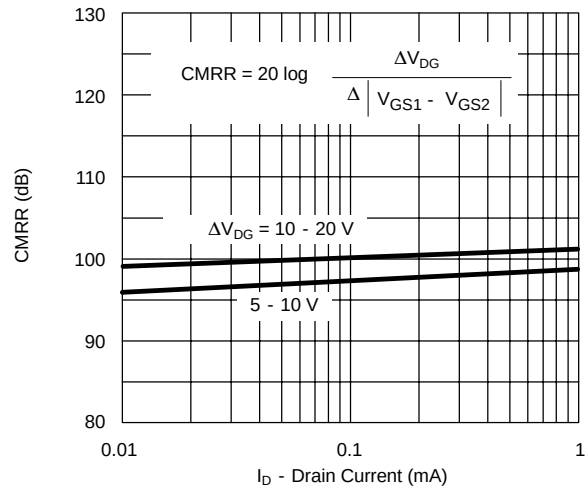
Gate-Source Differential Voltage vs. Drain Current



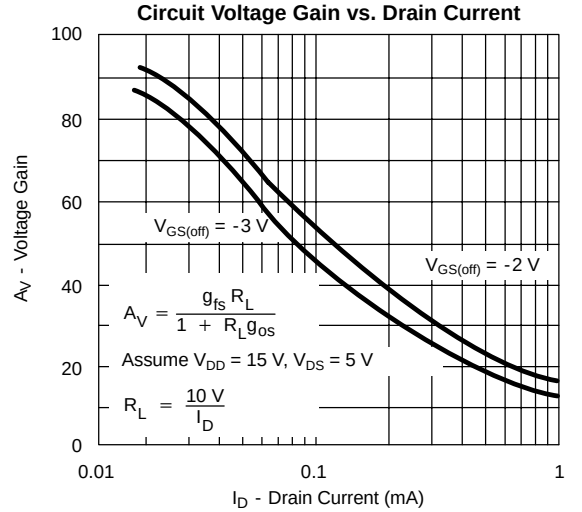
Voltage Differential with Temperature vs. Drain Current



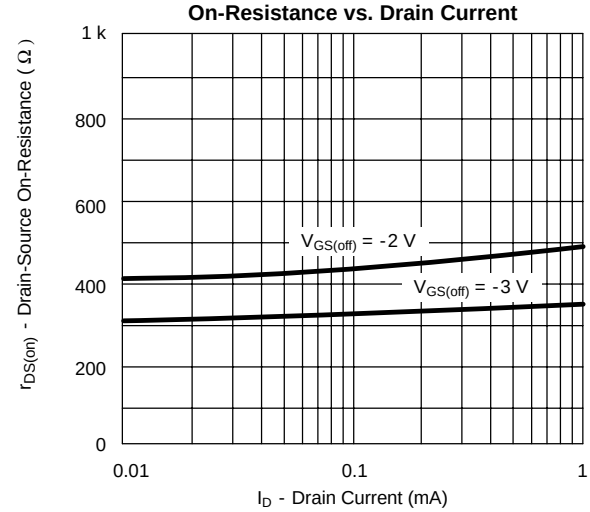
Common Mode Rejection Ratio vs. Drain Current



Circuit Voltage Gain vs. Drain Current

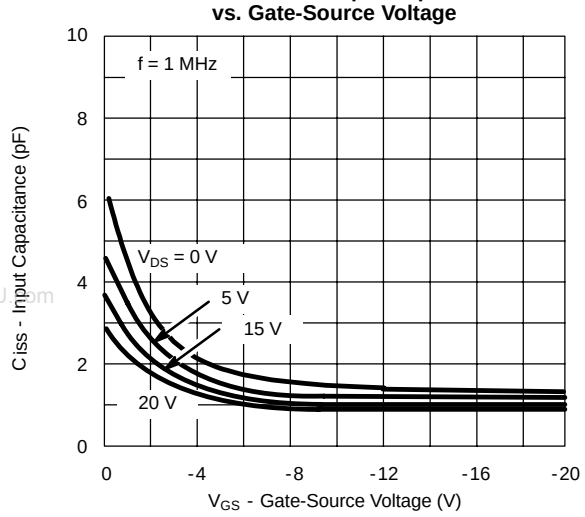


On-Resistance vs. Drain Current

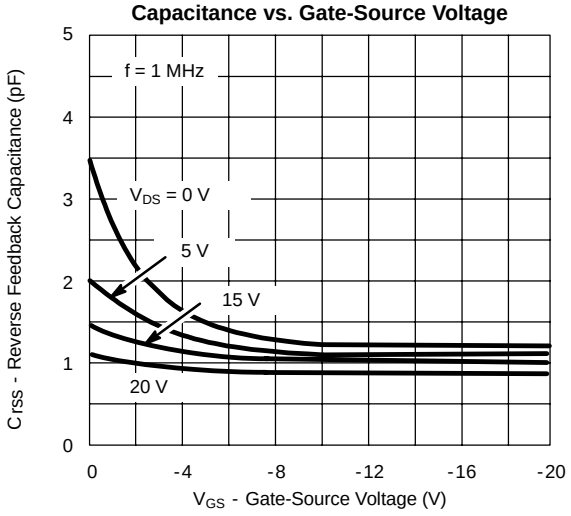


TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

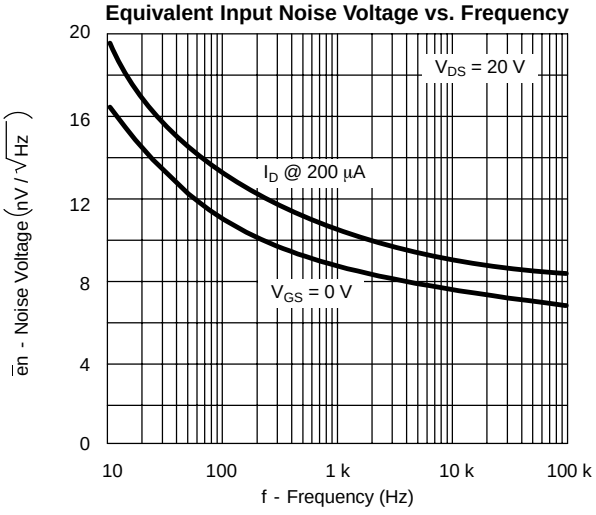
Common-Source Input Capacitance vs. Gate-Source Voltage



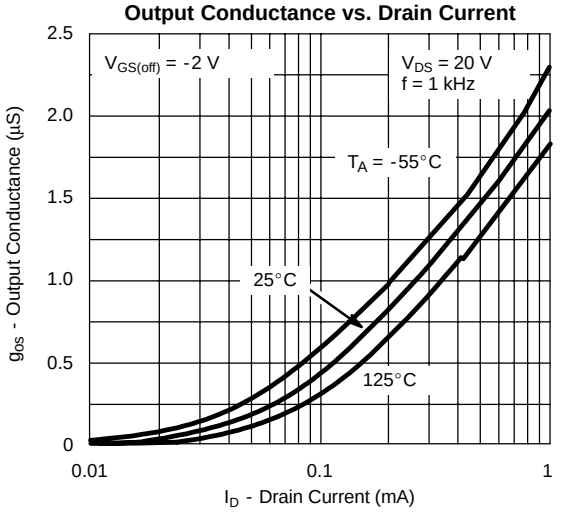
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



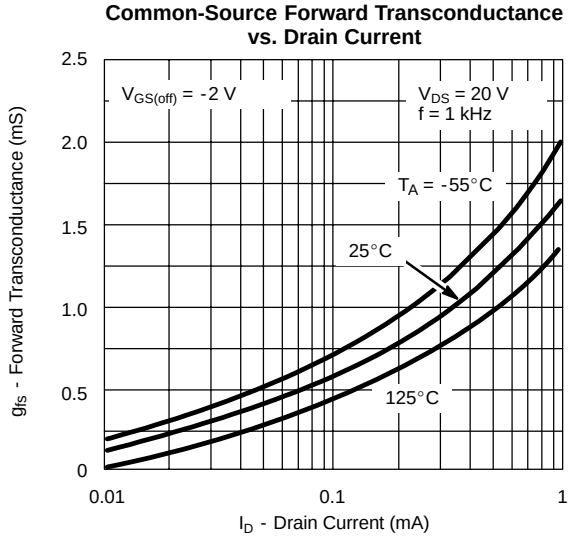
Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



Common-Source Forward Transconductance vs. Drain Current



On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage