MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MPS-U03
MPS-U04

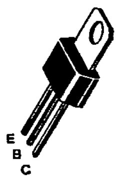
NOT RECOMMENDED FOR NEW DESIGNS

NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for horizontal drive applications, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage — $V_{(BR)CEO}$ = 180 Vdc (Min) @ I_C = 1 mAdc — MPS-U04
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 200 mAdc
- High Power Dissipation — P_D = 10 W @ T_C = 25°C

NPN SILICON AMPLIFIER TRANSISTORS

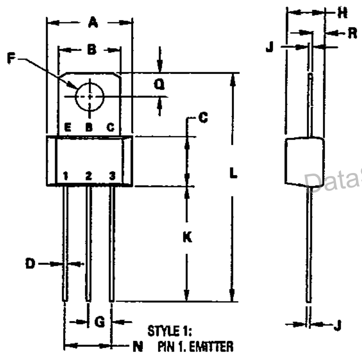


MAXIMUM RATINGS

Rating	Symbol	MPS-U03	MPS-U04	Unit
Collector-Emitter Voltage	V_{CEO}	120	180	Vdc
Collector-Base Voltage	V_{CB}	120	180	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current	I_C	1		Adc
Total Power Dissipation @ T_A = 25°C Derate Above 25°C	P_D	1 8		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C
Solder Temperature, 1/16" From Case for 10 Seconds	—	260		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTE:
1. LEADS WITHIN 0.15 mm(0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ($I_C = 1.0$ mAdc, $I_B = 0$)	MPS-U03 MPS-U04	$V_{(BR)CEO}$	120 180	– –	Vdc
Collector-Base Breakdown Voltage ($I_C = 100\ \mu$Adc, $I_E = 0$)	MPS-U03 MPS-U04	$V_{(BR)CBO}$	120 180	– –	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100\ \mu$Adc, $I_C = 0$)		$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current ($V_{CB} = 100$ Vdc, $I_E = 0$) ($V_{CB} = 150$ Vdc, $I_E = 0$)	MPS-U03 MPS-U04	I_{CBO}	– –	0.1 0.1	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain ($I_C = 10$ mAdc, $V_{CE} = 10$ Vdc)		h_{FE}	40	–	–
Collector-Emitter Saturation Voltage ($I_C = 200$ mAdc, $I_B = 20$ mAdc)		$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter On Voltage ($I_C = 200$ mAdc, $V_{CE} = 1.0$ Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product ($I_C = 50$ mAdc, $V_{CE} = 20$ Vdc, f = 20 MHz)		f_T	35	–	MHz
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, f = 100 kHz)		C_{ob}	–	12	pF
Input Capacitance ($V_{BE} = 0.5$ Vdc, $I_C = 0$, f = 100 kHz)		C_{ib}	–	110	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN – BANDWIDTH PRODUCT

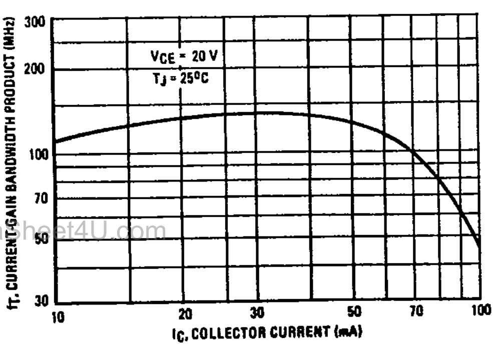
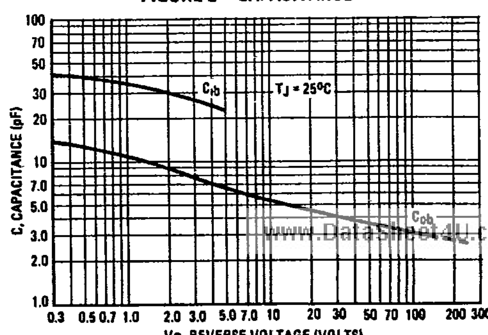


FIGURE 2 – CAPACITANCE



TYPICAL CHARACTERISTICS (Continued)

FIGURE 3 — DC CURRENT GAIN

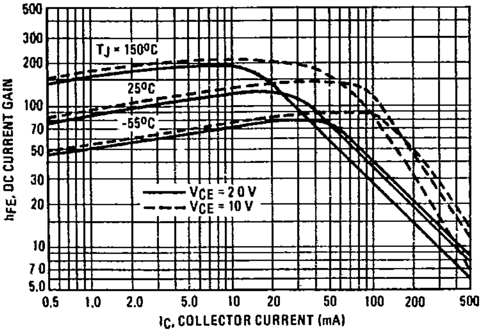


FIGURE 4 — "ON" VOLTAGE

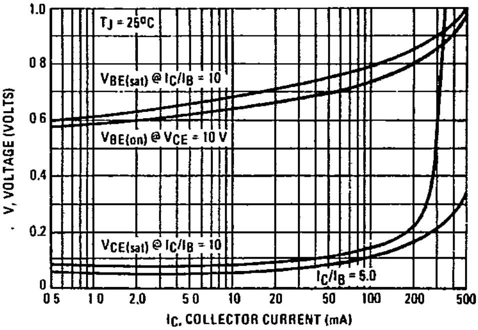


FIGURE 5 — COLLECTOR SATURATION REGION

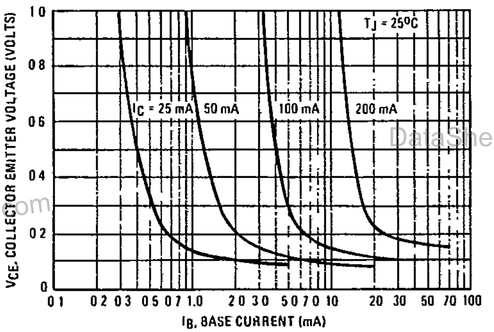


FIGURE 6 — TEMPERATURE COEFFICIENTS

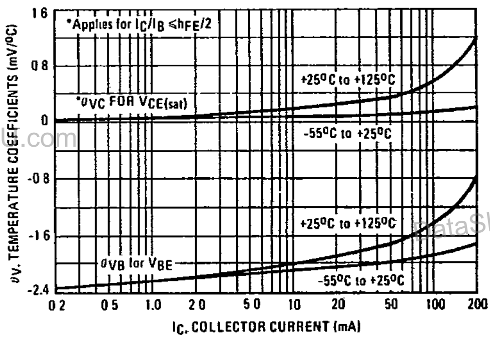


FIGURE 7 — COLLECTOR CHARACTERISTICS

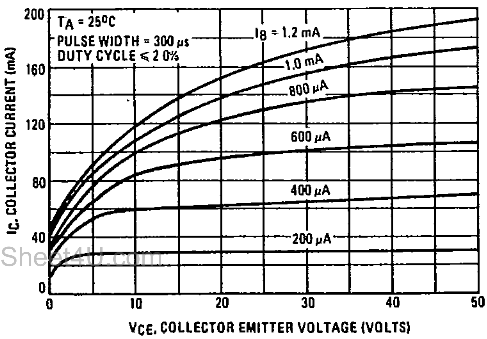


FIGURE 8 — COLLECTOR CUTOFF REGION

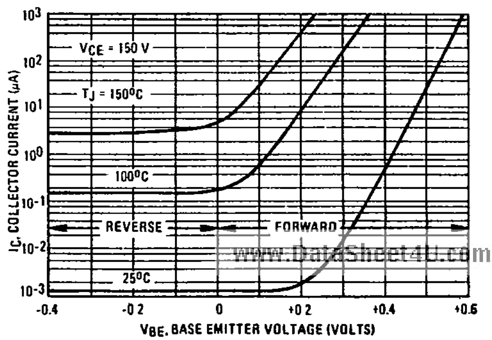


FIGURE 9 — THERMAL RESPONSE

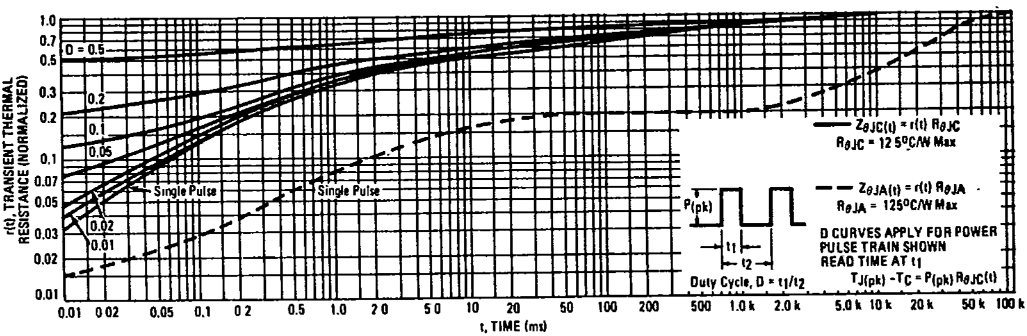
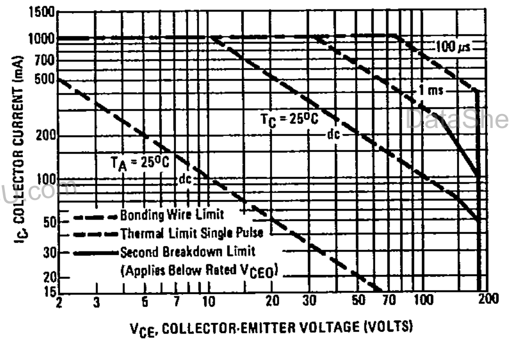


FIGURE 10 — ACTIVE REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 — POWER DERATING