ITE 聯陽半導體 ITE Tech. Inc.

IT7020C/CY

Durable High-Voltage 240-Channel Common Driver for Dot-Matrix STN LCD

Preliminary Specification V0.7

INTEGRATED TECHNOLOGY EXPRESS, INC.

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Revision History

Section	Revision	Page No.
-	• IT7020C/H was changed into IT7020C/CY in this version. • Section 4.2 “Chip Form Package (349 bumps)” of version 0.6 was deleted.	-
10	• The figures in section10 were revised.	25, 26
11	• The ordering information was revised.	27

CONTENTS

FIGURES

TABLES

1. Features

- **Supports up to 1/240 display duty**
- **Supports 43V LCD drive voltage at maximum**
- **Supports 2.5 to 5.5V operating voltage**
- **Provides 240 LCD drive circuit**
- **Provides built-in power circuit for generating –21.5 V**
- **Provides the intermediate voltage interface**
- **Provides 3 selections of output modes:**
  - 240-output mode
  - 200-output mode
  - 160-output mode
- **Built-in alternating signal generation circuit (programmable through the MWS0 – MWS4 pins) is provided to restrain crosstalk**
- **Supports the display-off function**
- **Package**
  - 273-pin Flex TCP

2. General Description

The IT7020C/CY features a high-voltage common driver, which consists of 240 channels. The IT7020C/CY can drive a dot matrix STN LCD panel, and has been designed specifically to meet the LCD requirement in PDA devices. It can be used in conjunction with the segment drivers: IT7010C/H or IT7012C/H.

In terms of power consumption, the device is able to reduce the required voltage level and power consumption considerably. Additionally, the built-in screen display off function supported in the device can also help to reduce the overall power consumption while the LCD panel is not actively in use. In logic portion, the IT7020C/CY operates with a low 3V logic drive voltage to help reduce power consumption.

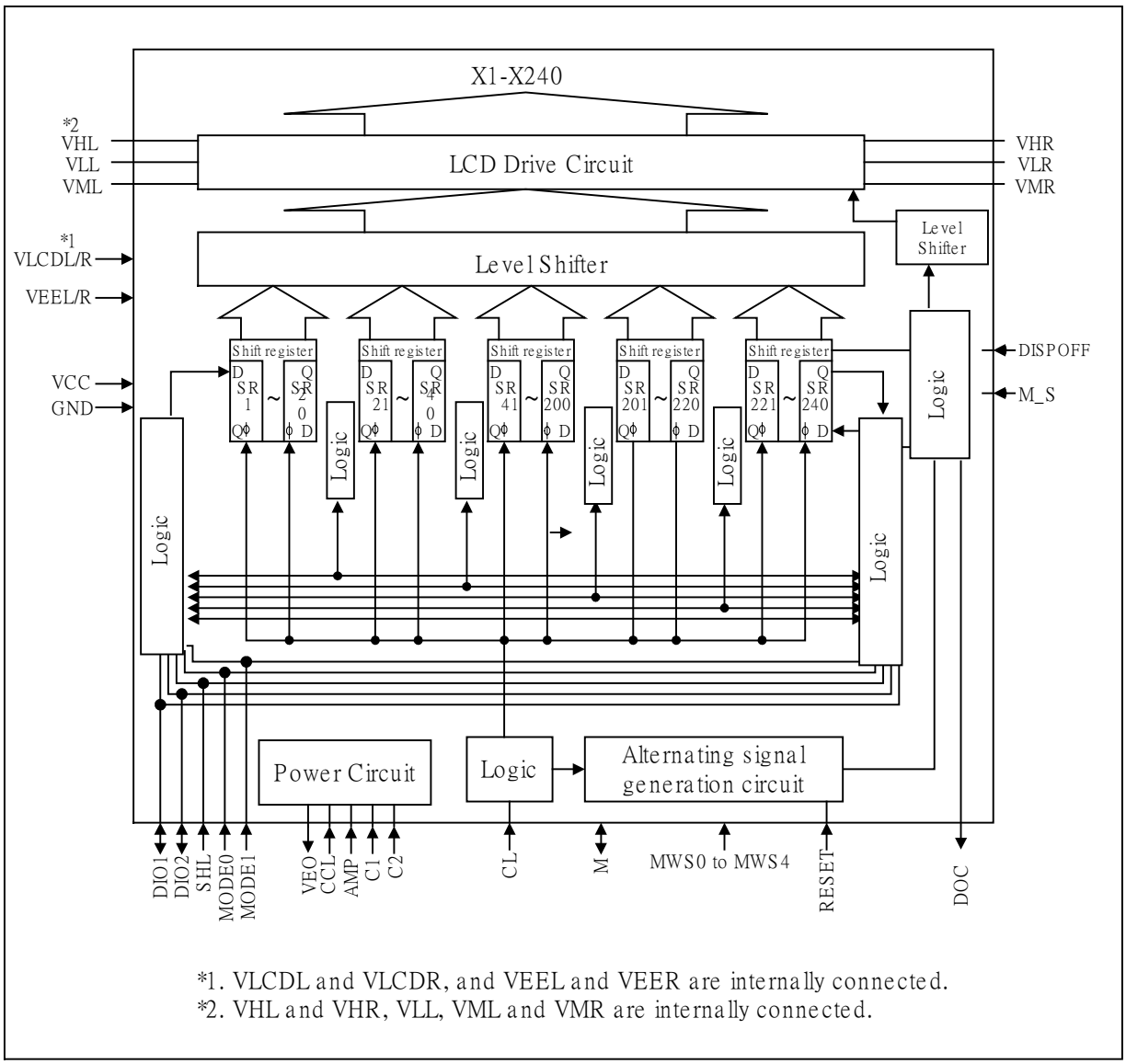
The device can generate a high voltage drive of +21.5V and –21.5V through a 43V high voltage CMOS process technology. By the built-in power circuit and external capacity, the generation of –21.5V will occur from +21.5V.

In addition, users are allowed the selection of 240-, 200- and 160-channel output mode by conveniently changing the mode according to what panel resolution they have.

Moreover, ITE also provides users with complete local technical support. The company is dedicated to assisting customers in procuring multiple competitive edges, such as reducing development time, cost effectiveness and low power consumption for expanding the STN-LCD market share in a fast move.

ITE is committed to launching the LCD driver and controller series products, and will offer the most competitive solution through high integration and solid R&D expertise.

3. Block Diagram



*1. VLCDL and VLCDR, and VEEL and VEER are internally connected.
*2. VHL and VHR, VLL, VML and VMR are internally connected.

4. Pin Configuration

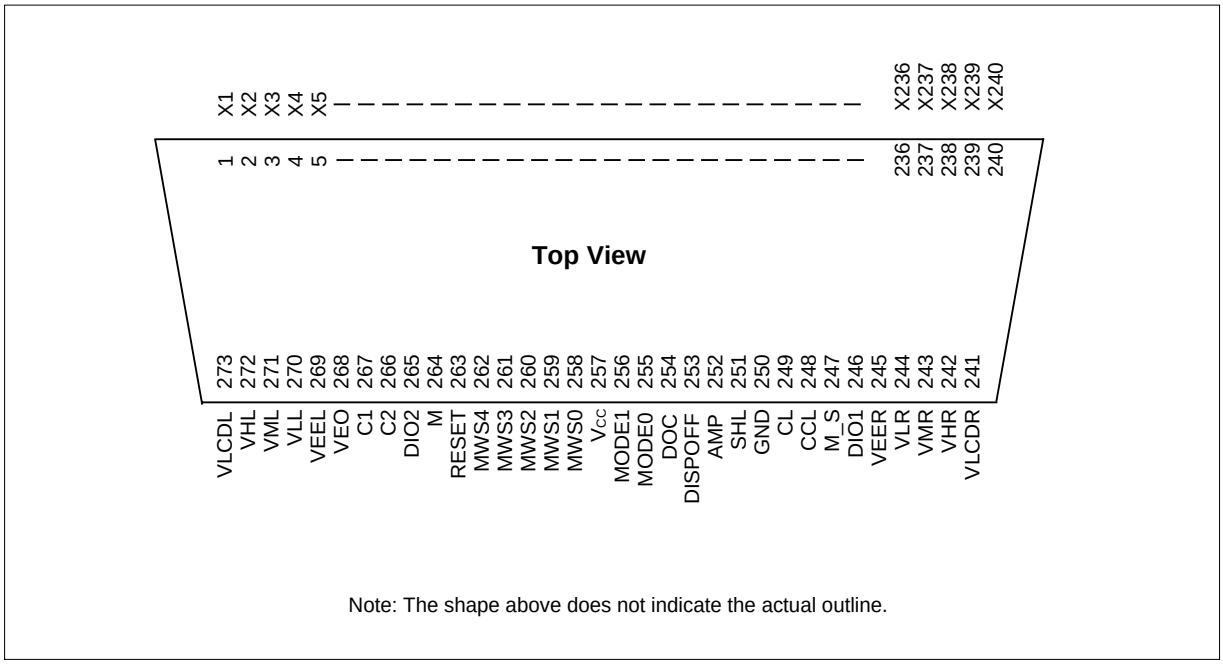


Figure 4-1. 273-pin TCP

5. IT7020C/CY Pin Descriptions

Table 5-1. Pin Descriptions of Power Signals

Pin(s) No.	Symbol	Attribute	Description
267, 266	**C1, C2**	-	Connect the external capacitance here when the power circuit is enabled for VEE generation. It is advisable that users should not connect any traces to these pins if the built-in power circuit is not used.
273, 241 **269, 245** **257, 250**	**VLCDL/R** **VEEL/R** **Vcc, GND**	-	VLCDL/R and VEEL/R are used to provide the power supply for the usage of LCD drive. VEEL/R are used to provide the power supply for the usage of power circuits. Vcc, GND are used to provide the power supply for the usage of logic circuits.
272, 242 **270, 244** **271, 243**	**VHL/R** **VLL/R** **VML/R**	Input	These pins are used to provide the power supply for LCD drive level. VHL/R and VLL/R indicate the selected level of LCD drive. Note that VHL/R is set to the same voltage as VLCDL/R while VLL/R is set to the same voltage as VEEL/R. VML/R indicates the non-selected LCD drive level. It provides the power supply for the built-in power circuits as well.
268	**VEO**	Output	Connect VEO pin to the VEEL/R pins when the built-in power circuit is enabled to generate VEE voltage. In this case, the VM voltage is used as the point of reference and the output voltage of VEO is equal to (2*VM – VLCD). Users are advised not to connect any lines to this pin if the built-in power circuit is not used.

Table 5-2. Pin Descriptions of Control Signals

Pin(s) No.	Symbol	Attribute	Description
252	**AMP**	Input	This signal is used to control the on and off states the built-in power circuit. When the circuit is used, this pin must be tied to Vcc. When the built-in power circuit is not used, this pin must be tied to GND.
248	**CCL**	Input	Indicates the built-in power circuit clock input. When the built-in power circuit is enabled and VEE is generated, this pin is connected to the CL pin. When the built-in power circuit is not used, CCL must be tied to GND.
249	**CL**	Input	***Shift Clock Input.*** Data is shifted and latched at the falling edge of CL in the shift register.
246 **265**	**DIO1** **DIO2**	Input/ Output	***Serial Data Input/Output Pin.*** When the SHL is high, the DIO1 is the serial output pin and DIO2 is the serial input pin. When the SHL is low, the DIO1 is the serial input pin and DIO2 is the serial output pin.
253	**DISPOFF**	Input	Set LCD drive outputs of X1 to X240 to the VM level by connecting this pin to GND.

Table 5-2. Pin Descriptions of Control Signals [cont'd]

<table>
<tr><th>Pin(s) No.</th><th>Symbol</th><th>Attribute</th><th>Description</th></tr>
<tr><td>254</td><td>DOC</td><td>Output</td><td>When the M_S pin is set to high level, the output level of DOC pin is the same as the DISPOFF pin.
When the M_S pin is set to low level, DOC pin outputs low level until serial data input 16 times. See Figure 5-1 for more details.
Note that when M_S is set to low level, the DOC pin should be connected to IT7010C DOF_N control pin.</td></tr>
<tr><td>264</td><td>M</td><td>Input/Output</td><td>Input or output the toggling waveform for LCD drive output level.</td></tr>
<tr><td>247</td><td>M_S</td><td>Input</td><td>Control the LCD display-off function and determine the LCD display-off signal to output from DOC pin.
When the M_S is set to high level and the DISPOFF is low level, X1-X240 pins will set to the VM level.
When the M_S is set to low level, the X1-X240 pins will stay on the VM level until serial data input 16 times (See Figure 5-1).</td></tr>
<tr><td>255
256</td><td>MODE0
MODE1</td><td>Input</td><td>Input terminals for specifying the effective number of LCD drive output pins.
<table>
<tr><th>MODE0</th><th>MODE1</th><th>Shift Direction</th></tr>
<tr><td>“H”</td><td>“H”</td><td>240-output (X1, X2, X3…X238, X239, X240)</td></tr>
<tr><td>“H”</td><td>“L”</td><td>200-output (X21, X22, X23…X218, X219, X220)</td></tr>
<tr><td>“L”</td><td>“H”</td><td>160-output (X41, X42, X43…X198, X199, X200)</td></tr>
<tr><td>“L”</td><td>“L”</td><td>Undefined. Use at your own risk!</td></tr>
</table></td></tr>
<tr><td>258
259
260
261
262</td><td>MWS0
MWS1
MWS2
MWS3
MWS4</td><td>Input</td><td>These pins are used to specify the frequency of the toggling signal (M signal) in the unit of number of display lines. The number of display lines is an integer ranging from 2 to 31 and is specified in the table below. Typically, the number of display lines ranges from 10 to 31.
If IT7020 is configured in the slave mode, i.e., driven by an external M signal, MWS0 – MWS4 should be tied to low level.
<table>
<tr><th>Number of lines</th><th>MWS 4</th><th>MWS 3</th><th>MWS 2</th><th>MWS 1</th><th>MWS 0</th><th>Line toggling waveform</th><th>M-pin status</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-</td><td>Input</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Prohibited</td><td rowspan="5">Output</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2 lines alternated</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>3 lines alternated</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>31</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31 lines alternated</td></tr>
</table></td></tr>
<tr><td>263</td><td>RESET</td><td>Input</td><td>Initialize the toggling signal (M signal) circuit by connecting this pin to GND. Tied to Vcc for normal operation.</td></tr>
<tr><td>251</td><td>SHL</td><td>Input</td><td>This pin is used to switch the shift directions.
<table>
<tr><th>SHL</th><th>MODE0</th><th>MODE1</th><th>Shift Direction</th></tr>
<tr><td></td><td></td><td></td><td>Right shift</td></tr>
<tr><td rowspan="3">“H” level</td><td>“H”</td><td>“H”</td><td>DIO2→SR1…SR240→DIO1</td></tr>
<tr><td>“H”</td><td>“L”</td><td>DIO2→SR21…SR220→DIO1</td></tr>
<tr><td>“L”</td><td>“H”</td><td>DIO2→SR41…SR200→DIO1</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td></td><td></td><td></td><td>Left shift</td></tr>
<tr><td rowspan="3">“L” level</td><td>“H”</td><td>“H”</td><td>DIO1→SR240…SR1→DIO2</td></tr>
<tr><td>“H”</td><td>“L”</td><td>DIO1→SR220…SR21→DIO2</td></tr>
<tr><td>“L”</td><td>“H”</td><td>DIO1→SR200…SR41→DIO2</td></tr>
</table>
SR1, SR2…SR240 are the outputs of the shift registers and correspond to X1, X2…X240.
Note: The 40 or 80 pins, which are invalidated at the 200 or 160-output mode, will output the non-selected level (VM).</td></tr>
</table>

Table 5-3. Pin Descriptions of LCD Drive Output Signals

Pin(s) No.	Symbol	Attribute	Description
1 to 240	**X1 to X240**	Output	***LCD Drive Output.*** When DISPOFF is set to Vcc, the output level of X1 – X240 are determined by the combination of the display data and the M signal. Either one of VH, VL, or VM is selected and then transmitted to the output circuit. See Figure 5-2 for more details.

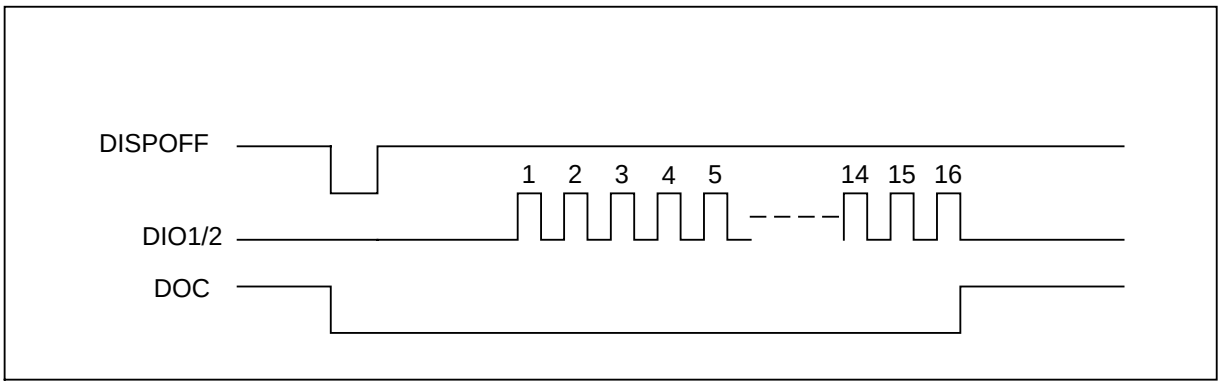


Figure 5-1. DOC Waveform

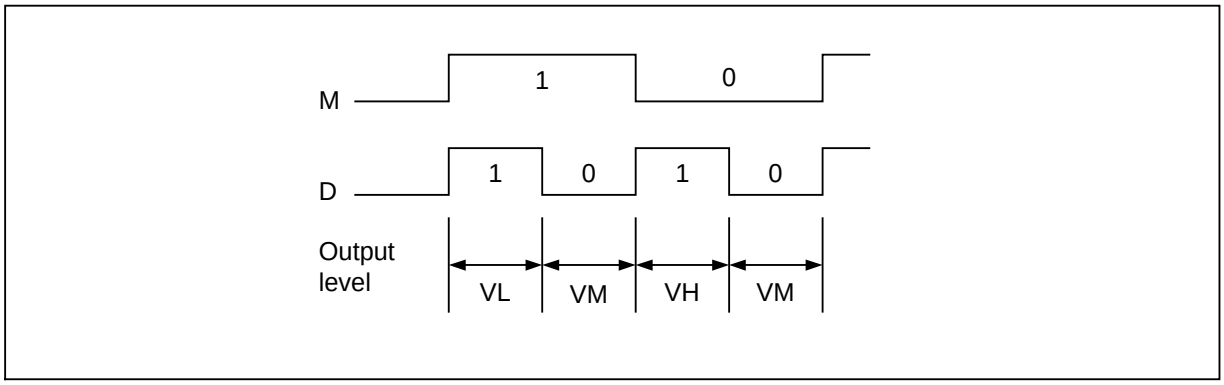


Figure 5-2. LCD Driver Terminal Output Voltage Level

6. System Configuration

6.1 Overview

The IT7020 is composed of 4 main elements to work properly: LCD Drive Circuits, Level Shifter, Shift Register Circuit, and Alternating Signal Generation Circuits. The functional descriptions for each of the 4 elements are described below:

6.2 LCD Drive Circuit

The device consists of 240 LCD drive circuits, and each of the LCD drive circuit is responsible to select and output the three level signals for the LCD drive. Either one of VH, VL and VM will be selected and transmitted to the output circuit by combining the data in the shift register and M signal together. The level shifter is responsible for boosting a logic voltage to the high for LCD drive.

6.3 Shift Register Circuit

The shift register circuit is made up of 240 bits and is bi-directional. The first line marker signal, coming from either DIO1 or DIO2 pins, can be sequentially shifted through the shift register circuit via the shift clock. The first line marker signal can be then sequentially shifted via the shift clock CL. The shifting direction is determined by SHL pin.

6.4 Alternating Signal (M) Generation Circuit

The alternating Signal Generation circuit is used to generate an alternating signal (M signal) for proper LCD display. To restrain the crosstalk function, the signal is alternated from several lines to a host of lines. If pins MWS0 to MWS4 are connected to Vcc or GND, the intended number of signals can be alternated. Note that the connection of pins MWS0 to MWS4 with GND can be done when the alternating signals are input externally.

7. Terminal Configuration

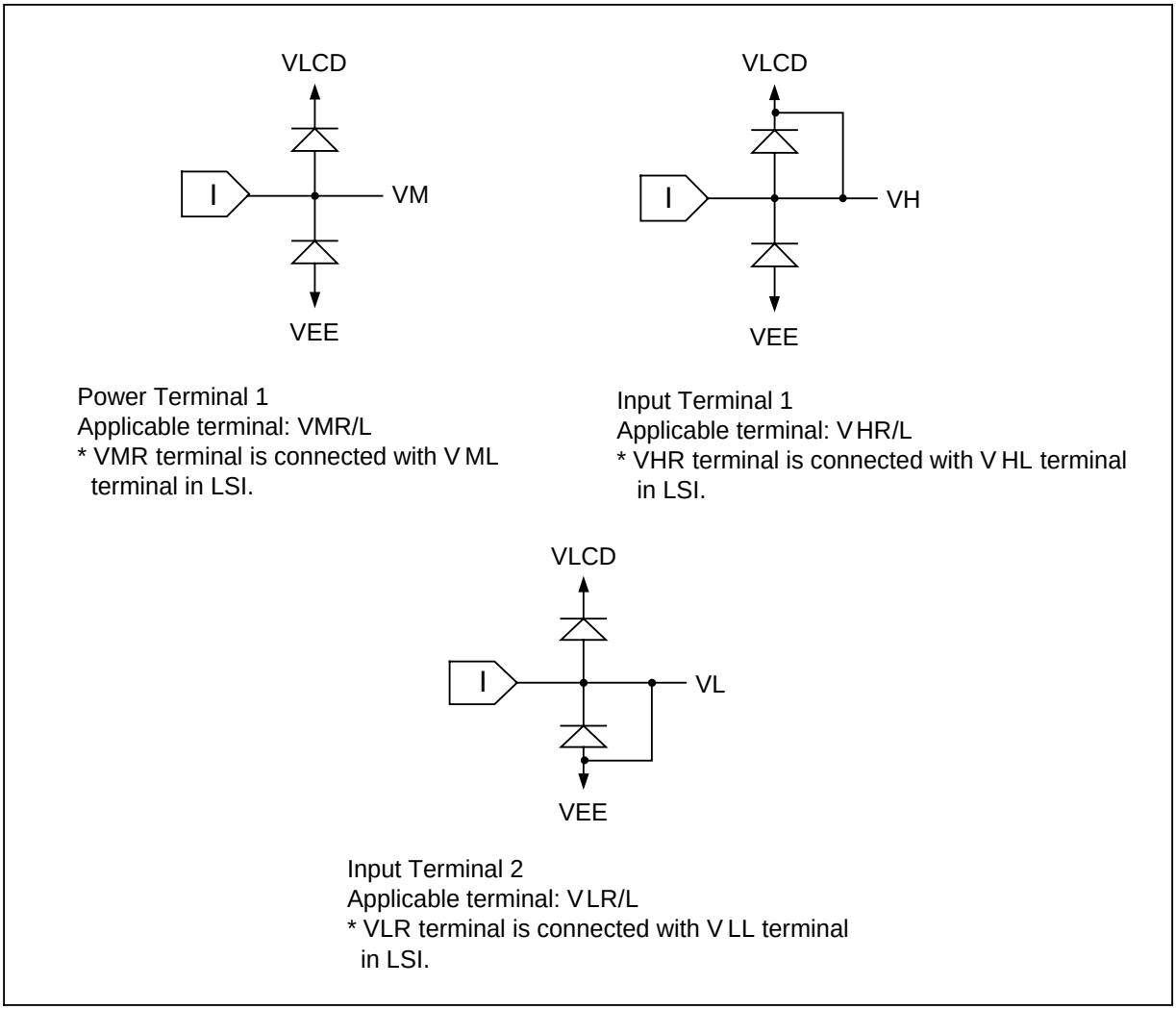


Figure 7-1. IT7020 Power and Input Terminal Configuration

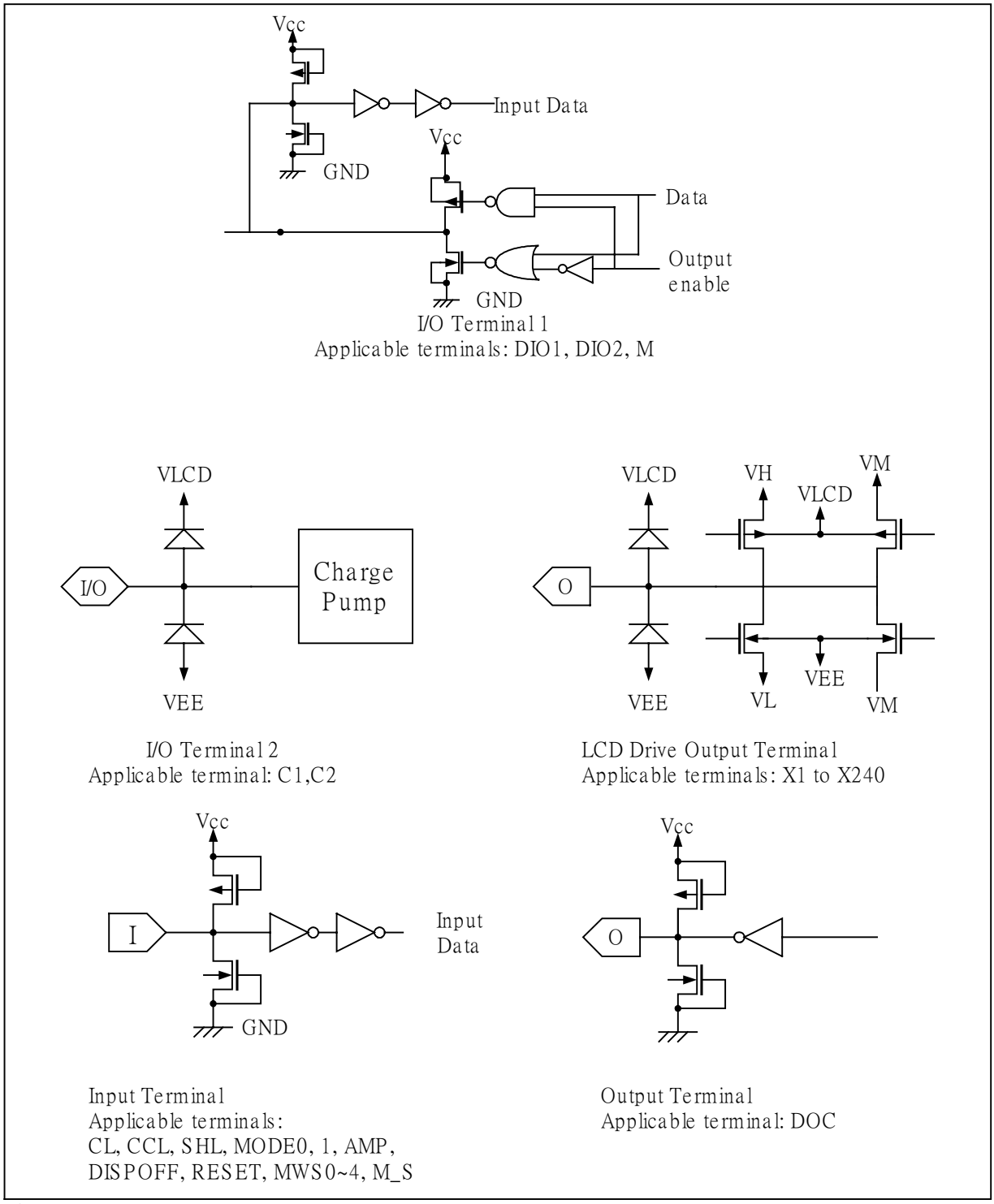


Figure 7-2. IT7020 I/O, Input and Output Terminal Configuration

8. DC Electrical Characteristics

Absolute Maximum Ratings

Power Supply (Vcc) ..... -0.3 to +7.0V
Power Supply (VLCD)..... -0.3 to +25.0V
Power Supply (VEE) ..... -23.0 to +0.3V
Input Voltage (1) (VT1)..... -0.3 to Vcc +0.3
Input Voltage (2) (VH) ..... -0.3 to VLCD
Input Voltage (3) (VL)..... -0.3 to VEE
Input Voltage (4) (VM)..... -0.3 to +5.0V
Operating temperature (Topr)..... -25 to +75°C
Storage temperature (Tetg).....-55 to +110°C

***Comments:**

Stresses above those listed under ″Absolute Maximum Ratings″ may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Symbol	Ratings	Unit	Notes
Power supply voltage	Logic circuit	Vcc	-0.3 to + 7.0	V	1, 8
	LCD drive circuit	VLCD	-0.3 to + 25.0	V	1, 3, 8
		VEE	-23.0 to + 0.3	V	1, 4, 8
Input voltage (1)		VT1	-0.3 to Vcc + 0.3	V	1, 2
Input voltage (2)		VH	-0.3 to VLCD	V	1, 5, 8
Input voltage (3)		VL	-0.3 to VEE	V	1, 6, 8
Input voltage (4)		VM	-0.3 to + 5.0	V	1, 7, 8
Operating temperature		Topr	-25 to + 75	°C	-
Storage temperature		Tetg	-55 to + 110	°C	-

Notes: 1. Indicates the voltage from GND.
2. The input voltage (1) is applicable to DIO1, DISPOFF, SHL, M, MWS0-MWS4, RESET, MODE0, MODE1, CL, M_S, AMP, CCL, and DIO2.
3. The power supply voltage for LCD drive circuits can be applied to VLCDL/R pins.
4. The power supply voltage for LCD drive circuits can be applied to VEE/R pins.
5. The input voltage (2) is applied to VHL/R pins.
6. The input voltage (3) is applied to VLL/R pins.
7. The input voltage (4) is applied to VML/R pins.
8. See section 8.1 for details.

8.1 Activation and Inactivation Sequence

Make sure to follow activation and inactivation sequence for power supplies and signals as illustrated in the Figure 8-1. This sequence is applied to the built-in power circuit. It is recommended that users must follow the sequence correctly; otherwise, the device malfunction, permanent damage, or undesired effects may occur.

8.1.1 Power On Sequence

1. Power on the power supply in the order listed below:
   Power On order: GND-Vcc, GND-VLCD (VH), and VM.
   VM-VEE is generated automatically. Input GND power to the DISPOFF pin.
2. The LCD level is forced to output the VM level through the DISPOFF function.
3. The DISPOFF function has a higher priority even if the input signal distortion occurs instantly after Vcc input.
4. Then input the preset signals to get the driver registers initialized. In this case, make sure a period that lasts more than one frame is reserved.
5. The preceding work for normal display is completed here. At this point, users should cancel the DISPOFF function by setting the DISPOFF pin to Vcc. The voltage levels of VEE (VL), VLCD (VH) and VM must have reached the preset voltage respectively.

8.1.2 Power Down Sequence

Shut down the power in an opposite order described for power on sequence on the last page.

1. Firstly, the DISPOFF pin should be set to GND.
2. Secondly, the LCD power supply of GND-VLCD (VH) should be turned off. At the same time, GND-VEE (VL) gets to VM. Shut off the VM next.
3. Vcc should be set, and the input signal should be set to GND.
4. At this moment, the inputs of pins VEE (VL), VLCD (VH) and VM must go down to 0 V completely.
   In addition, an incorrect display may occur at power down or power on. This is because the function of DISPOFF is inactivated when the Vcc level goes down to GND, which may cause the LCD to output a level other than VM.

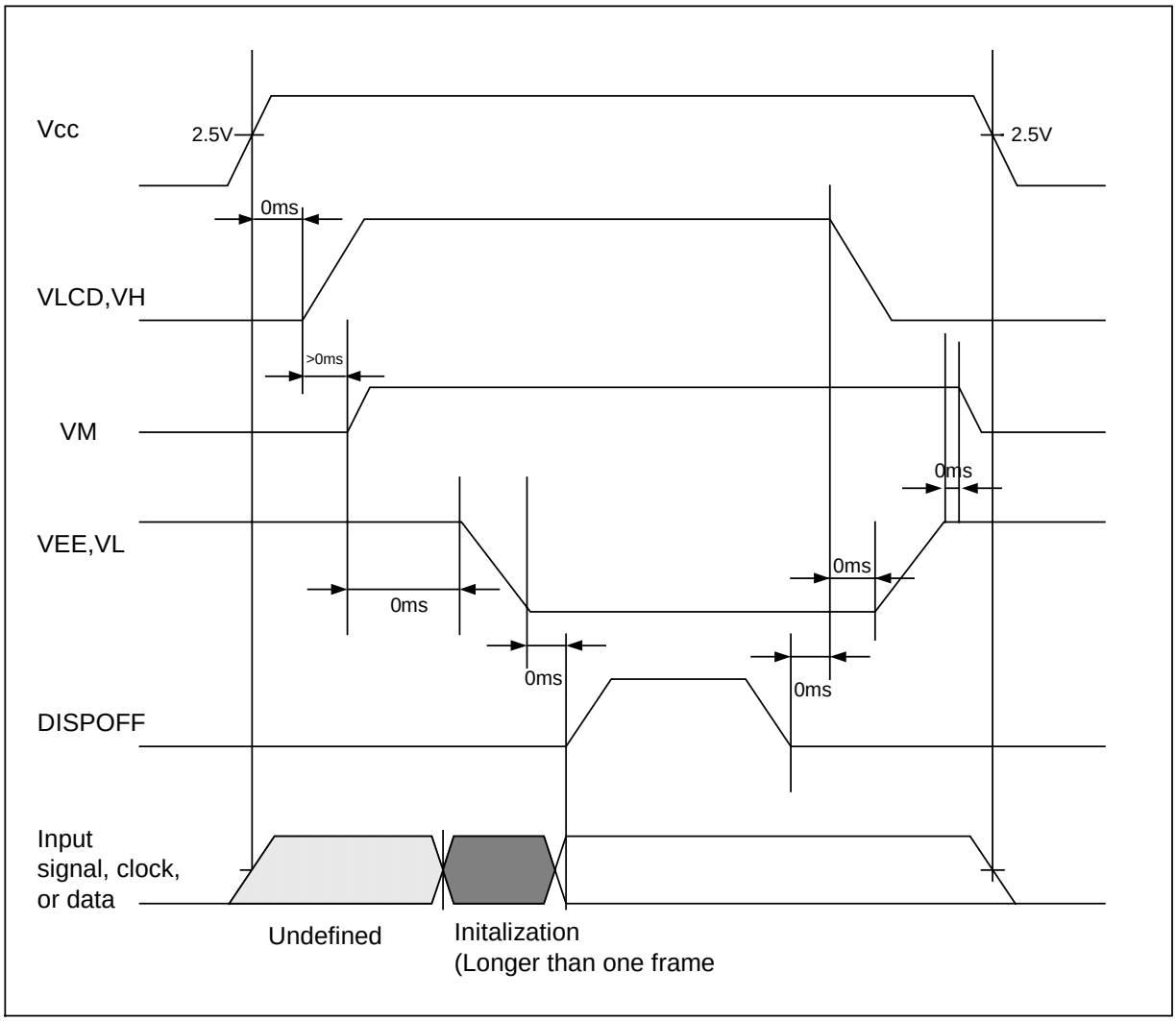


Figure 8-1. IT7020 Power On/Down Scenario

8.2 DC Electrical Characteristics (Vcc = 2.5 to 5.5V, GND = 0V, VLCD – VEE = 15 to 43V, Ta = –25 to +75 °C)

1. The parameter ″ON resistance between Vi —Xj″ in the table below indicates a resistance value between of the X and one of the V pins (either one of VH, VL, or VM) when a load current is applied to one of X1 to X240 pins. These resistance values are specified under the conditions listed below:
   VLCD = VH = 21.75V, VEE = VL =-18.5V, VM = 1.75V, GND = 0V.
   Use VH, VL, and VM in the range of VLCD – VM ≥ VH – VM = 21.5 to 7.5V, VEE – VM≤VL – VM = -21.5 to –7.5V in the relation of VH>VM>VL.
2. The current applied between the input and output is removed. The power supply current will increase through the current flows between the power supplies under the condition that an input to a CMOS gate is at an intermediate level. Therefore, use V_{IH} = Vcc and V_{IL} = GND.
3. The voltage relationship of each signal is illustrated in Figure 8-2:

Table 8-1. DC Characteristics (Vcc = 2.5 to 5.5V, GND = 0V, VLCD – VEE = 15 to 43V, Ta = –25 to +75 °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions	Applicable Pin(s)
V_{IH}	Input high-level voltage	0.7×Vcc	—	Vcc	V		DIO1, DISPOFF, SHL, M, M_S, MWS0~4, RESET CL, MODE0, MODE1, AMP, CCL, DIO2
V_{IL}	Input low-level voltage	0	—	0.3×Vcc	V		
V_{OH}	Output high-level voltage	Vcc-0.4	—	—	V	I_{OH} = -0.4 mA	M, DOC, DIO1, DIO2
V_{OL}	Output low-level voltage	—	—	0.4	V	I_{OL} = 0.4 mA	
RON	ON resistance between Vi —Xj	—	0.7	2.0	kΩ	I_{ON} = 150 µA	X1-X240, V pin
$I_{IL}1$	Input leak current (1)	-5	—	5	µA		DIO1, DISPOFF, SHL, M, M_S, MWS0~4, RESET, CL, MODE0, MODE1, AMP, CCL, DIO2
$I_{IL}2$	Input leak current (2)	-25	—	25	µA		VH, VL, VM
$I_{CC}1$	Current consumption (1)	—	5	40	µA		Vcc=3.3V, V_{LCD} - V_{EE}=40V, F_{CL}=19.2kHZ, f_M=1.5kHz,
$I_{CC}2$	Current consumption (2)	—	10	50	µA		Vcc=5.0V, V_{LCD} - V_{EE}=40V, F_{CL}=19.2kHZ, f_M=1.5kHz,
I_{LCD}	Current consumption (3)	—	25	100	µA	No loading, External charge bump	Vcc=3.3V, V_{LCD} - V_{EE}=40V, F_{CL}=19.2kHZ, f_M=1.5kHz,

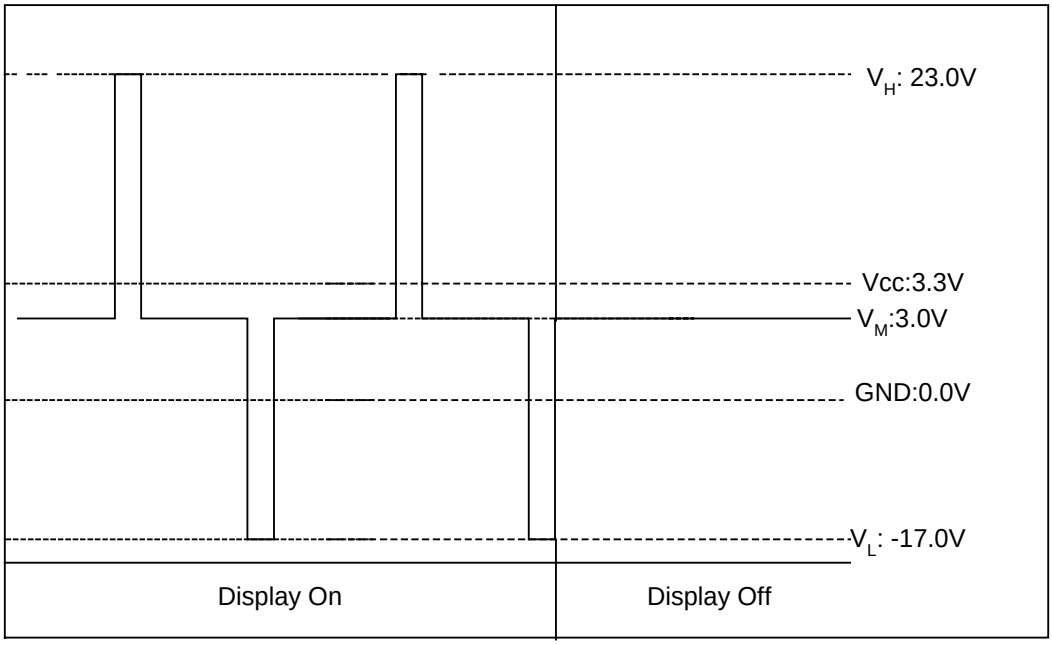


Figure 8-32. LCD Common Drive Output Waveform & Voltage Level

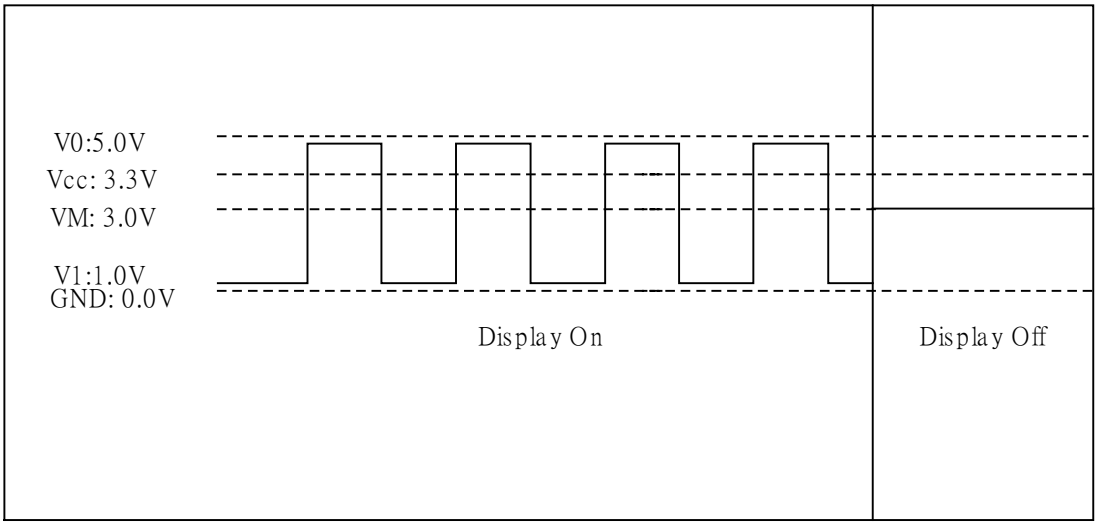


Figure 8-3. LCD Segment Drive Output Waveform & Voltage Level

9. AC Characteristics

9.1 AC Characteristics 1 (Vcc = 2.5 to 5.5V, GND = 0V, VLCD – VEE = 15 to 43V, Ta = –25 to +75 °C)

Table 9-1. AC Characteristics 1(Vcc = 2.5 to 5.5V, GND = 0V, VLCD – VEE = 15 to 43V, Ta = –25 to +75 °C)

Symbol	Parameter	Applicable Pins	Min.	Typ.	Max.	Unit
t_{CYC}	Clock cycle time	CL	400		—	ns
t_{CWH}	CL high-level width	CL	25		—	ns
t_{CWL}	CL low-level width	CL	370		—	ns
t_r	CL rising time	CL	—		30	ns
t_f	CL falling time	CL	—		30	ns
t_{DS}	Data set-up time	DIO1, DIO2, CL	100		—	ns
t_{DH}	Data hold time	DIO1, DIO2, CL	10		—	ns
t_{DD}	Data output delay time	DIO1, DIO2, CL	—		200	ns
t_{MD}	M output delay time	M, CL	—		200	ns
t_{MS}	M setup time	M, CL	20		—	ns
t_{MH}	M hold time	M, CL	20		—	ns
t_{DOC1}	DOC delay time 1	DISPOFF, DOC	—		300	ns
t_{DOC2}	DOC delay time 2	DIO1, DIO2, DOC	—		300	ns

9.2 AC Characteristics 2 (Vcc = 2.5 to 4.5V, GND = 0V, VLCD – VEE = 43V, Ta = –25 to +75 °C)

Table 9-2. AC Characteristics 2 (Vcc = 2.5 to 4.5V, GND = 0V, VLCD – VEE = 43V, Ta = –25 to +75 °C)

Symbol	Parameter	Applicable Pins	Typ.	Min.	Max.	Unit
t_{pd1}	Output delay time 1	X (n), M		—	1.2	µs

9.3 AC Characteristics 3 (Vcc = 4.5 to 5.5V, GND = 0V, VLCD – VEE = 43V, Ta = –25 to +75 °C)

Table 9-3. AC Characteristics 3 (Vcc = 4.5 to 5.5V, GND = 0V, VLCD – VEE = 43V, Ta = –25 to +75 °C)

Symbol	Parameter	Applicable Pins	Typ.	Min.	Max.	Unit
t_{pd1}	Output delay time 1	X (n), M		—	0.7	µs

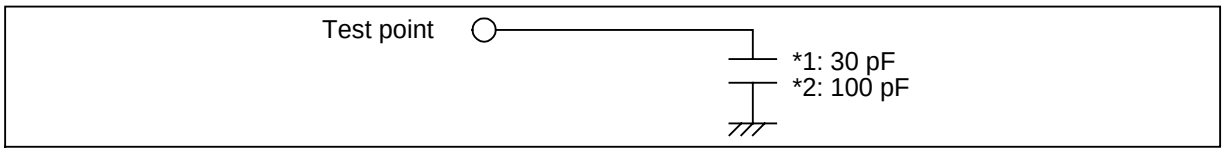


Figure 9-1. AC Characteristics Testing Configuration

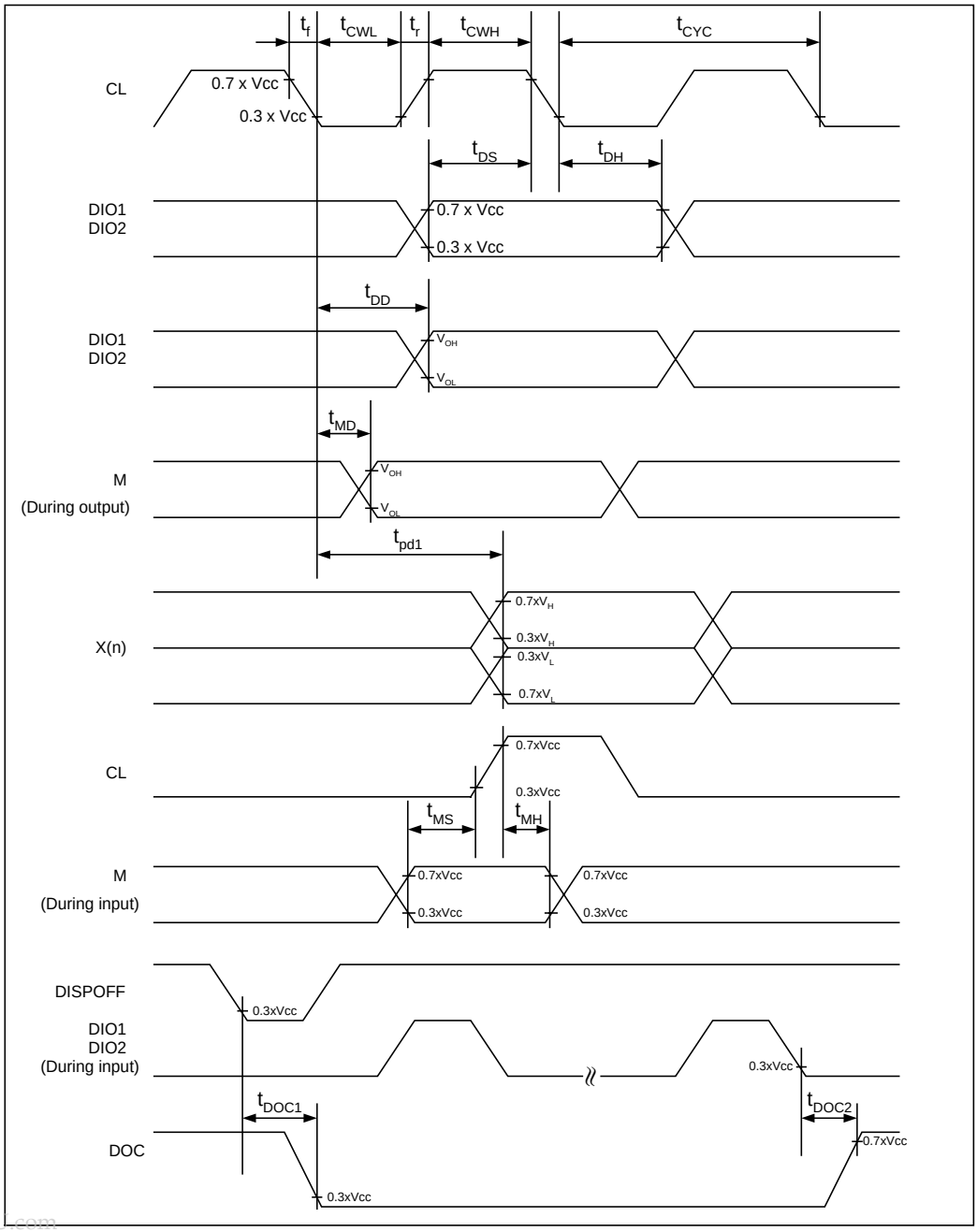


Figure 9-2. IT7020 Timing Diagram

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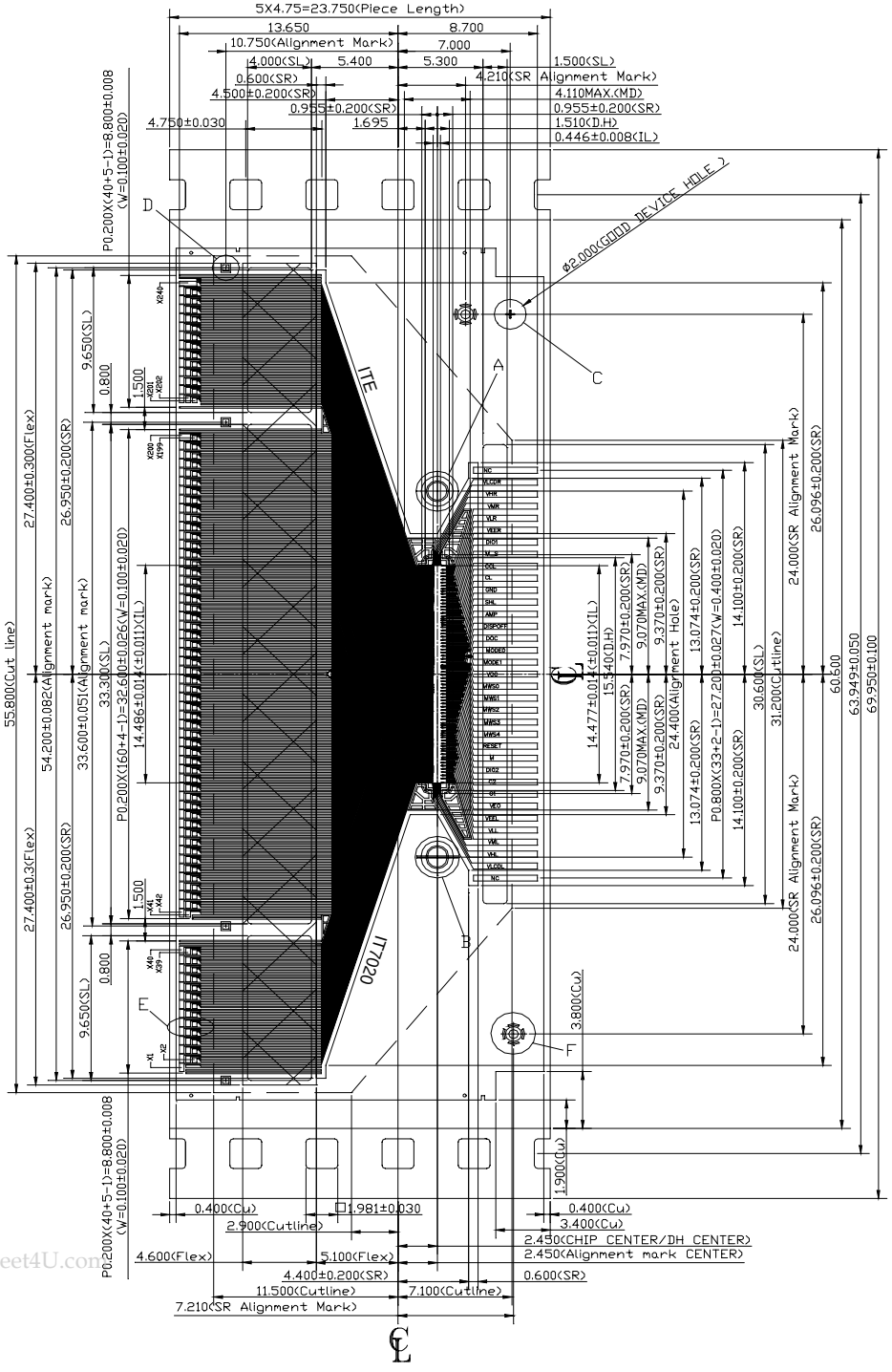
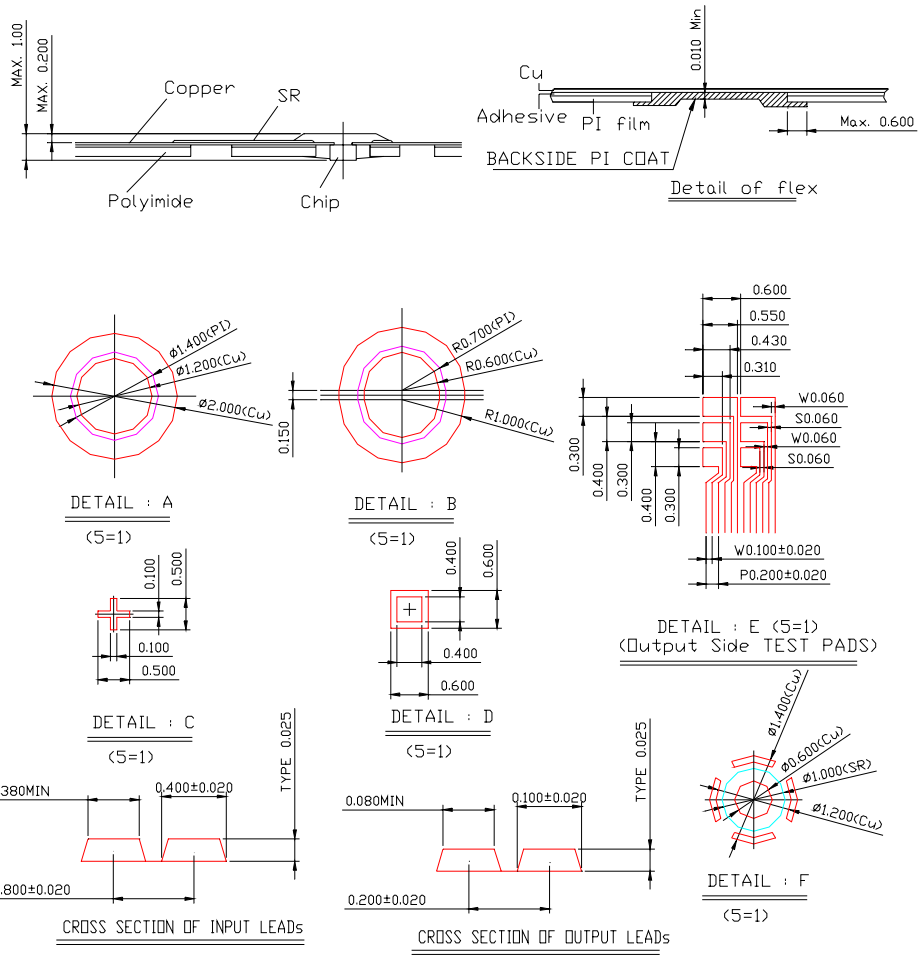
10. Package Information

TCP Outline Dimensions **unit: mm**

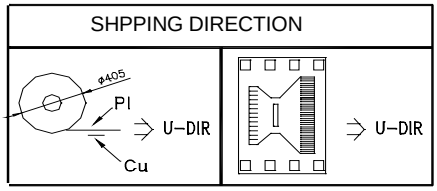


INPUT LEAD NAME

NC
VLCDR
VHR
VMR
VLR
VEER
DIO1
M_S
CCL
CL
GND
SHL
AMP
DISPOFF
DOC
MODE0
MODE1
Vcc
MWS0
MWS1
MWS2
MWS3
MWS4
RESET
M
DIO2
C2
C1
VEO
VEEL
VLL
VML
VHL
VLCDL
NC



NOTE:
1. Film: UPILEX-S 75±5um thickness
   Copper: FQ-VLP 25±5um thickness
   Adhesive: Toray #7100 12±2um thickness
   Solder resist: AE-70-M11 26±14um thickness
2. Flex material: FS-100L 10um min.
3. Plating: Pure Sn thickness : 0.21±0.05um
4. All corner radii of Base Film are less than 0.200mm unless otherwise noted
5. Other specs than displayed in this drawing are based on the standard spec lists
6. All dimensional tolerances of "SR" are ±0.200mm unless otherwise noted
7. All dimensional tolerances of "base film" are ±0.05mm unless otherwise noted
8. Inner lead accumulative pitch:
   output side:14.486±0.014(±0.011) mm
   input side:14.477±0.014(±0.011) mm
9. PKG Reel Size: Ø405 mm



11. Ordering Information

Part No.	Package
IT7020C/CY	273-TCP