IT7012C/H

320-Channel STN LCD Segment Driver

Preliminary Specification V0.4

INTEGRATED TECHNOLOGY EXPRESS, INC.

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Revision History

Section	Revision	Page No.
	• IT7012C was revised to IT7012C/H in this version.	
1	• In section 1, package was revised.	1
2	• In section 2 line7, “Packaged in a fine-pitch flex tape-carrier package (Flex-TCP)” was revised to “Packaged in a fine-pitch flex tape-carrier package (Flex-TCP) and CHIP FORM (433 bumps)”.	3
4	• 4.2 CHIP FORM was added in section 4.	7-13
10	• Section 10 ordering information was revised.	33

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1. Features

- **Supports up to 1/240 duty cycle**
- **Provides 320 LCD drive circuits**
- **Provides 2.6 to 5.5V LCD drive voltage**
- **Provides 2.5 to 5.5V operating voltage**
- **Provides 4-bit or 8-bit parallel data input**
- **Maximum shift clock frequency:**
  - 6.5 MHz (VCC=3V)
  - 8 MHz (VCC=5V)
- **Two output modes are selectable:**
  - 320 output mode
  - 240 output mode
- **Supports screen display off function**
- **Supports the automatic generation of chip enable signal**
- **Supports power standby function**
- **Package:**
  - Flex-TCP
  - can also be shipped in CHIP Form (433 bumps)

2. General Description

The IT features a 320-channel segment driver, which consists, and was designed to drive a mono dot matrix STN-LCD panel, yet requires low voltages.

In power, the device only requires a low 5V LCD drive voltage, and a low 3V-logic drive voltage in logic portion. In terms of power consumption, the device is able to reduce the required voltage level and power consumption considerably. Additionally, the power standby function supported in the device can also help to reduce the overall power consumption while the LCD panel is not actively in use.

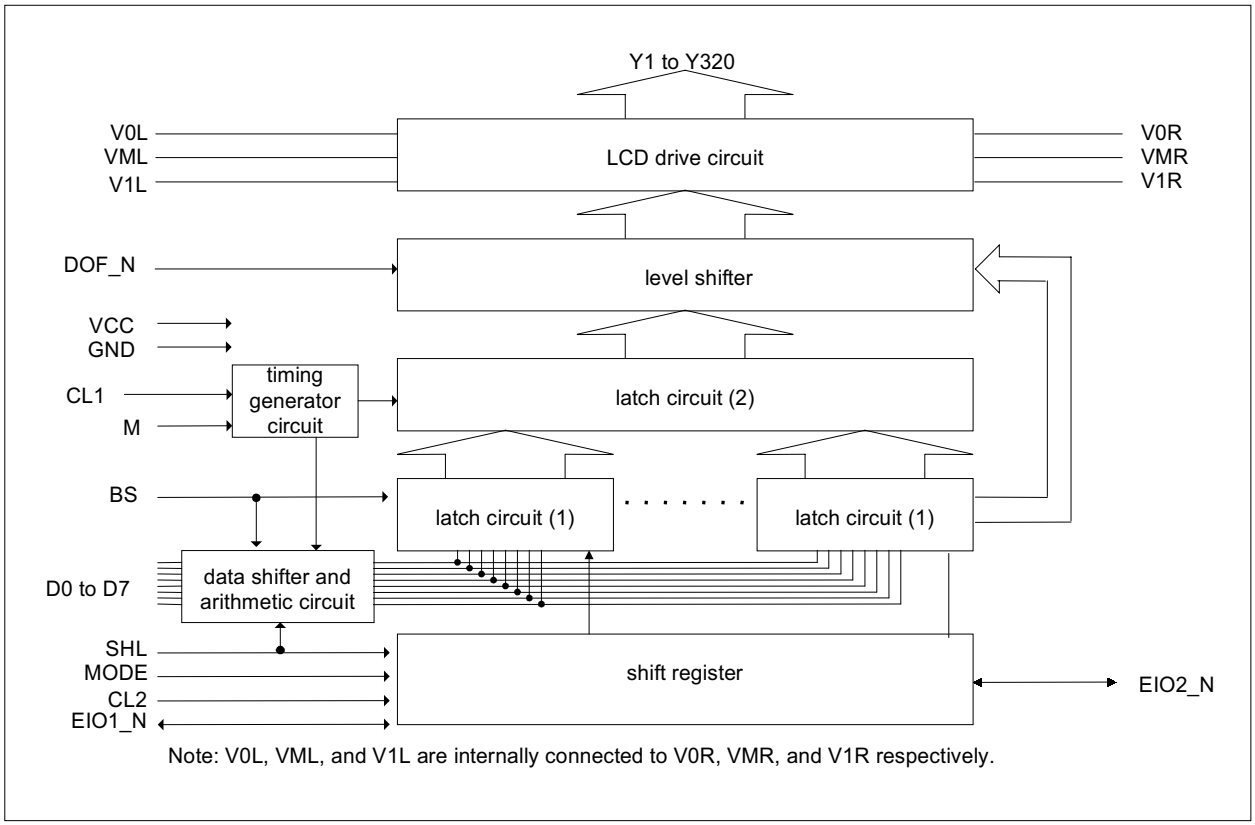
Packaged in a fine-pitch flex tape-carrier package (Flex-TCP) and CHIP FORM (433 bumps), the cost-effective IT provides 4 or 8 data bits, and the shift clock speed allowed is up to 6.5MHz and 8MHz for 3V logic drive voltage and 5V LCD drive voltage respectively.

In addition, users are allowed to select either 320-channel or 240-channel output mode by conveniently changing the mode according to what panel resolution they have.

In addition, ITE also provides users with complete local technical support, and will assist customers in procuring multiple competitive edges, such as reducing development time, cost effectiveness and low power consumption for expanding the STN-LCD market share.

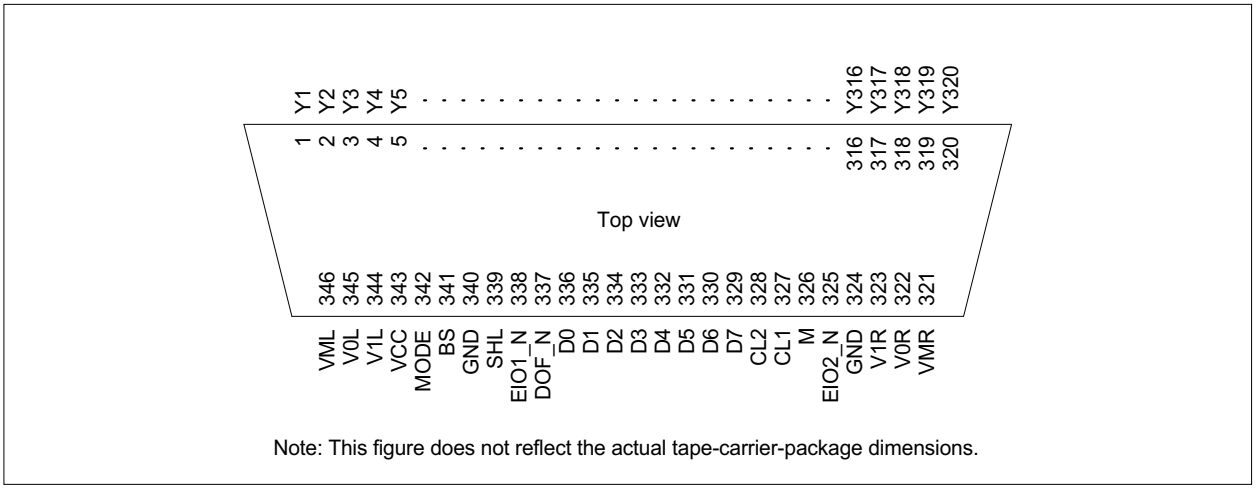
ITE is committed to launching the LCD driver and controller series products, and will offer the most competitive solution through high integration and solid R&D expertise.

3. Block Diagram



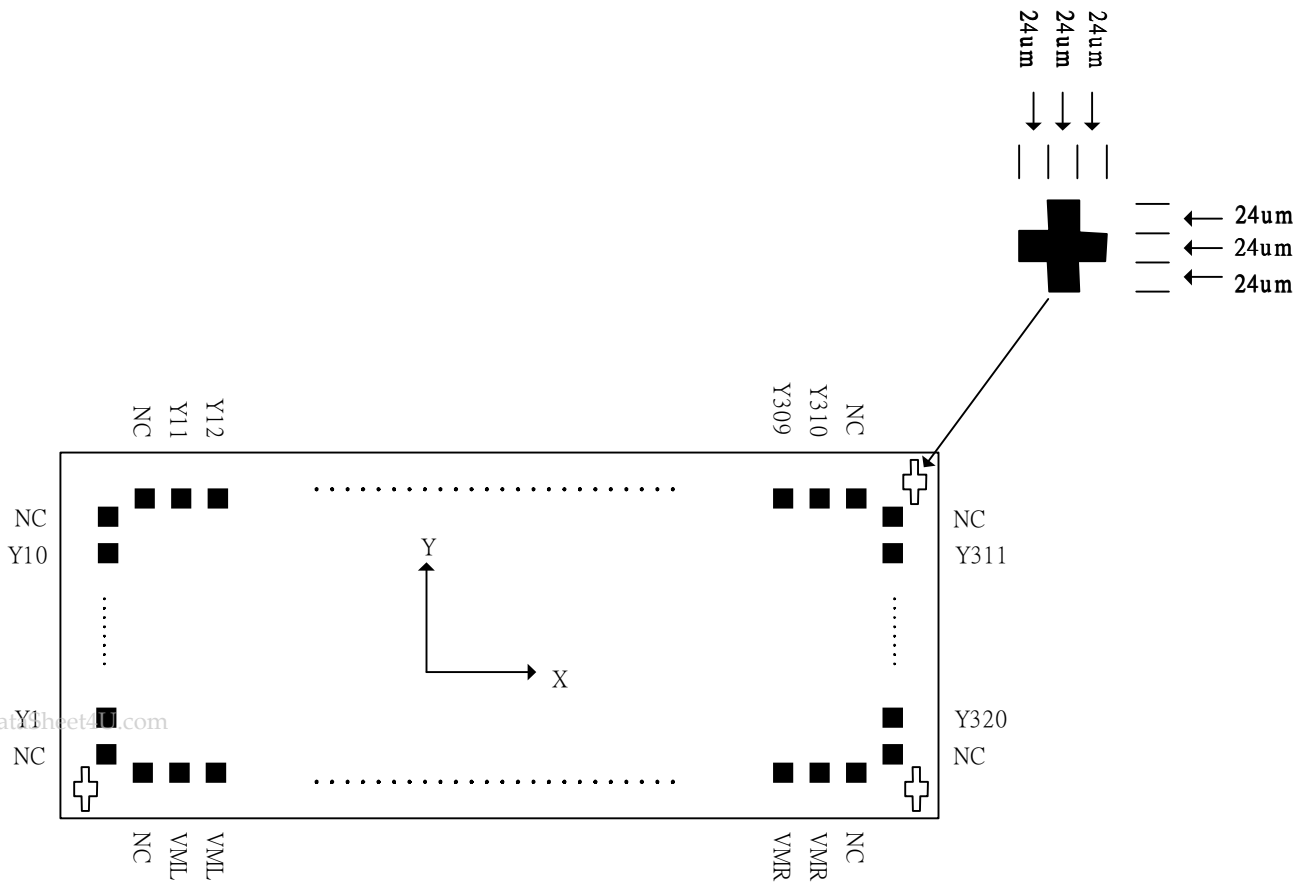
4. Pin Configuration

4.1 Flex-TCP



Note: This figure does not reflect the actual tape-carrier-package dimensions.

4.2 CHIP FORM (433 bumps)



1. Chip size: 18090μm * 1012μm (exclude scribe line).
2. Coordinate: Bump center
3. Origin: Chip center
4. Chip window: (-9045, -506), (9045, 506)
5. Minimum bump pitch: 55μm
6. Chip thickness: 21mil (Typical)

Table 4–1. Bump Name and Bump Size

Bump No.	Bump Name	Bump size (Typical)		
		X (μm)	Y (μm)	H (μm)
1, 302 315, 421	NC	58	60	18
2~301	Y310 ~ Y11	40	70	18
304 ~ 313	Y10 ~ Y1	70	37	18
423 ~ 432	Y320 ~ Y311	70	37	18
303, 314 422, 433	NC	60	58	18
*****	Other bumps	58	60	18

Table 4–2. Align Mark Locations

Align mark type	Align mark center coordinate		Align mark size or diameter (μm)
	X (μm)	Y (μm)	
Cross	8971.05	439.65	72
Cross	8971.05	-426	72
Cross	-8972.8	-426	72

Notes:

1. Don’t connect any wires to NC bumps.

Table 4–3. Bump Center Coordinates (Unit: µm)

Bump No.	Bump Name	Coordinate		Bump No.	Bump Name	Coordinate		Bump No.	Bump Name	Coordinate	
		X-axis	Y-axis			X-axis	Y-axis			X-axis	Y-axis
1	NC	8884.5	442	33	Y279	6991.5	437	65	Y247	5103.5	437
2	Y310	8820.5	437	34	Y278	6932.5	437	66	Y246	5044.5	437
3	Y309	8761.5	437	35	Y277	6873.5	437	67	Y245	4985.5	437
4	Y308	8702.5	437	36	Y276	6814.5	437	68	Y244	4926.5	437
5	Y307	8643.5	437	37	Y275	6755.5	437	69	Y243	4867.5	437
6	Y306	8584.5	437	38	Y274	6696.5	437	70	Y242	4808.5	437
7	Y305	8525.5	437	39	Y273	6637.5	437	71	Y241	4749.5	437
8	Y304	8466.5	437	40	Y272	6578.5	437	72	Y240	4690.5	437
9	Y303	8407.5	437	41	Y271	6519.5	437	73	Y239	4631.5	437
10	Y302	8348.5	437	42	Y270	6460.5	437	74	Y238	4572.5	437
11	Y301	8289.5	437	43	Y269	6401.5	437	75	Y237	4513.5	437
12	Y300	8230.5	437	44	Y268	6342.5	437	76	Y236	4454.5	437
13	Y299	8171.5	437	45	Y267	6283.5	437	77	Y235	4395.5	437
14	Y298	8112.5	437	46	Y266	6224.5	437	78	Y234	4336.5	437
15	Y297	8053.5	437	47	Y265	6165.5	437	79	Y233	4277.5	437
16	Y296	7994.5	437	48	Y264	6106.5	437	80	Y232	4218.5	437
17	Y295	7935.5	437	49	Y263	6047.5	437	81	Y231	4159.5	437
18	Y294	7876.5	437	50	Y262	5988.5	437	82	Y230	4100.5	437
19	Y293	7817.5	437	51	Y261	5929.5	437	83	Y229	4041.5	437
20	Y292	7758.5	437	52	Y260	5870.5	437	84	Y228	3982.5	437
21	Y291	7699.5	437	53	Y259	5811.5	437	85	Y227	3923.5	437
22	Y290	7640.5	437	54	Y258	5752.5	437	86	Y226	3864.5	437
23	Y289	7581.5	437	55	Y257	5693.5	437	87	Y225	3805.5	437
24	Y288	7522.5	437	56	Y256	5634.5	437	88	Y224	3746.5	437
25	Y287	7463.5	437	57	Y255	5575.5	437	89	Y223	3687.5	437
26	Y286	7404.5	437	58	Y254	5516.5	437	90	Y222	3628.5	437
27	Y285	7345.5	437	59	Y253	5457.5	437	91	Y221	3569.5	437
28	Y284	7286.5	437	60	Y252	5398.5	437	92	Y220	3510.5	437
29	Y283	7227.5	437	61	Y251	5339.5	437	93	Y219	3451.5	437
30	Y282	7168.5	437	62	Y250	5280.5	437	94	Y218	3392.5	437
31	Y281	7109.5	437	63	Y249	5221.5	437	95	Y217	3333.5	437
32	Y280	7050.5	437	64	Y248	5162.5	437	96	Y216	3274.5	437

Table 4-3. Bump Center Coordinates (Unit: μm) [cont'd]

Bump No.	Bump Name	Coordinate		Bump No.	Bump Name	Coordinate		Bump No.	Bump Name	Coordinate	
		X-axis	Y-axis			X-axis	Y-axis			X-axis	Y-axis
97	Y215	3215.5	437	129	Y183	1327.5	437	161	Y151	-560.5	437
98	Y214	3156.5	437	130	Y182	1268.5	437	162	Y150	-619.5	437
99	Y213	3097.5	437	131	Y181	1209.5	437	163	Y149	-678.5	437
100	Y212	3038.5	437	132	Y180	1150.5	437	164	Y148	-737.5	437
101	Y211	2979.5	437	133	Y179	1091.5	437	165	Y147	-796.5	437
102	Y210	2920.5	437	134	Y178	1032.5	437	166	Y146	-855.5	437
103	Y209	2861.5	437	135	Y177	973.5	437	167	Y145	-914.5	437
104	Y208	2802.5	437	136	Y176	914.5	437	168	Y144	-973.5	437
105	Y207	2743.5	437	137	Y175	855.5	437	169	Y143	-1032.5	437
106	Y206	2684.5	437	138	Y174	796.5	437	170	Y142	-1091.5	437
107	Y205	2625.5	437	139	Y173	737.5	437	171	Y141	-1150.5	437
108	Y204	2566.5	437	140	Y172	678.5	437	172	Y140	-1209.5	437
109	Y203	2507.5	437	141	Y171	619.5	437	173	Y139	-1268.5	437
110	Y202	2448.5	437	142	Y170	560.5	437	174	Y138	-1327.5	437
111	Y201	2389.5	437	143	Y169	501.5	437	175	Y137	-1386.5	437
112	Y200	2330.5	437	144	Y168	442.5	437	176	Y136	-1445.5	437
113	Y199	2271.5	437	145	Y167	383.5	437	177	Y135	-1504.5	437
114	Y198	2212.5	437	146	Y166	324.5	437	178	Y134	-1563.5	437
115	Y197	2153.5	437	147	Y165	265.5	437	179	Y133	-1622.5	437
116	Y196	2094.5	437	148	Y164	206.5	437	180	Y132	-1681.5	437
117	Y195	2035.5	437	149	Y163	147.5	437	181	Y131	-1740.5	437
118	Y194	1976.5	437	150	Y162	88.5	437	182	Y130	-1799.5	437
119	Y193	1917.5	437	151	Y161	29.5	437	183	Y129	-1858.5	437
120	Y192	1858.5	437	152	Y160	-29.5	437	184	Y128	-1917.5	437
121	Y191	1799.5	437	153	Y159	-88.5	437	185	Y127	-1976.5	437
122	Y190	1740.5	437	154	Y158	-147.5	437	186	Y126	-2035.5	437
123	Y189	1681.5	437	155	Y157	-206.5	437	187	Y125	-2094.5	437
124	Y188	1622.5	437	156	Y156	-265.5	437	188	Y124	-2153.5	437
125	Y187	1563.5	437	157	Y155	-324.5	437	189	Y123	-2212.5	437
126	Y186	1504.5	437	158	Y154	-383.5	437	190	Y122	-2271.5	437
127	Y185	1445.5	437	159	Y153	-442.5	437	191	Y121	-2330.5	437
128	Y184	1386.5	437	160	Y152	-501.5	437	192	Y120	-2389.5	437

Table 4-3. Bump Center Coordinates (Unit: μm) [cont'd]

Bump No.	Bump Name	Coordinate		Bump No.	Bump Name	Coordinate		Bump No.	Bump Name	Coordinate	
		X-axis	Y-axis			X-axis	Y-axis			X-axis	Y-axis
193	Y119	-2448.5	437	225	Y87	-4336.5	437	257	Y55	-6224.5	437
194	Y118	-2507.5	437	226	Y86	-4395.5	437	258	Y54	-6283.5	437
195	Y117	-2566.5	437	227	Y85	-4454.5	437	259	Y53	-6342.5	437
196	Y116	-2625.5	437	228	Y84	-4513.5	437	260	Y52	-6401.5	437
197	Y115	-2684.5	437	229	Y83	-4572.5	437	261	Y51	-6460.5	437
198	Y114	-2743.5	437	230	Y82	-4631.5	437	262	Y50	-6519.5	437
199	Y113	-2802.5	437	231	Y81	-4690.5	437	263	Y49	-6578.5	437
200	Y112	-2861.5	437	232	Y80	-4749.5	437	264	Y48	-6637.5	437
201	Y111	-2920.5	437	233	Y79	-4808.5	437	265	Y47	-6696.5	437
202	Y110	-2979.5	437	234	Y78	-4867.5	437	266	Y46	-6755.5	437
203	Y109	-3038.5	437	235	Y77	-4926.5	437	267	Y45	-6814.5	437
204	Y108	-3097.5	437	236	Y76	-4985.5	437	268	Y44	-6873.5	437
205	Y107	-3156.5	437	237	Y75	-5044.5	437	269	Y43	-6932.5	437
206	Y106	-3215.5	437	238	Y74	-5103.5	437	270	Y42	-6991.5	437
207	Y105	-3274.5	437	239	Y73	-5162.5	437	271	Y41	-7050.5	437
208	Y104	-3333.5	437	240	Y72	-5221.5	437	272	Y40	-7109.5	437
209	Y103	-3392.5	437	241	Y71	-5280.5	437	273	Y39	-7168.5	437
210	Y102	-3451.5	437	242	Y70	-5339.5	437	274	Y38	-7227.5	437
211	Y101	-3510.5	437	243	Y69	-5398.5	437	275	Y37	-7286.5	437
212	Y100	-3569.5	437	244	Y68	-5457.5	437	276	Y36	-7345.5	437
213	Y99	-3628.5	437	245	Y67	-5516.5	437	277	Y35	-7404.5	437
214	Y98	-3687.5	437	246	Y66	-5575.5	437	278	Y34	-7463.5	437
215	Y97	-3746.5	437	247	Y65	-5634.5	437	279	Y33	-7522.5	437
216	Y96	-3805.5	437	248	Y64	-5693.5	437	280	Y32	-7581.5	437
217	Y95	-3864.5	437	249	Y63	-5752.5	437	281	Y31	-7640.5	437
218	Y94	-3923.5	437	250	Y62	-5811.5	437	282	Y30	-7699.5	437
219	Y93	-3982.5	437	251	Y61	-5870.5	437	283	Y29	-7758.5	437
220	Y92	-4041.5	437	252	Y60	-5929.5	437	284	Y28	-7817.5	437
221	Y91	-4100.5	437	253	Y59	-5988.5	437	285	Y27	-7876.5	437
222	Y90	-4159.5	437	254	Y58	-6047.5	437	286	Y26	-7935.5	437
223	Y89	-4218.5	437	255	Y57	-6106.5	437	287	Y25	-7994.5	437
224	Y88	-4277.5	437	256	Y56	-6165.5	437	288	Y24	-8053.5	437

Table 4-3. Bump Center Coordinates (Unit: μm) [cont'd]

Bump No.	Bump Name	Coordinate		Bump No.	Bump Name	Coordinate		Bump No.	Bump Name	Coordinate	
		X-axis	Y-axis			X-axis	Y-axis			X-axis	Y-axis
289	Y23	-8112.5	437	321	V0L	-8050	-442	353	NC	-2800	-442
290	Y22	-8171.5	437	322	NC	-7780	-442	354	DOF_N	-2530	-442
291	Y21	-8230.5	437	323	NC	-7700	-442	355	DOF_N	-2450	-442
292	Y20	-8289.5	437	324	V1L	-7430	-442	356	NC	-2180	-442
293	Y19	-8348.5	437	325	V1L	-7350	-442	357	NC	-2100	-442
294	Y18	-8407.5	437	326	NC	-7120	-442	358	D0	-1830	-442
295	Y17	-8466.5	437	327	VCC	-6890	-442	359	D0	-1750	-442
296	Y16	-8525.5	437	328	VCC	-6810	-442	360	NC	-1480	-442
297	Y15	-8584.5	437	329	VCC	-6730	-442	361	NC	-1400	-442
298	Y14	-8643.5	437	330	VCC	-6650	-442	362	D1	-1130	-442
299	Y13	-8702.5	437	331	NC	-6380	-442	363	D1	-1050	-442
300	Y12	-8761.5	437	332	NC	-6300	-442	364	NC	-780	-442
301	Y11	-8820.5	437	333	MODE	-6030	-442	365	NC	-700	-442
302	NC	-8884.5	442	334	MODE	-5950	-442	366	D2	-430	-442
303	NC	-8980.5	319	335	NC	-5680	-442	367	D2	-350	-442
304	Y10	-8975.5	247.5	336	NC	-5600	-442	368	NC	-80	-442
305	Y9	-8975.5	192.5	337	BS	-5330	-442	369	NC	0	-442
306	Y8	-8975.5	137.5	338	BS	-5250	-442	370	D3	270	-442
307	Y7	-8975.5	82.5	339	NC	-5020	-442	371	D3	350	-442
308	Y6	-8975.5	27.5	340	GND	-4790	-442	372	NC	620	-442
309	Y5	-8975.5	-27.5	341	GND	-4710	-442	373	NC	700	-442
310	Y4	-8975.5	-82.5	342	GND	-4630	-442	374	D4	970	-442
311	Y3	-8975.5	-137.5	343	GND	-4550	-442	375	D4	1050	-442
312	Y2	-8975.5	-192.5	344	NC	-4280	-442	376	NC	1320	-442
313	Y1	-8975.5	-247.5	345	NC	-4200	-442	377	NC	1400	-442
314	NC	-8980.5	-319	346	SHL	-3930	-442	378	D5	1670	-442
315	NC	-8884.5	-442	347	SHL	-3850	-442	379	D5	1750	-442
316	VML	-8750	-442	348	NC	-3580	-442	380	NC	2020	-442
317	VML	-8670	-442	349	NC	-3500	-442	381	NC	2100	-442
318	NC	-8440	-442	350	EIO1_N	-3230	-442	382	D6	2370	-442
319	V0L	-8210	-442	351	EIO1_N	-3150	-442	383	D6	2450	-442
320	V0L	-8130	-442	352	NC	-2880	-442	384	NC	2720	-442

Table 4-3. Bump Center Coordinates (Unit: μm) [cont'd]

Bump No.	Bump Name	Coordinate		Bump No.	Bump Name	Coordinate		Bump No.	Bump Name	Coordinate	
		X-axis	Y-axis			X-axis	Y-axis			X-axis	Y-axis
385	NC	2800	-442	402	EIO2_N	5870	-442	419	VMR	8670	-442
386	D7	3070	-442	403	EIO2_N	5950	-442	420	VMR	8750	-442
387	D7	3150	-442	404	NC	6180	-442	421	NC	8884.5	-442
388	NC	3420	-442	405	GND	6410	-442	422	NC	8980.5	-319
389	NC	3500	-442	406	GND	6490	-442	423	Y320	8975.5	-247.5
390	CL2	3770	-442	407	GND	6570	-442	424	Y319	8975.5	-192.5
391	CL2	3850	-442	408	GND	6650	-442	425	Y318	8975.5	-137.5
392	NC	4120	-442	409	NC	6920	-442	426	Y317	8975.5	-82.5
393	NC	4200	-442	410	NC	7000	-442	427	Y316	8975.5	-27.5
394	CL1	4470	-442	411	V1R	7270	-442	428	Y315	8975.5	27.5
395	CL1	4550	-442	412	V1R	7350	-442	429	Y314	8975.5	82.5
396	NC	4820	-442	413	NC	7620	-442	430	Y313	8975.5	137.5
397	NC	4900	-442	414	NC	7700	-442	431	Y312	8975.5	192.5
398	M	5170	-442	415	V0R	7970	-442	432	Y311	8975.5	247.5
399	M	5250	-442	416	V0R	8050	-442	433	NC	8980.5	319
400	NC	5520	-442	417	V0R	8130	-442				
401	NC	5600	-442	418	NC	8400	-442				

5. Pin Descriptions

Table 5–1. Pin Descriptions of Power Supply Signals

Symbol	Pin(s) No.	Attribute	Description
VCC **GND**	**343** **324, 340**	Power Supply	***VCCGND: Logic Power Supply.***
V0L, V0R **VML, VMR** **V1L, V1R**	**345, 322** **346, 321** **344, 323**	Input	***LCD Drive-level Voltage.*** See Figure 5-1.

Table 5–2. Pin Descriptions of Control Signals

Symbol	Pin(s) No.	Attribute	Description
CL1	**327**	Input	***Data Latch Clock.*** The LCD drive signal corresponding to the display data is output at the falling edge of this signal.
CL2	**328**	Input	***Display Data Capture Clock.*** Display data is latched at the falling edge of this signal.
M	**326**	Input	***AC Signal Input.*** Used to change the LCD drive outputs to AC.
D0-D7	**336-329**	Input	***Display Data.*** When the display data is 1 (VCC level), the LCD drive output level is the selection level and the liquid-crystal display is on. When the display data is 0 (GND level), they are non-selection level and off respectively.
SHL	**339**	Input	***Shift Left Signal.*** A control signal to switch the data output destination. See the section on switching the data output destination
EIO1_N **EIO2_N**	**338** **325**	Input/output	***Enable Input/Output for Chip Selection.*** If SHL is at the GND level, EIO1_N inputs the chip enable signal and EIO2_N outputs the chip enable signal; and if it is at the VCC level, the opposite occurs. Enable input: The chip enable-input pin of the first IT must be fixed to the GND level, and the other chip-enable input pins must be connected to the chip enable-output pins of the previous IT7012C/H. Enable output: The chip enable-output pin must be connected to the chip enable-input pin of the next IT.
DOF_N	**337**	Input	***Display Off.*** A low DOF_N level sets LCD drive outputs Y1 to Y320 to the VM level.
BS	**341**	Input	***Data Bus Selection.*** Used to switch the number of input bits for the display data. BS=VCC: 8-bit input mode BS=GND: 4-bit input mode (Captures data from D0~D3. At this time, connect D4~D7 to GND.
MODE	**342**	Input	***Mode Selection.*** Switch the number of output bits for the display data. MODE=VCC: 320 output mode MODE=GND: 240 output mode (Y41~Y280 are valid output. The other 80 pins output the VM level.)
Y1-Y320	**1-320**	Output	***LCD Drive Output.*** Either level V0 or V1 is output according to the combination of the M signal and display data when the DOF_N pin is set at VCC. See Figure 5-2.

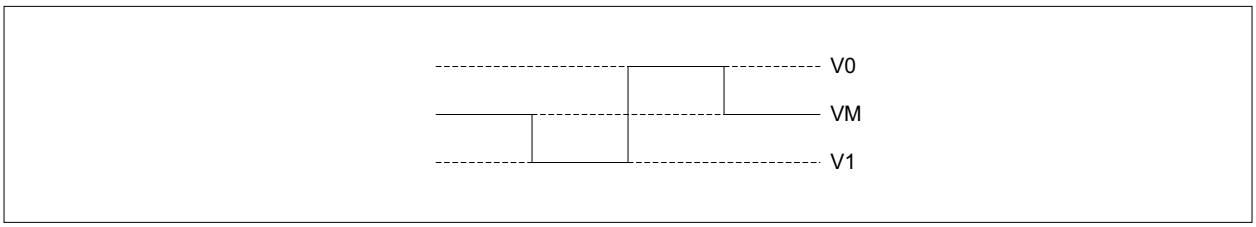


Figure 5-1. LCD Drive Level Voltage

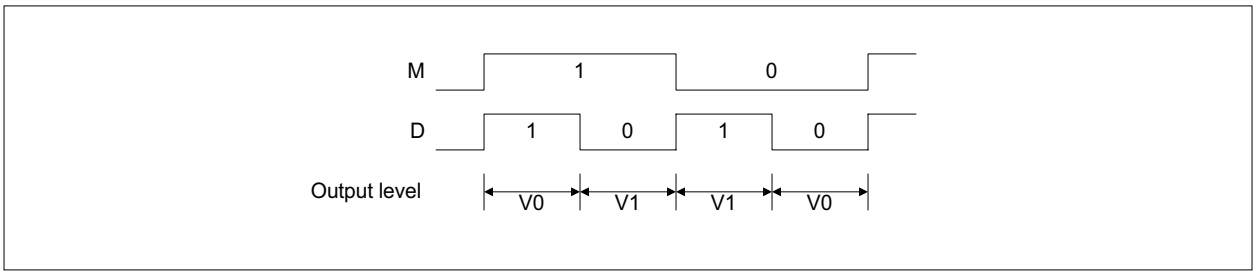


Figure 5-2. Selection of LCD Drive Output Level

6. System Configuration

6.1 Overview

The IT is composed of 7 main elements to work properly: LCD Drive Circuit, Level Shifter, Latch Circuit (2), Latch Circuit (1), Shift Register, Data Shifter and Arithmetic Circuit, and Timing Generator Circuit. The functional descriptions for each of the 7 elements are described below:

6.1.1 LCD Drive Circuit

The LCD drive circuit, which consists of 320 bits, is responsible for generating three voltage levels V0, V1, and VM, which drive the LCD panel. One of these three levels is output to the corresponding Y pin, depending on the data in latch circuit (2) and the DOF_N and M signals.

6.1.2 Level Shifter

The level shifter is used to convert logic signals to LCD voltage signal outputs.

6.1.3 Latch Circuit (2)

The latch circuit (2), which consists of 320 bits, is used to latch the data input from latch circuit (1), and output the latched data to the level shifter and the LCD drive circuit at the falling edge of each clock 1 (CL1) pulse.

6.1.4 Latch Circuit (1)

The latch circuit (1) is used to latch the 4/8-bit parallel data input via the D0 to D7 pins according to the timing generated by the 80-bit shift register, and output the 320-bit latched data to latch circuit (2).

6.1.5 Shift Register

The shift register, which consists of 80 bits, is responsible for the generation and the output of the data latch signals for latch circuit (1) at the falling edge of each clock 2 (CL2) pulse.

6.1.6 Data Shifter and Arithmetic Circuit

The data shifter shifts the destinations of data output when the condition requires. The arithmetic circuit performs operations for the data and AC signal M.

6.1.7 Timing Generator Circuit

The timing generator circuit is responsible for generating the data latch pulses for latch circuit (2), and changing pulse the LCD drive outputs to AC.

6.2 Switching the Data Output Destination

As illustrated in the figure below, the destination of the output data latched by the SHL signal is switched left or right. At this time, the input and output of the enable signal pins can also be switched.

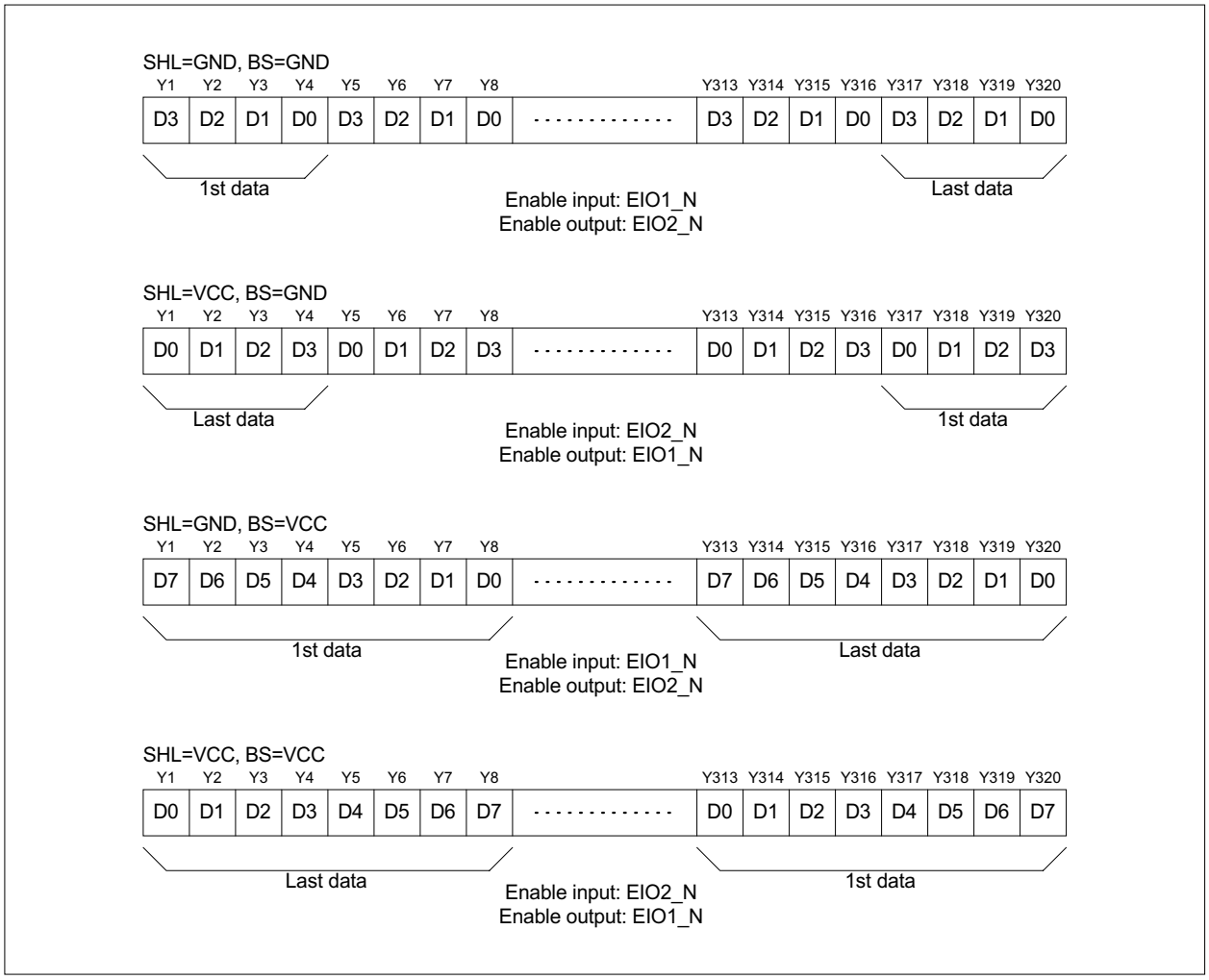


Figure 6-1. Data Output Destination

6.3 Operation Timing

6.3.1 4-bit capture mode (1 line, 640 dots, BS=GND)

Figure 6-2 below illustrates the 4-bit data-latch timing when the EIO1_N pin is a chip-enable input and the EIO2_N pin is a chip-enable output (SHL=GND). When SHL = Vcc, the EIO1_N pin is a chip-enable output, and the EIO2_N pin is a chip-enable input.

The IT is first released from the data-standby state when a low chip-enable signal is input via the EIO1_N pin. Shortly after, the IT7012C/H will be released completely from the standby state and starts to latch data when the IT7012C/H is latched at the falling edge of the CL2 pulse that follows.

The device latches the 4 bits of at the falling edge of each CL2 pulse. When it has latched 316 bits of data, it sets the EIO2_N signal to low. When it has latched 320 bits of data, it stops automatically and enters the standby state to initiate the next IT7012C/H under the condition that pin EIO2_N is connected to pin EIO1_N of the next IT7012C/H.

The IT7012C/H outputs one line of data from the Y1 to Y320 pins at the falling edge of each CL1 pulse. Data d1 is output from Y1, and d320 from Y320 when SHL = GND, and d1 is output from Y320, and d320 from Y1 when SHL = Vcc.

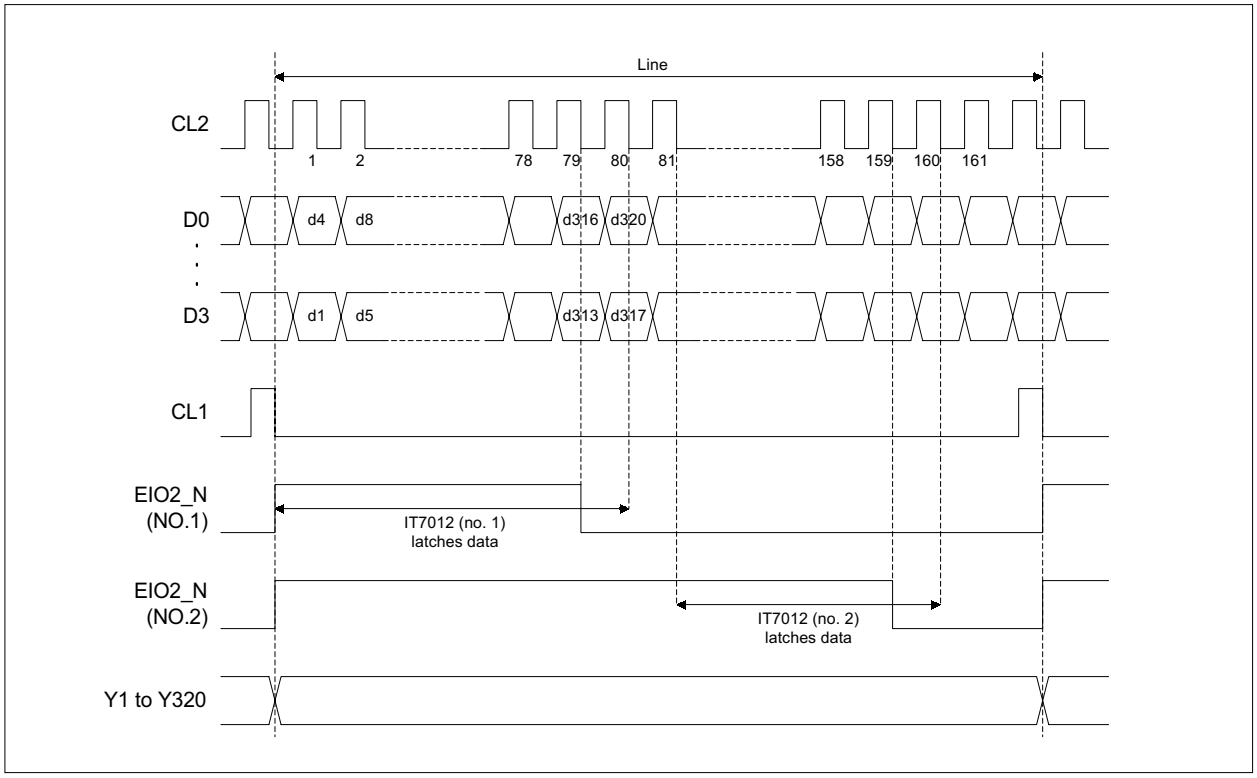


Figure 6-2. Data Latch Timing (1)

6.3.2 8-bit capture mode (1 line, 640 dots, BS=VCC)

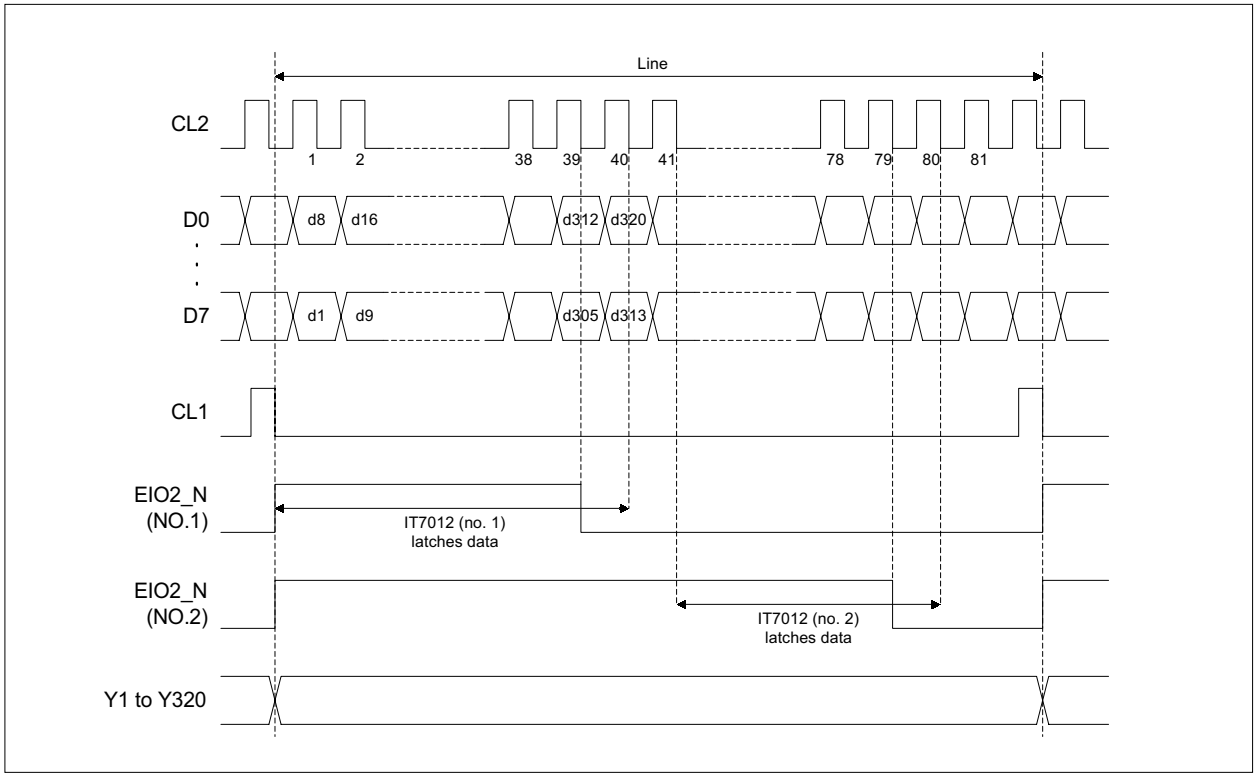


Figure 6-3. Data Latch Timing (2)

7. DC Electrical Characteristics

Absolute Maximum Ratings

Power Supply (Vcc) ..... -0.3 to +7.0V
Power Supply (V0)..... -0.3 to +7.0V
Input Voltage (1) (VT1) ..... -0.3 to Vcc +0.3
Input Voltage (2) (VT2) ..... -0.3 to V0 +0.3
Operating temperature (Topr)..... -30 to +75°C
Storage temperature (Tstg) ..... - 55 + 110°C

***Comments:**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

7.1 Absolute Maximum Ratings

Parameter		Symbol	Ratings	Unit	Applicable Pins	Notes
Power supply voltage	Logic circuit	Vcc	–0.3 to +7.0	V		1 and 2
	LCD drive circuit	V0	–0.3 to +7.0	V		1 and 2
Input voltage (1)		VT1	–0.3 to Vcc +0.3	V	CL1, CL2, SHL, EIO1_N, EIO2_N, DOF_N, D0-D7, M, BS, MODE	
Input voltage (2)		VT2	–0.3 to V0 +0.3	V	VML, VMR, V1L, V1R	1 and 2
Operating temperature		Topr	–30 to +75	°C		
Storage temperature		Tstg	–55 to +110	°C		

Notes: 1. For voltage VCC, V0, VT1 and VT2, the reference point is GND (0V).
2. See section 7.2.

7.2 Power On and Power Off Sequence

Make sure to follow the sequence of power on and power off for power supplies and signals as illustrated in Figure 7-1. It is recommended that users must follow the sequence correctly; otherwise, the undesired occurrences of device malfunction, permanent damage or results may take place.

7.2.1 Power On Sequence

1) Power on the device in the order listed below:
GND-Vcc, GND-V0, and VM/V1. Then, input GND power to the DOF_N pin.
2) The LCD forces to output the VM level through the function of display off.
3) The display off function has a higher priority even if an input signal distortion occurs instantly after the Vcc input.
4) Next, input the specific signal to get the registers in the driver initialized. In this case, make sure a period that lasts more than one frame is reserved.
5) The preceding work for the normal display is completed here. At this point, users should shut off the display off function by setting the DOF_N pin to Vcc level. At this time, the voltage level of pins V0, VM, and V1 must rise to the specific potential.

7.2.2 Power Off Sequence

The procedure is basically the opposite of that used to turn on the power.

1) Firstly, the DOF_N pin should be set to GND.
2) Secondly, the LCD power supply must be shut off in the order of VM/V1 and GND-V0.
3) Lastly, ground VCC and an input signal.
   At this moment, the inputs of pins V0, VM, and V1 must go down to 0V completely. In addition, an incorrect display may occur at power off or power on. This is because the display off function is invalidated when Vcc falls to 0V, and the LCD may output a voltage level other than VM.

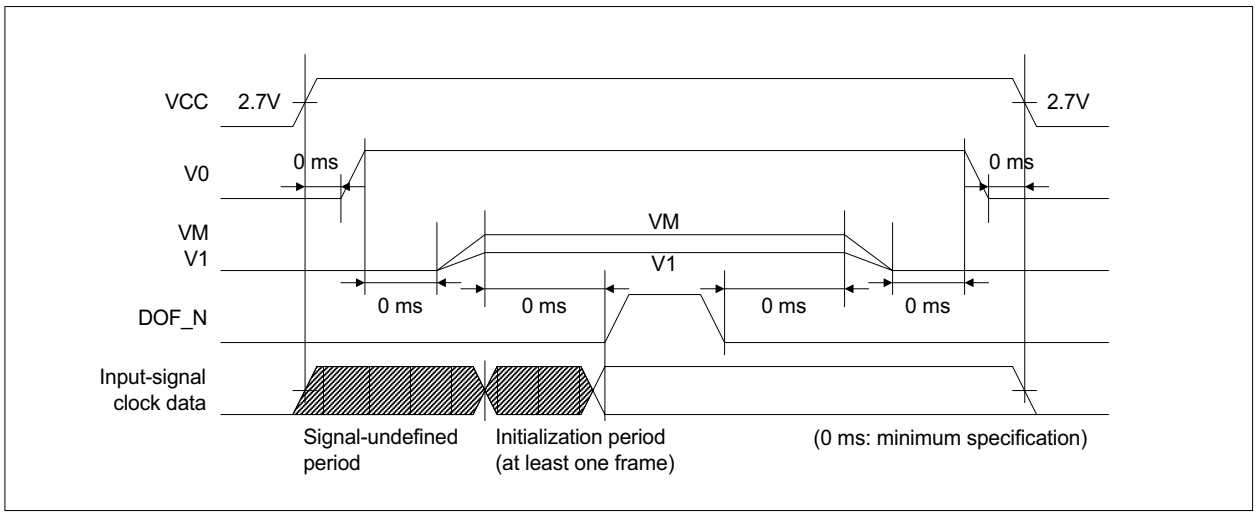


Figure 7-1. IT7012C/H Power On/Off Scenario

7.3 DC Characteristics 1 (VCC = 2.5 to 4.5V, V0 – GND = 2.6 to 5.5V, and Ta = –30 to +75°C)

Table 7–1. DC Characteristics (3V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
VIH	Input high-level voltage	—	0.8 × VCC	—	VCC	V	CL1, CL2, SHL, M, EIO1_N, EIO2_N, MODE, DOF_N, D0 to D7, BS
VIL	Input low-level voltage		0	—	0.2 × VCC	V	
VOH	Output high-level voltage	IOH = –0.4mA	VCC – 0.4	—	—	V	EIO1_N and EIO2_N
VOL	Output low-level voltage	IOL = 0.4mA	—	—	0.4	V	
RON	Vi – Xj ON resistance *1	ION = 150μA	—	0.7	2.0	kΩ	Y1 to Y320, V0L, and V0R
			—	2.0	3.0	kΩ	Y1 to Y320, VML, and VMR
			—	0.7	2.0	kΩ	Y1 to Y320, V1L, and V1R
IIL1	Input leakage current (1)	VIN = VCC – GND	–5.0	—	5.0	μA	CL1, CL2, SHL, M, EIO1_N, EIO2_N, MODE, DOF_N, D0 to D7, BS
IIL2	Input leakage current (2)	VIN = V0 – GND	–25	—	25	μA	VML, VMR, V1L, and V1R
ICC	Current consumption (1) *2	VCC = 3.3V V0 = 2.7V fCL2 = 3.5MHz fCL1 = 19.2kHz fM = 1.5kHz	—	150	300	μA	VCC
IV0	Current consumption (2) *2		—	60	200	μA	V0L and V0R
IST	Current consumption (3) *2, *3		—	50	100	μA	VCC

7.4 DC Characteristics 2 (VCC = 4.5 to 5.5V, V0 – GND = 2.6 to 5.5V, and Ta = –30 to +75°C)

Table 7–2. DC Characteristics (5V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Applicable Pins
VIH	Input high-level voltage	—	0.8 × VCC	—	VCC	V	CL1, CL2, SHL, M, EIO1_N, EIO2_N, MODE, DOF_N, D0 to D7, BS
VIL	Input low-level voltage		0	—	0.2 × VCC	V	
VOH	Output high-level voltage	IOH = –0.4mA	VCC – 0.4	—	—	V	EIO1_N and EIO2_N
VOL	Output low-level voltage	IOL = 0.4mA	—	—	0.4	V	
RON	Vi–Xj ON resistance *1	ION = 150µA	—	0.7	2.0	kΩ	Y1 to Y320, V0L, and V0R
			—	2.0	3.0	kΩ	Y1 to Y320, VML, and VMR
			—	0.7	2.0	kΩ	Y1 to Y320, V1L, and V1R
IIL1	Input leakage current (1)	VIN = VCC – GND	–5.0	—	5.0	µA	CL1, CL2, SHL, M, EIO1_N, EIO2_N, MODE, DOF_N, D0 to D7, BS
IIL2	Input leakage current (2)	VIN = V0 – GND	–25	—	25	µA	VML, VMR, V1L, and V1R
ICC	Current consumption (1) *2	VCC = 5.0V V0 = 2.7V fCL2 = 3.5 MHz fCL1 = 19.2 kHz fM = 1.5 kHz	—	230	450	µA	VCC
IV0	Current consumption (2) *2		—	60	200	µA	V0L and V0R
IST	Current consumption (3) *2, *3		—	80	150	µA	Vcc

Notes: 1. Indicates the resistance between one of the pins Y1 to Y320 and one of the voltage supply pins, when load current is applied to the Y pin; defined under the following conditions:
V0–GND = 5.5V
VM = (V0 + V1)/2
V1 = GND + 1
V1 should be near the GND level, and the VM should be near the middle voltage between V1 and V0. V1 should be within the range of ΔV = 0.25V0, which is the range within which RON, the LCD drive circuit's output impedance, is stable. See Figure 7-2.

2. Input and output currents are excluded. When CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, VIH and VIL must be used at VCC and GND, respectively.
3. Standby current.
4. The voltage of each signal is illustrated in Figure 7-3 and Figure 7-4.

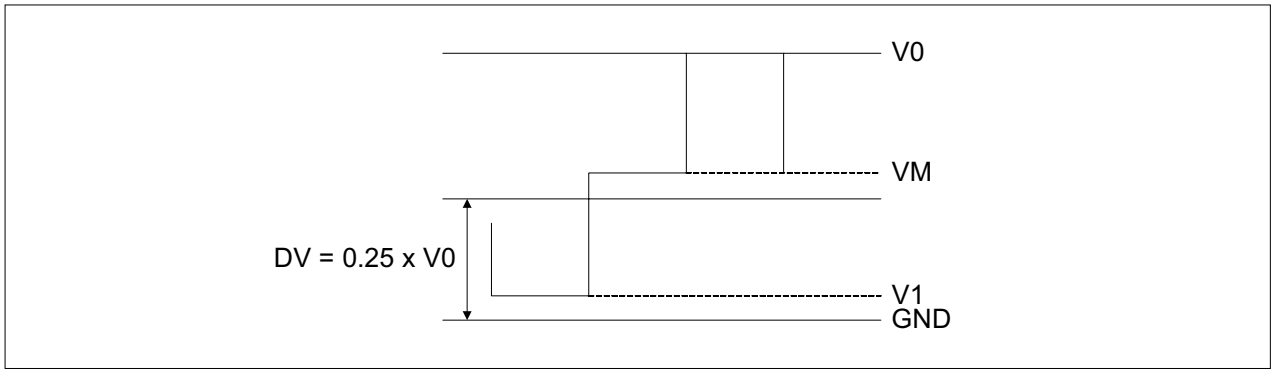


Figure 7-2. Relationship Between Driver-Output Waveforms and Each Level Voltage

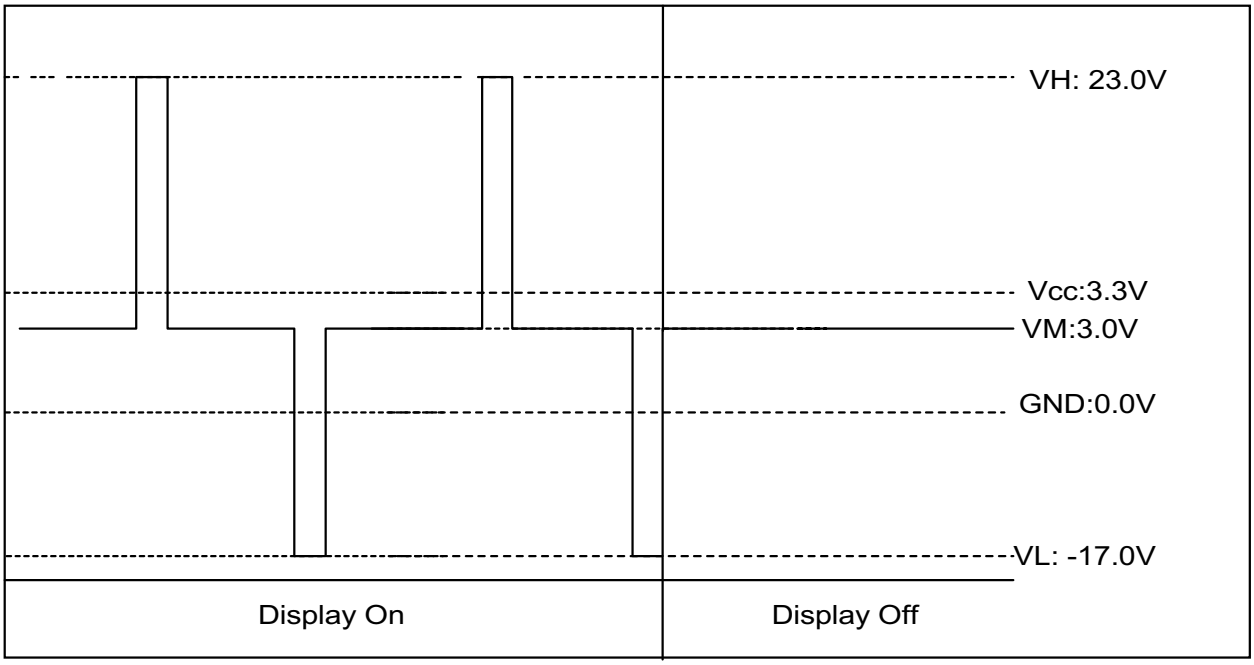


Figure 7-3. LCD Common Drive Output Waveform & Voltage Level

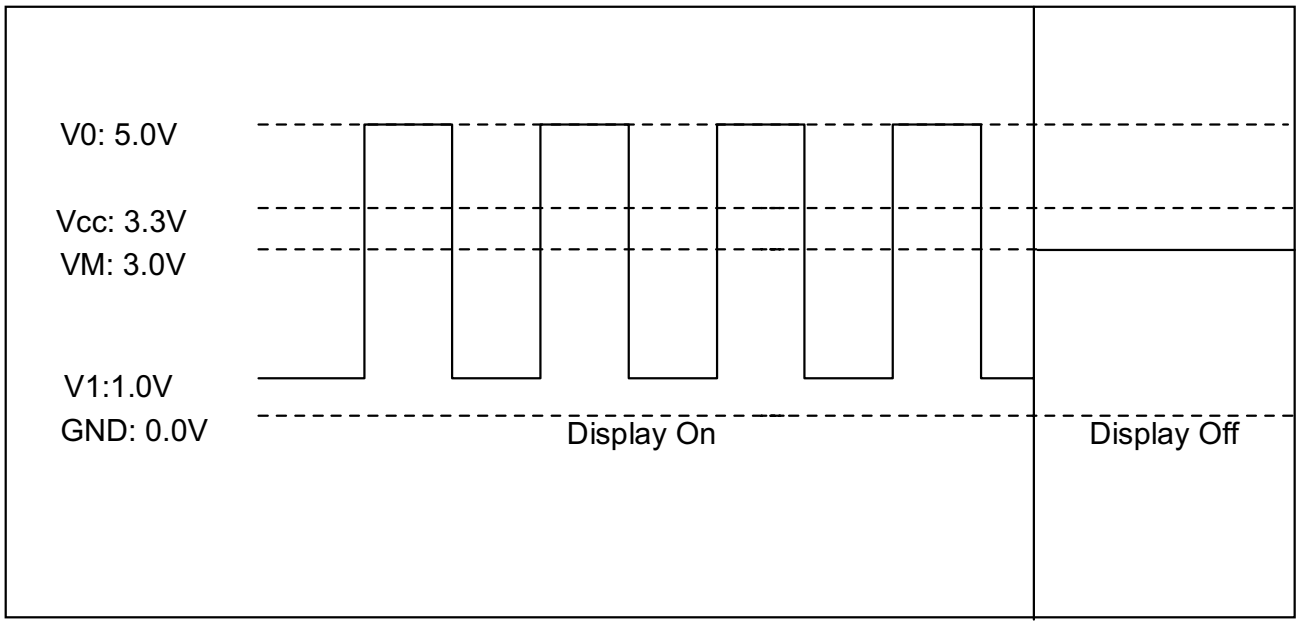


Figure 7-4. LCD Segment Drive Output Waveform & Voltage Level

8. AC Characteristics

8.1 AC Characteristics 1 (VCC = 2.5 to 4.5V, V0 – GND = 2.6 to 5.5V, and Ta = –30 to +75°C)*1

Table 8–1. AC Characteristics (3V)

Symbol	Parameter	Applicable Pin(s)	Min.	Max.	Unit
t_{CYC}	Clock cycle time	CL2	152	—	ns
t_{CWH2}	Clock high-level width (1)	CL2	65	—	ns
t_{CWL2}	Clock low-level width (1)	CL2	65	—	ns
t_{CWH1}	Clock high-level width (2)	CL1	65	—	ns
t_{SCL}	Clock setup time	CL1 and CL2	80	—	ns
t_{HCL}	Clock hold time	CL1 and CL2	80	—	ns
t_r	Clock rise time	CL1 and CL2	—	30	ns
t_f	Clock fall time	CL1 and CL2	—	30	ns
t_{DS}	Data setup time	D0 to D7, and CL2	50	—	ns
t_{DH}	Data hold time	D0 to D7, and CL2	50	—	ns
t_{MS}	M setup time	M and CL1	20	—	ns
t_{MH}	M hold time	M and CL1	20	—	ns
t_{pd1}	Output delay time (1)	CL1, and Y1 to Y320	—	1000	ns

Note 1: The load must be less than 10pF between the EIO2_N and EIO1_N connections of the IT7012C/H.

8.2 AC Characteristics 2 (VCC = 4.5 to 5.5V, V0 – GND = 2.6 to 5.5V, and Ta = –30 to +75°C)*1

Table 8–2. AC Characteristics (5V)

Symbol	Parameter	Applicable Pin(s)	Min.	Max.	Unit
t_{CYC}	Clock cycle time	CL2	125	—	ns
t_{CWH2}	Clock high-level width (1)	CL2	45	—	ns
t_{CWL2}	Clock low-level width (1)	CL2	45	—	ns
t_{CWH1}	Clock high-level width (2)	CL1	45	—	ns
t_{SCL}	Clock setup time	CL1 and CL2	80	—	ns
t_{HCL}	Clock hold time	CL1 and CL2	80	—	ns
t_r	Clock rise time	CL1 and CL2	—	20	ns
t_f	Clock fall time	CL1 and CL2	—	20	ns
t_{DS}	Data setup time	D0 to D7, and CL2	20	—	ns
t_{DH}	Data hold time	D0 to D7, and CL2	20	—	ns
t_{MS}	M setup time	M and CL1	20	—	ns
t_{MH}	M hold time	M and CL1	20	—	ns
t_{pd1}	Output delay time (1)	CL1, and Y1 to Y320	—	1000	ns

Notes: 1. The load must be less than 10pF between the EIO2_N and EIO1_N connections of the IT7012C/H.

2. For output delay time (1), connect the load circuit as shown in Figure 8-1.

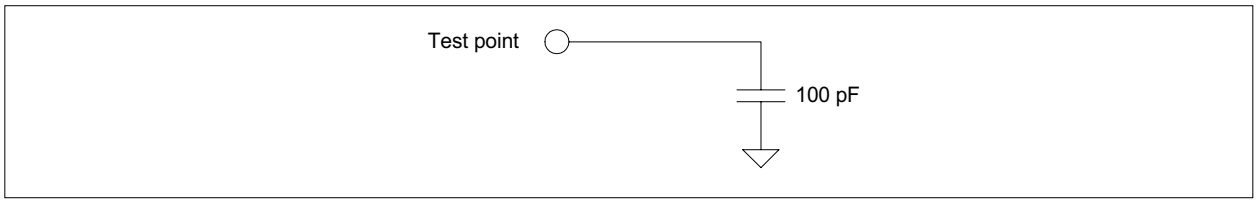


Figure 8-1. Load Circuit for Output Delay Time (1)

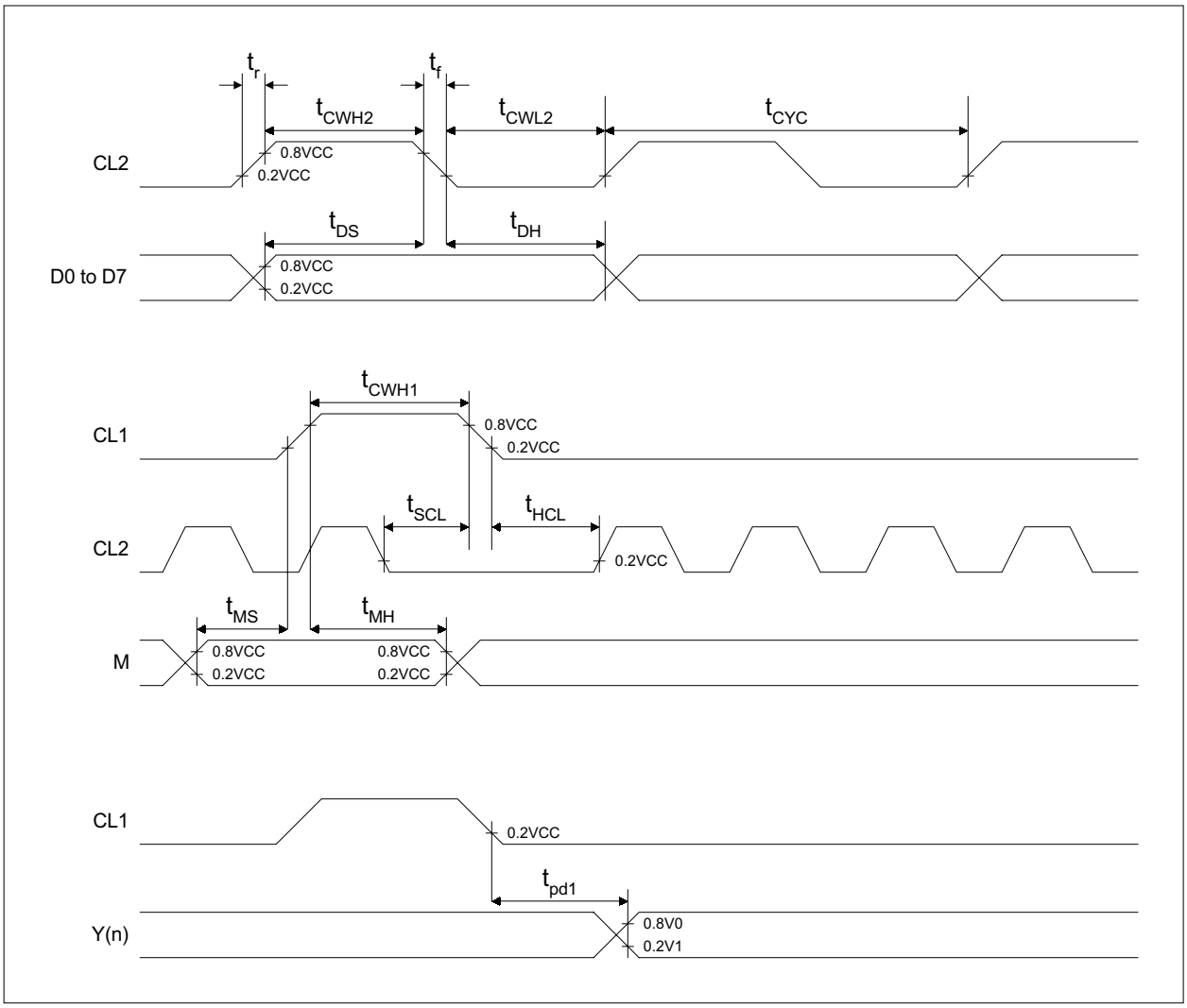
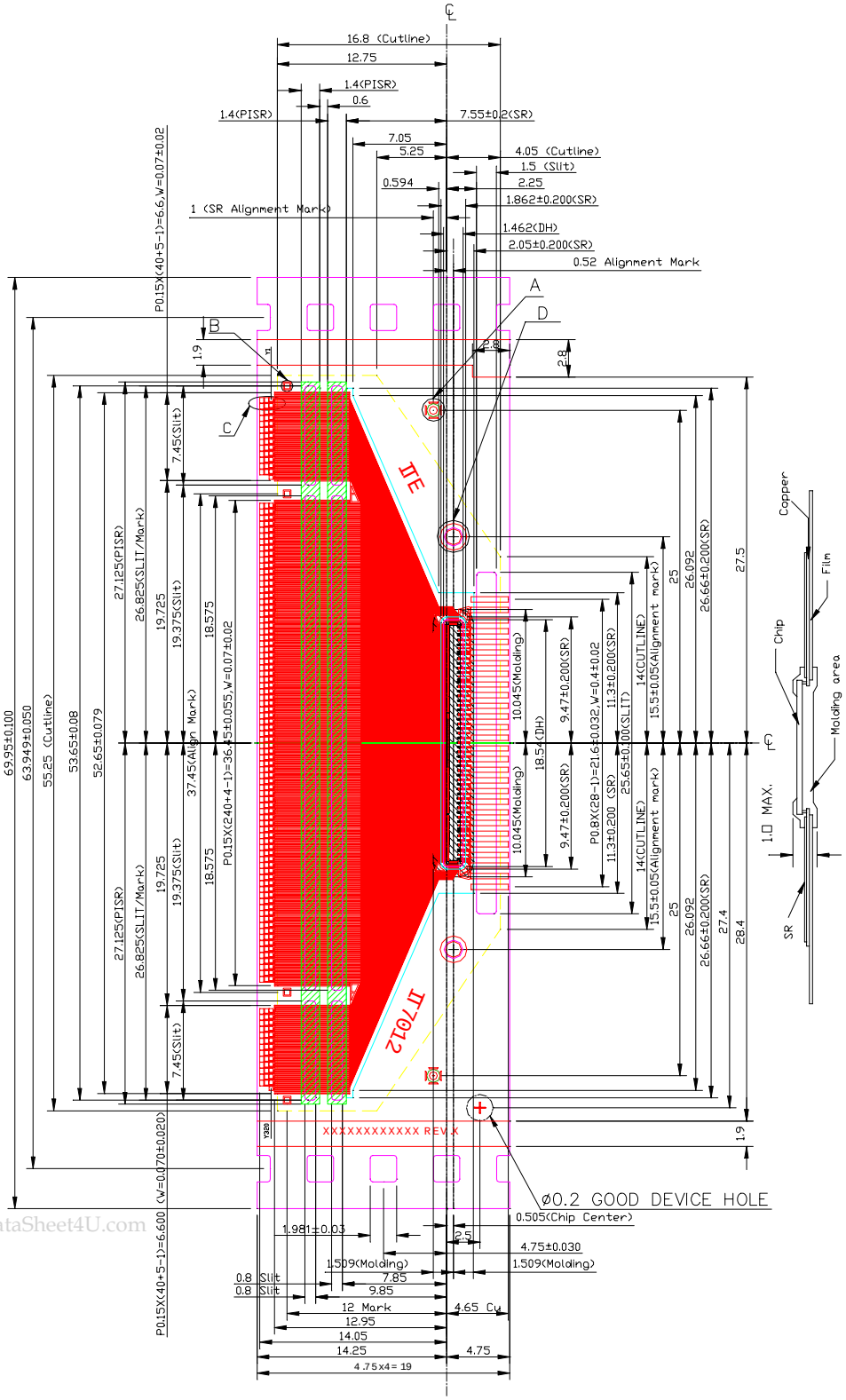


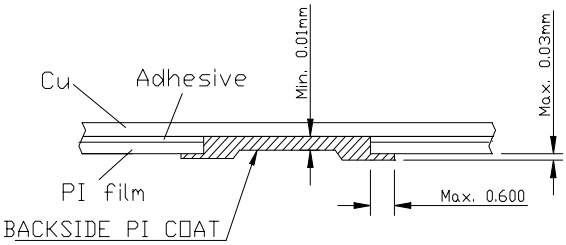
Figure 8-2. AC Characteristics

9. Package Information

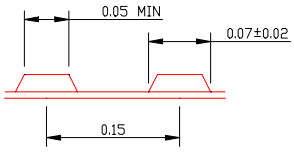


INPUT LEAD NAME

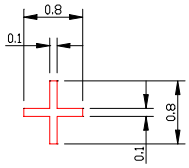
NC
VML
V0L
V1L
VCC
MODE
BS
GND
SHL
EIO1_N
DOF_N
D0
D1
D2
D3
D4
D5
D6
D7
CL2
CL1
M
EIO2_N
GND
V1R
V0R
VMR
NC



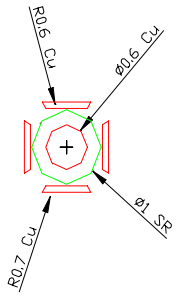
Detail of flex



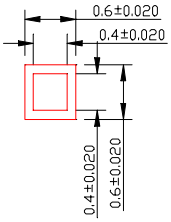
CROSS SECTION OF OUTPUT LEADs



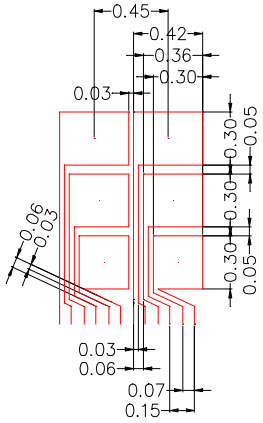
GOOD DEVICE HOLE



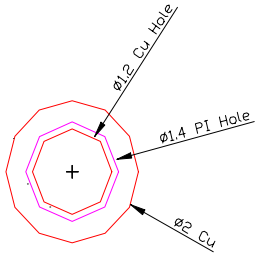
DEATIL :A



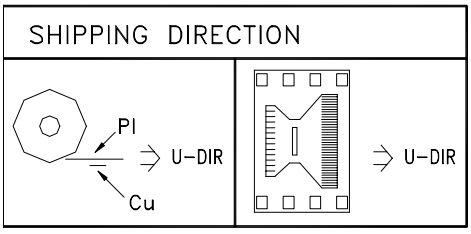
DEATIL :B



DETAIL : C
(Output Side TEST PADS)



DEATIL :D



NOTE:

1. Film: UPILEX-S 75±6um thickness
   Copper: FQ-VLP 18um thickness
   Adhesive: Toray #7100 12±3um thickness
   Solder resist: AE-70-M11 26±14um thickness
   Flex Coating: FS-100L Min. 10um
2. Plating: Sn thickness : 0.21±0.05 um
   unless otherwise noted
3. All corner radii of Base Film are less than 0.2mm
4. Other specs than displayed in this drawing are based on the standard spec lists
5. All dimensional tolerances of "SR" are ±0.3mm unless otherwise noted
6. All dimensional tolerances of "base film" are ±0.05mm unless otherwise noted
7. Reel Size: ø405 mm.

10. Ordering Information

Part No.	Package
IT7012C	346-TCP
IT7012H	CHIP FORM (433 bumps)