

Description

The iT3011E is a RoHS-6-compliant limiting amplifier for use as a post amplifier in OC-192 and STM-64 optical receivers. Signals as small as +/-7 mVpp differential can be amplified to 1.28 Vpp differential. Offset correction and output voltage control are provided. Both AC and DC coupling are allowed at the input and output. The high sensitivity allows the device to be used at the output of a transimpedance amplifier.

Features

- 3-dB bandwidth: 10 GHz
- Differential gain: 42 dB
- Saturated output: 640 mVpp on each output into 50 ohms
- Input sensitivity 2.5 mVpp at BER<1E-12
- Single bias supply: -5.2 V
- Power consumption: Less than 572 mW
- Bias current: 95 mA
- DC offset correction
- Amplitude voltage control
- Low RMS jitter degradation
- RoHS-6-compliant 4x4 mm QFN (MO-220) package



Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
Vee1, 2	Power supply voltage	-8	0	V
Vd	Applied voltage at data input (differential)		3	V
Vm	Applied voltage at data input (single ended)		1.5	V
Ioffset(+),(-)	Offset control current		5	mA
Tch	Maximum channel temperature		150	°C
Tstg	Storage temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Tc	Operating temperature range (Tcase)	0		85	°C
Vee1	Power supply voltage	-5.45	-5.2	-4.95	V
Vee2	Power supply voltage	-5.45	-5.2	-4.95	V
Iee1+Iee2	Total bias supply current	80	95	110	mA
Voffset (+)	Offset control voltage	-5		5	V
Voffset (-)	Offset control voltage	-5		5	V
Vctrl	Amplitude voltage control	-5.2		0	V
Vd	Applied peak to peak voltage at data input (differential)	7		1000	mV
Vm	Applied peak to peak voltage at data input (single ended)	14		1000	mV
	Input/output interface	AC and DC coupled			
Vindc	DC input voltage (with DC-coupled input)	-0.5		0.5	V



Electrical Characteristics

At ambient Temperature
Vee1,2 = -5.2 V

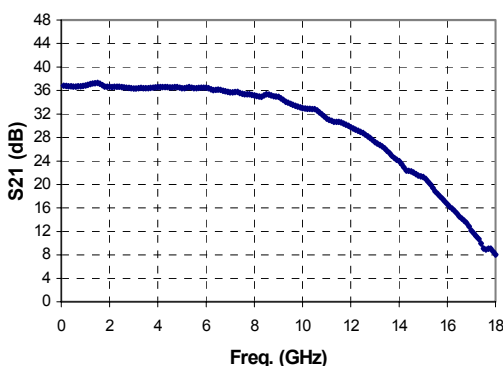
Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
P	Power consumption	416	494	572	mW
G	Differential small signal gain	41	42		dB
B3dB	3 dB bandwidth	9	10		GHz
RLin	Input return loss (up to 10 GHz)	12	20		dB
RLout	Output return loss (up to 10 GHz)	10	15		dB
Vin	Input sensitivity differential input (BER <1E-12, 2 ²³ -1PRBS, 12.5 Gb/s)	+/-2.5			mVpp
Vout	Output peak to peak voltage (either Q or /Q) (Vctrl = 0 V for max. output voltage)	550	640		mVpp
ΔVout	Vout sensitivity vs. bias (Vee = -5.2 V +/-5%)			+/-11	%
Voutdc	load	-450	-350	-250	mV
Trse	Rise time (20% - 80%)		21	27	ps
Tfse	Fall time (20% - 80%)		17	23	ps
Jrms*	Jitter RMS Degradation Jrms*=(Jmeas^2-Jthru^2)^.5		1	1.5	ps

S-Parameter Data

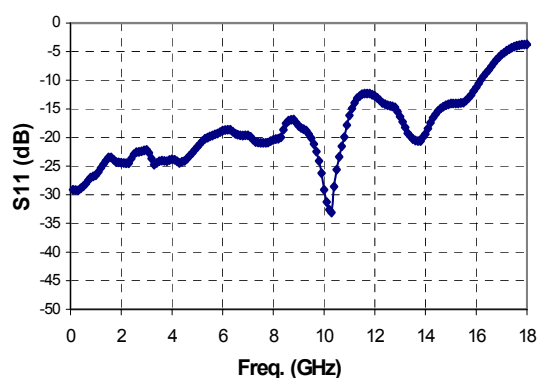
(Measured on connectorized evaluation board)

Vee1 = Vee2 = -5.2 V
Iee1+Iee2 = 95 mA

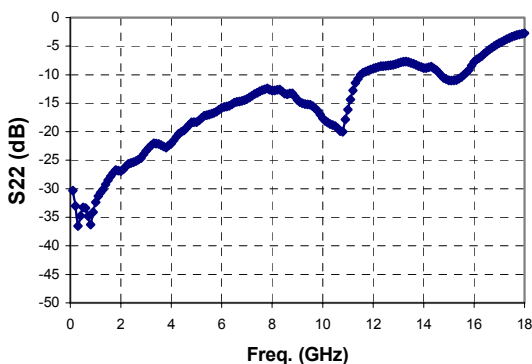
iT3011 Single Ended Gain



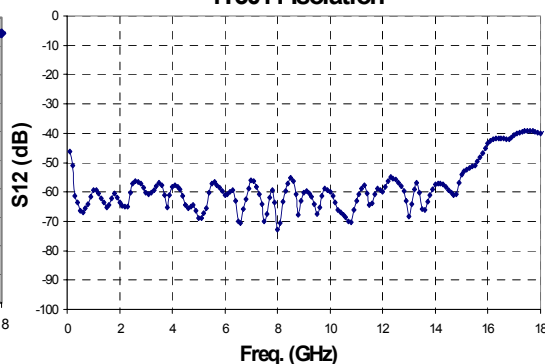
iT3011 Input Return Loss



iT3011 Output Return Loss

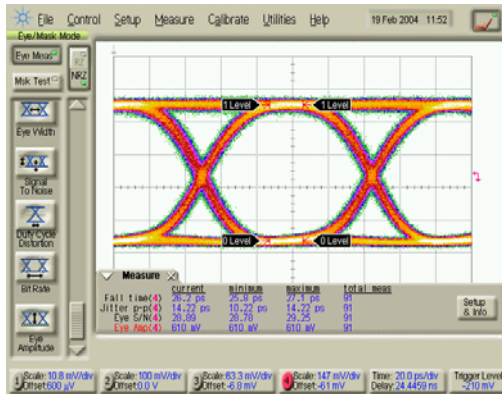


iT3011 Isolation

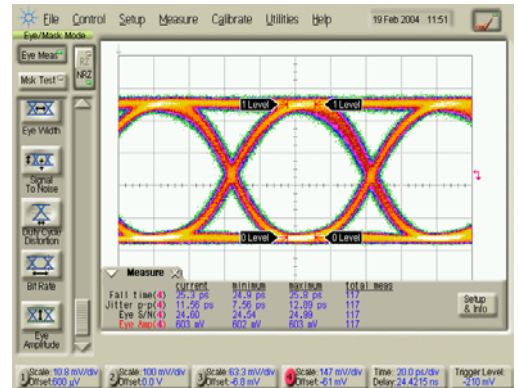


Eye Diagram Performance

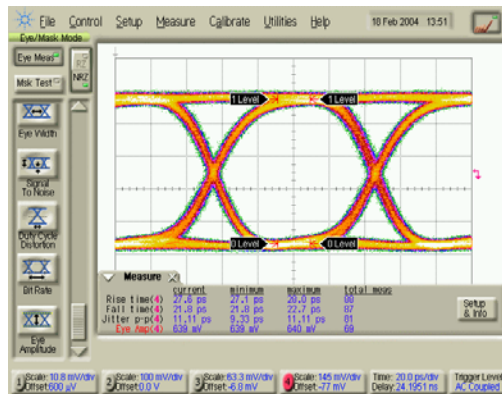
Vee1= Vee2 = -5.2 V
Iee1+Iee2 = 95 mA



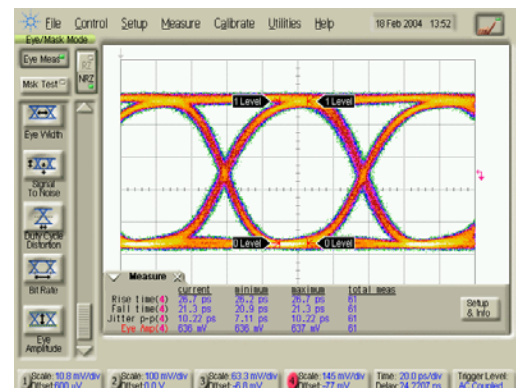
Bit rate: 10.7 Gb/s
Vin = +/-6 mVpp, Vout = +/-610 mVpp



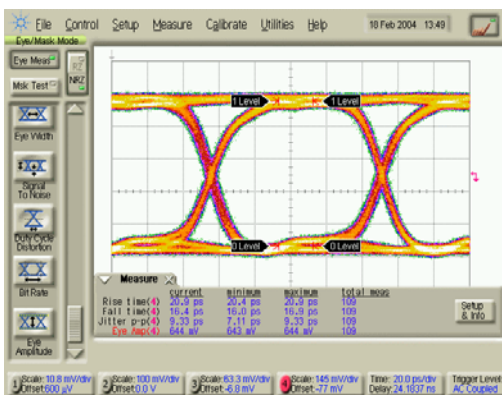
Bit rate: 12.5 Gb/s
Vin = +/-6 mVpp, Vout = +/-603 mVpp



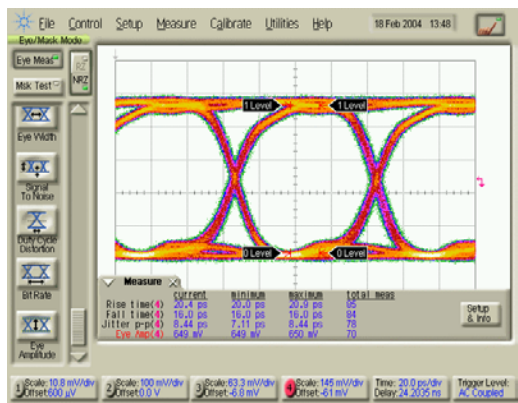
Bit rate: 10.7 Gb/s
Vin = +/-8 mVpp, Vout = +/-640 mVpp



Bit rate: 12.5 Gb/s
Vin = +/-8 mVpp, Vout = +/-638 mVpp



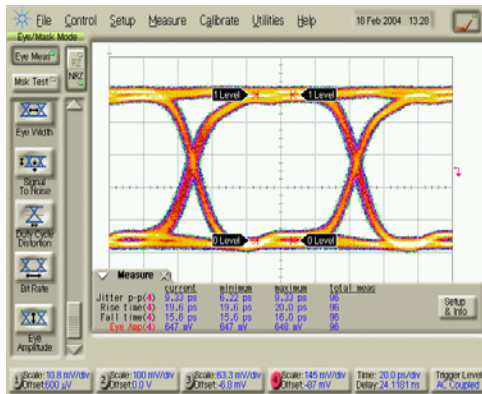
Bit rate: 10.7 Gb/s
Vin = +/-200 mVpp, Vout = +/-644 mVpp



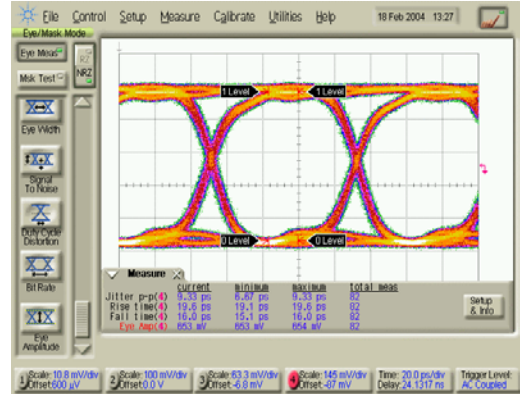
Bit rate: 12.5 Gb/s
Vin = +/-200 mVpp, Vout = +/-644 mVpp



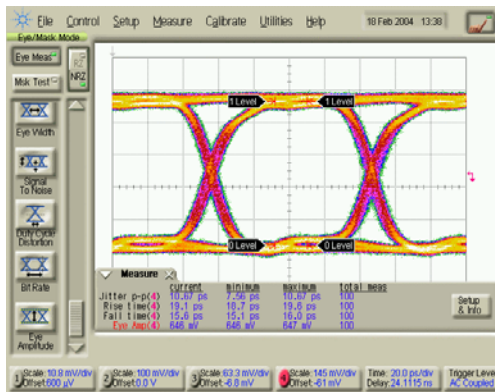
Eye Diagram Performance (cont.)



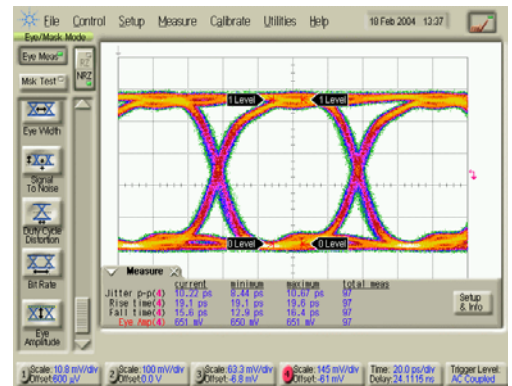
Bit rate: 10.7 Gb/s
Vin = +/-200 mVpp, Vout = +/-653 mVpp



Bit rate: 12.5 Gb/s
Vin = +/-200 mVpp, Vout = +/-653 mVpp



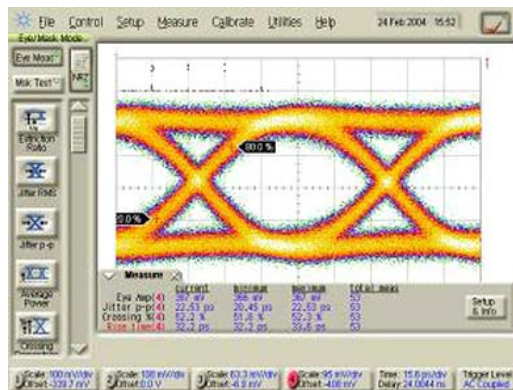
Bit rate: 10.7 Gb/s
Vin = +/-1 mVpp, Vout = +/-653 mVpp



Bit rate: 12.5 Gb/s
Vin = +/-1 mVpp, Vout = +/-653 mVpp

Input Sensitivity

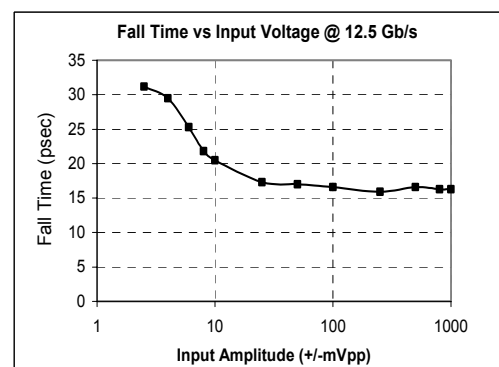
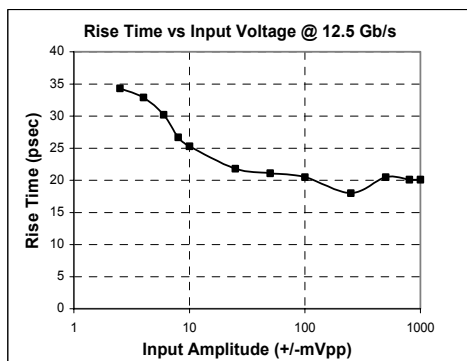
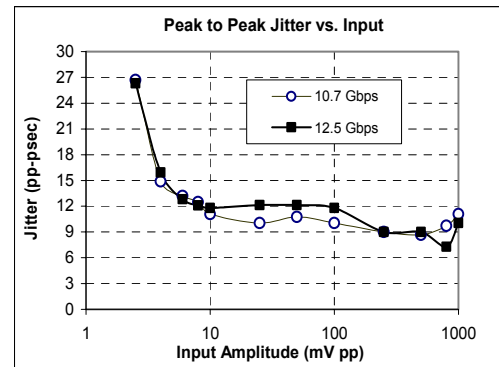
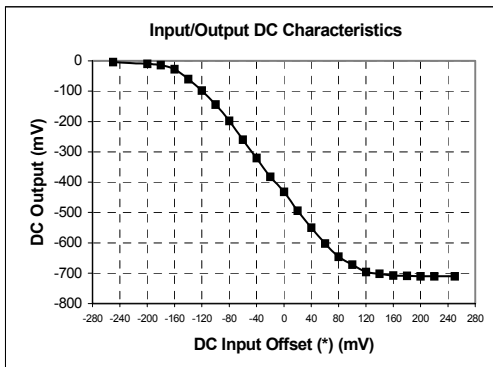
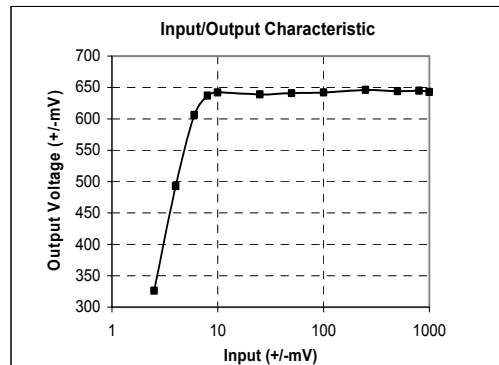
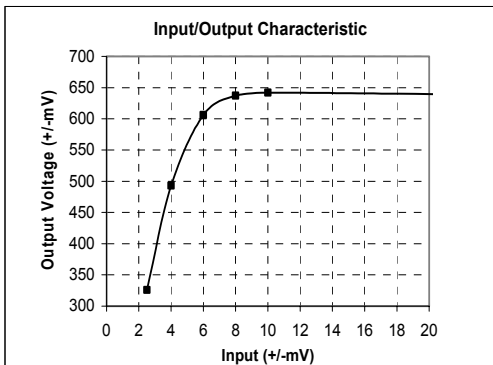
Vee1 = Vee2 = -5.2 V
Iee1+Iee2 = 95 mA



Input sensitivity = +/-2.5 mVpp differential input, 12.5 Gb/s
BER < 1E-12
Output voltage = 367 mVpp single-ended



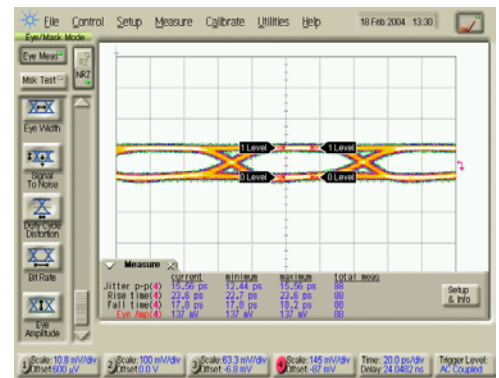
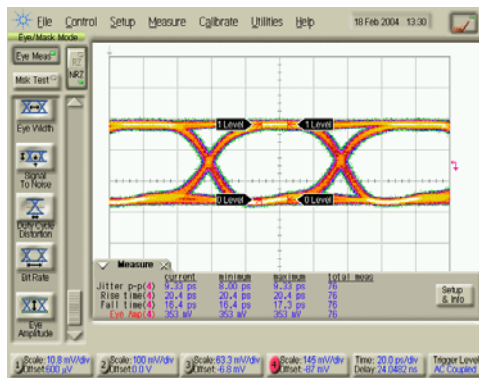
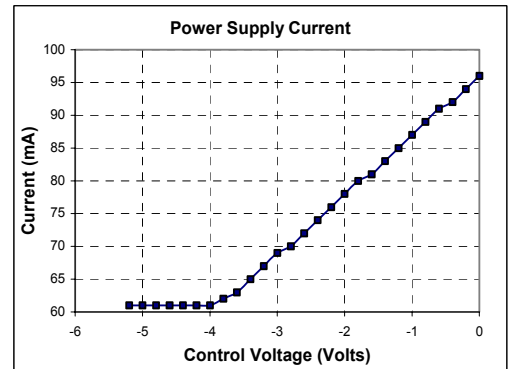
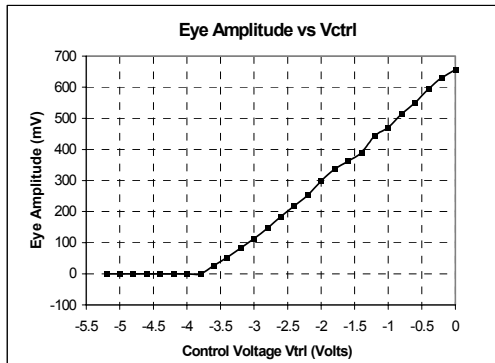
Performance As Function of Input Voltage



(*) Input applied to the offset control pin (Voffset1) and open output.



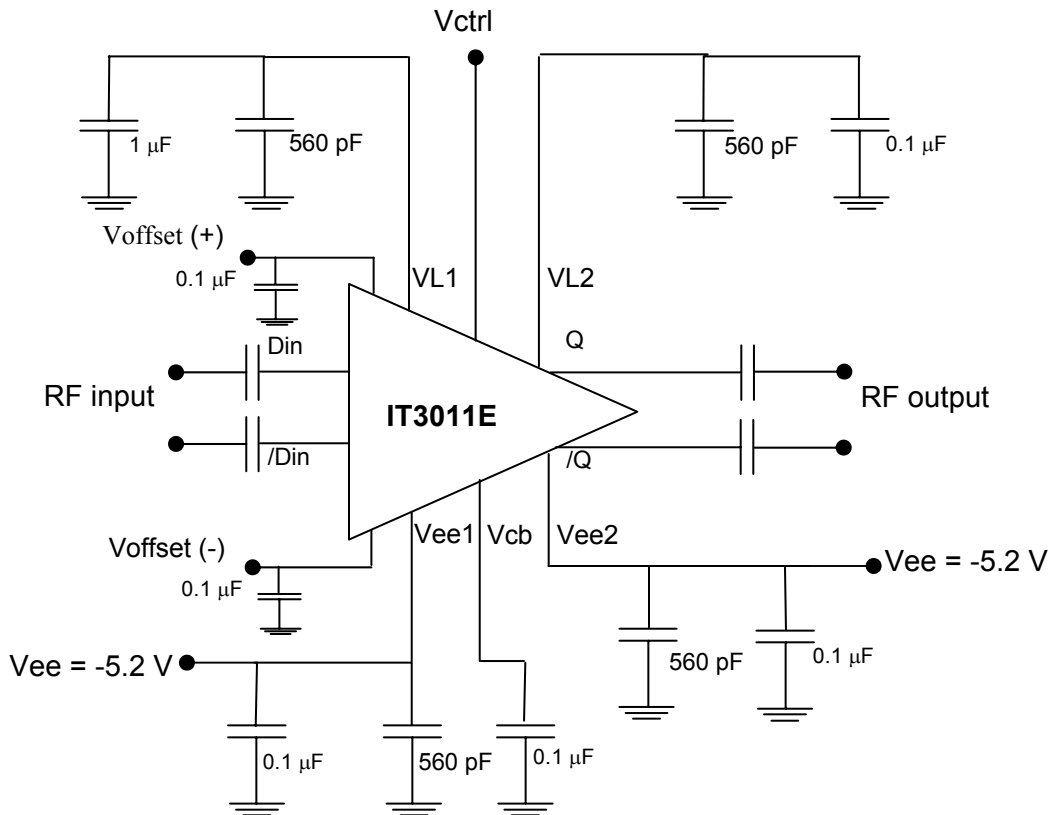
Output Voltage Control



Recommended Operational Setup

Apply -5.2 V at Vee1 and Vee2
Apply 0 V at Vctrl
for maximum output

DC blocking capacitors optional



“E” Package Drawings, Pinouts, Marking

Notes:

Dimensions in inches (mm)

Tolerances are ± 0.0039 in. (0.100 mm)

Package drawing encompasses JEDEC MO-220 Version VGGC-2.

See iTerra Application Note 10 for recommended pad layout. RoHS parts are backward compatible if application note pad layout is followed.

Lead frame material is copper alloy.

Mold compound is UL94V0 compliant.

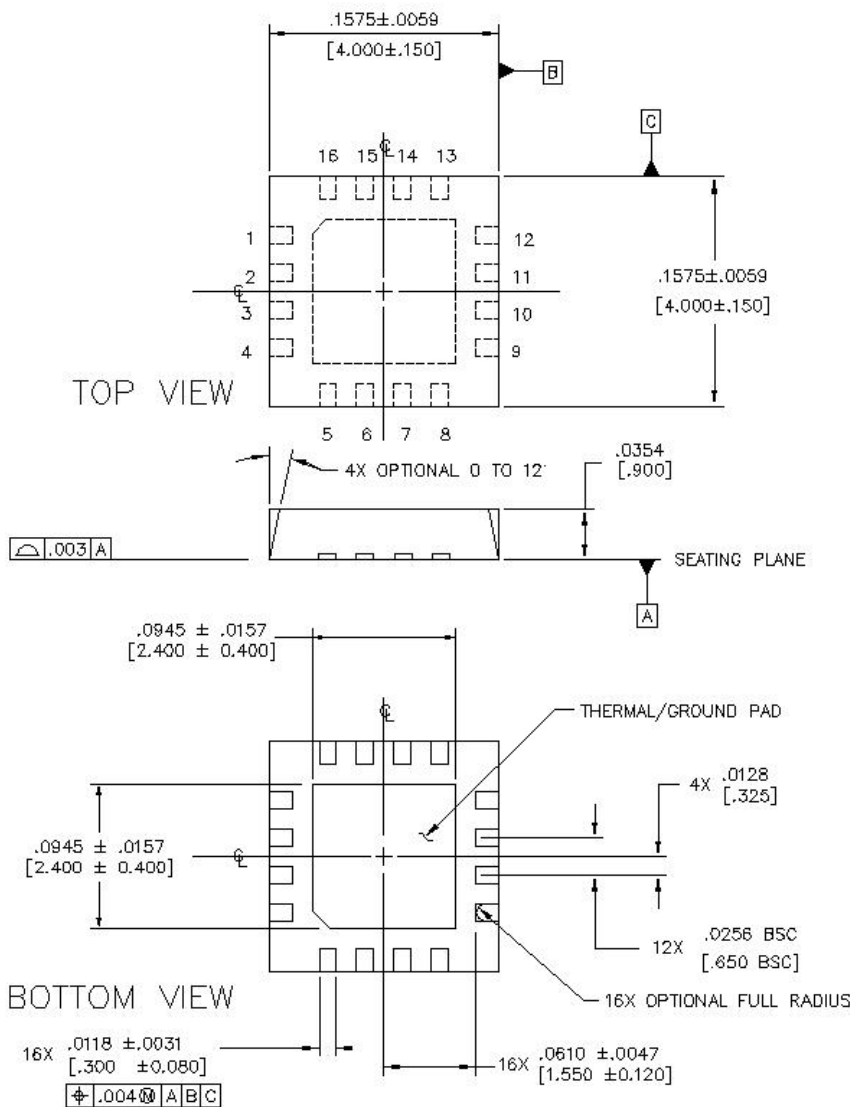
Lead finish is NiPdAu.

Marking Information

iTerra
 MMMMEA
 XXNNNN
 LLYYWW

Where,

MMMM = part no.
 E = Package Type
 A =Temp. Range
 XX = Wafer Lot
 NNNN = Ser. No.
 LLYYWW =MFG D/C



Pinouts

P1: GND	P9: GND
P2: Din (RF input)	P10: /Q (/RF Out)
P3: /Din (/RF input)	P11: Q (RF Out)
P4: GND	P12: GND
P5: Voffset (-)	P13: VL1
P6: Vee1	P14: Vctrl (voltage control)
P7: Vcb	P15: VL2
P8: Vee2	P16: Voffset (+)

