ACT7005/7006
Single Package Solution
Dual Transceiver, Protocol, Subsystem

Features

- **Incorporates Transceivers, Protocol, and System Interface Components into a Single Hybrid Package**
- **Functions as a Remote Terminal or Bus Controller**
- **Interfaces to µP as a Simple Peripheral Unit**
- **+5V Operation**
- **Provides 2k by 16 of Double Buffered RAM Storage for Transmit and Receive Subaddresses**
- **Pin Programmable for 8-bit or 16-bit Microprocessors**
- **Full Military (-55°C to +125°C) Temperature Range**

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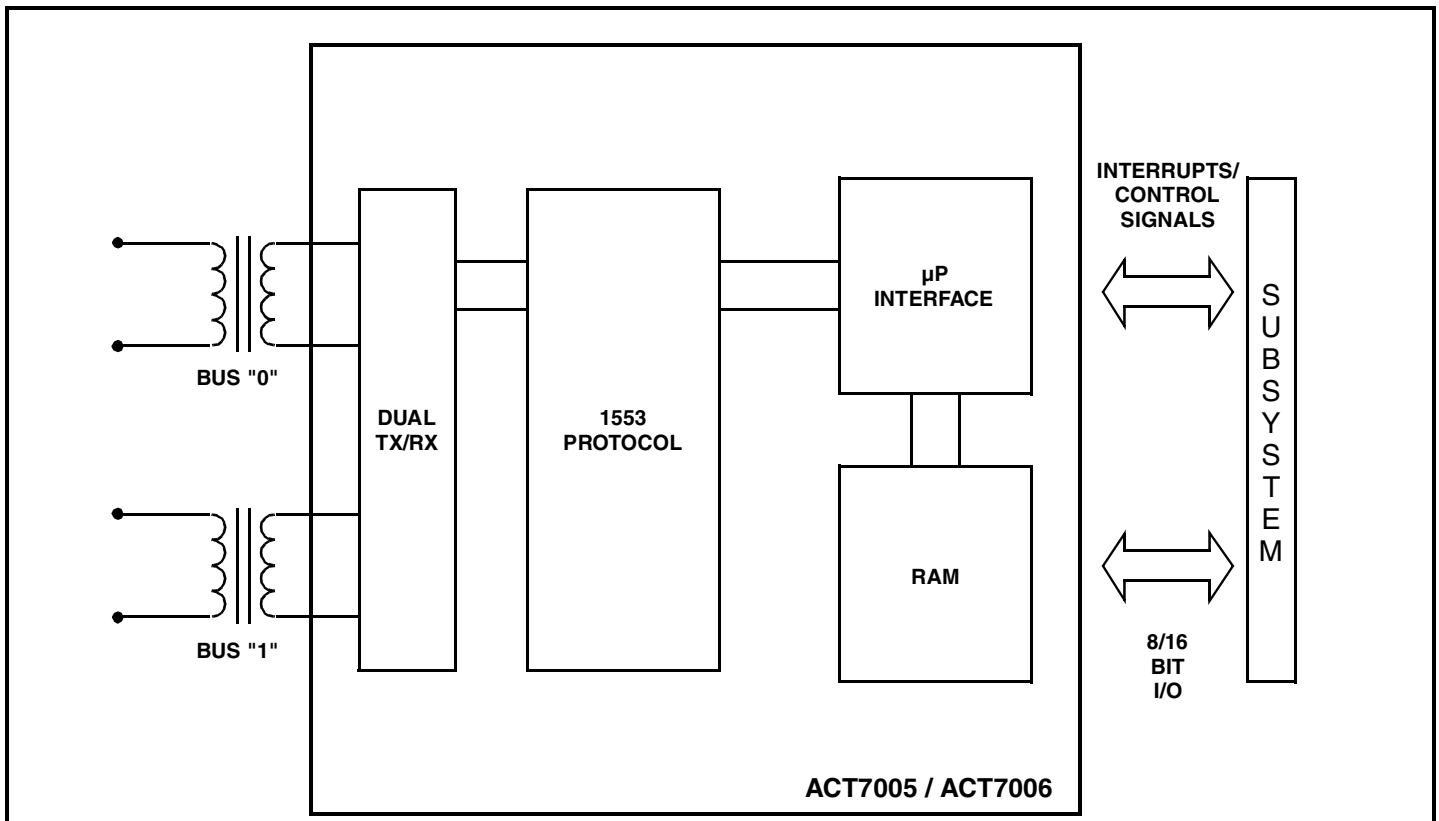
General Description

The ACT7005/6 Series provides a complete one package interface between the MIL-STD-1553 bus and all microprocessor systems. The hybrid provides all data buffers and control registers to function as a Bus Controller or Remote Terminal. Control of the hybrid by the subsystem is through simple I/O port commands. Internal hybrid logic removes all critical timing imposed on a typical subsystem, thereby simplifying the implementation of this interface.



Block Diagram

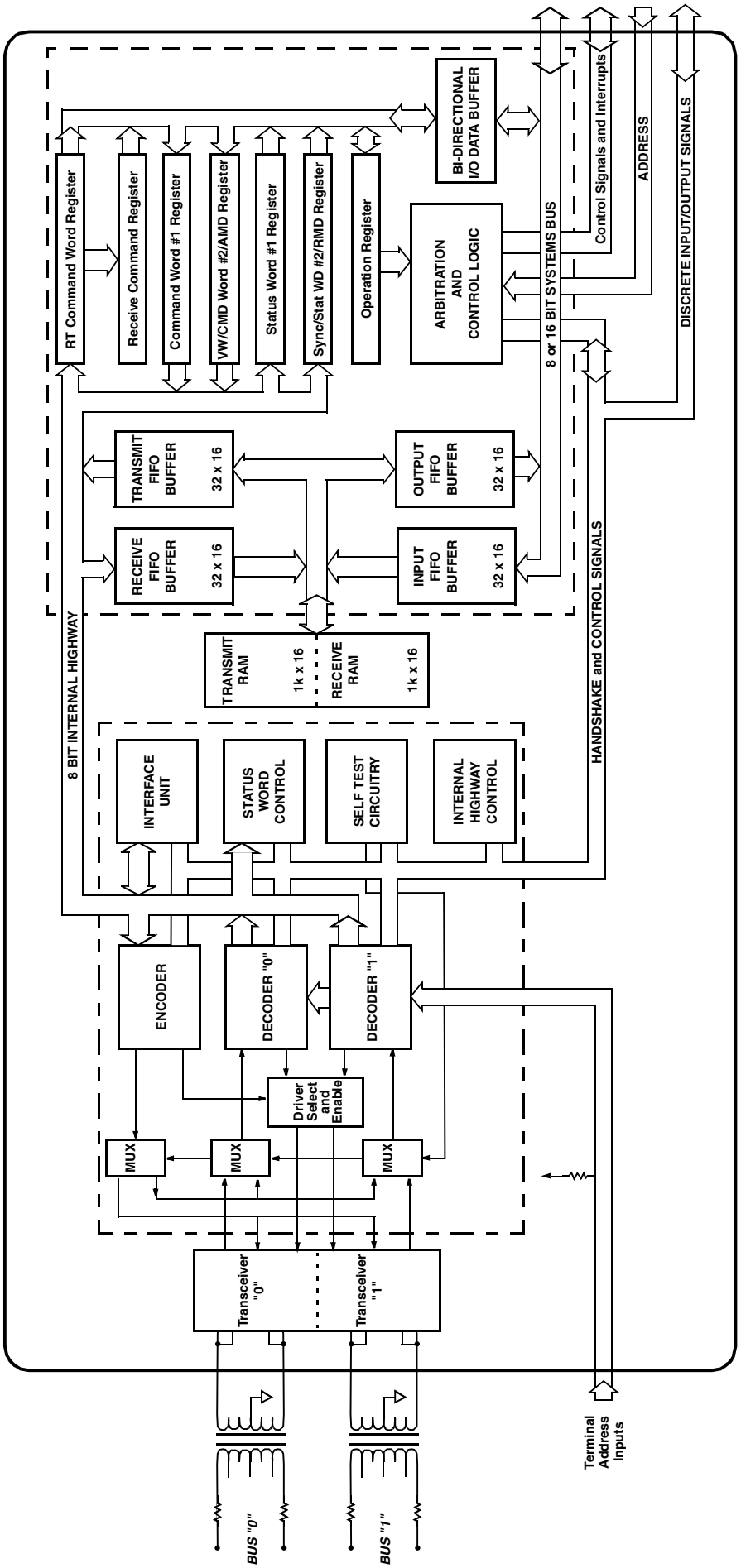


Figure 1 – FUNCTIONAL BLOCK DIAGRAM

Parameter	Min	Max	Units
Power Supply Voltage (V_{CC})	-0.3	7.0	V
Power Supply Voltage (V_{CCL} & V_{DD})	-0.3	7.0	V
Receiver Differential Input (DATA CH A/B / $\overline{\text{DATA CH A/B}}$)	-10	+10	V
Receiver Input Voltage (DATA CH A/B or $\overline{\text{DATA CH A/B}}$ – Common Mode)	-5	+5	V
Operating Case Temperature Range (T_C)	-55	+125	°C
Transmission Duty Cycle at T_C = +125°C	-	100	%

Table 1 – Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.75	5	5.5	mA
Total supply current "standby" mode or transmitting at less than 1% duty cycle (e.g. 20µs of transmission every 2ms or longer interval). 2/	I_{CC}@1%		18	30	mA
Total supply current transmitting at 1MHz into a 35Ω load at Point A in Figure 1. 2/ 1/	I_{CC} @ 25% I_{CC} @ 50% I_{CC} @ 100%		150 300 600	175 350 700	mA mA mA

Note:

1/ Decreases linearly to applicable "standyby" values at zero duty cycle.

2/ Represents one channel only.

Table 2 – Analog Transceiver Power Supply Characteristics

Parameter/Condition		Symbol	Min	Max	Unit
Differential impedance DC to 1MHz, See Figure 4	Point A	Z_{IO}	2K		Ω
	Point C		1K		Ω
Differential voltage range		V_{DIR}	-10	+10	V_{PEAK}
Input common mode voltage range		V_{ICR}	-5	+5	V_{PEAK}
Common mode rejection ratio (from point A, Figure 4)		CMRR	40		dB
Threshold characteristics (sine wave at 1MHz) NOTE: Threshold voltages refer Figure 4	Point A	V_{TH1}	0.8	1.1	Vp-p
	Point C	V_{TH2}	0.56	0.86	Vp-p

Table 3 – Analog Transceiver Electrical Characteristics (Receiver Section) (Over Full Temperature Range)

Parameter / Condition		Symbol	Min	Typ	Max	Unit
Differential output level at point B, See Figure 4	140Ω Point B	V_O	24		35	Vp-p
	70Ω Point C		18		25	Vp-p
Differential Output Noise at Point A, See Figure 4		V_{NOI}			10	mVp-p
Output Offset at point A in Figure 4, 2.5µs after mid-bit crossing of parity bit of last word of a 660µs message	Point A (35Ω)	V_{os1}	-90		+90	mV
	Point C (70Ω)	V_{os2}	-250		+250	mV
Rise and Fall times (10% to 90% of p-p output)		t_R & t_F	100	160	300	ns

Table 4 – Analog Transceiver Electrical Characteristics (Transmitter Section) (Over Full Temperature Range)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Logic Supply	4.5	5.0	5.5	VDC	
V_{IH}	Input "1"	2.4			V	
V_{IL}	Input "0"			0.6	V	
I_L	Input I	-450	-600	-900	µA	Note 1A
I_{IH}	Input I	-250	-400	-750	µA	Note 1B
I_L	Input I	-50	-200	-800	µA	Note 1C
I_{IH}	Input I	-50	-200	-800	µA	Note 1D
I_L	Input I	-25	-125	-400	µA	Note 2A
I_{IH}	Input I	-25	-125	-400	µA	Note 2B
V_{OH}	Output "1"	2.4			VDC	Note 3A
V_{OL}	Output "0"			0.4	VDC	Note 3B
V_{DD}	Static I			50	mA	Note 4A
V_{DD}	Dynamic I			170	mA	Note 4B

Notes:

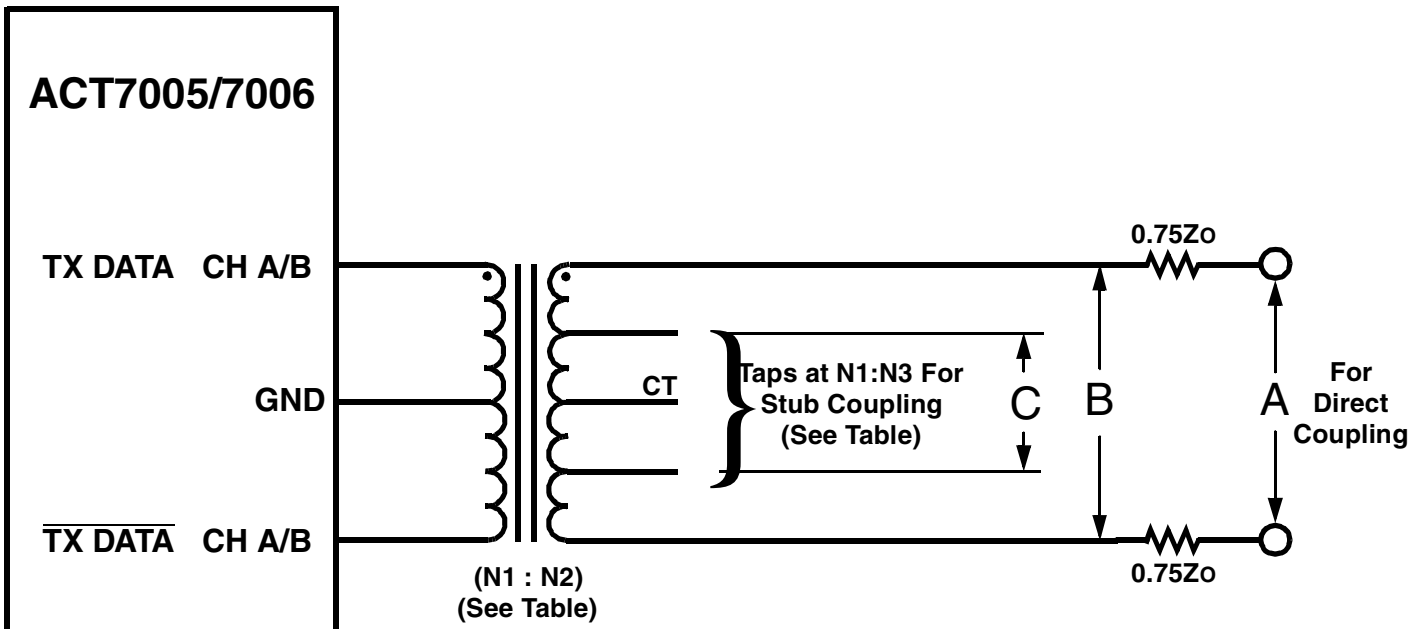
1. V_{DD} = 5.5V
   A. For RTAD0/1/2/3/4 and RTADPAR with VIL = 0.4V
   B. For RTAD0/1/2/3/4 and RTADPAR with VIH = 2.4V
   C. FOR BCSTEN WITH VIL = 0.4V, Test 1, 6MHz
   D. FOR BCSTEN WITH VIH = 2.4V, Test 1, 6MHz

2. All remaining inputs and I/O
   VDD = 5.5V
   A. VIL = 0.4V
   B. VIH = 2.4V

3. A. VDD = 4.5V and IOH = 3mA
   B. VDD = 5.5V and IOL = 3mA

4. VDD = 5.5V
   A. Clock Input = 6MHz (45-55% Duty Cycle / TTL Levels), All remaining inputs = VDD, All Outputs = Open Circuit
   B. During a 32 word FIFO to RAM or RAM to FIFO block move.

Table 5 – Logic Electrical Characteristics (Over Full Temperature Range)



TURNS RATIO	ACT7005/7006
N1:N2	1:2.5
N1:N3	1:1.79
Technitrol Part #	T-1553-45

Figure 2 – Transformer Configuration

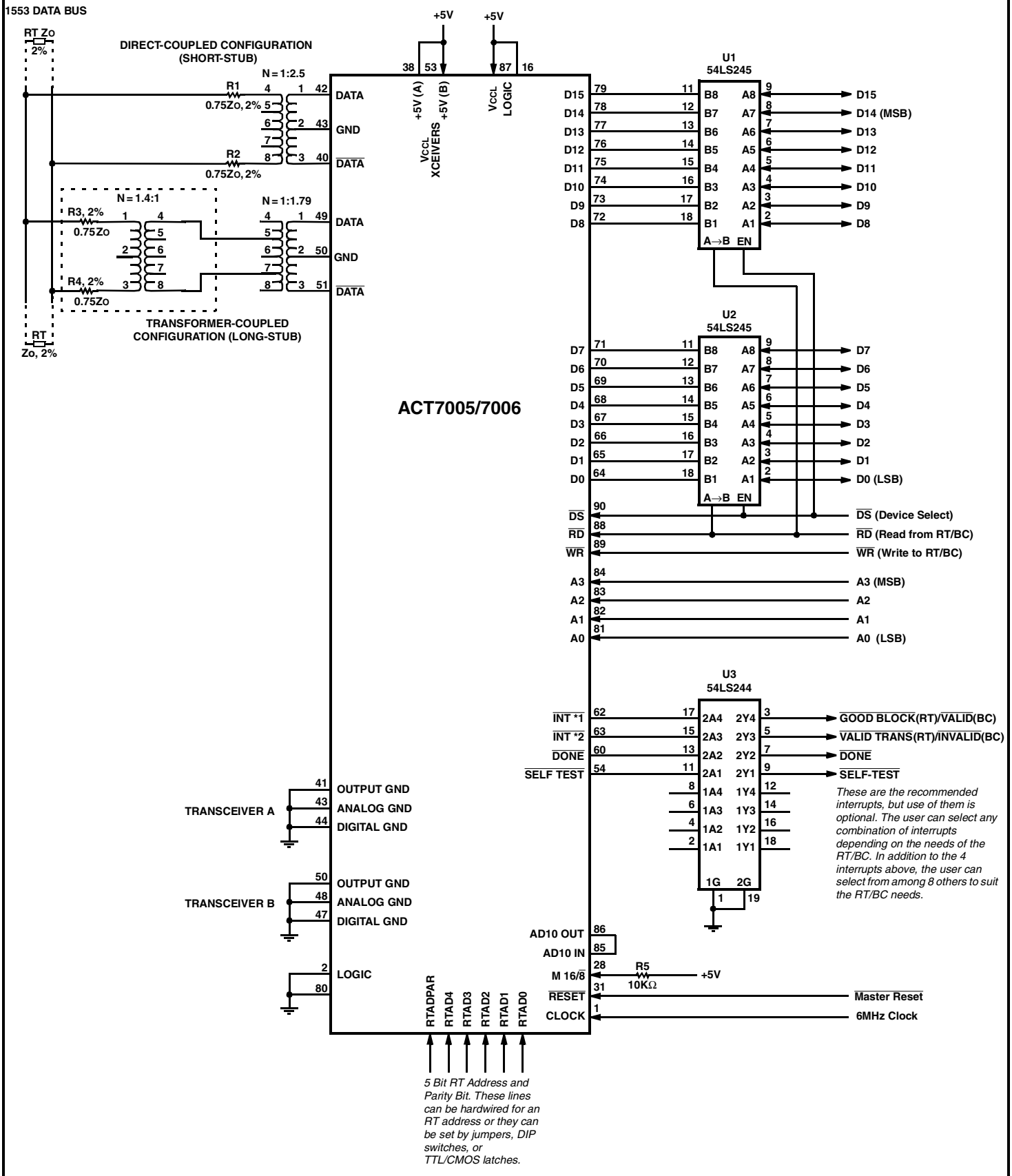


Figure 3 – Typical Interface Connections

SINGLE HYBRID PROTOCOL SUBSYSTEM INTERFACE

KEY FEATURES

- **Functional Superset of CT1800**
- **Downward compatible with existing designs base of CT1800**
- **Incorporates Transceivers, Protocol and Interface Hybrids into a single package**
- **Functions as a Remote Terminal or Bus Controller**

GENERAL

The ACT7005/6 Series provides a complete interface between the MIL-STD-1553 bus and any micro-processor system. Functioning as a superset of the CT1800 interface, the hybrid provides all data buffers and control registers necessary to implement RT and BC functions. Internal arbitration and data transfer control circuitry eliminates subsystem response requirements. All data written into or read from this interface are double buffered on a message basis. Only valid and complete receive messages are transferred into the receive RAM.

The ACT7005/6 Series supports all 15 mode codes and all types of data transfers allowed by MIL-STD-1553B. All circuitry (excluding transceiver drivers) are CMOS, which results in very low power requirements.

Interfacing to the subsystem is simplified through the use of tri-stated input/output buffers onto the subsystem bus. Control signals basically consist of four address lines, a device select input, read strobe, write strobe, and several interrupts, the use of which are optional. The Hybrid is accessed as a memory mapped I/O port of a microprocessor system. Valid transmission and reception of data are indicated to the subsystem through the use of interrupts. This frees up the system processor from actively monitoring the port until a valid message is received.

OPERATION

The ACT7005/6 Series (Single Package Solution) resides between a microprocessor interface and a MIL-STD-1553 data bus. The addition of two transformers and fault isolation resistors are the only external components required to complete the interface. Information on the bus is received or transmitted through the transceiver (converted from Manchester II to complimentary TTL signals and visa versa) to the protocol section. The ACT7005/6 Series incorporates a single +5VDC only transceiver.

The protocol section internally interfaces to the transceivers. Control of the transceivers is provided by the protocol section. This is determined by which bus the command word was received on in the remote terminal mode; or in the bus controller mode, which bus was selected for transmission by the state of a bit in the operation register. An autonomous self-test can be performed either off-line or on-line through the transceivers This self-test is controlled by the operation register and will be discussed thoroughly in the self-test section. The other test function is that in addition to the protocol criteria that is tested during every transmission; i.,e., proper sync character, 16 data bits, Manchester II coded, contiguous words, and odd parity, a bit per bit comparison of the contents of the parallel data will insure a higher degree of functionality of this section of the hybrid.

Data received by the protocol section will be placed in the receive FIFO buffer. Transmitted data will be taken from the transmit FIFO buffer. Other than the remote terminal address and parity, the discretes to control the resetting of the terminal flag and subsystem error bits, and a few discrete interrupts and error signals, control over the protocol section resides in the operation register of the subsystem interface section.

The subsystem interface section has primary control of the data that resides in the 2k of RAM. The RAM is segregated into two 1k blocks of data, one contains 30 blocks of transmit data messages and the other one contains 30 blocks of receive data messages. This is not absolute since the subsystem has control of the A10 bit. Data entries to or from the RAM are arbitrated by the control logic residing in this function, and is buffered via FIFO's on the input from the protocol section and on the output to the subsystem's data bus. This guarantees that only current and valid data blocks will reside in RAM. This is true for remote terminal and bus controller applications.

Seven dedicated registers are provided to ease the interfacing with the subsystem. These will be discussed in the Register Operation section of this document. The register of primary concern to a subsystem designer is the operation register. This provides the means to accomplish data transfers to/from the RAM, as well as control of remote terminal or bus control modes of operation. All registers are accessed via simple I/O commands, utilizing A0 through A3, Device Select, and Read or Write strobes.

Receive Commands

When a valid receive command is received, it is first loaded into the Command Word Register. The data words associated with this command are received, validated, and loaded one by one into the RCV FIFO buffer. Once the entire message is received, and only if the complete block of data is valid, will the

command word be transferred to the RCV Command Register. This block of data is then burst (by the internal controller) into the corresponding internal RAM location, which is memory mapped by the subaddress contained in the RCV Command Register. Once this operation is complete, a discrete interrupt pulse called INT #1 is sent the subsystem.

If this interrupt is used, the subsystem would read the command word from the RCV Command Register. The data could then be transferred to the OUTPUT FIFO buffer, and read by the subsystem. Each receive subaddress section of the internal RAM will contain only the most recent, valid, and complete block of data to that subaddress. This is true for Remote Terminal and Bus Controller operations.

Transmit Commands

If a valid transmit command is received, the command word is first loaded into the Command Word Register. The block of data corresponding to the subaddress of the transmit command is then transferred from the internal RAM to the XMIT FIFO buffer. Upon completion of this transfer, INT #2 is sent to the subsystem.

The transmit section of the internal RAM is generally initialized at power up and periodically updated as required.

Appropriate subsystem response to INT #2 for an RT implementation would be to read the command word from the Command Word Register. The data to this subaddress could now be refreshed in preparation for the next time it was requested to be transmitted across the 1553 bus.

Mode Codes

All 15 mode codes are serviced by the protocol section, and most do not require subsystem intervention. Discrete interrupt signals are available for each of the Synchronize (with and without data), Vector Word, Reset, and Dynamic Bus Control Acceptance mode codes. Mode command words are loaded into the Command Word Register. Separate registers are provided for the synchronize data word and the vector data words.

Bus Control Operation

Upon initialization of power to the ACT7005/6 Series, all registers are reset. The operation register is reset to FF80H; this setting defaults to the remote terminal mode of operation with the Busy Bit set. To enter into the Bus Control Mode of operation, bit 8 of the operation register must be asserted low. While in this mode, the upper byte (8 bits) of the operation register controls Bus Control functionality. This includes TEST/NORMAL operation, RT to RT commands, BUS selection and RETRY initialization of a faulty transaction.

A typical Bus Control transaction would operate as follows: All areas of internal RAM that will be used for transmission are initialized by the subsystem with the desired data. To accomplish this, the subsystem will first WRITE to the INPUT buffer the number of words to be transferred. This information is now transferred to the internal RAM under control of the OPERATION register by specifying the subaddress bits 0-4, setting the T/R bit (bit 5) and I/O bit (bit 6) high. This will be executed by issuing an EXECUTE operation I/O command. When the transfer has been completed, the DONE interrupt will pulse low, and valid data will now reside in this RAM location. Next, the subsystem will write the command word to COMMAND WORD #1 register. If it were an RT-to-RT transfer, the transmitting RT command word would be written into COMMAND WORD #2 register. The next register to be intitialized would be the OPERATION register, which controls which bus to transmit on and if retry will be an option. This information will be enacted upon when the subsystem issues a TRIGGER I/O command. The return status word from the remote terminal or status words for RT-to-RT transfers will reside in their appropriate registers upon the issuance of INT #1. If the RETRY option had been selected and a valid transfer had not occurred, the RETRY interrupt would have occurred instead of INT #1. Three retrys are the maximum number allowed. The retrys can be accomplished on the primary or secondary bus determined by programming bits in the operation register.

A retry will be initiated if the retry bits are set in the OPERATION register. The criteria for attempting a retry is the lack of a returned status word or returned mode data, or that 768µsec has transpired since the start of the data transfer. A retry will not be executed if bits are set in the return status word(s); this is up to the subsystem to interpret the status word contents and to reinitiate the transfer if desired.

Discrete Interrupts

Twelve discrete interrupt output signals are available for the subsystem interface. Any or all of these may be used depending on subsystem requirements. Excluding the signal $\overline{\text{BUFF EF}}$, all interrupts are low going pulse signals. Interrupt and status signals RESET, DBCREQ, and NBGT are 500ns wide nominally, and VECTOR is typically 1.5µs wide. All remaining interrupts are nominally 160ns.

The output buffer empty flag ($\overline{\text{BUFF EF}}$), which is a level, is also made available for subsystem use. When low, it indicates the output buffer is empty. See Table 6 for additional information.

REGISTER SUMMARY

Remote Terminal Command Word Register: This Register is utilized in the RT mode and is read only. It contains all valid received command words, i.e. transmit, receive, and mode command.

Receive Command Word Register: After the reception of a valid receive message, and the GOOD BLOCK interrupt has been issued, the Receive Command word will be transferred from the Remote Terminal Command Word Register to this register. The purpose of double buffering receive command words is to maximize the time a subsystem has to read this command since GOOD BLOCK comes at the end of the data transfer, and the next command word could overwrite the contents of the Remote Terminal Command Word Register. This is a READ ONLY register in RT mode.

Command Word #1 Register: This register contains the first command word to be transmitted during an RT to RT transfer, or the command word for a BC to RT, or RT to BC transfer. This register is a read or write register.

Vector Word/Command Word #2 Associated Mode Data Register: This register is used to accomplish multiple functions in Bus Controller and Remote Terminal Modes. In BC Mode it will contain the second command word for (RT to RT) transfers, or Associated Mode Data that is required by certain mode codes; i.e., Sync (with data). When operated in the RT Mode, this register contains the Vector Word required by mode code Transmit Vector Word Command.

STATUS Word #1 Register: The utilization of this register in the BC mode is read only. It contains the returned status word for BC to RT, RT to BC mode, or the first returned status in RT to RT mode. At reset or the initiation of a bus transfer, the contents of this register will be set to all high, FFFFH.

Synchronize/Status Word #2/ Return Mode Data Register: In Bus Controller mode this register will either contain the second returned status word for RT to RT transfers or the returned mode data; i.e., BIT word or Vector word, Last Status word, or Last Command word. In BC mode this register is initialized to all highs, FFFFH. Unlike the other status word register, this does function in the RT mode, but is still read only in either mode. In RT mode it will contain the SYNC data word received in association with the Synchronize with Data Mode Code.

Operation Register: This register contains information provided by the subsystem to control the interface. This register sets up the mode of operation for the interface (BC or RT), selects the available options (BUS Select and Auto Retry), and contains information for reading or writing data to the Internal RAM. (See note below.) This register also provides software control of the DBCACC, SERVREQ, and SSERR bits of the status word. Following power-up master reset, bit 7 of this register will be set high. This bit corresponds to the busy bit of the Remote Terminal Status Word. The subsystem reads and writes to this register under I/O commands. The transfer functions defined by this register are executed by either of the two I/O EXECUTE Commands.

Note: The Internal RAM is divided into transmit or receive sections. In general, data is written to the transmit section and read from the receive section. However, either section may be read from or written to via the T/R bit in this register.

SELF TEST

The inclusion of simple wraparound self test circuitry in the protocol section insures that a high percentage of coverage is attainable. Testing requires simple subsystem intervention. A word is first placed in the VECTOR WORD Register. Test bit 9 in the OPERATION Register is asserted low and the I/O TEST TRIGGER address is written. The LT LOCAL (Bit 10 of the Operation Register) determines if this will be an ON/OFF line test. OFF line tests are performed by the inclusion of digital multiplexers in front of the encoder, bypassing the transceiver, providing a path to the decoder. The ON line tests are accomplished when not connected to a bus network, such as a maintenance test station, since this test utilizes the transceiver to provide the loop back path instead of the internal multiplexers. In this mode test words would appear on the bus. First, the primary bus will be tested with the data that resides in the VECTOR WORD Register. It is encoded then looped back, decoded and presented to the subsystem as a normal data transfer would be accomplished. This word will be stored in the RT Command Word Register. The secondary bus is sequentially tested after the primary bus is completed, utilizing the word residing in the VECTOR WORD Register. Upon successful completion of the test, the PASS interrupt will be asserted low.

In addition to this test of the protocol section, the subsystem data handling capability is also testable via the OPERATION Register. This is accomplished by writing a message to the INPUT FIFO Buffer; this data can be placed in any location determined by the SA0 through SA4 Bits, or in either the transmit or receive section (T/R Bit). This same data can now be transferred from this RAM location to the OUTPUT FIFO Buffer and compared with the data originally written to the INPUT FIFO Buffer. Providing this type of testing provides a high degree of functional verification.

This test implementation not only verifies MIL-STD-1553 protocol compliance (proper sync character, 16 data bits, Manchester 11 coding, odd

parity, and contiguous word checking), but also the inclusion of a bit by bit comparison of transmitted data has been added. The added circuitry is used to insure that the internal functional blocks, encoder, decoder, and internal control circuitry are functioning properly. The internal data path can be verified as fault free by comparing the returned data word with the supplied data. The most effective data pattern to accomplish this is HEX AA55, since each bit is toggled (8 bit internal highway) on a high/low byte basis. Total time to complete the test is 89 microseconds. TEST ENABLE (bit 9) must remain low this entire time to ensure proper operation of the self test.

USE OF A10 AND A10IN

The standard configuration of the ACT7005/6 Series divides the INTERNAL RAM into separate RECEIVE and TRANSMIT sections. For this configuration A10 is connected to A10IN. When A10 is high, it addresses the TRANSMIT section; when low, the RECEIVE sections. A10IN is the address input to the INTERNAL RAM.

The interface may be configured with one common section for both RECEIVE and TRANSMIT data. To configure this, A10 is not connected, and A10IN is fixed at either a logic high or low. This bit can also be controlled by the subsystem to provide double buffering of the contents of common RAM section for receive and transmit data. If A10 and A10IN are not directly connected together but gated together, then no more than 100nsec of propagation delay should be introduced.

NON-REGISTER OPERATIONAL COMMANDS

There are six operational commands that are not register read or write operations. These commands are summarized in Table 8. The two execute operations are dependent on the contents of the OPERATION register. The address codes for all the operational commands are summarized in the 8 bit and 16 bit I/O OPERATIONAL tables.

OPTIONAL STATUS WORD CONTROL

Message Error Bit

The ACT7005/6 monitors all receptions for errors and sets the Message Error Bit as prescribed in MIL-STD-1553B. The subsystem designer may, however, exercise the option of monitoring for illegal commands and forcing the Message Error Bit to be set.

The word count and subaddress lines for the current command are valid when $\overline{\text{INCMD}}$ goes low. The subsystem must then determine whether or not the word count or subaddress is to be considered illegal by the RT. If either of them is considered illegal, the subsystem must produce a negative-going pulse called $\overline{\text{MEREQ}}$. The negative-going edge of $\overline{\text{MEREQ}}$ must occur within 500 nSec of the falling edge of $\overline{\text{INCMD}}$.

Subsystem Flag and Terminal Flag Bits

The conditions that cause the Subsystem Flag and Terminal Flag Bits in the Status Word to be reset may be controlled by the subsystem using the $\overline{\text{ENABLE}}$, $\overline{\text{BIT DECODE}}$, $\overline{\text{NEXT STATUS}}$, and $\overline{\text{STATUS UPDATE}}$ inputs. If $\overline{\text{ENABLE}}$ is inactive (high), then the Terminal Flag and Subsystem Flag behavior is the same as described below: (i.e. the other three option lines are disabled).

Subsystem Flag Bit: This bit is reset to logic zero by a power up initialization or the servicing of a legal mode command to reset the remote terminal (code 01000).

This bit shall be set in the current status register if the subsystem error line, $\overline{\text{SSERR}}$, from the subsystem ever goes active low. This bit shall also be set if an RT/subsystem handshaking failure occurs. This bit, once set, shall be repeatedly set until the detected error condition is known to be no longer present.

Terminal Flag Bit: This bit is reset to logic zero by a power up initialization or the servicing of a legal mode command to reset the remote terminal (code 01000). This bit can be set to logic one in the current status register in four possible ways:

a) If the RX detects any message encoding or content error in the terminals transmission. A loop test failure, LTFAIL, will be signalled which shall cause the Terminal Flag to be set and the transmission aborted.

b) If a transmitter timeout occurs while the terminal is transmitting.

c) If a remote terminal self test fails.

d) If there is a parity error in the hard wired address to the RX chip.

This bit, once set, shall be repeatedly set until the detected error condition is known to be no longer present. The transmission of this bit as a logic one can be inhibited by a legal mode command to inhibit terminal flag bit (code 00110). Similarly, this inhibit can be removed by a mode command to override inhibit terminal flag bit (code 00111), a power up initialization or a legal mode command to reset remote terminal (code 01000).

If $\overline{\text{ENABLE}}$ is held low, then the three options

described below are available and are essentially independent. Any, all, or none may be selected. Also, reporting of faults by the subsystem requires that $\overline{\text{SSERR}}$ be latched (not pulsed) low until the fault is cleared.

Resetting SSF and TF on Receipt of Valid Commands

If $\overline{\text{ENABLE}}$ is selected and the other three option lines are held high, then the Status Word Register will be reset on receipt of any valid command with the exception of Transmit Status and Transmit Last Command. Note that in this mode, the TF will never be seen in the Status Word, and the SSF will only be seen if $\overline{\text{SSERR}}$ is latched low. Also note that the SSF will not be seen in response to Transmit Status or Transmit Last Command if the preceding Status Word was clear, regardless of actions taken on the $\overline{\text{SSERR}}$ line after the clear status transmission.

Status Register Update at Fault Occurrence

If $\overline{\text{STATUS UPDATE}}$ is selected (held low), then the TF or SSF will appear in response to a Transmit Status or Transmit Last Command issued as the first command after the fault occurs. Any other command (except as noted in the Preserving the BIT Word section) will reset the TF and SSF. Repeated Transmit Status or Transmit Last Command immediately following the fault will continue to show the TF and/or SSF in the Status Word. Note that this behavior may not meet the "letter-of-the-spec" as described in MIL-STD-1553B, but is considered the "preferred" behavior by some users.

TF and SSF Reporting in the Next Status Word – After the Fault

If $\overline{\text{NEXT STATUS}}$ is selected (held low), then the TF or SSF will appear in response to the very next valid command after the fault except for Transmit Status or Transmit Last Command. The flag(s) will be reset on receipt of any valid command following the status transmission with the flag(s) set except for Transmit Status, Transmit Last Command, or as noted in the following section on Preserving the BIT Word.

Preserving the BIT Word

In order to preserve the Transmitter Timeout Flag, Subsystem Handshake Failure, and Loop Test Failure Bits in the BIT Word, it is necessary to select $\overline{\text{BIT DECODE}}$ (hold it low). This will prevent resetting those bits if the Transmit Bit Word Mode Command immediately follows the fault or follows a Transmit Last Command or Transmit Status immediately following the fault. It will also prevent resetting the TF and SSF Bits in the Status Word. Any other valid commands will cause those BIT Word Bits and the Status Word Bits to be reset.

Name	Use
$\overline{\text{INT \#1}}$	
$\overline{\text{GOOD BLOCK}}$ (RT)	Indicates reception of a valid block of data. The RECEIVE COMMAND WORD is loaded in RCV CMD WD Register. This interrupt is issued after the new block of data is moved into the Internal RAM.
$\overline{\text{VALID}}$ (BC)	Indicates that the Bus Controller has initiated and observed a valid message transfer on the 1553 data bus.
$\overline{\text{INT \#2}}$	
$\overline{\text{VALID TRANS}}$ (RT)	Indicates reception of a valid TRANSMIT COMMAND WORD. The TRANSMIT COMMAND WORD is loaded in CMD WD Register. Note: This interrupt does not necessarily indicate that the transmitted data was received by the bus controller.
$\overline{\text{INVALID}}$ (BC)	Indicates that the Bus Controller has initiated a message transfer on the data bus, but the message traffic has been deemed invalid.
$\overline{\text{SYNC NO DATA}}$	Indicates reception of a valid mode command SYNCHRONIZE WITHOUT DATA
$\overline{\text{SYNC W/DATA}}$	Indicates reception of a valid mode command SYNCHRONIZE WITH DATA. The synchronize data word is loaded into the SYNC/STAT WD #2/RMD REGISTER. This interrupt will not be issued if a word count high or low error occurs.
$\overline{\text{DONE}}$	This interrupt is issued in response to an I/0 command from the subsystem. In response to an I/0 load OUTPUT buffer command, it indicates that the complete 32 word message block (SUBADDRESS) has been loaded into the OUTPUT FIFO buffer. In response to an I/0 load internal RAM from INPUT FIFO buffer command, it indicates the full message (1 to 32 WORDS) has been loaded. TIMING a. In response to an I/0 load OUTPUT buffer: 16.5 to 33 µsec.* b. In response to an I/0 load RAM from INPUT buffer: 16.5 to 33 µsec for 32 WORDS*, for SHORTER LOAD OPERATIONS SUBTRACT 0.5 µsec per (16 bit) word, i.e., 17 µsec to 0.5 µsec for single word. *NOTE: In the unusual case where a superceding transmit command on the redundant bus occurs at the returned status time for a valid 32 word receive, simultaneously with an I/0 transfer request, the DONE interrupt may be delayed for an additional 16.5 usec.
$\overline{\text{BUFF EF}}$	This flag may be used to speed up read data operation in response to an I/0 load OUTPUT FIFO buffer command. The $\overline{\text{BUFF EF}}$ flag will go high when the first word is loaded into the OUTPUT FIFO buffer. The word may be read at that time. Please see Figure 6.
$\overline{\text{MODERESET}}$	Indicates reception of a valid RESET mode command.

Table 6 – Discrete Interrupts Summary

Name	Use
$\overline{\text{VECTOR}}$	Indicates that a transmit VECTOR mode command has been received. VECTOR DATA is transmitted from VW/CMD WD #2/AMD Register.
$\overline{\text{DBCREQ}}$	Indicates acceptance of DYNAMIC BUS CONTROL COMMAND REQUEST Note: RTU will not accept valid DBC mode command unless DBCACC bit is set low in the OPERATION Register.
$\overline{\text{RETRY}}$	Indicates that an error has occurred in the data transfer and that a retry will be performed if the retry option is selected. If all retries that were selected fail, INVALID TRANSFER INTERRUPT would be asserted on the final failure.
$\overline{\text{SELF TEST}}$	Indicates that the INITIATE SELF TEST mode command is being serviced.
$\overline{\text{PASS}}$	Active low pulse output signal which indicates that a sub-system initiated self-test (on-or off-line) operation has been sucessfully completed. This interrupt will be issued approximately 90µs after the self-test operation has been triggered.

Table 6 – Discrete Interrupts Summary (continued)

Bit	Name	Function
0-4	SA BITS	SUBADDRESS BITS Define SUBADDRESS MESSAGE BLOCK in INTERNAL RAM. BIT SUBADDRESS BIT 0 SA0 (LSB) 1 SAI 2 SA2 3 SA3 4 SA4 (MSB) These bits correspond directly to 1553B definition in the command word. Although SUBADDRESSES 00000_B and 11111_B are illegal in 1553B, message blocks specified by them are both READABLE and WRITABLE by the SUBSYSTEM. They are not accessible from the 1553B BUS.
5	T/$\overline{\text{R}}$ BIT	TRANSMIT/RECEIVE BIT points INPUT/OUTPUT OPERATIONS to either the TRANSMIT SECTION or RECEIVE SECTION of the INTERNAL RAM.
6	I/$\overline{\text{O}}$	INPUT/OUTPUT BIT DEFINES DIRECTION OF DATA TRANSFER 1. SET HIGH: INPUT OPERATION An EXECUTE operation will transfer the Data currently loaded in the input FIFO buffer to the specified message block (SUBADDRESS) in the internal RAM. Between 1 and 32 data words must be loaded in the input FIFO buffer when using an EXECUTE command with this bit set. 2. SET LOW: OUTPUT OPERATION EXECUTE operation will transfer a complete block of data (32 words) to the output FIFO buffer from the specified subaddress of internal RAM.

Table 7 – Operational Register

<table>
<tr><th>Bit</th><th>Name</th><th>Function</th></tr>
<tr><td>7</td><td>BUSY BIT</td><td>RTU BUSY
HIGH- BUSY
LOW - NOT BUSY
MASTER RESET SETS BIT HIGH</td></tr>
<tr><td>8</td><td>RT/$\overline{BC}$</td><td>Remote Terminal/Bus Controller Bit. This line, when set HIGH, causes the hybrid to function as a Remote Terminal. When set LOW, it will function as a Bus Controller. Master Reset sets this bit HIGH</td></tr>
<tr><td>9</td><td>Transaction/
$\overline{Test}$</td><td>Transaction/Test Mode Bit. When this bit is set high, normal transactions will be handled, eg., BC to RT, RT to BC, RT to RT. If this bit is set low and a trigger transaction is issued, the self-test will be performed for the MIL-STD-1553 protocol chip.</td></tr>
<tr><td>10</td><td>$\overline{LT\ Local}$</td><td>Loop Test Local Bit (Used in conjunction with BIT 9). This signal selects the self test path. When set LOW, the internal digital path is selected. When set HIGH, the external path, including transceivers, is selected.</td></tr>
<tr><td>11</td><td>Bus Select</td><td>Bus Select (Bus Controller Only). When set high, Bus 1 is selected. When set LOW, Bus 0 is selected.</td></tr>
<tr><td>12</td><td>Normal/$\overline{RT\text{-}RT}$</td><td>Normal/Remote Terminal-Remote Terminal Bit. When set HIGH, BC to RT and RT to BC transfers are performed. When set LOW RT to RT transfers are performed. Two command words are required and two returned status words will be expected.</td></tr>
<tr><td>13</td><td>$\overline{SERV\ REQ}$/
Auto-Retry
(LSB)</td><td>Service Request/Auto-Retry (LSB) Bit.
RT MODE: A LOW in this bit will cause the service request bit in the status word to be set.
BC MODE: This is the LSB of the Auto-Retry options. See table on this page, Bit 14</td></tr>
<tr><td>14</td><td>$\overline{SERR}$
Auto-Retry
(MSB)</td><td>Subsystem Error/Auto-Retry (MSB) Bit.
RT MODE: A LOW in this bit will cause a Subsystem Error Bit in the status word to be set.
BC MODE: This is the MSB of the Auto-Retry option
<table>
<tr><th colspan="4">AUTO-RETRY OPERATIONS</th></tr>
<tr><th colspan="2">Options selected:</th><th colspan="2">Auto-Retry Other Bus Bit 15</th></tr>
<tr><th>Bit 14</th><th>Bit 13</th><th>0</th><th>1</th></tr>
<tr><td>0</td><td>0</td><td>No Retry</td><td>No Retry</td></tr>
<tr><td>0</td><td>1</td><td>P</td><td>S</td></tr>
<tr><td>1</td><td>0</td><td>P/P</td><td>P/S</td></tr>
<tr><td>1</td><td>1</td><td>P/P/P</td><td>P/S/S</td></tr>
</table></td></tr>
<tr><td>15</td><td>$\overline{DBCACC}$/
Auto-Retry
Other Bus</td><td>Dynamic Bus Control Accept/Auto-Retry Bus Bit.
RT MODE: This bit should be LOW if the subsystem is able to accept control of the bus, if offered.
BC MODE: This bit should be HIGH if an invalid transfer is to be retried according to the selected auto-retry option listed above.</td></tr>
</table>

Table 7 – Operational Register (continued)

Operation	Function
RESET	RESET INPUT/OUTPUT BUFFERS This command clears both the input and output FIFO buffers. The $\overline{\text{BUFF EF}}$ flag will go low indicating the output buffer is empty.
READ OUTPUT DATA BUFFER	READ OUTPUT FIFO READS the data moved from the INTERNAL RAM in response to an UNLOAD execute operation. The order of the data words corresponds to the same order that they would be received on the 1553B bus. That is the first data word read is the first data word following the COMMAND word. In the 8 bit mode the HIGH BYTE is read FIRST.
WRITE OUTPUT DATA BUFFER	WRITE INPUT FIFO WRITES the data that will be moved into the INTERNAL RAM in response to a LOAD execute operation. The order of the data words corresponds to the same order that they would be transmitted on the 1553B bus. That is the first data word written is the first data word transmitted following the status word. In 8 bit mode the HIGH BYTE is written FIRST.
EXECUTE OP	EXECUTES OPERATION SPECIFIED IN OPERATION REGISTER 1. I/O BIT HIGH Data currently in INPUT FIFO BUFFER is loaded into the INTERNAL RAM block specified by the T/$\overline{\text{R}}$ BIT and SUBADDRESS FIELD of the OPERATION REGISTER. The INPUT BUFFER must have at least one data word. The DONE interrupt is pulsed when the operation is completed. 2. I/O BIT LOW An entire block of data (32 words) specified by the T/R and the SUBADDRESS field of the OPERATION REGISTER is unloaded from the INTERNAL RAM into the OUTPUT FIFO BUFFER. The $\overline{\text{BUFF EF}}$ Flag goes high when the first data word is moved into the OUTPUT BUFFER. The DONE interrupt is pulsed when the complete message has been moved.
EXECUTE OP WITH RPT OPTION	EXECUTES OPERATION SPECIFIED IN OPERATION REGISTER WITH REPEAT OPTION 1. I/O BIT HIGH Data previously written into the INPUT BUFFER is loaded into a new INTERNAL RAM block specified by the T/R and SUBADDRESS field of the OPERATION REGISTER. This operation allows a block of data loaded in the INPUT BUFFER to be repeatedly copied into multiple subaddresses of the INTERNAL RAM without the subsystem having to reload the data. The DONE interrupt is pulsed when the operation is completed. The intent of the operation is to minimize the time required to initialize the INTERNAL RAM. 2. I/O BIT LOW Operation identical to EXECUTE OP. WITHOUT RPT option.
TRIGGER TRANSACTION TRIGGER TEST	TRANSACTION/TEST TRIGGER This signal executes the desired Bus Controller Function or test of the protocol section determined by the Operation Register.

Table 8 – Non-Register Operational Commands

Operation	$\overline{RD}$	$\overline{WT}$	$\overline{DS}$	AD3	AD2	AD1	AD0
BC AND RT MODE							
No Operation-I/O Bus Tri-stated	x	x	1	x	x	x	x
Read Operation Reg. High Byte	*P	1	0	0	0	0	1
Read Operation Reg. Low Byte	P	1	0	0	0	0	0
Write Operation Reg. High Byte	1	P	0	0	0	0	1
Write Operation Reg. Low Byte	1	P	0	0	0	0	0
Read Output FIFO (High Byte First)	P	1	0	1	1	1	0
Write Input FIFO (High Byte First)	1	P	0	1	1	1	0
Execute Operation (Load/Unload RAM)	1	P	0	1	0	0	0
Execute Operation with Repeat	1	P	0	1	0	1	0
Reset Input FIFO	1	P	0	1	0	1	1
Reset Output FIFO	1	P	0	1	1	0	1
Reset Input and Output FIFOS	1	P	0	1	1	0	0
RT MODE ONLY							
Read RT Command Word Reg. High Byte	P	1	0	0	1	0	1
Read RT Command Word Reg. LowByte	P	1	0	0	1	0	0
Read Receive Command Reg. High Byte	P	1	0	0	0	1	1
Read Receive Command Reg. LowByte	P	1	0	0	0	1	0
Read SYNC Data Reg. High Byte	P	1	0	0	1	1	1
Read SYNC Data Reg. Low Byte	P	1	0	0	1	1	0
Write Vector Word Reg. High Byte	1	P	0	0	1	1	1
Write Vector Word Reg. Low Byte	1	P	0	0	1	1	0
BC MODE ONLY							
Read Status Word #1 Reg. High Byte	P	1	0	0	0	1	1
Read Status Word #1 Reg. Low Byte	P	1	0	0	0	1	0
Read Status Word #2/RMD Reg. High Byte	P	1	0	0	1	1	1
Read Status Word #2/RMD Reg. Low Byte	P	1	0	0	1	1	0
Write Command Word #1 Reg. High Byte	1	P	0	0	0	1	1
Write Command Word #1 Reg. Low Byte	1	P	0	0	0	1	0
Write Command Word #2/AMD Reg. High Byte	1	P	0	0	1	1	1
Write Command Word #2/AMD Reg. Low Byte	1	P	0	0	1	1	0
Trigger Transaction	1	P	0	1	0	0	1

*P = Active Low Strobe

Note: When operating in 8-bit mode it is recommended that FIFO access be confined to even numbers of Read or Write operations only. Failure to conform to this can result in incorrect data being transferred to internal RAM.

Table 9 – 8-Bit Mode I/O Operations

Operation	$\overline{RD}$	$\overline{WT}$	$\overline{DS}$	AD3	AD2	AD1	AD0
RT AND BC MODE							
No Operation - I/O Bus Tri-Stated	x	x	1	x	x	x	x
Read Operation Register	*P	1	0	0	0	0	0
Write Operation Register	1	P	0	0	0	0	0
Execute Operation (Load/Unload Ram)	1	P	0	1	0	0	0
Execute Operation with Repeat	1	P	0	1	0	1	0
Read Output FIFO	P	1	0	1	1	1	0
Write Input FIFO	1	P	0	1	1	1	0
Reset Input FIFO	1	P	0	1	0	1	1
Reset Output FIFO	1	P	0	1	1	0	1
Reset Input and Output FIFO	1	P	0	1	1	0	0
RT MODE ONLY							
Read RT Command Word Register	P	1	0	0	1	0	0
Read Receive Command Register	P	1	0	0	0	1	0
Read SYNC Data Register	P	1	0	0	1	1	0
Write Vector Word Register	1	P	0	0	1	1	0
BC MODE ONLY							
Read Status Word #1 Register	P	1	0	0	0	1	0
Read Status Word #2/RMD Register	P	1	0	0	1	1	0
Write Command Word #1 Register	1	P	0	0	0	1	0
Write Command Word #2/AMD Register	1	P	0	0	1	1	0
Trigger Transaction	1	P	0	1	0	0	1

*P = Active Low Strobe

Table 10 – 16-Bit Mode I/O Operations

Pin #	Signal Name	Signal Description
16	VDD	Digital Supply Voltage
87	VDD	Digital Supply Voltage
2	GND	Digital Grounds
34	N/C / $\overline{\text{SERR}}$	N/C - ACT7005, $\overline{\text{SERR}}$ on ACT7006 - Subsystem Error. When low sets the $\overline{\text{SSF}}$ Bit in the RT's return status word.
80	GND	Digital Grounds
38	VccL (A)	Transceiver A +5VDC Supply Voltage
44	GND (A)	Digital Ground A
43	GND (A)	Analog Ground A
39	N/C	No Connection
41	GND (A)	Transceiver A Output Ground
53	VccL (B)	Transceiver B +5VDC Supply Voltage
47	GND (B)	Digital Ground B
48	GND (B)	Analog Ground B
52	N/C	No Connection
50	GND (B)	Transceiver B Output Ground
81	AD0	Address Inputs AD0 - LSB AD3 - MSB These four signals provide the address codes that control the operation of the interface.
82	AD1	
83	AD2	
84	AD3	
85	A10 IN	A10 IN is the address input to the internal RAM.
86	A10 OUT	A10 OUT buffered TX/$\overline{\text{RX}}$ bit when tied to A10 IN segregates the 2k by 16 RAM into two 1k by 16 blocks of memory: one for Receive, the other for Transmit Data.
23	BCSTEN	Broadcast Enable. When low, the recognition of Broadcast Command is prevented on the specified bus.
25	$\overline{\text{BIT}}$ $\overline{\text{DECODE}}$	Built-In Test Decode. When held low, prevents resetting TXTO Bit, HSFAIL Bit, and LTFAIL Bit in the Bit Word (as well as TF and SSF Bits in the Status Word) upon receipt of a Transmit Bit Word Mode Command.
59	$\overline{\text{BUFF}}$ $\overline{\text{EF}}$	Buffer Empty Flag - goes low when the output FIFO Buffer is empty. Will transition to the high state when the first word appears in the Buffer.

Table 11 – Pin Number Description

Pin #	Signal Name	Signal Description
1	CLOCK	6 MHz Master Clock.
42	DATA CHA	DATA CHANNEL A. (BUS 0). This is the combined signals, RX Data In and TX Data Out, that connect to the IN phase primary terminal of the Bus Transformer.
40	$\overline{\text{DATA CHA}}$	DATA CHANNEL A. (BUS 0) This is the combined signals $\overline{\text{RX Data In}}$ and $\overline{\text{TX Data Out}}$, that connect to the OUT of phase primary terminal of the Bus Transformer.
49	DATA CHB	Same as DATA CHA, except for Channel B. (BUS 1).
51	$\overline{\text{DATA CHB}}$	Same as $\overline{\text{DATA CHA}}$, except for Channel B. (BUS 1).
64	DB0	I/O DATA BUS. Data Bus for all SUBSYSTEM READ and WRITE OPERATIONS. 16 BIT MODE 8 BIT MODE DB0 = LSB DB0/DB8 = LSB DB15 = MSB DB7/DB15 = MSB When used in 8 BIT MODE the data bus must be connected as follows: DB0 TO DB8 DB4 TO DB12 DB1 TO DB9 DB5 TO DB13 DB2 TO DB10 DB6 TO DB14 DB3 TO DB11 DB7 TO DB15
65	DB1	
66	DB2	
67	DB3	
68	DB4	
69	DB5	
70	DB6	
71	DB7	
72	DB8	
73	DB9	
74	DB10	
75	DB11	
76	DB12	
77	DB13	
78	DB14	
79	DB15	
56	$\overline{\text{DBCREQ}}$	Dynamic Bus Control Request. If OPERATION Register bit i5 is set LOW, this line will pulse LOW in response to a Valid Dynamic Bus Control Mode Command, indicating ACCEPTANCE of Bus Control Function.
90	$\overline{\text{DS}}$	Device Select. This signal must be low before the interface can be selected for an I/O Read or Write function. The I/O Data Bus will remain tri-stated, no operations will be executed when this signal is high.
60	$\overline{\text{DONE}}$	Low Pulse Indicates an I/O Operation has completed

Table 11 – Pin Number Description (continued)

Pin #	Signal Name	Signal Description
24	$\overline{\text{ENABLE}}$	Enable. When held low, enables Bit Decode, Next Status, and Status Update program lines.
62	$\overline{\text{INT \#I}}$	Good Block (RT) / VALID TRANSFER (BC)
63	$\overline{\text{INT \#2}}$	VALID Transmit (RT) / INVALID TRANSFER (BC)
33	$\overline{\text{LTFAIL}}$	Loop Test Fail. This line goes low if any error in the terminals own transmitted waveform is detected or if any parity error in the hardwired RT address is detected.
3	$\overline{\text{MEREQ}}$	Message Error Request. To set the Message Error bit in the Status Word, this signal must go low within 650 nsec of $\overline{\text{INCMD}}$ going low and remain valid for the DURATION of $\overline{\text{INCMD}}$.
57	$\overline{\text{MODEREST}}$	Mode Reset. This line pulses low for 500 ns on completion of the servicing of a valid Reset Remote Terminal Mode Command.
28	M16/$\overline{8}$	Programs Interface for 8 Bit or 16 Bit Data Buses. 16/$\overline{8}$ = LOW (0) 8 BIT MODE 16/8 = HIGH (1) 16 BIT MODE
55	$\overline{\text{NBGT}}$	New Bus Grant. Pulses low whenever a new command is accepted.
26	$\overline{\text{NEXT STATUS}}$	Next Status. When held low, causes TF or SSF to appear in very next Status Word after fault occurrence (except for Transmit Status or Transmit Last Command).
58	$\overline{\text{PASS}}$	Pass. Interrupt indicates that the protocol self-test has completed with no faults.
88	$\overline{\text{RD}}$	Read Strobe. Must GO LOW together with $\overline{\text{DS}}$ to perform a READ OPERATION. Note: $\overline{\text{WT}}$ STROBE MUST BE HIGH.
61	$\overline{\text{RETRY}}$	Retry Interrupt
31	$\overline{\text{RESET}}$	System MASTER Reset. When low resets all registers and INPUT/OUTPUT FIFO buffers. Minimum Low Time for reset 0.5 µsec.
17	RTADPAR	RT Address Parity. This must be hardwired by the user to give odd parity.
22	RTAD0	RT Address Lines. These should be hardwired by the user. RTAD4 is the most significant bit.
21	RTAD1	
20	RTAD2	
19	RTAD3	
18	RTAD4	

Table 11 – Pin Number Description (continued)

Pin #	Signal Name	Signal Description
32	RTADER	Remote Terminal Address Error. This line goes low if an error is detected in the RT address parity of the selected receiver. Any receiver detecting an error in the RT address will turn itself off.
11	SA0	Subaddress. These five lines are a label for the data being transferred. Valid when INCMD is low. SA4 is the most significant bit.
13	SA1	
15	SA2	
14	SA3	
12	SA4	
54	SELFTEST	Self Test Interrupt indicates that the Initiate Self Test Mode Command is being served.
27	STATUSUPDATE	Status Update. When held low, causes TF or SSF to appear in Status Word response to Transmit Status or Transmit Last Command issued immediately after fault occurrence.
36	SYNCND	Synchronize No Data Interrupt
37	SYNCWD	Synchronize with Data Interrupt
29	TEST #I	Test #1 Factory Test Point (Do not connect).
30	TEST #2	Test #2 Factory Test Point (Do not connect).
8	TX/RX	Transmit/Receive. The state of this line informs the subsystem whether it is to transmit or receive data. The signal is valid while INCMD is low.
35	VECTOR	Vector Interrupt
4	WC0	Word Count. These Five lines specify the requested number of Data Words to be received or transmitted. Valid when INCMD is low. WC4 is the most significant bit.
5	WC1	
7	WC2	
9	WC3	
10	WC4	
89	WT	Write Strobe. Must GO LOW together with DS to perform a write operation. NOTE: RD must be high.
6	INCMD	IN COMMAND. Goes low when the interface is servicing a valid command. Can be utilized to enable external firm-ware to illegalize subaddresses and mode command not allowed by

Table 11 – Pin Number Description (continued)

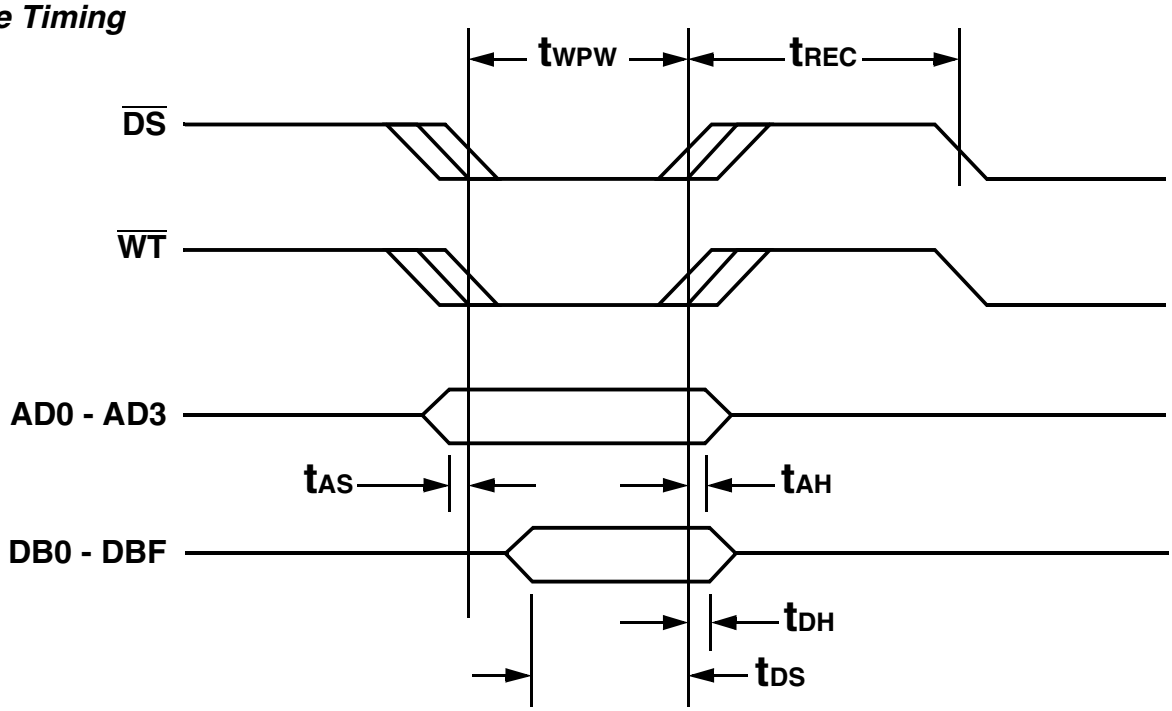
Symbol	Parameter	Min	Typ	Max	Units	Notes
t_{WPW}	Write Pulse Width	50			nsec	1, 2
t_{RPW}	Read Pulse Width	50			nsec	3
t_{AS}	Address Set Up Time	15			nsec	
t_{AH}	Address Hold Time	15			nsec	
t_{DS}	Write Data Set Up Time	15			nsec	
t_{DH}	Write Data Hold Time	0			nsec	2
t_{DA}	Read Data Access Time			50	nsec	
t_{IPW}	Interrupt Pulse Width	140	160	180	nsec	4
t_{REC}	Recovery Time	100			nsec	

Conditions: ($-55°C \leq T_A \leq +125°C$) $V_{CC} = +5.0V \pm 10\%$

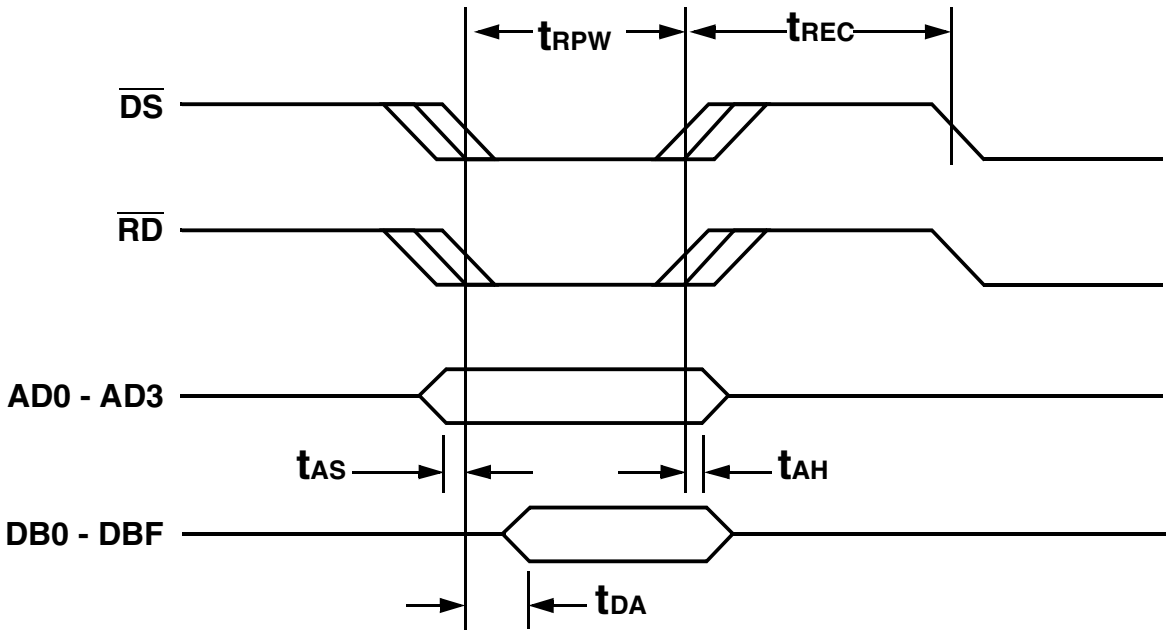
Notes:
1. Write pulse width t_{WPW} is the time when both $\overline{DS}$ and $\overline{WT}$ are simultaneously low. Either $\overline{DS}$ or $\overline{WT}$ may go low or return high first.
2. Write hold time:
   $t_{DH} = 0$ for $t_{WPW} \geq 450$nsec
   $t_{DH} = 10$nsec for $50\text{nsec} < t_{WPW} < 450\text{nsec}$
3. Read pulse time t_{RPW} is the time where both $\overline{DS}$ and $\overline{RD}$ are simultaneously low. Either $\overline{DS}$ or $\overline{RD}$ may go low or return high first.
4. Refer to “Discrete Interrupt” text for further information.

Table 12 – AC Electrical Characteristics

I/O Write Timing



I/O Read Timing



Output Interrupts

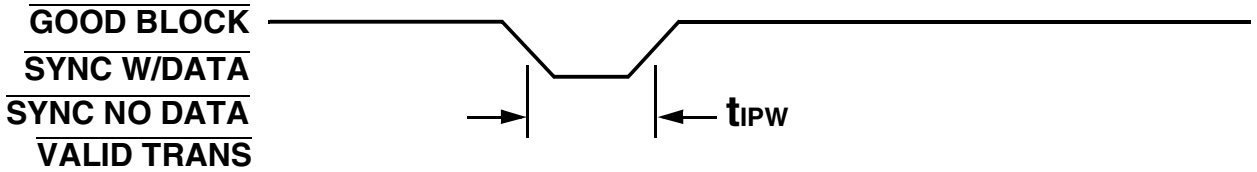


Figure 4 – Subsystem Interface Timing

Signal Name	Function
A0 - A3	INPUT ADDRESS A0 = LSB A3 = MSB These four signals provide the address codes that control the operation of the interface.
$\overline{DS}$	$\overline{DEVICE\ SELECT}$ Used in conjunction with the address signals. The input/output interface data bus will remain tri-stated and no operation will be executed when this signal is high, regardless of the state of the address signals. $\overline{DS}$ = LOW (0) INTERFACE SELECTED $\overline{DS}$ = HIGH (1) INTERFACE NOT SELECTED
DB0-DB15	I/O DATA BUS Data Bus for all SUBSYSTEM READ and WRITE OPERATIONS. **16 BIT MODE** **8 BIT MODE** DB0 = LSB DB0/DB8 = LSB DB15 = MSB DB7/DB15 = MSB When used in 8 BIT MODE the data bus must be connected as follows: DB0 TO DB8 DB4 TO DB12 DB1 TO DB9 DB5 TO DB13 DB2 TO DB10 DB6 TO DB14 DB3 TO DB11 DB7 TO DB15
16/$\overline{8}$	PROGRAMS INTERFACE FOR 8 BIT OR 16 BIT DATA BUSES 16/$\overline{8}$ = LOW (0) 8 BIT MODE 16/$\overline{8}$ = HIGH (1) 16 BIT MODE
$\overline{MASTER\ RESET}$	SYSTEM RESET When low resets all registers and INPUT/OUTPUT buffers. Minimum Low Time for reset = 0.5 µsec.
$\overline{WT}$	WRITE STROBE Must GO LOW together with $\overline{DS}$ to perform a WRITE OPERATION. NOTE: RD MUST BE HIGH.
$\overline{RD}$	READ STROBE Must GO LOW together with $\overline{DS}$ to perform a READ OPERATION. NOTE: WT STROBE MUST BE HIGH.
INTERRUPTS	Refer to DISCRETE INTERRUPT TABLE.

Table 13 – Subsystems Interface Signals

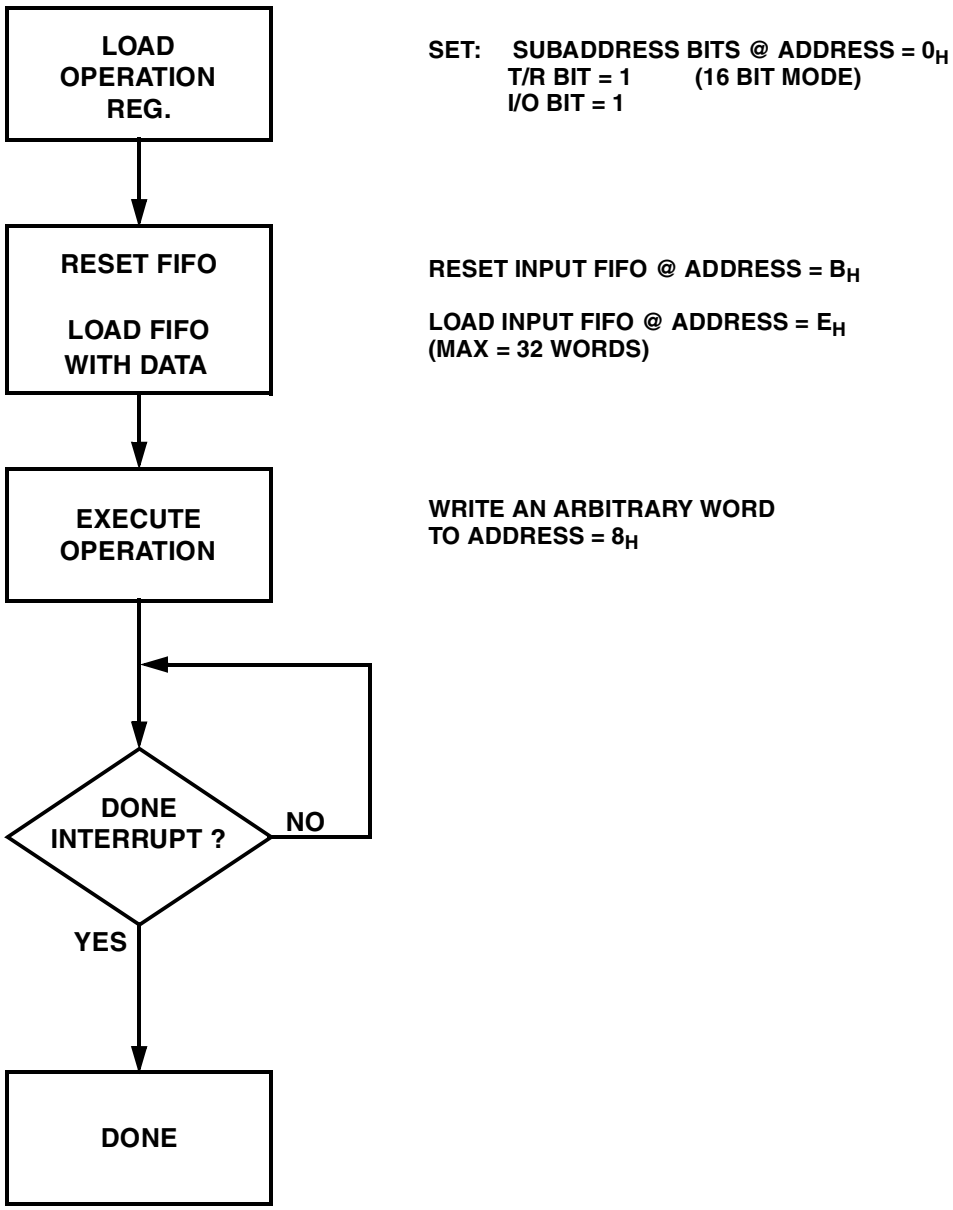
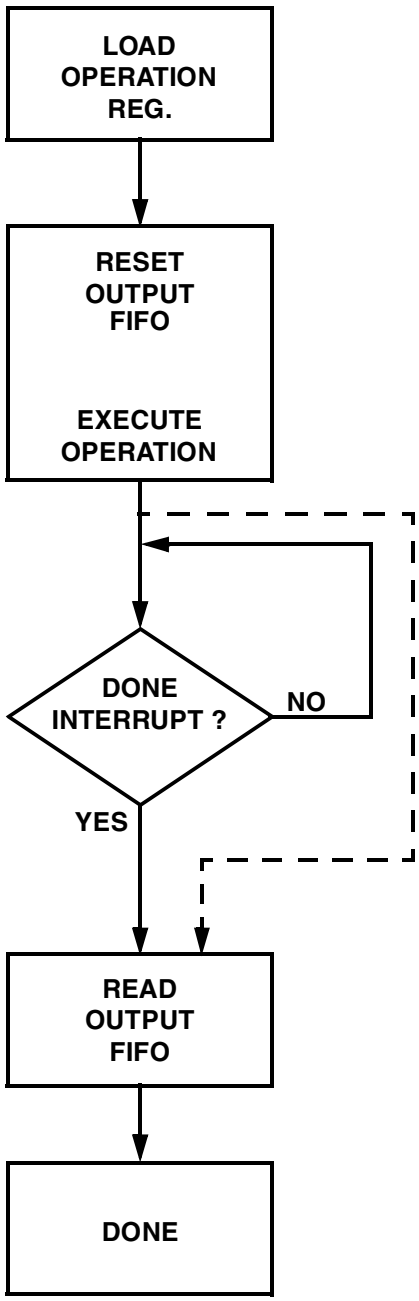


Figure 5 – Flowchart # 1 – Load Data into Transmit RAM



SET: SUBADDRESS BITS @ ADDRESS = 0_H
T/R BIT = 0 (16 BIT MODE)
I/O BIT = 0

RESET OUTPUT FIFO @ ADDRESS = D_H

WRITE AN ARBITRARY WORD TO ADDRESS = 8_H

*FIFO CAN BE READ OUT BEFORE THE DONE INTERRUPT. FIFO READ CAN COMMENCE AS SOON AS THE $\overline{\text{BUFF EF}}$ SIGNAL GOES HIGH. WORDS CAN BE READ AT A MAXIMUM RATE OF 500ns/WORD THEREAFTER.

READ OUTPUT FIFO @ ADDRESS = E_H
(MAX = 32 WORDS)

Figure 6 – Flowchart # 2 - Unload Data from Receive RAM

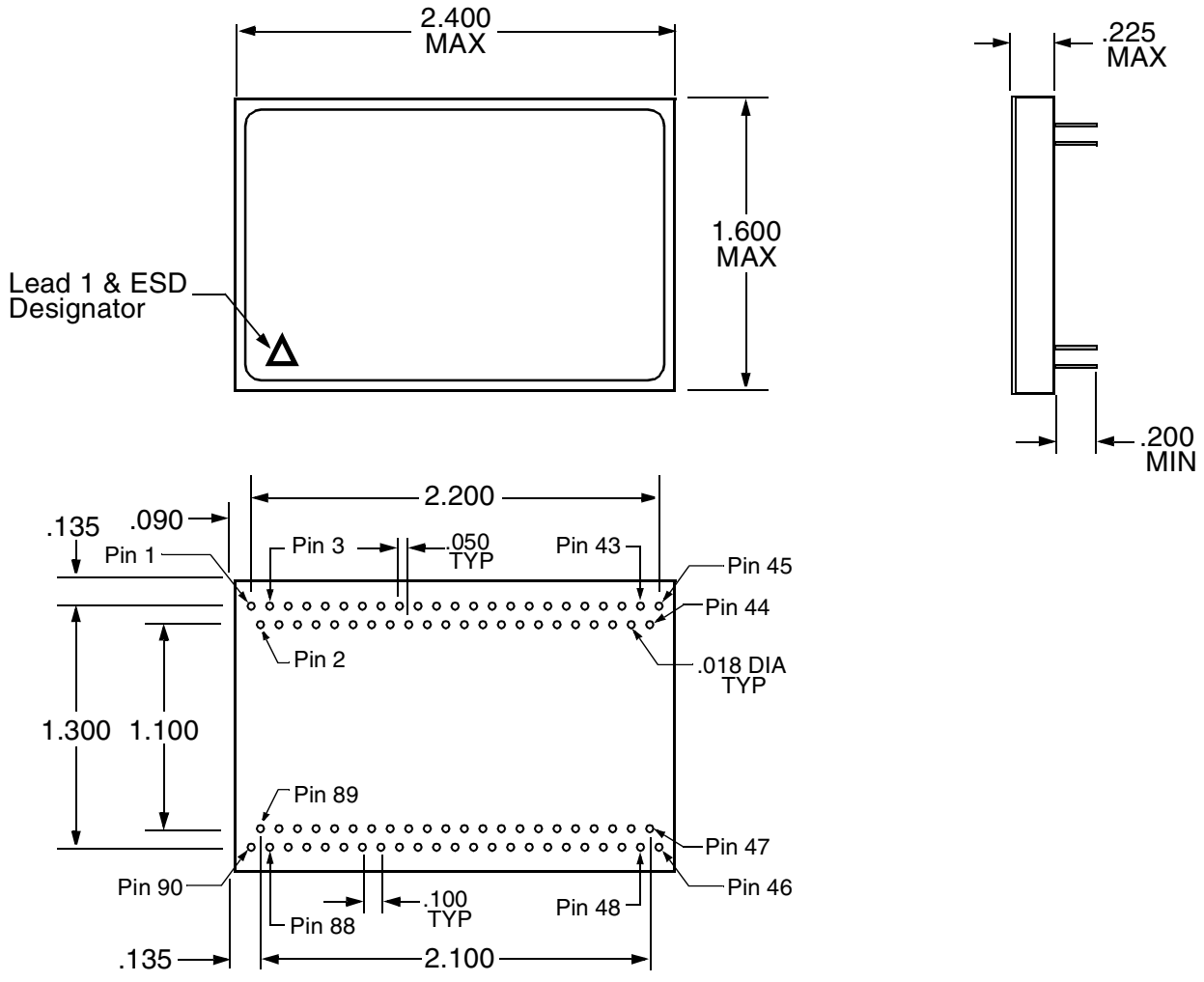
Pin #	Function	Pin #	Function	Pin #	Function
1	6MHZ CLOCK INPUT	31	$\overline{\text{RESET}}$ [MASTER]	61	$\overline{\text{RETRY}}$
2	GND [LOGIC]	32	$\overline{\text{RTADER}}$	62	$\overline{\text{GOODBLK}}$ / $\overline{\text{VALIDTXFR}}$
3	$\overline{\text{MEREQ}}$	33	$\overline{\text{LTFAIL}}$	63	$\overline{\text{VALIDXMIT}}$ / $\overline{\text{INVLDTXFR}}$
4	WC0	34	N/C - ACT7005 / $\overline{\text{SERR}}$ - ACT7006	64	DB0
5	WC1	35	$\overline{\text{VECTOR}}$	65	DB1
6	$\overline{\text{INCMD}}$	36	$\overline{\text{SYNCND}}$	66	DB2
7	WC2	37	$\overline{\text{SYNCWD}}$	67	DB3
8	T/$\overline{\text{R}}$	38	V_{CC}L (A) [TX/RX / LOGIC]	68	DB4
9	WC3	39	N/C	69	DB5
10	WC4	40	$\overline{\text{DATA CH A}}$	70	DB6
11	SA0	41	OUTPUT GND A	71	DB7
12	SA4	42	DATA CH A	72	DB8
13	SA1	43	ANALOG GND A	73	DB9
14	SA3	44	DIGITAL GND A	74	DB10
15	SA2	45	N/C	75	DB11
16	+5V [V_{DD}]	46	N/C	76	DB12
17	RTADPAR	47	DIGITAL GND B	77	DB13
18	RTAD4	48	ANALOG GND B	78	DB14
19	RTAD3	49	DATA CH B	79	DB15
20	RTAD2	50	OUTPUT GND B	80	GND [LOGIC]
21	RTAD1	51	$\overline{\text{DATA CH B}}$	81	AD0
22	RTAD0	52	N/C	82	AD1
23	BCSTEN	53	V_{CC}L (B) [TX/RX / LOGIC]	83	AD2
24	$\overline{\text{ENABLE}}$	54	$\overline{\text{SELF TEST}}$	84	AD3
25	$\overline{\text{BIT DECODE}}$	55	$\overline{\text{NBGT}}$	85	A10 [IN]
26	$\overline{\text{NEXT STATUS}}$	56	$\overline{\text{DBCREQ}}$	86	A10 [OUT]
27	$\overline{\text{STATUS UPDATE}}$	57	$\overline{\text{MODE RESET}}$	87	+5V [V_{DD}]
28	MODE 16/$\overline{\text{8}}$	58	$\overline{\text{PASS}}$	88	$\overline{\text{RD}}$
29	TEST1	59	$\overline{\text{BUFF EF}}$	89	$\overline{\text{WT}}$
30	TEST2	60	$\overline{\text{DONE}}$	90	$\overline{\text{DS}}$

Table 14 – ACT7005 / 7006 DIP Package Pinouts

Ordering Information

Model Number	DESC Part Number	Package
ACT7005	Pending	2.40" x 1.60" Ceramic Plug In
ACT7006	Pending	2.40" x 1.60" Ceramic Plug In

Plug In Package Outline



Specifications subject to change without notice

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