WM8148

12-bit/12MSPS CCD/CIS Analogue Front End/Digitiser

Production Data, April 1999, Rev 4.0

DESCRIPTION

The WM8148 is a 12-bit, 12MSPS analogue front end/ digitiser IC, which interfaces to colour or monochrome linear array CCDs or contact image sensors (CIS). The device includes all the signal conditioning circuitry required to process the analogue signals from the CCD or CIS prior to the internal ADC.

Three signal-processing channels are included in the device. Each channel features reset level clamping, correlated double sampling (CDS), offset correction and programmable gain amplification (PGA). The output signal from each channel is then multiplexed into a high performance 12-bit analogue to digital converter (ADC).

The reset level clamp and/or CDS functions can be selected or bypassed depending on the application.

The WM8148 can be operated in several modes. The operational mode of the device, including the sampling scheme and power management is programmed via the serial/parallel control interface.

Output data is presented in either 12-bit parallel or byte-wide (8+4-bit) format.

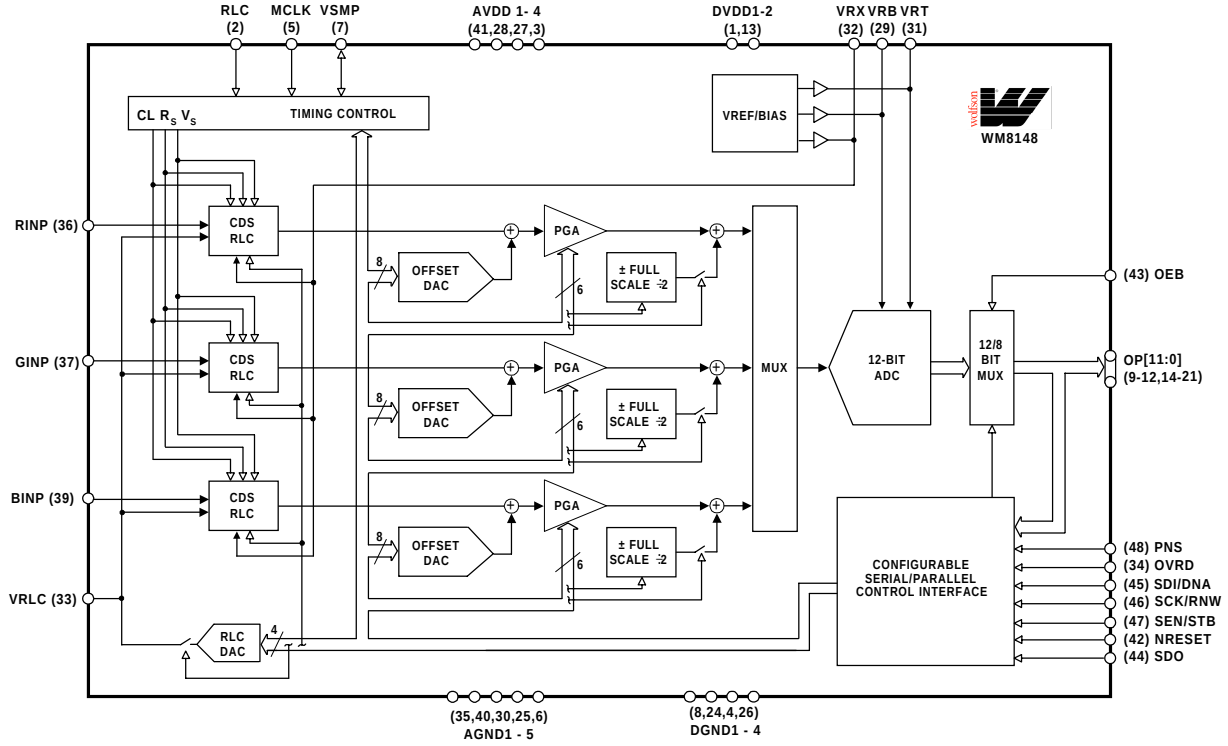
FEATURES

- **Correlated double sampling**
- **Programmable gain amplifier**
- **Programmable input clamp voltage**
- **Offset correction**
- **12-bit, 12MSPS ADC**
- **Internal voltage reference**
- **12-bit or 8+4 bit data output mode**
- **Single 5V supply or 5V analogue/3.3V digital supply**
- **Programmable sample timing**
- **Control interface compatible with previous Wolfson AFEs**
- **48-pin TQFP package**

APPLICATIONS

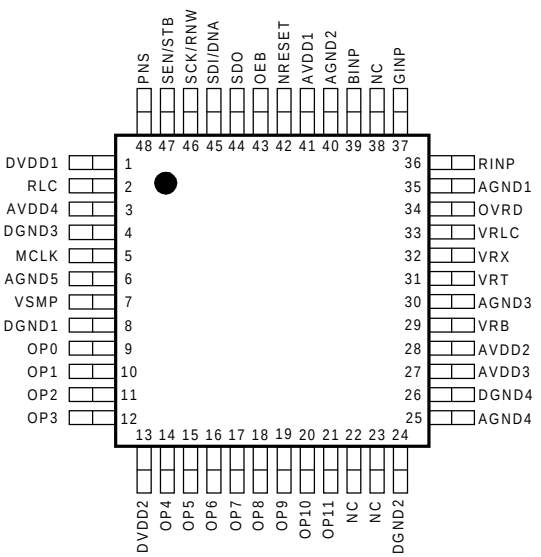
- **Flatbed scanners**
- **Document scanners**
- **Multi-function peripherals (MFPs)**
- **Colour copiers**
- **Character recognition systems**
- **Linear array CCDs**
- **Contact image sensors (CIS)**

BLOCK DIAGRAM



WOLFSON MICROELECTRONICS LTD
Lutton Court, Bernard Terrace, Edinburgh, EH8 9NX, UK
Tel: +44 (0) 131 667 9386
Fax: +44 (0) 131 667 5176
Email: sales@wolfson.co.uk
http://www.wolfson.co.uk

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
XWM8148CFT/V	0 to 70°C	48-pin 1mm thick body TQFP

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DVDD1	Supply	Digital supply (3.3V to 5V) for digital inputs and SDO.
2	RLC	Digital input	Selects whether reset level clamp is applied, active high. If RLC is required on every pixel then this pin can be tied high.
3	AVDD4	Supply	Analogue supply (5V).
4	DGND3	Ground	Digital ground (0V).
5	MCLK	Digital input	Master clock. This clock is applied at N times the input pixel rate (N = 12, 8, 6, or 4 dependent on input sampling mode). MCLK is divided internally by N to generate internal clocks and to provide the clock source for digital logic.
6	AGND5	Ground	Analogue ground (0V).
7	VSMP	Digital IO	Video sample synchronisation pulse. This pin may be either an input (default) or output. Input: This signal is pulsed externally to synchronise the WM8148's video input sample instant and the N-phase internal clock to CCD clocks and interface bus timing. Output: This signal is pulsed internally to flag the video input sample instant, to allow the CCD clocks and interface bus to be synchronised to the WM8148.
8	DGND1	Ground	Digital ground (0V) for output drivers.
9	OP0	Digital output	12-bit signal data output bus. Data is output MSB on OP[11] and LSB on pin OP[0]. See description of pins 14-21 for mode definitions.
10	OP1	Digital output	
11	OP2	Digital output	
12	OP3	Digital output	
13	DVDD2	Supply	Digital supply (3.3V-5V) for Digital IO pins and OP0 to OP3
14	OP4	Digital IO	12-bit bi-directional data bus. On pins OP[4] to OP[11], signal data is output if OEB = 0 and register write data is input if OEB = 1. There are five main modes: • Hi-Z: when OEB = 1 • Output 12-bit: twelve bit signal data output from bus • Output 8-bit muxed: signal data output on OP[11:4] at 2 ∗ ADC conversion rate • Input 8-bit: register write data input on OP[11:4] • Output 8-bit: register readback data output on OP[11:4]
15	OP5	Digital IO	
16	OP6	Digital IO	
17	OP7	Digital IO	
18	OP8	Digital IO	
19	OP9	Digital IO	
20	OP10	Digital IO	
21	OP11	Digital IO	

PIN	NAME	TYPE	DESCRIPTION	
22	NC		No internal connection.	
23	NC		No internal connection.	
24	DGND2	Ground	Digital ground (0V) for output drivers.	
25	AGND4	Ground	Analogue ground (0V).	
26	DGND4	Ground	Digital ground (0V).	
27	AVDD3	Supply	Analogue supply (5V).	
28	AVDD2	Supply	Analogue supply (5V).	
29	VRB	Analogue output	Lower reference voltage. This pin must be connected to AGND and VRT via decoupling capacitors. See Recommended External Components section for details.	
30	AGND3	Ground	Analogue ground (0V).	
31	VRT	Analogue output	Upper reference voltage. This pin must be connected to AGND and VRB via decoupling capacitors. See Recommended External Components section for details.	
32	VRX	Analogue output	Input return bias voltage. This pin must be connected to AGND via decoupling capacitors. See Recommended External Components section for details.	
33	VRLC	Analogue IO	Selectable analogue output voltage for RLC or single-ended bias reference. This pin would typically be connected to AGND via a decoupling capacitor. See Recommended External Components section for details. VRLC can be externally driven if programmed Hi-Z.	
34	OVRD	Analogue input	Override pin. Typically tied low externally. The sense of this pin defines the device function on reset. Refer to the description of pin 42 for details.	
35	AGND1	Ground	Analogue ground (0V).	
36	RINP	Analogue input	Red channel input video.	
37	GINP	Analogue input	Green channel input video.	
38	NC		No internal connection.	
39	BINP	Analogue input	Blue channel input video.	
40	AGND2	Ground	Analogue ground (0V).	
41	AVDD1	Supply	Analogue supply (5V).	
42	NRESET	Digital input	Reset input, active low. This signal forces a reset of all internal registers. Registers are set to defaults if pin OVRD is tied low. If pin OVRD is tied high then all registers are set to defaults except EN which is set to 1 and RLCEXT which is set to 0. This will turn on all analogue circuitry including the RLC DAC buffers driving the VRLC pin.	
43	OEB	Digital input	Output enable control, all outputs disabled when OEB = 1. This pin must be externally connected.	
44	SDO	Digital output	Serial Interface: register read-back, VSMP output, setup error flag or over-range flag (depending on control bits SDO [1:0]).	Parallel Interface: Hi-Z, VSMP output, set-up error flag or over-range flag (depending on control bits SDO [1:0]).
45	SDI/DNA	Digital input	Serial interface: serial input data signal.	Parallel interface: High = data, Low = address.
46	SCK/RNW	Digital input	Serial interface: serial clock signal.	Parallel interface: High = OP[11:4] is output bus, Low = OP[11:4] is input bus (Hi-Z).
47	SEN/STB	Digital input	Serial interface: enable pulse, active high.	Parallel interface: strobe, active low.
48	PNS	Digital input	Low = serial interface, High = parallel interface. This pin must be externally connected.	

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

As per JEDEC specifications A112-A and A113-B, this product requires specific storage conditions prior to surface mount assembly and will be supplied in vacuum-sealed moisture barrier bags. It has been classified as having a Moisture Sensitivity Level of 2.

CONDITION	MIN	MAX
Analogue supply voltages: AVDD1 – 4	GND - 0.3V	GND + 7V
Digital supply voltages: DVDD1 – 2	GND - 0.3V	GND + 7V
Digital grounds: DGND1 – 4	GND - 0.3V	GND + 0.3V
Analogue grounds: AGND1 – 5	GND - 0.3V	GND + 0.3V
Digital inputs and SDO	GND - 0.3V	DVDD1 + 0.3V
Digital outputs (not SDO)	GND - 0.3V	DVDD2 + 0.3V
Digital IO pins	GND - 0.3V	DVDD2 + 0.3V
RINP, GINP, BINP	GND - 0.3V	AVDD + 0.3V
Other pins	GND - 0.3V	AVDD + 0.3V
Operating temperature range: T_A	0°C	+70°C
Storage temperature	-50°C	+150°C
Lead temperature (soldering, 10 seconds)		+260°C
Lead temperature (soldering, 2 minutes)		+183°C

Notes:

- GND denotes the voltage of any ground pin. AVDD denotes the voltage applied to any AVDD pin.
- AGND and DGND pins are intended to be operated at the same potential. Differential voltages between these pins will degrade performance.

RECOMMENDED OPERATING CONDITIONS

CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Operating temperature range	T_A	0		70	°C
Digital input and output supply voltages	DVDD1 – 2	2.97	5	5.25	V
Analogue supply voltages	AVDD1 – 4	4.75	5	5.25	V

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS

AVDD = 4.75 to 5.25V, DVDD1 and DVDD2 = 2.97 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 48MHz unless otherwise stated (AVDD denotes the voltage applied to all AVDD pins).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall System Performance Including 12-bit ADC, PGA, Offset and CDS Functions NO MISSING CODES GUARANTEED						
Full-scale input voltage range		Max Gain Gain = 1.0 Min Gain		0.413 3.0 4.13		V V V
Zero-scale transition error		Gain = 1.0		20		mV
Full-scale transition error		Gain = 1.0		20		mV
Differential non-linearity	DNL	Gain = 1.0		0.25	1.00	LSB
Integral non-linearity	INL	Gain = 1.0		1.0		LSB
ANALOGUE SPECIFICATION						
Input Multiplexer						
Channel to channel gain matching				1		%
Input voltage range	V_{IN}		0		AVDD	V
References						
Upper reference voltage	VRT		3.00	3.30	3.60	V
Lower reference voltage	VRB		1.50	1.80	2.10	V
Input return bias voltage	VRX		1.50	1.75	2.00	V
Diff. reference voltage (VRT-VRB)	V_{RTB}		1.30	1.50	1.70	V
Output resistance VRT, VRB, VRX		VRT, VRB, VRX buffers enabled		2		Ω
Resistance VRT to VRB		VRT, VRB buffers disabled	500	800	1100	Ω
VRX Hi-Z leakage current		VRX buffer disabled			1	µA
VRLC/Reset-Level Clamp (RLC)						
RLC switching impedance				75		Ω
VRLC Hi-Z leakage current		VRLC = 0 to AVDD			1	µA
VRLC DAC resolution			4			bits
VRLC DAC step		AVDD = 5V	290	333	370	mV/step
VRLC short-circuit current				5		mA
VRLC output resistance		VRLC = AVDD VRLC = 0V VRLC = other		80 80 5		Ω Ω Ω
Offset DAC						
Resolution			8			bits
Differential non-linearity	DNL		-0.25	0.05	0.25	LSB
Integral non-linearity	INL		-0.50	0.10	0.50	LSB
Output voltage		Code 00(hex) Code FF(hex)		-200 200		mV mV
Programmable Gain Amplifier. Monotonicity Guaranteed						
Resolution			6			bits
Max gain, each channel	G_{MAX}			7.4		V/V
Min gain, each channel	G_{MIN}			0.74		V/V
Gain error, each channel				2	5	%

TEST CONDITIONS

AVDD = 4.75 to 5.25V, DVDD1 and DVDD2 = 2.97 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 48MHz unless otherwise stated (AVDD denotes the voltage applied to all AVDD pins).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL SPECIFICATIONS						
Digital Inputs						
High level input voltage	V_{IH}		0.8 ∗ DVDD1			V
Low level input voltage	V_{IL}				0.2 ∗ DVDD1	V
High level input current	I_{IH}				1	µA
Low level input current	I_{IL}				1	µA
Input capacitance	C_I			5		pF
Digital Outputs						
High level output voltage	V_{OH}	I_{OH} = 1mA, DVDD = DVDD1 or DVDD2	DVDD - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
High impedance output current	I_{OZ}				1	µA
Output rise/fall time		C_{LOAD} = 10pF		3		ns
Digital IO Pins						
Applied high level input voltage	V_{IH}		0.8 ∗ DVDD2			V
Applied low level input voltage	V_{IL}				0.2 ∗ DVDD2	V
High level output voltage	V_{OH}	I_{OH} = 1mA	DVDD2 - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
Low level input current	I_{IL}				1	µA
High level input current	I_{IH}				1	µA
High impedance output current	I_{OZ}				1	µA
Output rise/fall time		C_{LOAD} = 10pF		3		ns
Input capacitance	C_I			5		pF
SUPPLY CURRENTS						
Total supply current – active				75	100	mA
Total analogue supply current – active	I_{AVDD}			73		mA
Total digital supply current – active	I_{DVDD}			2		mA
Supply current – disabled				1	10	µA

INPUT VIDEO SAMPLING (EXTERNAL VSMP)

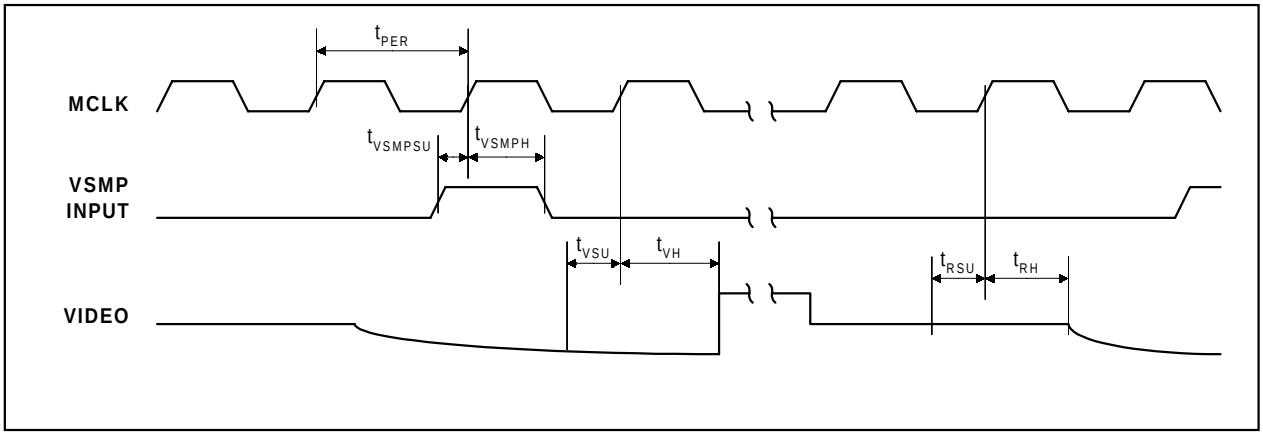


Figure 1 Input Video Timing (External VSMP)

TEST CONDITIONS

AVDD = 4.75 to 5.25V, DVDD1 and DVDD2 = 2.97 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 48MHz unless otherwise stated (AVDD denotes the voltage applied to all AVDD pins).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MCLK period (dependent on mode selected)	t_{PER}		20.8			ns
MCLK duty cycle			45		55	%
VSMP set-up time	t_{VSMPSU}		2			ns
VSMP hold time	t_{VSMPH}		5			ns
Video level set-up time	t_{VSU}		10			ns
Video level hold time	t_{VH}		10			ns
Reset level set-up time	t_{RSU}		10			ns
Reset level hold time	t_{RH}		10			ns

Notes: 1. t_{VSU} and t_{RSU} denote the set-up time required from when the input video signal has settled.

2. The reset sample point may be relative to either the rising or the falling edge of MCLK, depending on the setting of control bits RESREF[3:0].

3. Parameters are measured at 50% of the rising/falling edge.

INPUT VIDEO SAMPLING (INTERNAL VSMP)

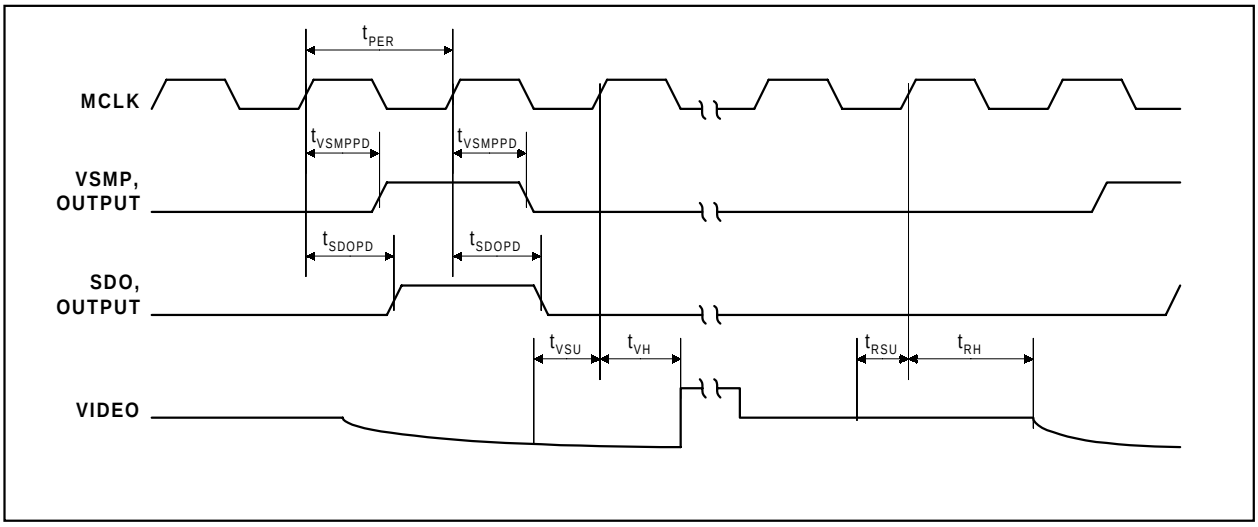


Figure 2 Input Video Timing (Internal VSMP)

TEST CONDITIONS

AVDD = 4.75 to 5.25V, DVDD1 and DVDD2 = 2.97 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 48MHz unless otherwise stated (AVDD denotes the voltage applied to all AVDD pins).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MCLK period	t_{PER}		20.8			ns
MCLK duty cycle			45		55	%
VSMP output propagation delay	t_{VSMPPD}	C_{LOAD} = 10pF		15	25	ns
SDO output propagation delay	t_{SDOPD}	C_{LOAD} = 10pF		20	35	ns
Video level set-up time	t_{VSU}		10			ns
Video level hold time	t_{VH}		10			ns
Reset level set-up time	t_{RSU}		10			ns
Reset level hold time	t_{RH}		10			ns

Notes: 1. t_{VSU} and t_{RSU} denote the set-up time required from when the input video signal has settled.

2. The reset sample point may be relative to either the rising or the falling edge of MCLK, depending on the setting of control bits RESREF[3:0].

3. Parameters are measured at 50% of the rising/falling edge.

RESET LEVEL CLAMP

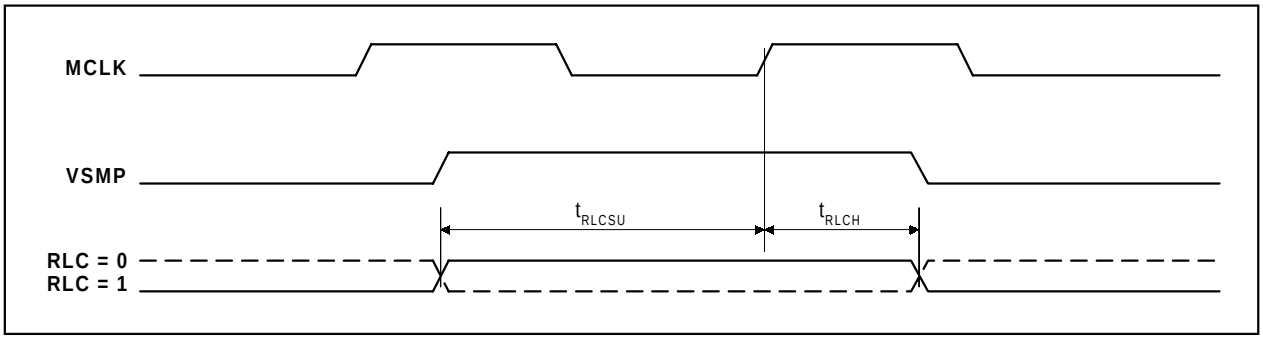


Figure 3 Reset Level Clamp Control Timing

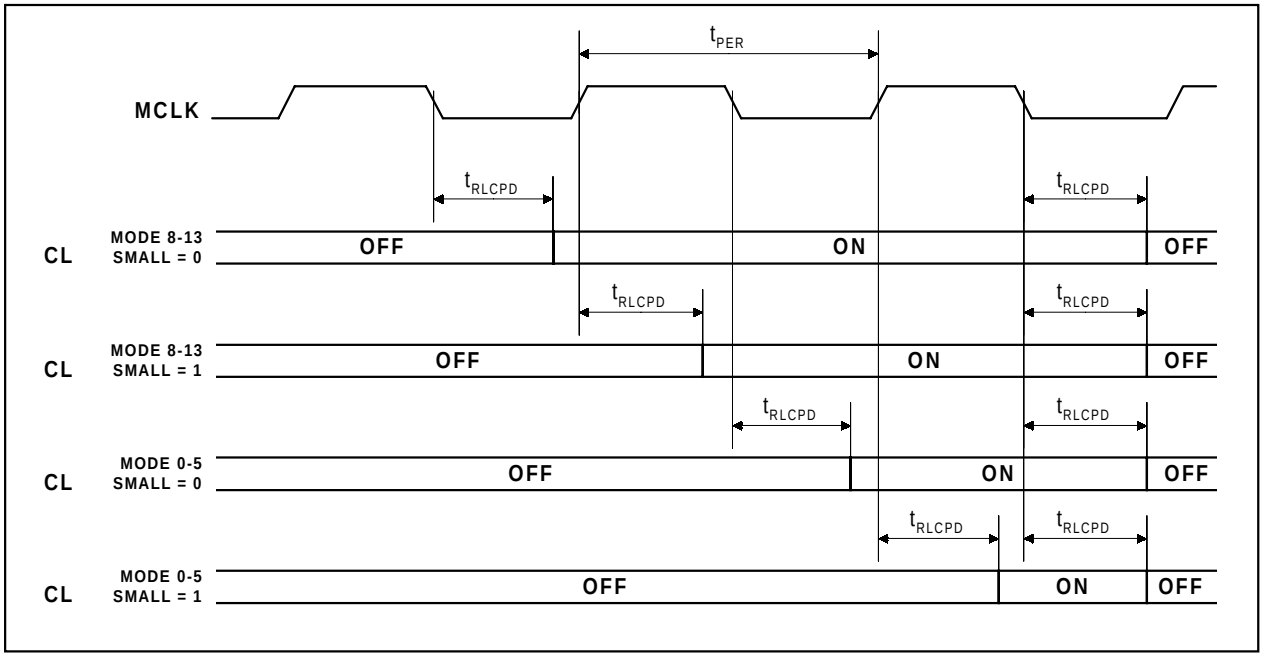


Figure 4 Internal Clamp Signal (CL) Timing

TEST CONDITIONS

AVDD = 4.75 to 5.25V, DVDD1 and DVDD2 = 2.97 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 48MHz unless otherwise stated (AVDD denotes the voltage applied to all AVDD pins).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MCLK period	t_{PER}		20.8			ns
Propagation delay	t_{RLCPD}			15		ns
Set-up time	t_{RLCSU}		10			ns
Hold time	t_{RLCH}		10			ns

Notes: 1. Internal clamp signal (CL) timing may be relative to either the falling or rising edge of MCLK depending on the setting of control bits RESREF[3:0].

2. Parameters are measured at 50% of the rising/falling edge.

OUTPUT DATA

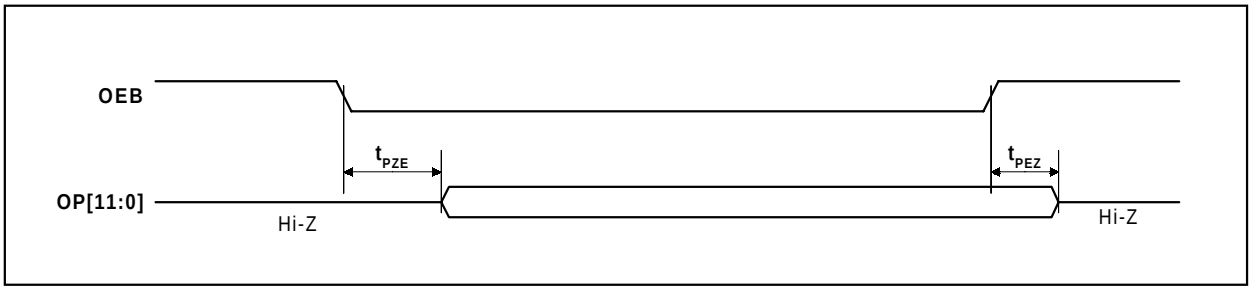


Figure 5 Output Data Enable Timing

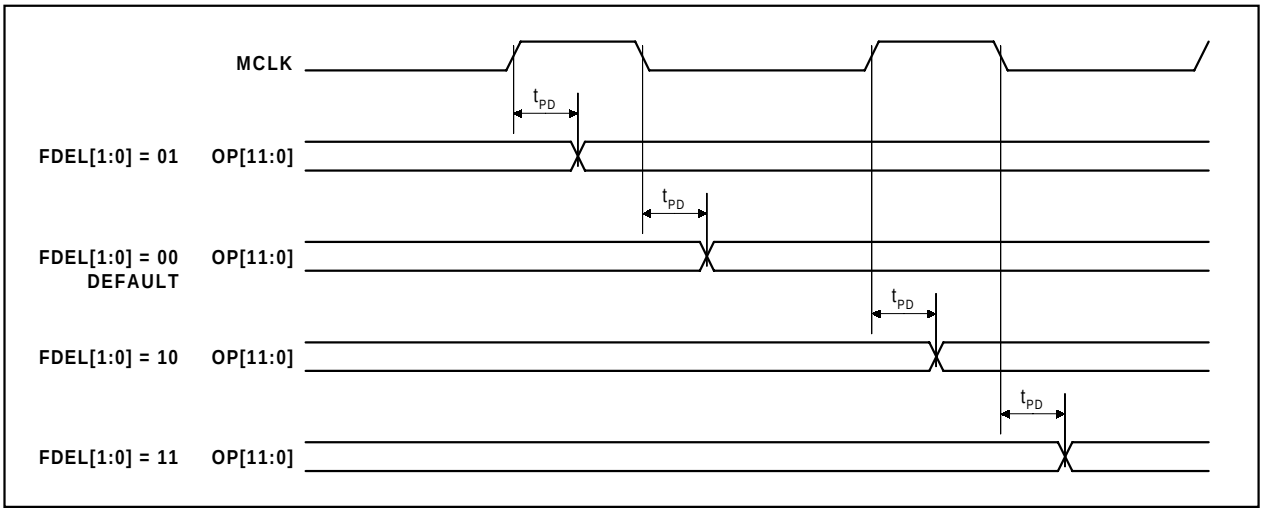


Figure 6 Output Data Timing (Including Fine Latency Control By FDEL[1:0])

TEST CONDITIONS

AVDD = 4.75 to 5.25V, DVDD1 and DVDD2 = 2.97 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 48MHz unless otherwise stated (AVDD denotes the voltage applied to all AVDD pins).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output propagation delay	t_{PD}	I_{OH} = 1mA, I_{OL} = 1mA	10	20	30	ns
Output enable time	t_{PZE}				15	ns
Output disable time	t_{PEZ}				15	ns

Note: Parameters are measured at 50% of the rising/falling edge.

SERIAL INTERFACE

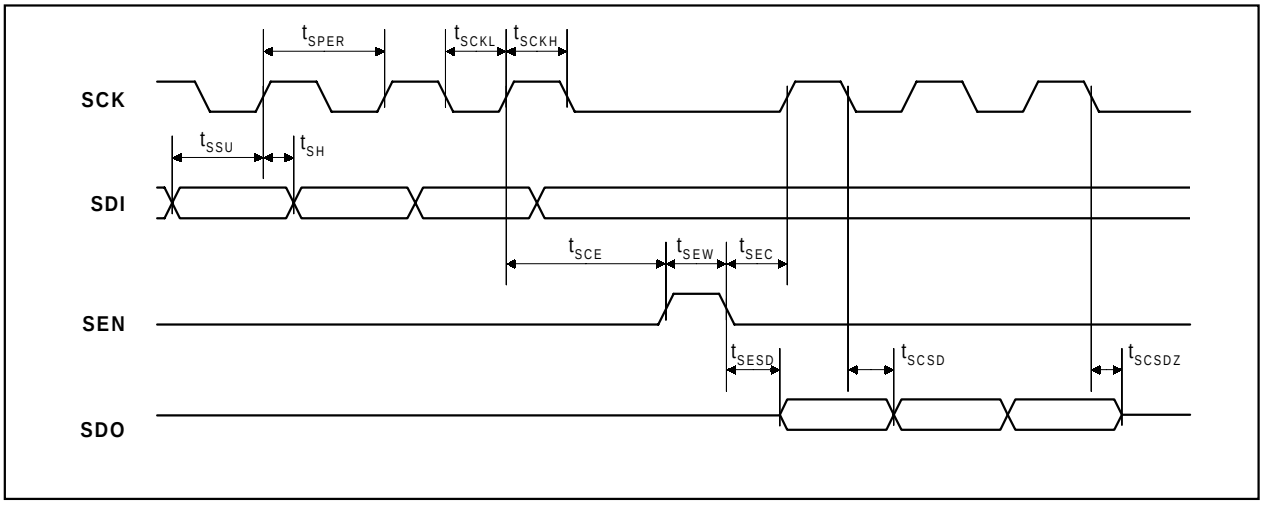


Figure 7 Serial Interface Timing

TEST CONDITIONS

AVDD = 4.75 to 5.25V, DVDD1 and DVDD2 = 2.97 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 48MHz unless otherwise stated (AVDD denotes the voltage applied to all AVDD pins).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SCK period	t_{SPER}		83.3			ns
SCK high	t_{SCKH}		20			ns
SCK low	t_{SCKL}		20			ns
SDI set-up time	t_{SSU}		10			ns
SDI hold time	t_{SH}		10			ns
SCK to SEN set-up time	t_{SCE}		20			ns
SEN to SCK set-up time	t_{SEC}		20			ns
SEN pulse width	t_{SEW}		50			ns
SEN low to SDO out	t_{SESD}				35	ns
SCK low to SDO out	t_{SCSD}				35	ns
SCK low to SDO high impedance	t_{SCSDZ}				25	ns

Note: Parameters are measured at 50% of the rising/falling edge.

PARALLEL INTERFACE

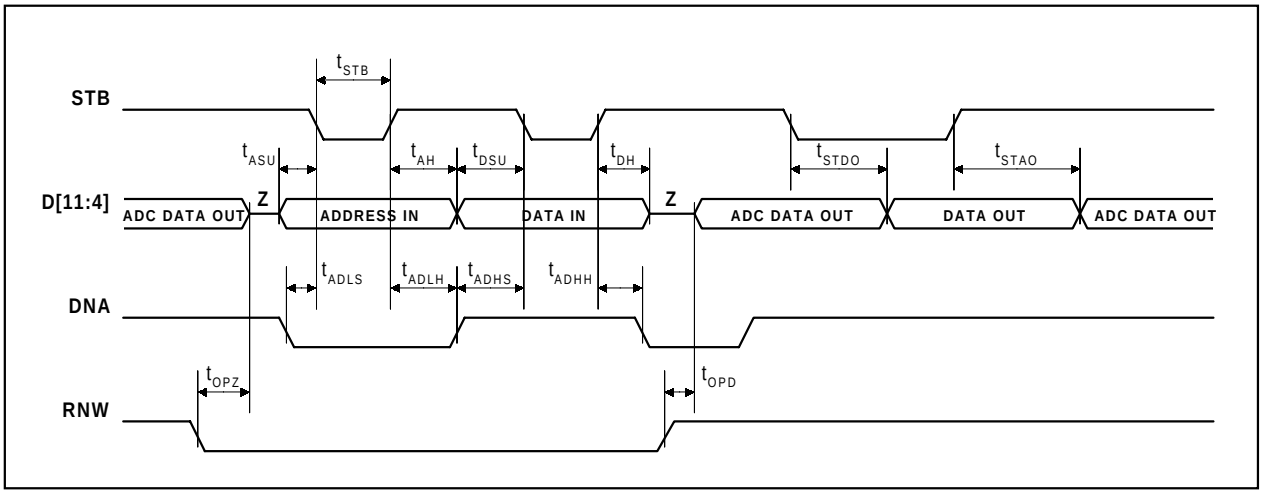


Figure 8 Parallel Interface Timing

TEST CONDITIONS

AVDD = 4.75 to 5.25V, DVDD1 and DVDD2 = 2.97 to 5.25V, AGND = DGND = 0V, T_A = 0 to 70°C, MCLK = 48MHz unless otherwise stated (AVDD denotes the voltage applied to all AVDD pins).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RNW Low to OP[11:4] Hi-Z.	t_{OPZ}				20	ns
Address set-up time to STB Low	t_{ASU}		10			ns
DNA Low set-up time to STB Low	t_{ADLS}		10			ns
Strobe Low time	t_{STB}		50			ns
Address hold time from STB High	t_{AH}		10			ns
DNA Low hold time from STB High	t_{ADLH}		10			ns
Data set-up time to STB Low	t_{DSU}		10			ns
DNA High set-up time to STB Low	t_{ADHS}		10			ns
Data hold time from STB High	t_{DH}		10			ns
Data High hold time from STB High	t_{ADHH}		10			ns
RNW High to OP[11:4] output	t_{OPD}				35	ns
Data output propagation delay from STB Low	t_{STDO}				35	ns
ADC data out propagation delay from STB High	t_{STAO}				35	ns

Note: Parameters are measured at 50% of the rising/falling edge.

TYPICAL OVERALL SYSTEM PERFORMANCE

(INCLUDING CDS, PGA AND ADC BLOCKS)

DNL VS CODES

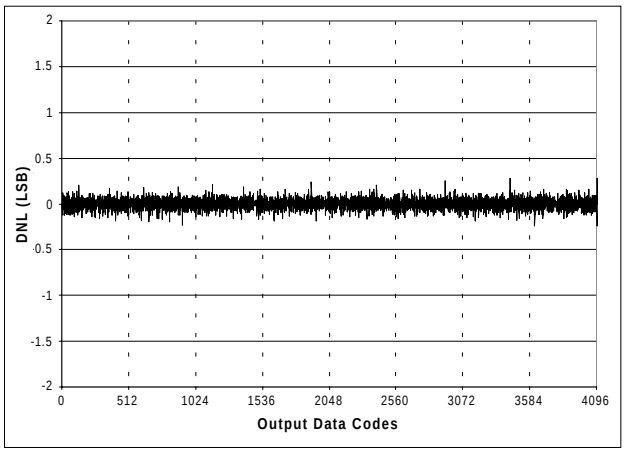


Figure 9 DNL Vs Output Data Codes
(MODE 1, MCLK = 32MHz, AVDD = 5V, DVDD = 3.3V)

INL VS CODES

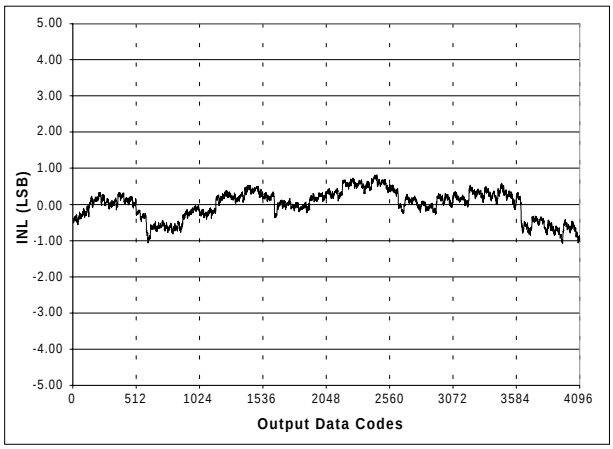


Figure 10 INL Vs Output Data Codes
(MODE 1, MCLK = 32MHz, AVDD = 5V, DVDD = 3.3V)

GROUNDED-INPUT HISTOGRAMS

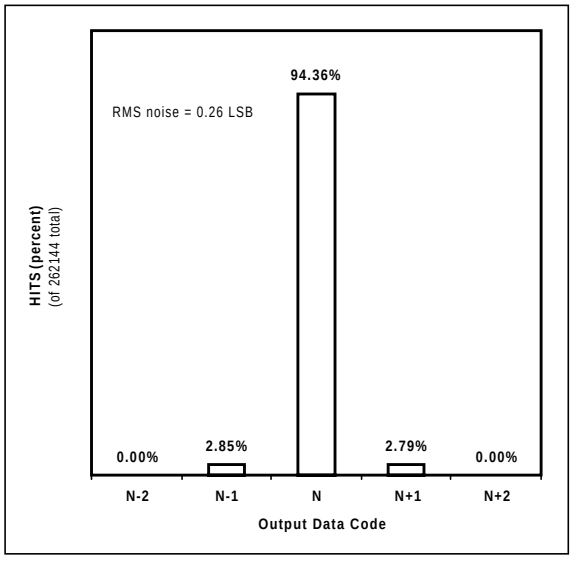


Figure 11 Unity Gain Histogram
(MODE 1, MCLK = 32MHz, GAIN = 1, AVDD = 5V, DVDD = 3.3V)

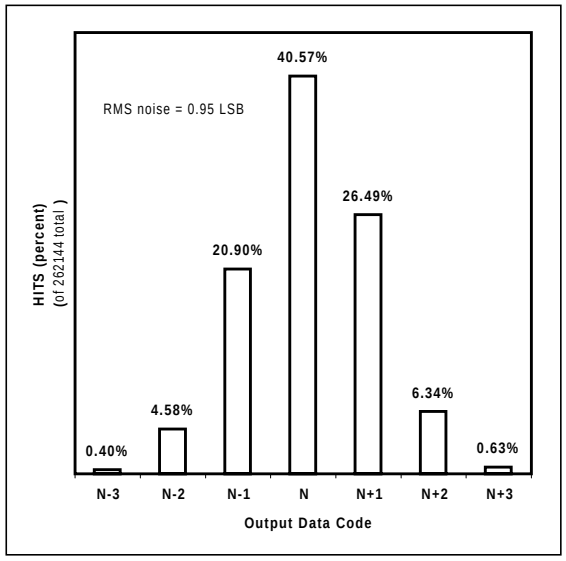


Figure 12 Maximum Gain Histogram
(MODE 1, MCLK = 32MHz, GAIN = 7.4, AVDD = 5V, DVDD = 3.3V)

SYSTEM INFORMATION

Figure 13 shows a system block diagram for a typical application. The CCD image sensor contains three parallel linear arrays of sensor elements (sensitive to Red, Green, and Blue light respectively). The Red, Green and Blue output signals are each applied to the RINP, GINP and BINP channel inputs respectively of the WM8148. Each of these channels provide gain adjust, for compensation of sensor sensitivity and offset adjust for nulling out d.c. offset voltages. The outputs of these three channels are time multiplexed into a single 12-bit resolution ADC. The digital output is then transferred to a digital ASIC or other digital processor. The corrected data can then be compressed if required before being output to a data storage device or a monitor.

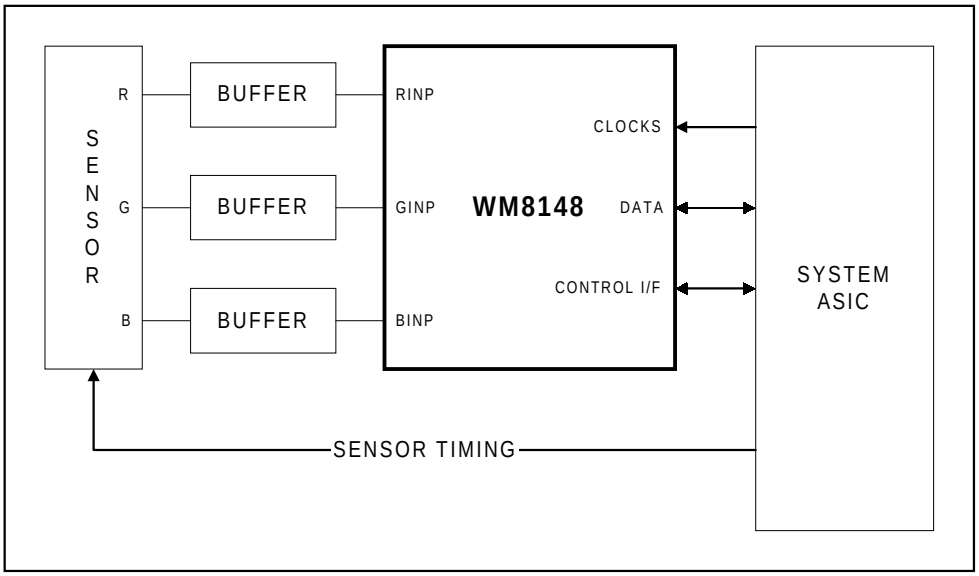


Figure 13 System Diagram

DEVICE DESCRIPTION

INTRODUCTION

The WM8148 samples up to three analogue inputs simultaneously, conditions these signals and converts each resulting analogue signal to a 12-bit digital word.

A block diagram is shown on page 1. Each of the three input channels consists of an Input Sampling block (CDS/RLC), an 8-bit programmable Offset DAC, and a 6-bit Programmable Gain Amplifier (PGA). The outputs from the three channels are multiplexed into a 12-bit ADC. The digital output from the ADC is presented on a 12-bit wide bi-directional bus.

A high-speed (up to 48MHz) master clock, MCLK, and a per-pixel synchronisation pulse, VSMP, drive a shared Timing Control block to generate input sampling signals and other internal clocks. Alternatively the device can operate from MCLK only, outputting VSMP synchronisation pulses to the rest of the system.

An internal reference provides buffered voltages VRT, VRB and VRX. A 4-bit DAC (RLC DAC) provides a programmable buffered voltage at pin VRLC for use as an input signal reference level or an input clamp voltage.

The operation of the device is controlled by internal control registers, which can be read from and written to via a Digital Management Interface (DMI) in either serial or parallel mode.

INPUT SAMPLING

Figure 14 shows the configuration of the Input Sampling Block for the red channel. (The green and blue channels are the same.)

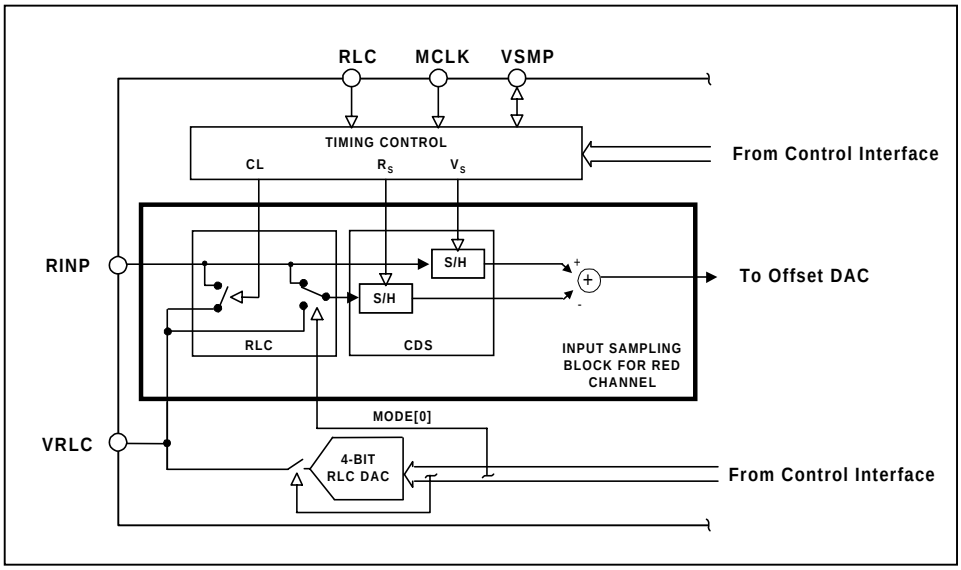


Figure 14 Input Sampling Block – Configuration for Red Channel

This block contains switches to perform Reset Level Clamping (RLC) and Correlated Double Sampling (CDS). Sample/Hold blocks sample the video and reset/reference levels of the input waveform, and pass the difference signal on to the rest of the channel. Internal clocks V_S and R_S define the timing of the sampling of the video signal and the reset/reference level respectively. When enabled by control input pin RLC, internal signal CL clamps the input pin RINP to the voltage on pin VRLC, which is driven either externally or from the 4-bit RLC DAC.

The detailed timing of the internal clock signals CL, V_S, and R_S, with respect to VSMP and MCLK, is controlled by the Timing Control block as programmed via the Digital Management Interface (DMI).

INPUT SAMPLING MODES

To suit different sensors and applications, the WM8148 can sample one, two, or three channels simultaneously, at the rate of the VSMP clock. In each case there are two possible ratios of VSMP frequency to the MCLK master clock frequency, and a choice of whether to use CDS. Table 1 summarises the options available, including the respective maximum sample rates. The mode of operation is set by the Control Register bits MODE[3:0] as shown. Note MODE[0] defines whether or not CDS is activated.

	MAX SAMPLE RATE PER CHANNEL (VSMP)	MCLK/VSMP FREQUENCY RATIO	MAX MCLK FREQENCY	MAX OUTPUT RATE	MODE NUMBER (MODE[3:0])	
	MSPS		MHz	MSPS	CDS	NON-CDS
Three-channel (8-phase)	4	8	32	12	0	1
Three-channel (12-phase)	4	12	48	12	8	9
Two-channel (6-phase)	5.33	6	32	10.66	4	5
Two-channel (8-phase)	6	8	48	12	12	13
One-channel CDS	6.66	6	40	6.66	2	N/A
One-channel non-CDS	10	4	40	10	N/A	3

Table 1 Modes of Operation

If an external VSMP signal is not available, the WM8148 can be configured to output a synchronisation pulse to the system by setting control bit FREE. The internally generated signal is presented on the VSMP and/or SDO pins depending on the settings of the control bits VSMPOP and SDO[1:0].

CORRELATED DOUBLE SAMPLING (CDS)

The input signal can be sampled in two ways: Correlated Double Sampling (CDS), or non-CDS.

CDS operation is summarised in Figure 15. The video signal processed is the difference between the voltage applied at the RINP input when R_S turns off and the voltage at the RINP input when V_S turns off, i.e. the difference between reset and video levels from the same pixel of the input signal. This method of sampling is recommended as it removes common-mode noise.

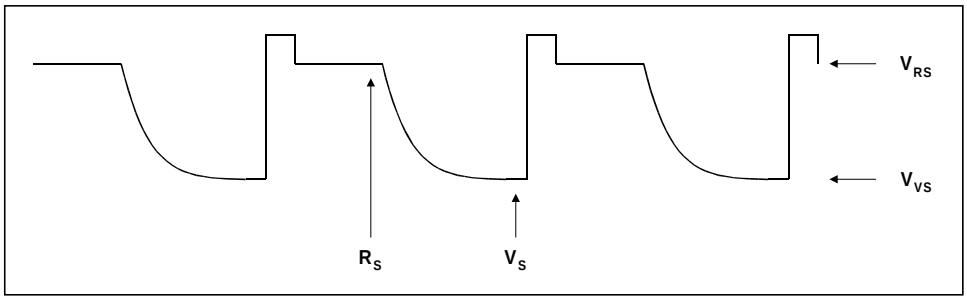


Figure 15 CDS Reset and Video Level Sampling

In non-CDS modes, R_S and V_S occur simultaneously. V_S samples the video signal, while R_S samples the reference level applied to the VRLC pin. The video signal processed is the difference between these samples (V_{RS}-V_{VS}). The voltage (V_{VRLC}), on pin VRLC, may be driven externally or internally by the RLC DAC. In these modes d.c. variations of the input signal are not rejected.

RESET LEVEL CLAMPING (RLC)

If the sensor output voltage is within the input range of the WM8148, the sensor may be d.c. coupled into the WM8148 either directly or via a buffer. If the output from the sensor is outside the input range of the WM8148, the signal has to be connected via a capacitor, C_{IN}, and the d.c. bias conditions must be defined on the WM8148 side of the capacitor (at RINP).

Setting of the d.c. bias conditions is best performed by Reset-Level Clamping, activated by pin RLC. Reset-Level Clamping is compatible with both CDS and non-CDS operating modes. A typical configuration is shown in Figure 16.

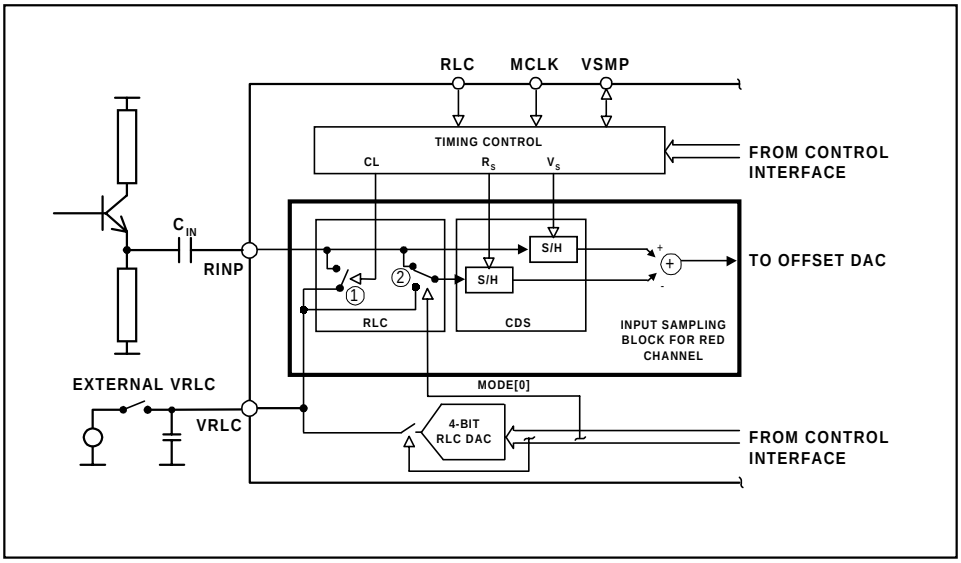


Figure 16 Reset-Level Clamping Circuitry

When the clamp pulse, CL, is active, the voltage on the WM8148 side of C_{IN}, at RINP, will be forced equal to the VRLC voltage, V_{VRLC}, by switch 1. When the CL pulse turns off, the RINP voltage will initially remain at V_{VRLC}, but any subsequent variation in sensor voltage appearing at the sensor side of C_{IN} will couple through C_{IN} to RINP. Switch 2 determines whether the R_S level is taken from the incoming signal (CDS operation) or the VRLC pin (non-CDS operation).

Figure 17 demonstrates the case of a typical CCD waveform, with CL applied during the reset period.

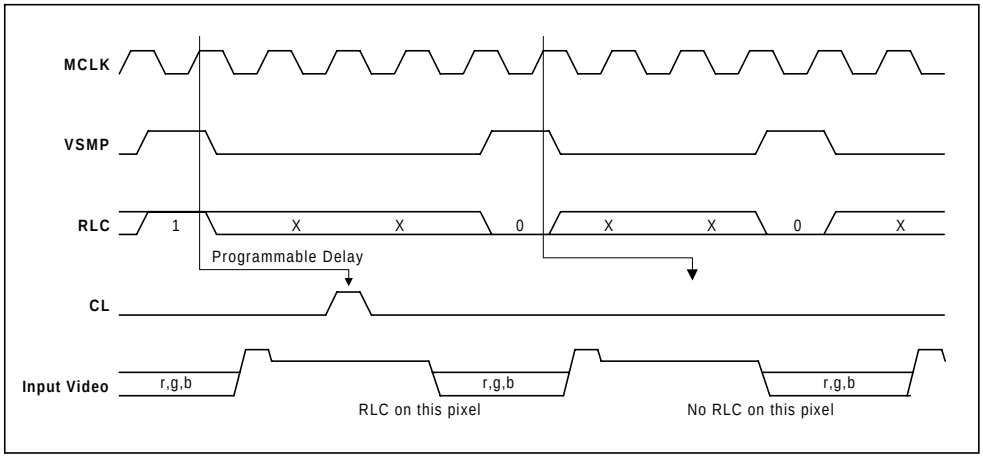


Figure 17 Relationship of RLC pin, MCLK and VSMP to Internal Clamp Pulse, CL

The input signal applied to the RLC pin is sampled on the positive edge of MCLK that occurs during each VSMP pulse. The sampled level, high (or low) controls the presence (or absence) of the internal CL pulse on the next reset level. The position and duration of CL is adjustable by control bits RESREF[3:0] and SMALL.

If pin RLC is tied high then reset level clamping is applied on every pixel. Alternatively, for line-by-line clamping, pin RLC can be driven high at the start of a line (during the dummy black pixel output), then driven low for the remainder of the line. If pin RLC is tied low then reset level clamping will not be applied.

The VRLC voltage, to which the reset level is clamped, can be defined either by an external voltage or internally via the 4-bit programmable RLC DAC. To clamp to an internally defined voltage RLCEXT must be set to '0'. Control bits RLCV[3:0] then program the RLC DAC to a voltage ranging between 0V and AVDD linearly over 15 steps. The voltage from the RLC DAC will also be presented on pin VRLC which should be decoupled to analogue ground. Alternatively, by setting control bit RLCEXT to '1', the RLC DAC is disconnected and the VRLC pin is driven externally to any voltage between 0V and AVDD.

PROGRAMMABLE OFFSET DAC

The output from the Input Sampling Block is added to the output of an 8-bit Offset DAC to allow cancellation of offsets in sensor black level and input offsets of the WM8148. The DACs cover a range of ±200mV in 255 equal steps of 1.57mV, programmable via the DMI. Programming 00(hex) to the DAC gives an offset adjustment of -200mV, FF(hex) adjusts the input signal by +200mV.

PROGRAMMABLE GAIN AMPLIFIERS (PGA)

When the black level has been adjusted using the Offset DAC, the gain of the PGA can be programmed to amplify the white level signal to cover the full ADC range (3V). Figure 18 shows a graph of the PGA gain response. This gain curve is non-linear, with gain given by:

Gain = 52 / {70 – PGA[5:0](dec)}

This gives a gain ranging from 0.74 times to 7.4 times over 63 steps, with minimum gain corresponding to 00(hex) and maximum gain corresponding to 3F(hex). Figure 19 shows the PGA gain code settings required, for PGA input voltages from 0.4V to 4.0V, to produce a PGA output equivalent to the full scale input range of the ADC (3V).

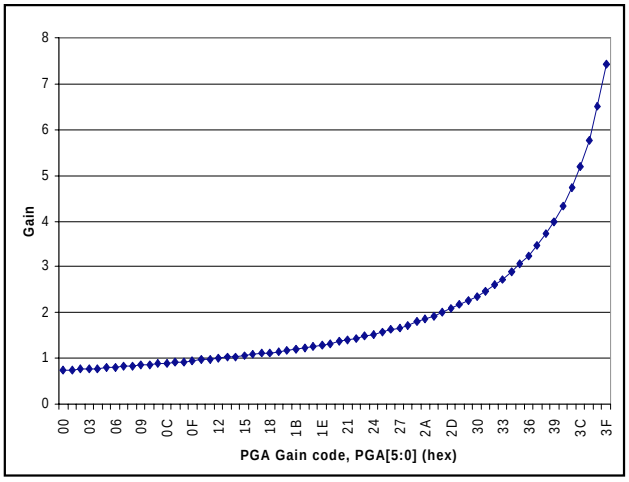


Figure 18 PGA Gain Response

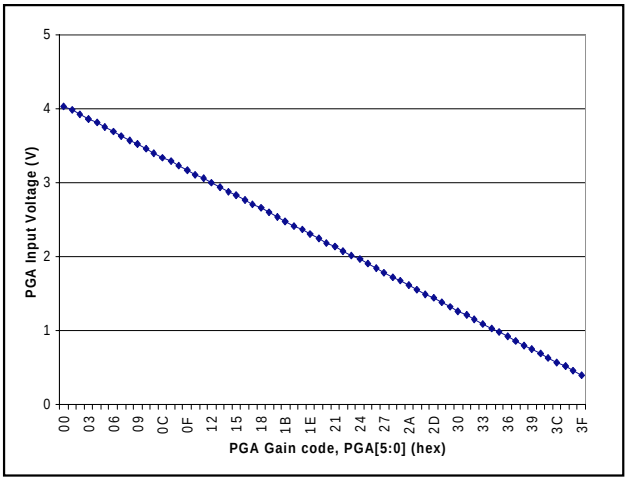


Figure 19 PGA Input vs Gain Code for Full Scale ADC Input

ANALOGUE TO DIGITAL CONVERTER (ADC)

The output of the PGA is applied to a high performance ADC. The differential signal from the PGA ranges from 0V (black level) to either +3V or -3V (white level), depending on the polarity of the input signal to the device. Control bits PGAFS[1:0] are used to configure the input of the ADC to accept the desired input signal range. This is achieved by adding 0, + or - half of the full scale voltage to the ADC input signal on a channel-by-channel basis, as shown in the block diagram on page 1. Table 2 shows the PGAFS[1:0] settings required for different video signal types.

VIDEO SIGNAL TYPE	DIFFERENTIAL SIGNAL RANGE		PGAFS[1:0]	OUTPUT CODE INVOP = 0	OUTPUT CODE INVOP = 1
	BLACK	WHITE			
Positive-going, e.g. many CIS	0V	3V	11	Black = 0 White = 4095	Black = 4095 White = 0
Negative-going, e.g. CCDs	0V	-3V	10	Black = 4095 White = 0	Black = 0 White = 4095
Bipolar	-1.5V	+1.5V	00, 01	Black = 0 White = 4095	Black = 4095 White = 0

Table 2 PGAFS[1:0] Setting for Video Signal Types

If the signal exceeds the chosen range, it is clipped and the error flag OVRNG is set, which may be output via the SDO or OP pins.

OVERALL SIGNAL FLOW SUMMARY

Figure 20 represents the processing of the video signal through the WM8148.

The **INPUT SAMPLING BLOCK** produces an effective input voltage **V_1**. For CDS, this is the difference between the input video level V_{IN} and the input reset level V_{RESET}. For non-CDS this is the difference between the input video level V_{IN} and the voltage on the VRLC pin, V_{VRLC}, optionally set via the RLC DAC.

The **OFFSET DAC BLOCK** then adds the amount of fine offset adjustment required to move the black level of the input signal towards 0V, producing **V_2**.

The **PGA BLOCK** then amplifies the white level of the input signal to maximise the ADC range, outputting voltage **V_3**.

The **ADC BLOCK** then converts the analogue signal, **V_3**, to a 12-bit unsigned digital output, **D_1**.

The digital output is then inverted if required, through the **OUTPUT INVERT BLOCK** to produce **D_2**.

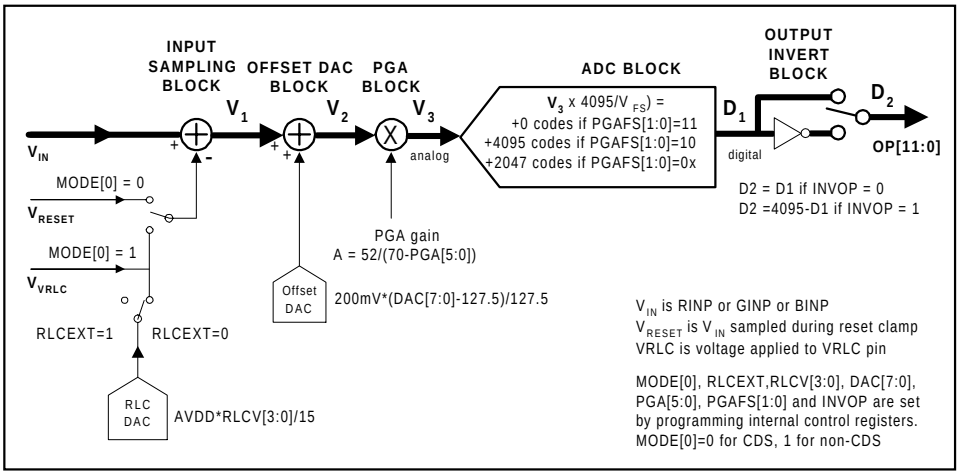


Figure 20 Overall Signal Flow

CALCULATING OUTPUT FOR ANY GIVEN INPUT

The following equations describe the processing of the video and reset level signals through the WM8148.

INPUT SAMPLING BLOCK: INPUT SAMPLING AND REFERENCING

If MODE[0] = 0, (i.e. CDS operation) the previously sampled reset level, V_{RESET}, is subtracted from the input video.

$$\mathbf{V_1} = V_{IN} - V_{RESET} \quad \text{Eqn. 1}$$

If MODE[0] = 1, (non-CDS operation) the simultaneously sampled voltage on pin VRLC is subtracted instead.

$$\mathbf{V_1} = V_{IN} - V_{VRLC} \quad \text{Eqn. 2}$$

If RLCEXT = 1, V_{VRLC} is an externally applied voltage on pin VRLC.

If RLCEXT = 0, V_{VRLC} is the output from the internal RLC DAC.

$$V_{VRLC} = AVDD * RLCV[3:0] / 15 \quad \text{Eqn. 3}$$

OFFSET DAC BLOCK: OFFSET (BLACK-LEVEL) ADJUST

The resultant signal $\mathbf{V_1}$ is added to the Offset DAC output.

$$\mathbf{V_2} = \mathbf{V_1} + 200mV * (DAC[7:0]-127.5) / 127.5 \quad \text{Eqn. 4}$$

PGA NODE: GAIN ADJUST

The signal is then multiplied by the PGA gain,

$$\mathbf{V_3} = \mathbf{V_2} * 52/(70- PGA[5:0]) \quad \text{Eqn. 5}$$

ADC BLOCK: ANALOGUE-DIGITAL CONVERSION

The analogue signal is then converted to a 12-bit unsigned number, with input range configured by PGAFS[1:0].

$$\mathbf{D_1}[11:0] = INT\{ (\mathbf{V_3}/V_{FS}) * 4095\} + 2047 \quad PGAFS[1:0] = 00 \text{ or } 01 \quad \text{Eqn. 6}$$

$$\mathbf{D_1}[11:0] = INT\{ (\mathbf{V_3}/V_{FS}) * 4095\} \quad PGAFS[1:0] = 11 \quad \text{Eqn. 7}$$

$$\mathbf{D_1}[11:0] = INT\{ (\mathbf{V_3}/V_{FS}) * 4095\} + 4095 \quad PGAFS[1:0] = 10 \quad \text{Eqn. 8}$$

where the ADC full-scale range, V_{FS}, = 3V.

OUTPUT INVERT BLOCK: POLARITY ADJUST

The polarity of the digital output may be inverted by control bit INVOP.

$$\mathbf{D_2}[11:0] = \mathbf{D_1}[11:0] \quad (INVOP = 0) \quad \text{Eqn. 9}$$

$$\mathbf{D_2}[11:0] = 4095 - \mathbf{D_1}[11:0] \quad (INVOP = 1) \quad \text{Eqn. 10}$$

OUTPUT DATA FORMAT

MULTIPLEXED AND NON-MULTIPLEXED OUTPUT FORMAT

Data is output from the device, by default, as a 12-bit wide word on OP[11:0]. The output changes on every Nth negative-going edge of MCLK where N = 2, 4, or 6 according to the video sampling mode. This is shown as byte C in Figure 21.

If control bit MUXOP is set high, data is output in a 2 x 8-bit word format, with data changing every Nth negative-going edge of MCLK, where N = 1, 2, or 3 according to video sampling mode. This is shown as bytes A and B in Figure 21. Data is presented on pins OP[11:4] at twice the output pixel rate. Bits CC[1] and CC[0] are used to indicate which channel the ADC input was taken from. Table 3 shows the channels corresponding to the CC[1:0] bit values. Bits TVIOL and OVRNG of byte B are Error Flags, these are described below.

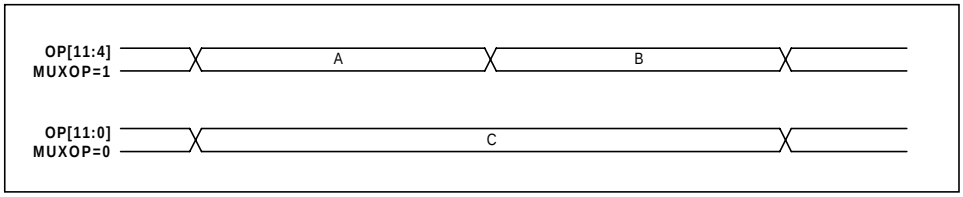


Figure 21 Output Data for 2 x 8-bit and 12 bit Output.

Where:

A = < d11, d10, d9, d8, d7, d6, d5, d4 >

B = < d3, d2, d1, d0, TVIOL, CC[1], CC[0], OVRNG >

C = < d11, d10, … d1, d0 >

COLOUR CODE BITS		CHANNEL
CC[1]	CC[0]	
0	0	Red
0	1	Green
1	0	Blue

Table 3 Colour Code Bits CC[1:0]

ERROR FLAGS

The two error flags are:

TVIOL: This goes high if the reset sample and clamp positions set up in bits RESREF[3:0], are inconsistent with the selected mode of operation.

OVRNG: This goes high if the input to the ADC exceeds its input range.

These flags are output in byte B of multiplexed-mode parallel output data as above. Each is also available via the SDO pin if so configured via the SDO[1:0] register bits.

LATENCY

Default latency from the last rising edge of MCLK during the VSMP pulse to data output depends on the chosen Input Sampling Mode. To align pixel outputs with post processing circuitry and to reduce interaction with video sampling instances, the latency through the WM8148 device can be adjusted by Control bits DEL[1:0] and FDEL[1:0].

DIGITAL MANAGEMENT INTERFACE (DMI)

The DMI is used to write contents to and read back contents from the internal registers in either serial or parallel mode. The PNS pin is tied low for serial and high for parallel mode.

SERIAL INTERFACE

REGISTER WRITE

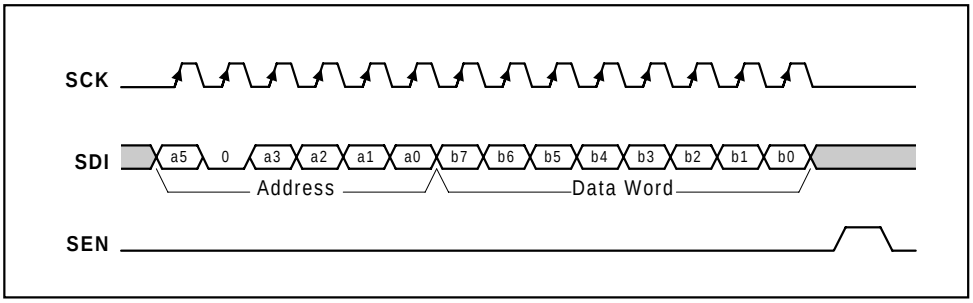


Figure 22 Serial Interface Register Write

Figure 22 shows register writing in serial mode. Three pins, SCK, SDI and SEN are used. A six-bit address (a5, 0, a3, a2, a1, a0) is clocked in through SDI, MSB first, followed by an eight-bit data word (b7, b6, b5, b4, b3, b2, b1, b0), also MSB first. Each bit is latched on the rising edge of SCK. When the data has been shifted into the device, a pulse is applied to SEN to transfer the data to the appropriate internal register. Note all valid registers have address bit a4 equal to 0 in write mode.

REGISTER READ-BACK

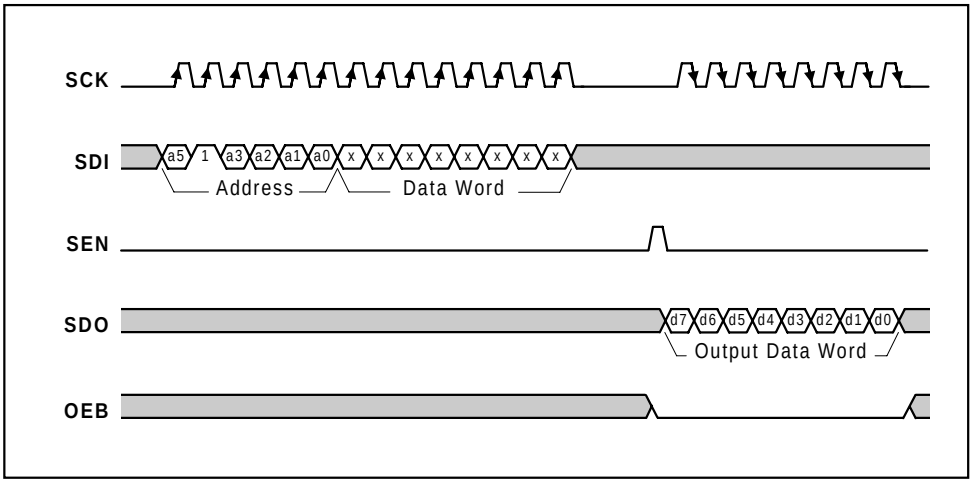


Figure 23 Serial Interface Register Read-back

Register read-back is initiated by writing to the serial bus as described, but with address bit a4 set to 1, followed by an 8-bit dummy data word. Writing address (a5, 1, a3, a2, a1, a0) will cause the contents (d7, d6, d5, d4, d3, d2, d1, d0) of corresponding register (a5, 0, a3, a2, a1, a0) to be output MSB first on pin SDO (on the falling edge of SCK), provided control bits SDO[1:0] = 00. If SDO[1:0] is not set to 00 then error flags will be output instead of the register contents. Note that if SDI and SDO are not connected together, the next word may be read in to SDI while the previous word is still being output on SDO. Alternatively, the user may tie the SDI and SDO pins together to make a 3-wire serial interface. The user must ensure that the circuit driving SDI is Hi-Z while the SDO pin is active.

Pin OEB must be low to enable the output data word to be output.

PARALLEL INTERFACE

REGISTER WRITE

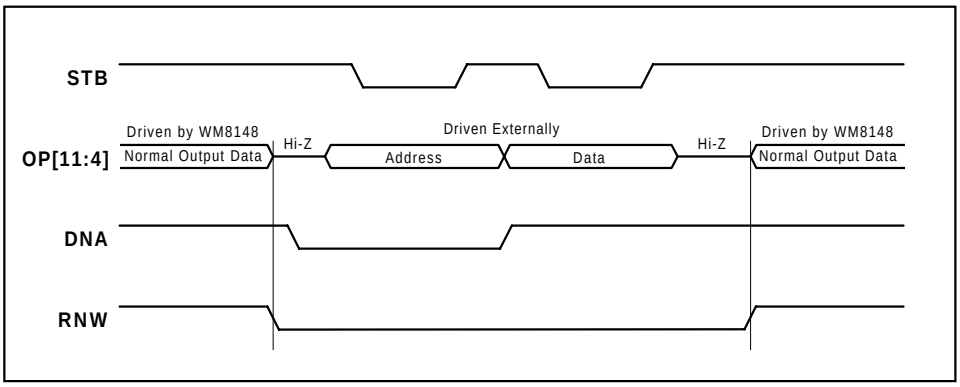


Figure 24 Parallel Interface Register Write

The parallel interface uses bits [11:4] of the OP bus and the STB, DNA and RNW pins. Pin RNW must be low during a write operation. The DNA pin defines whether the data byte is address (low) or data (high). The 6-bit address (a5, 0, a3, a2, a1, a0) is input into OP[9:4], LSB into OP[4], (OP[10] and OP[11] are ignored) when DNA is low, then the 8-bit data word is input into OP[11:4], LSB into OP[4], when DNA is high. The data bus OP[11:4] for both address and data is latched in during the low period of STB. Note all valid registers have address bit a4 equal to 0.

REGISTER READ-BACK

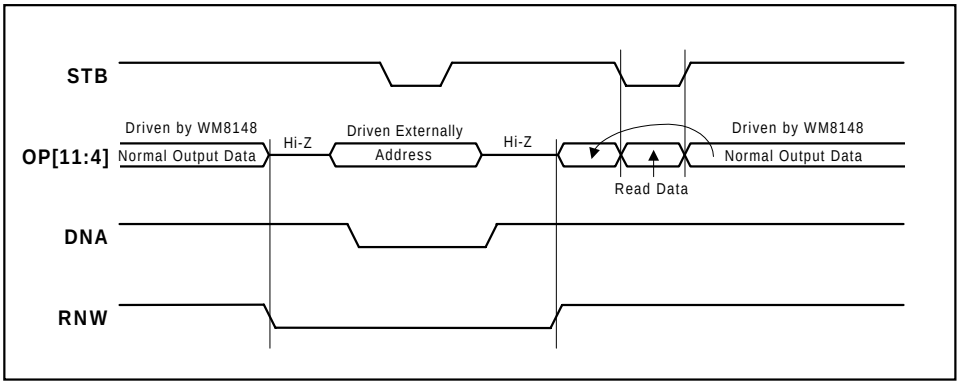


Figure 25 Parallel Interface Register Read-back

Register read-back is initiated by writing the 6-bit address (a5, 1, a3, a2, a1, a0) into OP[9:4] by pulsing the STB pin low. Note that a4 = 1 and pins RNW and DNA are low. When RNW and DNA are high and STB is strobed again, the contents (d7, d6, d5, d4, d3, d2, d1, d0) of the corresponding register (a5, 0, a3, a2, a1, a0) will be output on OP[11:4], LSB on pin OP[4]. Until STB is pulsed low, the current contents of the ADC (shown as Normal Output Data) will be present on OP[11:4].

OUTPUT ENABLE

When high, pin OEB makes pins OP[11:0] Hi-Z regardless of other pin settings. Therefore when the WM8148 is outputting normal ADC data, or during register read, pin OEB must be set to '0'. During register write, pin RNW set to '0' ensures that the outputs are Hi-Z, therefore pin OEB is 'don't care'. Table 4 shows the state of pins OP[11:0] for possible settings of OEB, RNW and STB.

OEB	RNW	STB	OP[11:0]
1	x	x	Hi-Z
x	0	x	Hi-Z
0	1	0	Read register data
0	1	1	Read ADC data

Table 4 State of OP[11:0] During Register Read/Write

POWER MANAGEMENT

Power management for the WM8148 is performed via the DMI. The device can be powered on or off completely by the control bit EN. Alternatively, when control bit SELEN is high, only blocks selected by further control bits SENBL[7:0] are powered up. This allows the user to optimise power dissipation in certain modes, or to define intermediate standby modes to allow a quicker recovery into a fully active state.

EN	SELEN	
0	0	Device completely powers down.
1	0	Device completely powers up.
x	1	Only blocks with respective SENBL bit high go/remain active.

Table 5 Power Down control

Control bit RLCEXT is used to disable the RLC DAC, regardless of EN or SENBL[7:0]. If this option is taken, pin VRLC can be driven externally for reset level clamping.

One-channel and Two-channel sampling modes do not automatically power down unused PGAs, the appropriate SENBL bits should be set during initialisation to save power. The WM8148 will still operate normally if the unused blocks are not powered down.

All the internal registers maintain their previously programmed value in power down modes, and the DMI inputs remain active.

REGISTER RESET

RESET ON POWER UP

To set the registers to their default values, pin NRESET must be held low during power-up. If pin OVRD is also held low, all of the registers will be set to their default values including bits SELEN and EN which will disable all of the analogue circuitry. If pin OVRD is held high during power up with pin NRESET held low, all of the registers will be set to their default value with the exception of EN and RLCEXT, which will enable all of the analogue circuitry in the device.

RESET DURING OPERATION

During device operation, pulsing NRESET low will reset all of the registers depending on the polarity of the OVRD pin as above.

The registers may also be reset by writing to bits SRES[1:0]. This allows reset of:

1) Only the PGA Gains and Offset DAC Values registers,
2) All registers except power-management registers SELEN, EN, and SENBL, or
3) All registers, equivalent to the NRESET function.

REFERENCE VOLTAGES

The ADC reference voltages are derived from an internal bandgap reference, and buffered to pins VRT and VRB, where they must be decoupled to ground. Pin VRX is driven by a similar buffer, and also requires decoupling. The output buffer from the RLC DAC also requires decoupling at pin VRLC.

Peak sink and source currents of the reference buffers are typically between ±1mA and ±6mA, depending on output voltage and current polarity. This limits the slew-rate into the decoupling capacitors on power-up. When disabled, the buffers become high-impedance ($I < 1\mu A$), so the decoupling capacitor voltage will not drop much during short (< 100ms) disable durations.

DETAILED MODE TIMING DIAGRAMS

The following diagrams show Input Signal Sampling Diagrams, Output Data Timing and Reset Sample/Clamp Positions for each mode of the WM8148.

INPUT SIGNAL SAMPLING DIAGRAMS

These diagrams show the required MCLK and VSMP (externally or internally generated) signals. From these signals, internally generated signals V_S and R_S are used to sample the video and reset levels (in CDS modes) respectively. In non-CDS modes, the reference level is sampled simultaneously with V_S. The position of the sampling point is indicated by the vertical lines which run from the sensor output waveform to the respective V_S or R_S sampling points, and by the inclusion of the arrow on the falling edge of the V_S or R_S pulse. Also shown is MCLK timing, which counts the number of MCLK periods in total, and MCLK phase, which counts the number of MCLK periods between each VSMP pulse. Note that the duration of the VSMP pulse must not include more than one MCLK rising edge, as this will reset the phase timing. The output waveforms are included. The position of the R_S pulse is programmable, therefore the RESREF[3:0] position for each diagram has been included.

OUTPUT DATA TIMING DIAGRAMS

The output timing diagrams are used to calculate the latency through the device, which is dependent on the operating mode. The latency can be programmed using the DEL[1:0] bits in setup register 4. Output timing and latency does not depend on the RESREF[3:0] control bits. As an example, Figures 26 and 27 show that a sample taken on the rising edge of MCLK at time 1, will emerge from the device on the falling edge of MCLK at time 19, i.e. a latency of 18.5 MCLK periods (DEL = 00).

RESET SAMPLE/CLAMP POSITIONS

In CDS modes, control bits RESREF[3:0] control the position of the reset sampling point, R_S, and the clamp pulse point, CL, if reset level clamping is selected. In non-CDS modes, control bits RESREF[3:0] control the position of CL only, if reset level clamping is selected. These diagrams show the positions to which the sampling or clamping pulse can be adjusted for each mode. Care must be taken to adjust the R_S position to one that will ensure that the reset sample and/or clamp point will be taken at the most appropriate moment during the reset portion of the input signal.

THREE-CHANNEL (8-PHASE) – MODES 0 AND 1

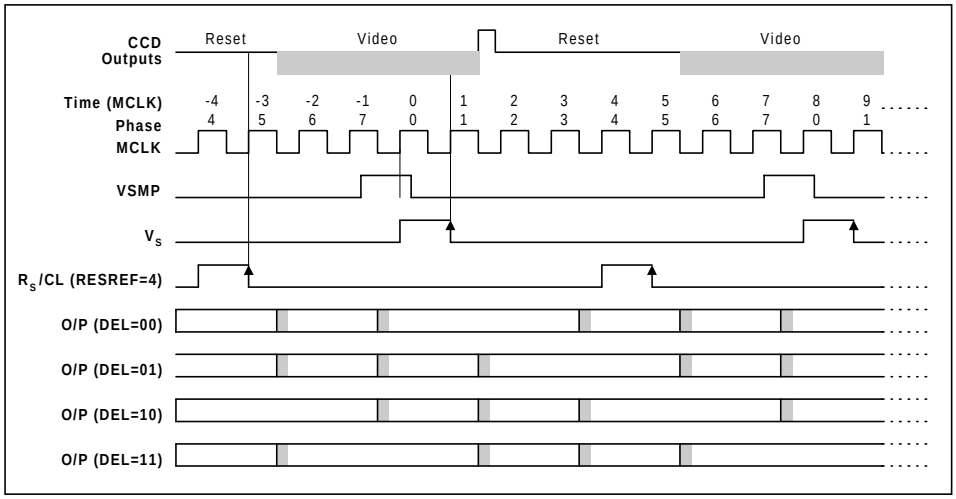


Figure 26 Modes 0 and 1 Input Signal Sampling

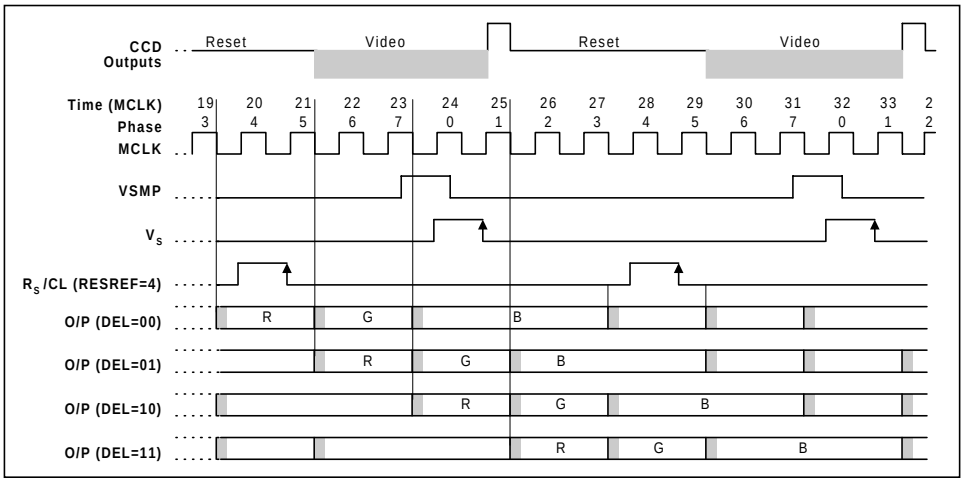


Figure 27 Modes 0 and 1 Output Data Timing

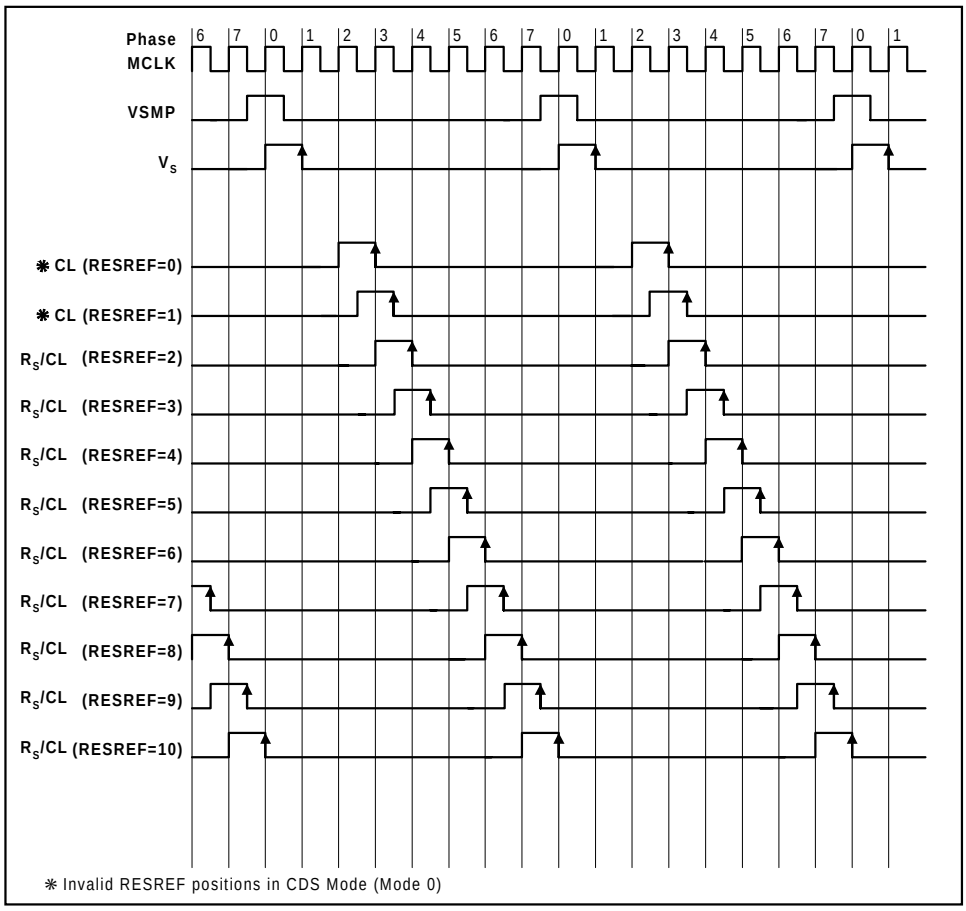


Figure 28 Modes 0 and 1 Reset Sample/Clamp Positions

ONE-CHANNEL CDS – MODE 2

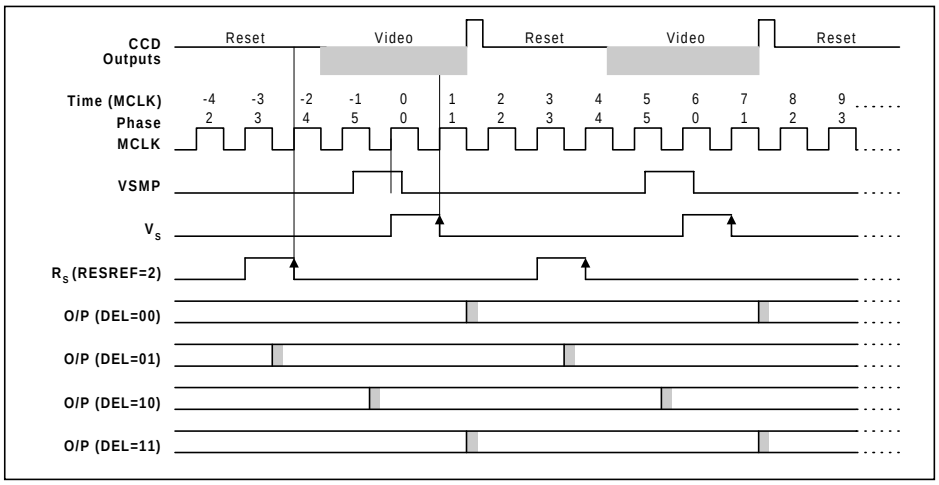


Figure 29 Mode 2 Input Signal Sampling

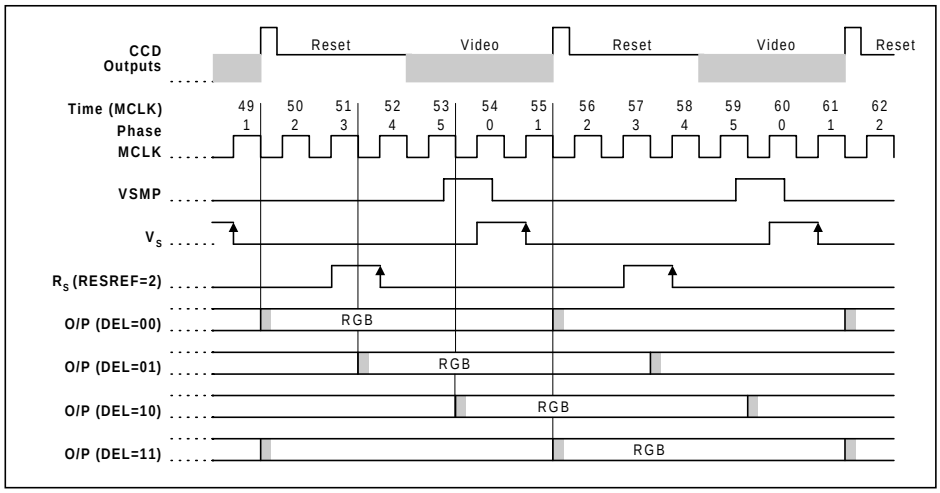


Figure 30 Mode 2 Output Data Timing

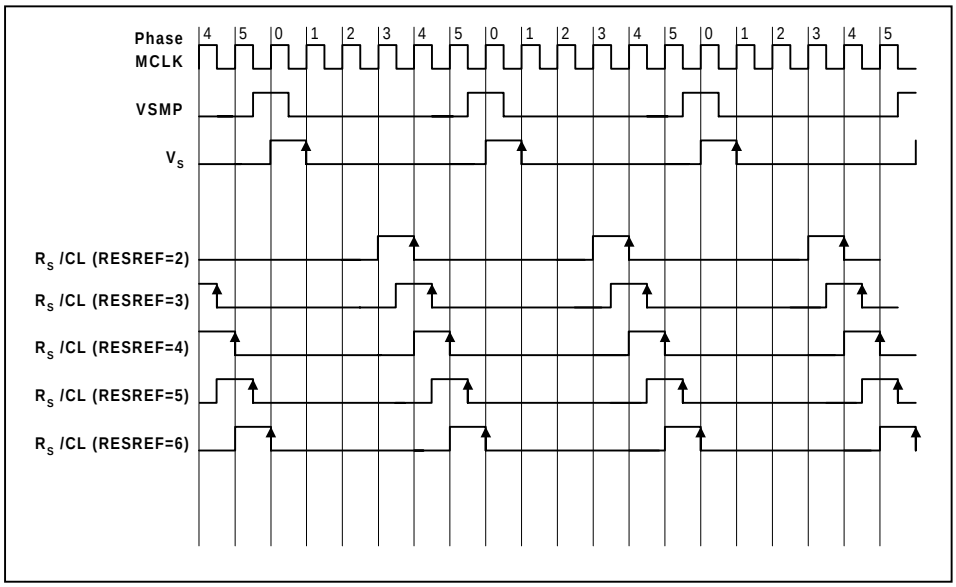


Figure 31 Mode 2 Reset Sample/Clamp Positions

ONE-CHANNEL NON-CDS – MODE 3

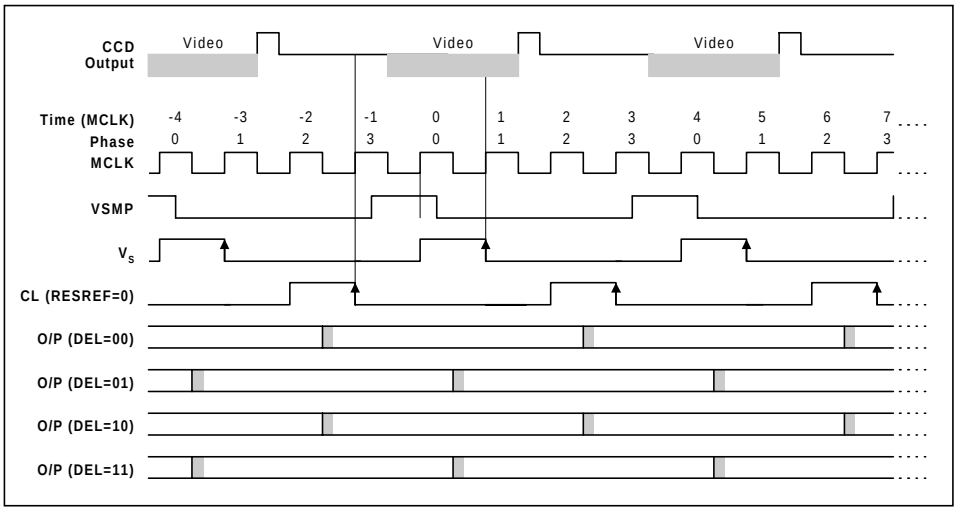


Figure 32 Mode 3 Input Signal Sampling

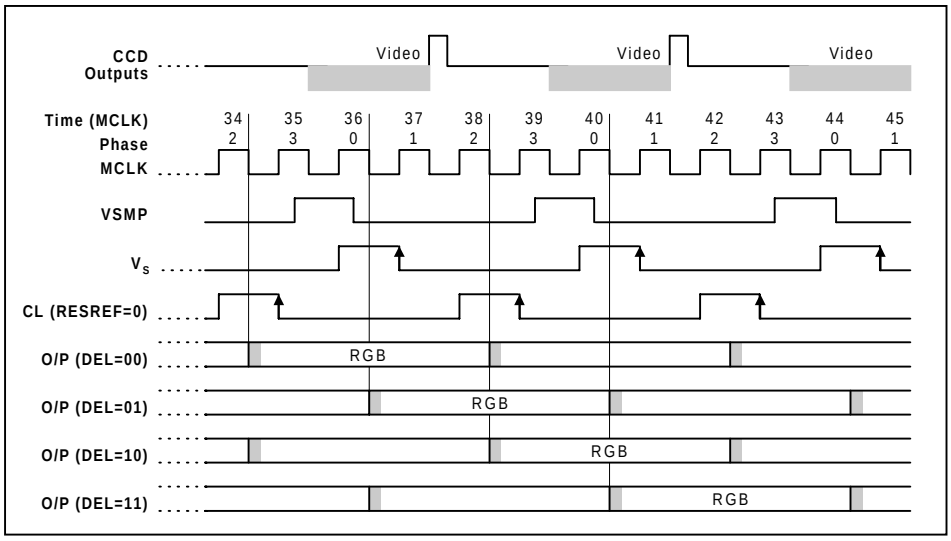


Figure 33 Mode 3 Output Data Timing

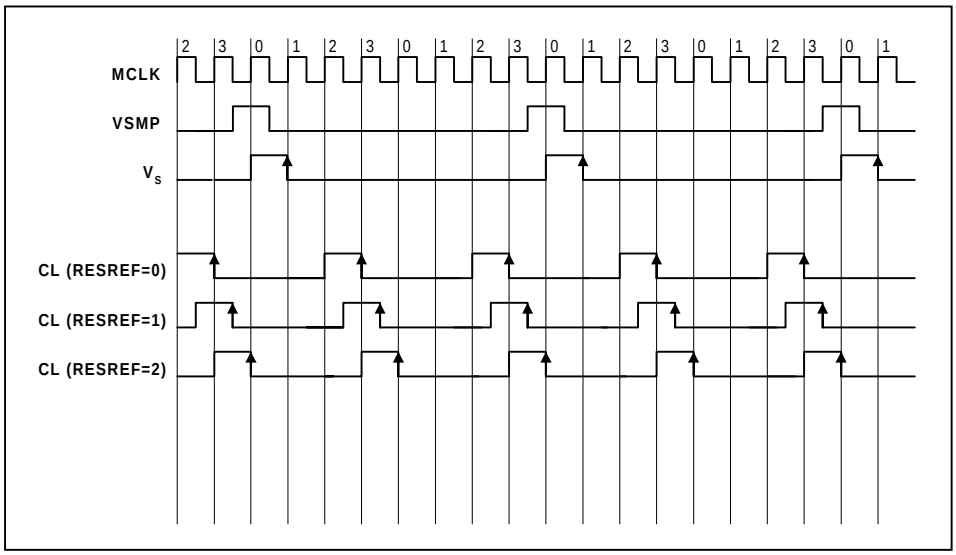


Figure 34 Mode 3 Reset Sample/Clamp Positions

TWO-CHANNEL (6-PHASE) – MODES 4 AND 5

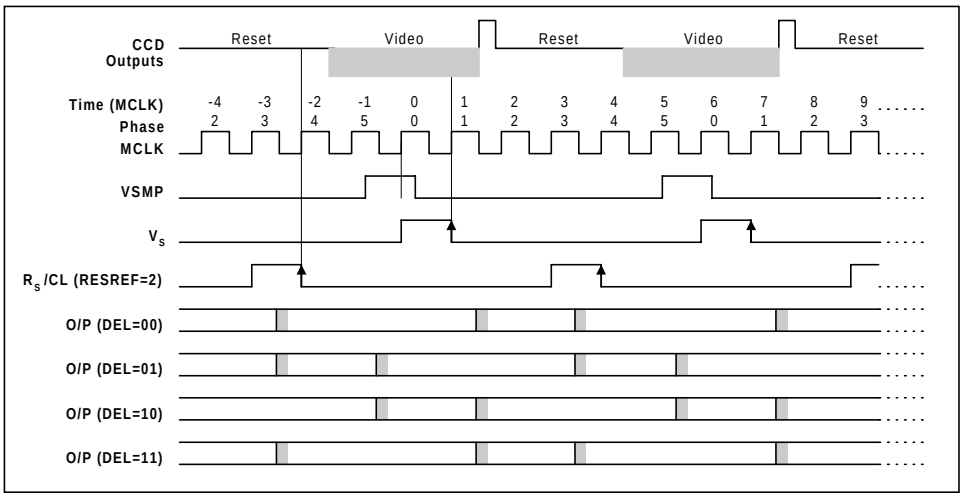


Figure 35 Modes 4 and 5 Input Signal Sampling

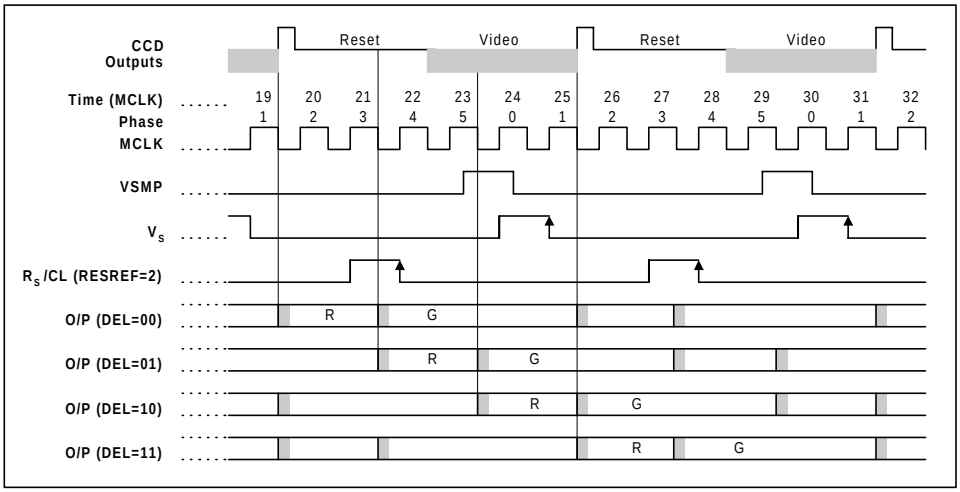


Figure 36 Modes 4 and 5 Output Data Timing

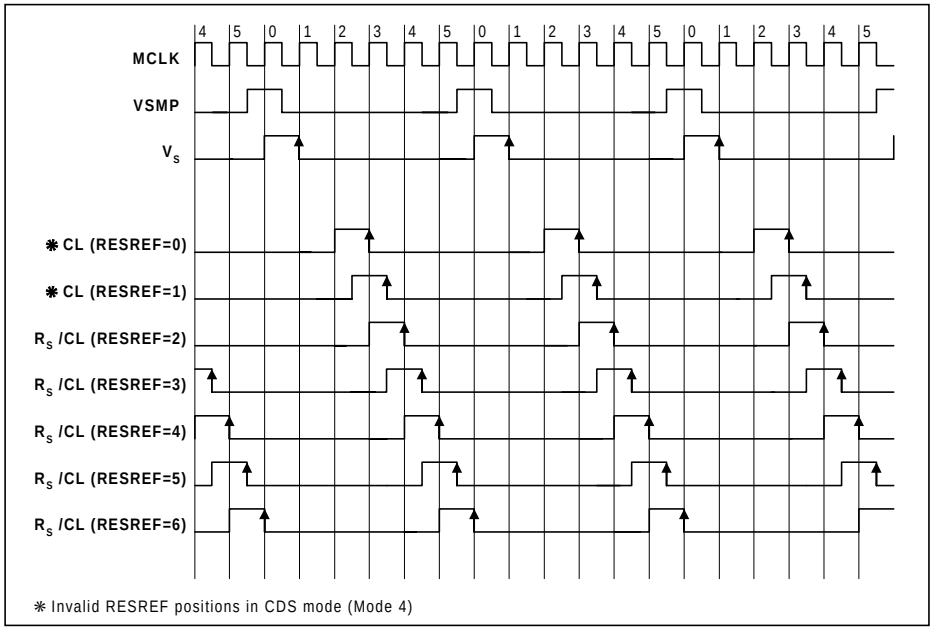


Figure 37 Modes 4 and 5 Reset Sample/Clamp Positions

THREE CHANNEL (12-PHASE) – MODES 8 AND 9

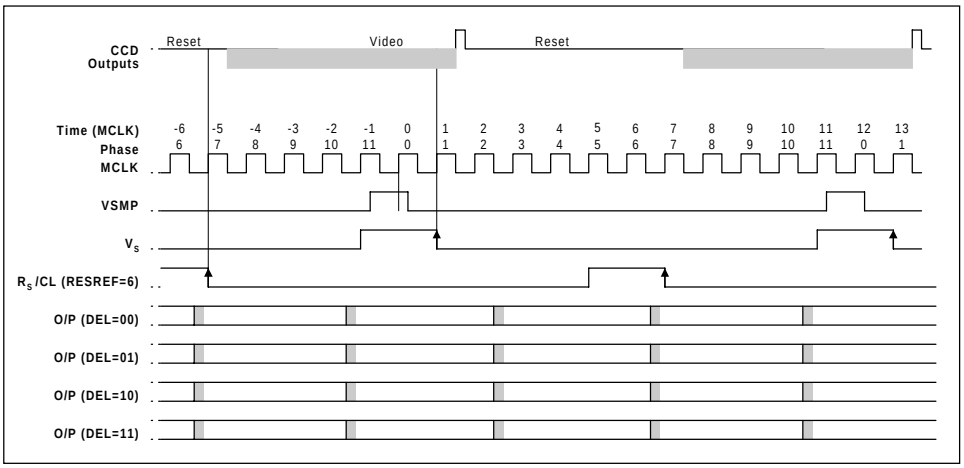


Figure 38 Modes 8 and 9 Input Signal Sampling

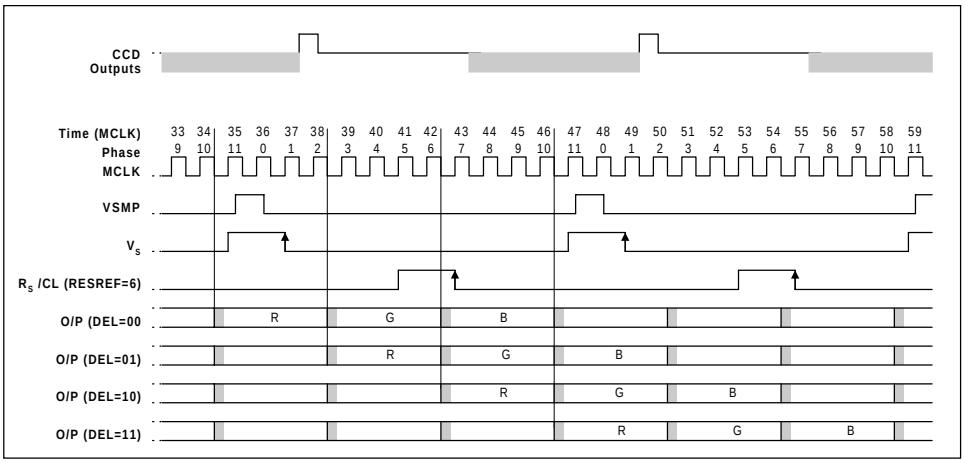


Figure 39 Modes 8 and 9 Output Data Timing

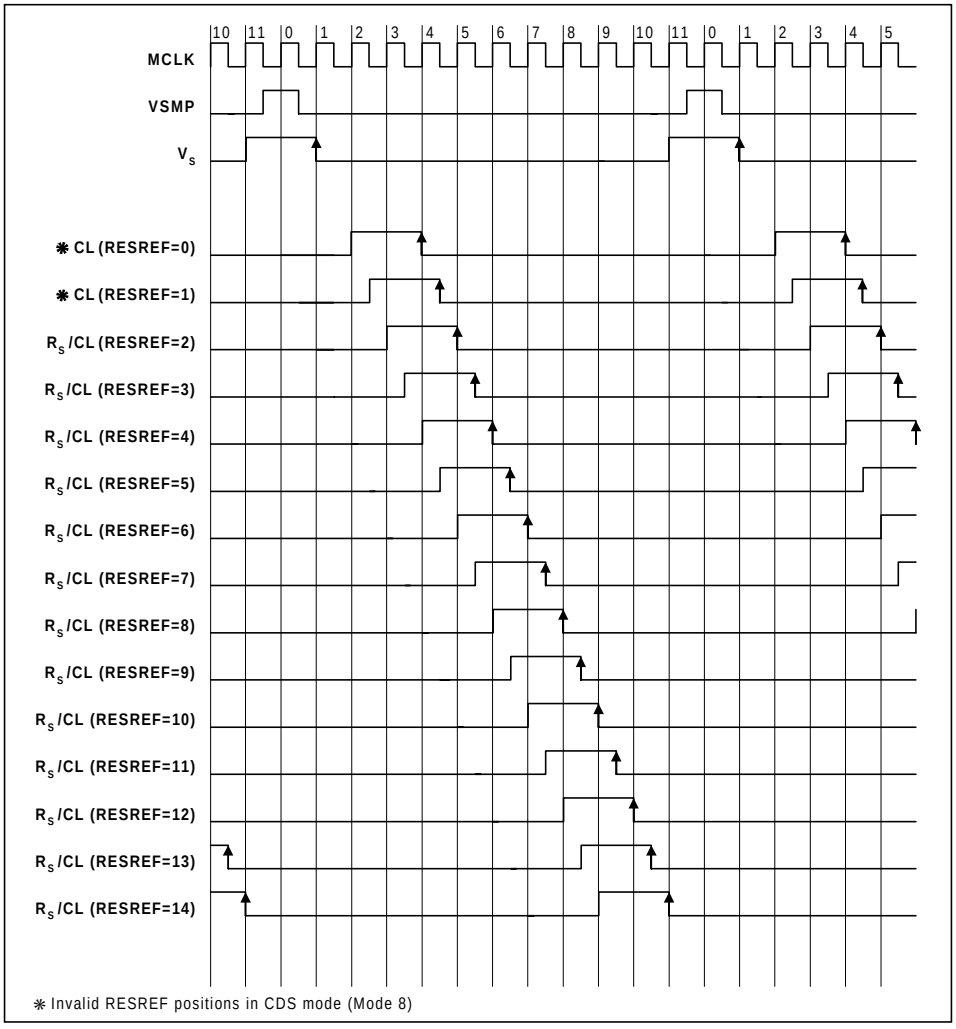


Figure 40 Modes 8 and 9 Reset Sample/Clamp Positions

TWO-CHANNEL (8-PHASE) – MODES 12 AND 13

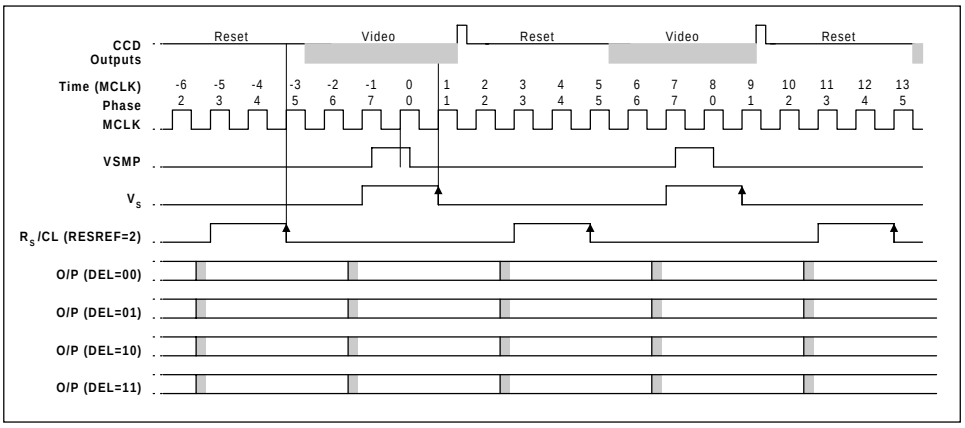


Figure 41 Modes 12 and 13 Input Signal Sampling

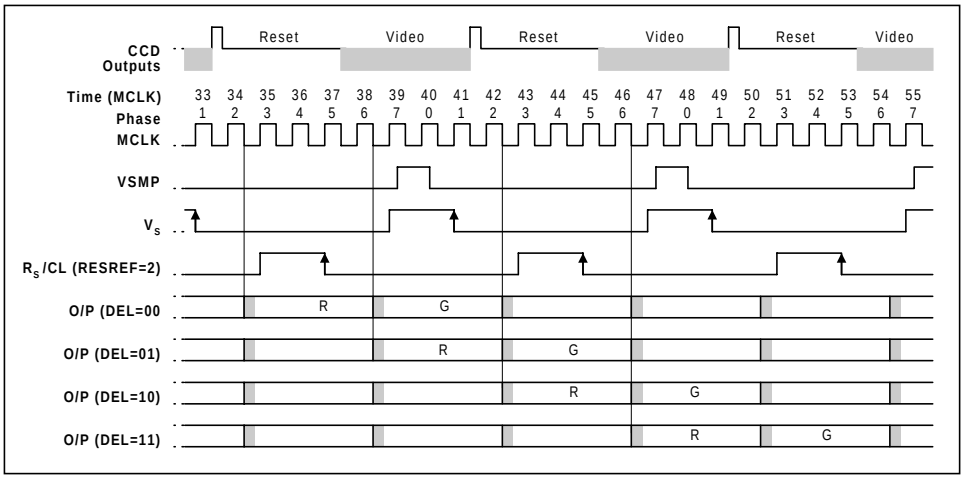


Figure 42 Modes 12 and 13 Output Data Timing

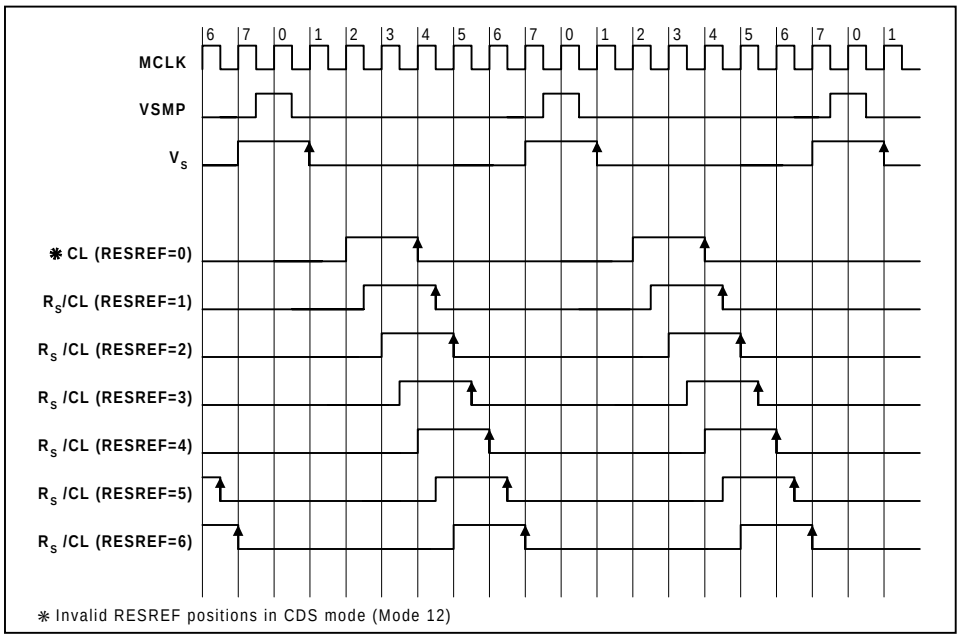


Figure 43 Modes 12 and 13 Reset Sample/Clamp Positions

DEVICE CONFIGURATION

The following section details the Control Register Map, the contents of which determines the operation of the WM8148, and the Control Bit table, which describes the possible settings of each of the bits in the Control Register Map.

INTERNAL REGISTER DEFINITION

Table 6 details the internal register contents.

SET-UP REGISTER 1

- Selects global power on/off or selective enable.
- Selects the function of the SDO pin.
- Controls input sampling mode the device is operating in.

SET-UP REGISTER 2

- Enables individual sections of the device such as sample and hold blocks or PGA.

SET-UP REGISTER 3

- Sets the clamp and reset sample position in CDS modes.
- Sets the clamp position in non-CDS modes.
- Enables the internal clocks to be free running without VSMP.
- Allows the video and reset sample pulse widths to be reduced by half an MCLK period.
- Selects the channel that the sample is taken from in One-Channel (or line by line) modes.

SOFTWARE RESET

- Writing to this register causes the device to reset. Three different reset types are available. See Control Bit Description Table for details.

SET-UP REGISTER 4

- Allows the latency through the device to be adjusted by ADC clock periods and by half-MCLK periods.
- Enables VSMP as input or output.
- Allows the external setting of RLC bias reference voltage.
- Controls parallel/multiplexed output format.
- Defines the polarity of the output data.

COARSE OFFSETS

- Controls the non-CDS reference voltage level or reset clamp level.
- Allows external reference to be used as reset clamp level.
- Adjusts the d.c. level of the PGA outputs to align with the ADC input range to suit different input video signal polarities.

REVISION NUMBER

- Allows the user to check which revision of the device is being used.

DAC VALUES

- Programmes the amount of offset applied to the input of each PGA. Table 7 describes the sub-address bits for each channel.

PGA GAINS

- Programmes the gain of each PGA. Table 7 describes the sub-address bits for each channel.

ADDRESS	DESCRIPTION	DEFAULT	RW	BIT							
<A5:A0>		(HEX)		B7	B6	B5	B4	B3	B2	B1	B0
000001	Setup Register 1	80	RW	MODE[3]	MODE[2]	MODE[1]	MODE[0]	SDO[1]	SDO[0]	SELEN	EN
000010	Setup Register 2	00	RW	SENBL[7]	SENBL[6]	SENBL[5]	SENBL[4]	SENBL[3]	SENBL[2]	SENBL[1]	SENBL[0]
000011	Setup Register 3	06	RW	CHAN[1]	CHAN[0]	SMALL	FREE	RESREF[3]	RESREF[2]	RESREF[1]	RESREF[0]
000100	Software Reset	00	W	0	0	0	0	0	0	SRES[1]	SRES[0]
000101	Setup Register 4	00	RW	INVOP	MUXOP	0	VSMPOP	FDEL[1]	FDEL[0]	DEL[1]	DEL[0]
000110	Coarse Offsets	1B	RW	0	PGAFS[1]	PGAFS[0]	RLCEXT	RLCV[3]	RLCV[2]	RLCV[1]	RLCV[0]
000111	Revision Number	43	R	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]
1000**XY**	DAC Values	80	RW	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]
1010**XY**	PGA Gains	00	RW	0	0	PGA[5]	PGA[4]	PGA[3]	PGA[2]	PGA[1]	PGA[0]

Note: Register address 000000 is reserved and should not be written to.

Table 6 Control Register Map

ADDRESS LSB DECODE	X	Y
Red register	0	0
Green register	0	1
Blue register	1	0
Red, Green, and Blue registers	1	1

Table 7 Red, Green, Blue, Sub-address Bits

CONTROL BIT DESCRIPTION

CONTROL BIT/WORD	DEFAULT	DESCRIPTION
Set-up Register 1	**Address 000001**	
EN b0 SELEN b1	0 0	Global power on/off or selective enable. SELEN EN 0 0 Complete power down (default). 0 1 Complete power on. 1 X Individual block power on/off (X denotes either 1 or 0) see SENBL[7:0] register description for details.
SDO[1:0] b3, b2	00	Multiplexes SDO output pin. SDO[1] SDO[0] 0 0 Register readback when requested, Hi-Z otherwise 0 1 TVIOL flag (RESREF inconsistent with MODE). 1 0 ADC over-range flag. 1 1 VSMP synchronous output.
MODE[3:0] b7, b6, b5, b4	1000	Device mode control bits. MODE[3] MODE[2] MODE[1] MODE[0] 0 0 0 0 Three-channel (8-phase) CDS 0 0 0 1 Three-channel (8-phase) non-CDS 0 0 1 0 One-channel CDS 0 0 1 1 One-channel non-CDS 0 1 0 0 Two-channel (6-phase) CDS 0 1 0 1 Two-channel (6-phase) non-CDS 1 0 0 0 Three-channel (12-Phase) CDS 1 0 0 1 Three-channel (12-Phase) non-CDS 1 1 0 0 Two-channel (8-Phase) CDS 1 1 0 1 Two-channel (8-Phase) non-CDS

CONTROL BIT/WORD	DEFAULT	DESCRIPTION
Set-up Register 2	**Address 000010**	
SENBL[7:0] b7…..b0	0000 0000	Selective power enable register, activated when SELEN = 1 (Set-up Register 1). Each bit activates respective cell when 1, de-activates when 0. SENBL[0] Bandgap/Bias SENBL[1] VRT, VRB buffers SENBL[2] VRX buffer SENBL[3] RLC DAC (allows VRLC to be externally driven) SENBL[4] Red S/H, PGA SENBL[5] Green S/H, PGA SENBL[6] Blue S/H, PGA SENBL[7] ADC
Set-up Register 3	**Address 000011**	
RESREF[3:0] b3, b2, b1, b0	0110	Selects the position of either the reset sample and the clamp points in CDS modes, or the position of just the clamp pulse in non-CDS modes. See Mode Descriptions for further details.
FREE b4	0	Enables internal clocks to be free running, without VSMP pulse input. FREE 0 Requires continuous VSMP pulse input every N periods of MCLK 1 Free running
SMALL b5	0	Reduces video and reset sample pulse widths by half an MCLK period. SMALL 0 Default pulse widths 1 Reduces pulse widths
CHAN[1:0] b7, b6	00	Selects the input channel in One-channel (line by line) modes. No effect when not in One-channel mode. CHAN[1] CHAN[0] 0 0 Red channel 0 1 Green channel 1 0 Blue channel 1 1 Reserved
Software Reset	**Address 000100**	
SRES[1:0] b1, b0	00	Writing to this register causes a software reset. There a three types of reset available: SRES[1] SRES[0] 0 0 Same action as NRESET pin 0 1 Resets all registers to default including RLCEXT. (Except EN, SELEN and SENBL[7:0], which are not changed) 1 X Resets PGA and DAC only (X denotes either 1 or 0)
Setup Register 4	**Address 000101**	
DEL[1:0] b1, b0	00	Adjusts the latency through the device in ADC clock periods. See Detailed Mode Timing Diagrams for details.
FDEL[1:0] b3, b2	00	Adjusts the latency through the device in half-MCLK increments. FDEL[1] FDEL[0] 0 0 Default position 0 1 Earlier by MCLK/2 1 0 Later by MCLK/2 Invalid in modes 0, 1, 4 and 5 1 1 Later by MCLK/2 Invalid in modes 0, 1, 4 and 5 In these invalid modes, output data is held constant, TVIOL is not flagged.
VSMPOP b4	0	Enables output of internally generated MCLK/N sync pulse (only if FREE also set). VSMPOP 0 Requires external VSMP 1 VSMP pin becomes sync output
b5	0	Reserved for Wolfson use only, must be programmed to 0.

CONTROL BIT/WORD	DEFAULT	DESCRIPTION
MUXOP b6	0	Changes the data output format from 12-bit parallel to 2 x 8 bit multiplexed. MUXOP 0 12-bit wide parallel data 1 8-bit wide multiplexed data
INVOP b7	0	Digitally inverts the polarity of output data. INVOP 0 Negative-going video gives negative-going output data 1 Negative-going video gives positive-going output data
Coarse Offsets	**Address 000110**	
RLCV[3:0] b3, b2, b1, b0	1011	Controls RLC DAC driving VRLC pin, to define single-ended signal-reference voltage or reset-level clamp voltage. F(hex) is VDD, 0(hex) is 0V, B(hex) (default) is 11/15 * AVDD (= 3.67V typically).
RLCEXT b4	1	Powers down the RLC DAC, tri-stating its output, allowing VRLC to be externally driven. RLCEXT 0 RLC DAC drives VRLC pin 1 RLC DAC Hi-Z
PGAFS[1:0] b6, b5	00	Configures the ADC input to accept the following video signal types: PGAFS[1] PGAFS[0] 0 0 Bipolar video 0 1 Bipolar video 1 0 Negative-going video 1 1 Positive-going video
Revision Number	**Address 000111**	
REV[7:0] b7, ...b0	43	Read-only register, allows the user to determine the revision level of the device. ASCII 7-bit code, e.g. 43(hex) = C
DAC Values	**Address 1000xy**	
DAC[7:0] b7, ...b0	1000 0000	The offset-setting data for the Red, Green and Blue offset DACs. 00(hex) gives -200mV offset referred to signal input, FF(hex) gives +200mV, 80(hex) (default) gives approximately zero offset.
PGA Gains	**Address 1010xy**	
PGA[5:0] b5, ... b0	000000	The gain setting data for the Red, Green, and Blue programmable gain amplifiers. 00(hex) gives min gain, 3F(hex) gives max gain.

Table 8 Control Register Bit Descriptions

RECOMMENDED EXTERNAL COMPONENTS

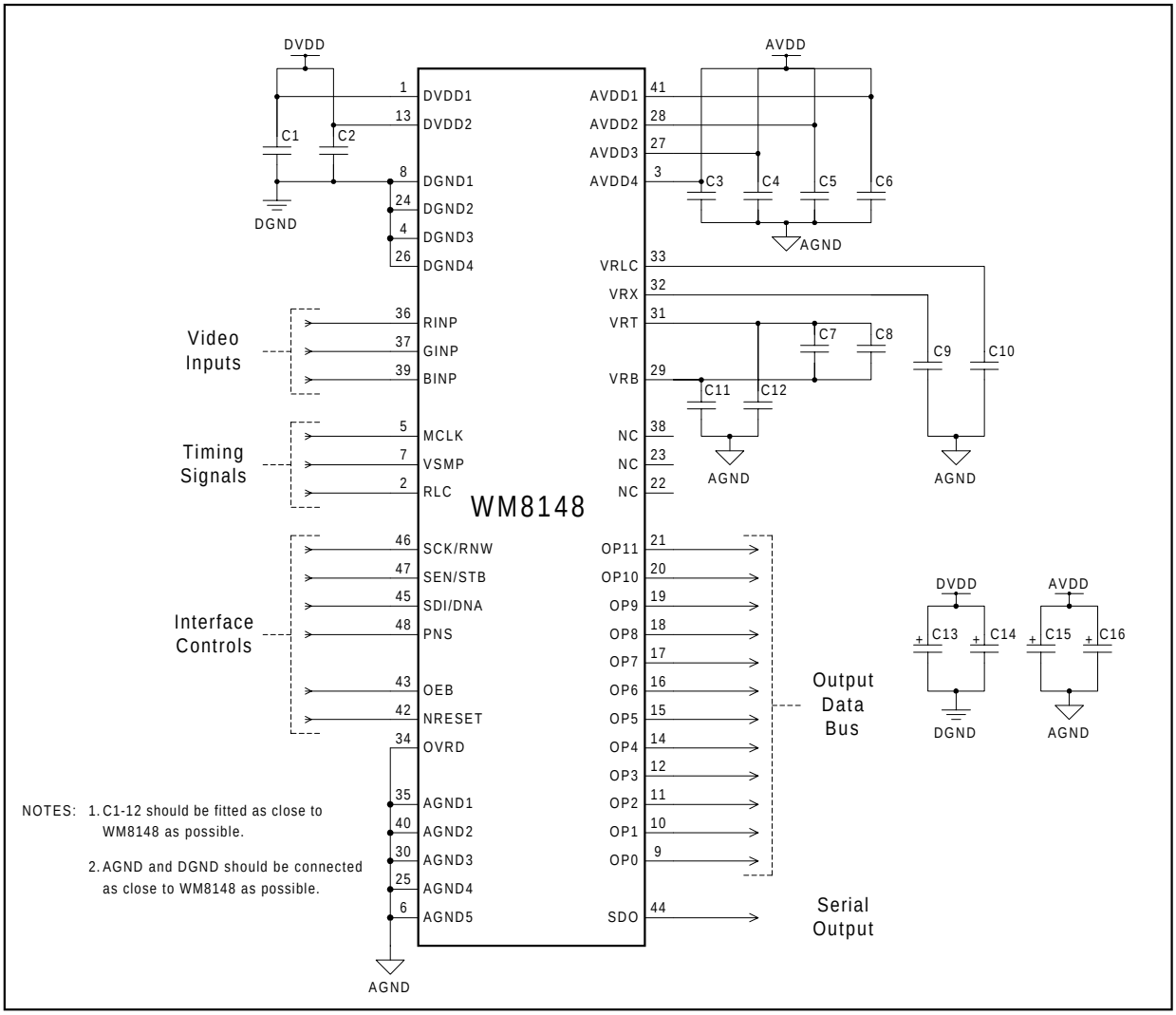


Figure 44 External Components Diagram

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	10nF	De-coupling for DVDD1.
C2	10nF	De-coupling for DVDD2.
C3	10nF	De-coupling for AVDD4.
C4	10nF	De-coupling for AVDD3.
C5	10nF	De-coupling for AVDD2.
C6	10nF	De-coupling for AVDD1.
C7	10nF	High frequency de-coupling between VRT and VRB.
C8	1µF	Low frequency de-coupling between VRT and VRB (non-polarised).
C9	100nF	De-coupling for VRX.
C10	100nF	De-coupling for VRLC.
C11	100nF	De-coupling for VRB.
C12	100nF	De-coupling for VRT.
C13	1µF	Reservoir capacitor for DVDD.
C14	1µF	Reservoir capacitor for DVDD.
C15	1µF	Reservoir capacitor for AVDD.
C16	1µF	Reservoir capacitor for AVDD.

Table 9 External Components Descriptions

APPLICATIONS RECOMMENDATIONS

INTRODUCTION

The WM8148 is a mixed signal device, therefore careful PCB layout is required. The following section contains PCB layout guidelines, which are recommended for optimal performance from the WM8148, and some typical applications circuits.

PCB LAYOUT

1) Use separate analogue and digital power and ground planes. The analogue and digital ground planes should be connected as close as possible to, or underneath, the WM8148.
2) Place all supply decoupling capacitors as close as possible to their respective supply pins and provide a low impedance path from the capacitors to the appropriate ground.
3) Avoid noise on AGND (in particular on pins 30, 35 and 40).
4) Avoid noise on reference pins VRT, VRB and VRX. Place the decoupling capacitors as close as possible to these pins and provide a low impedance path from the capacitors to analogue ground.
5) Input signals should be screened from each other and from other sources of noise to avoid cross talk and interference.
6) Minimise load capacitance on digital outputs. Capacitive loads of greater than 20pF will degrade performance. Use buffers if necessary and keep tracks short.

TYPICAL APPLICATIONS DIAGRAMS

CCDs are available in four basic types that are all compatible with the WM8148.

- Monochrome single output.
- Monochrome odd-even output.
- Colour 3 output.
- Colour 6 output.

Each of these applications is outlined in this section.

The output from a CCD sensor usually has a high impedance and must therefore be buffered as close to the sensor as possible. The sensor manufacturers' datasheets specify the buffer circuit to use.

Initially, the designer must decide if CDS and Reset Level Clamping is to be used. The WM8148 supports both of these functions and Wolfson recommend using both CDS and pixel-by-pixel clamping for optimal performance. In this case a low value a.c. coupling capacitor is required between the sensor and the WM8148. Experiments have shown that a 100pF capacitor is the optimum value to use, however this may vary for particular applications depending on speed of operation and PCB layout.

MONOCHROME SINGLE OUTPUT

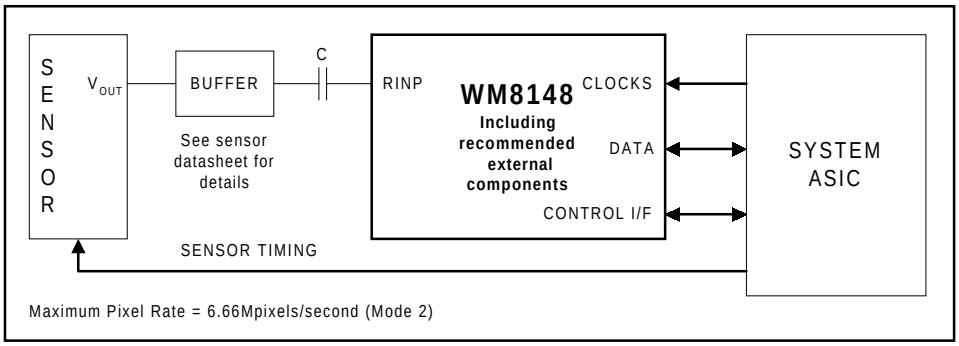


Figure 45 Block Diagram of Monochrome CCD Application

REGISTER		SETTING		NOTE
DESCRIPTION	**ADDRESS**	**HEX**	**BINARY**	
Set-up register 1	000001	22	0010 0010	MODE: Mode 2: single-channel CDS SELEN: selective power enable
Set-up register 2	000010	9F	1001 1111	SENBL: green/blue PGAs powered off
Set-up register 3	000011	02	0000 0010	CHAN: red channel selected RESREF: reset sample half-way between video samples
Set-up register 4	000101	80	1000 0000	INVOP: invert digital output (White = 4095)
Coarse offsets	000110	4B	0100 1011	PGAFS: ADC set up for negative polarity video RLCEXT, RLCV: internal VRLC voltage, set to 3.7V

Table 10 Typical Control Register Settings for Figure 45 (CDS, Negative-Going CCD Video Signal, MCLK/VSMP = 6)

MONOCHROME ODD-EVEN OUTPUT

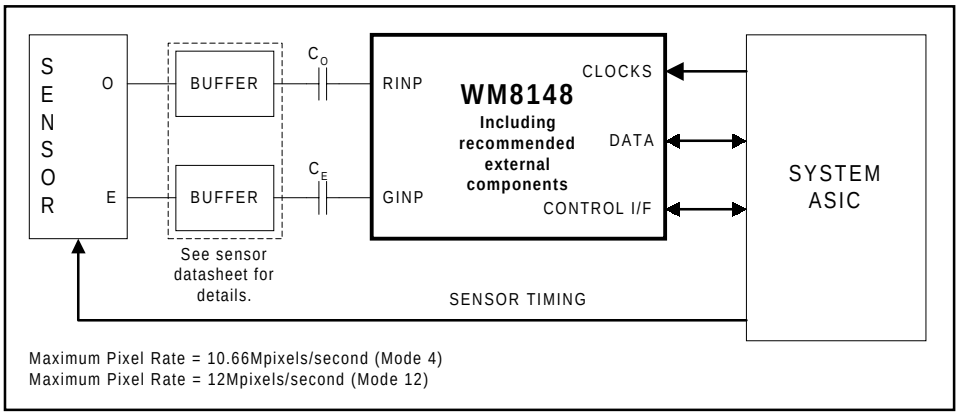


Figure 46 Block Diagram of Monochrome CCD (Odd-Even Outputs) Application

REGISTER		SETTING		NOTE
DESCRIPTION	**ADDRESS**	**HEX**	**BINARY**	
Set-up register 1	000001	42	0100 0010	MODE: Mode 4: Two-channel CDS SELEN: selective power enable
Set-up register 2	000010	BF	1011 1111	SENBL: blue PGAs powered off
Set-up register 3	000011	02	0000 0010	RESREF: reset sample half-way between video samples
Set-up register 4	000101	80	1000 0000	INVOP: invert digital output (White = 4095)
Coarse offsets	000110	4B	0100 1011	PGAFS: ADC set up for negative polarity video RLCEXT, RLCV: internal VRLC voltage, set to 3.7V

Table 11 Typical Control Register Settings for Figure 46 (CDS, Negative-Going CCD Video Signal, MCLK/VSMP = 6)

REGISTER		SETTING		NOTE
DESCRIPTION	**ADDRESS**	**HEX**	**BINARY**	
Set-up register 1	000001	C2	1100 0010	MODE: Mode 12: Two-channel CDS SELEN: selective power enable
Set-up register 2	000010	BF	1011 1111	SENBL: blue PGAs powered off
Set-up register 3	000011	02	0000 0010	CHAN: red channel selected RESREF: reset sample half-way between video samples
Set-up register 4	000101	80	1000 0000	INVOP: invert digital output (White = 4095)
Coarse offsets	000110	4B	0100 1011	PGAFS: ADC set up for negative polarity video RLCEXT, RLCV: internal VRLC voltage, set to 3.7V

Table 12 Typical Control Register Settings for Figure 46 (CDS, Negative-Going CCD Video Signal, MCLK/VSMP = 8)

COLOUR 3 OUTPUT

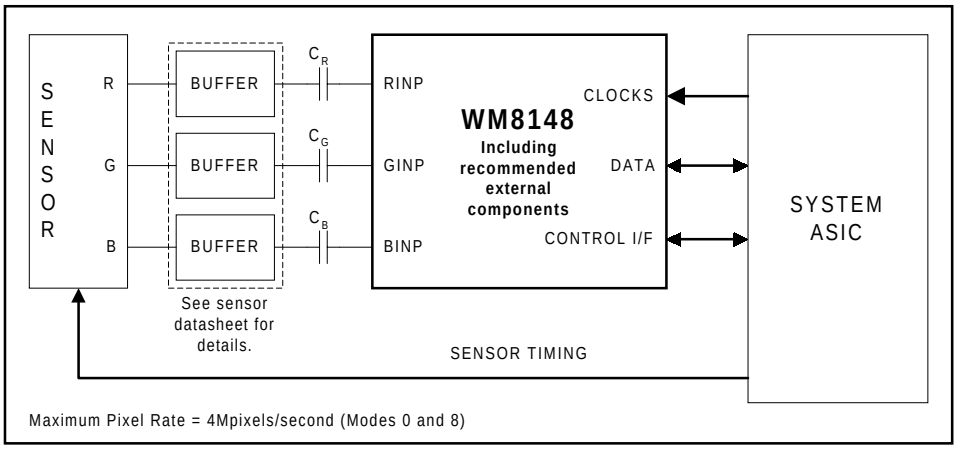


Figure 47 Block Diagram of Colour CCD Application

REGISTER		SETTING		NOTE
DESCRIPTION	**ADDRESS**	**HEX**	**BINARY**	
Set-up register 1	000001	01	0000 0001	MODE: Mode 0: Three-channel CDS (8-phase) SELEN, EN: fully enabled
Set-up register 2	000010	00	0000 0000	Default (don't care)
Set-up register 3	000011	04	0000 0100	RESREF: reset sample half-way between video samples
Set-up register 4	000101	80	1000 0000	INVOP: invert digital output (White = 4095)
Coarse offsets	000110	4B	0100 1011	PGAFS: ADC set up for negative polarity video RLCEXT, RLCV: internal VRLC voltage, set to 3.7V

Table 13 Typical Control Register Settings for Figure 47 (CDS, Negative-Going CCD Video Signal, MCLK/VSMP = 8)

REGISTER		SETTING		NOTE
DESCRIPTION	**ADDRESS**	**HEX**	**BINARY**	
Set-up register 1	000001	81	1000 0001	MODE: Mode 8: Three-channel CDS (12-phase) SELEN, EN: fully enabled
Set-up register 2	000010	00	0000 0000	Default (don't care)
Set-up register 3	000011	06	0000 0110	RESREF: reset sample half-way between video samples
Set-up register 4	000101	80	1000 0000	INVOP: invert digital output (White = 4095)
Coarse offsets	000110	4B	0100 1011	PGAFS: ADC set up for negative polarity video RLCEXT, RLCV: internal VRLC voltage, set to 3.7V

Table 14 Typical Control Register Settings for Figure 47 (CDS, Negative-Going CCD Video Signal, MCLK/VSMP = 12)

COLOUR 6 OUTPUT

For applications that require higher pixel rates, multiple WM8148 devices can be used. The following diagrams show typical configurations.

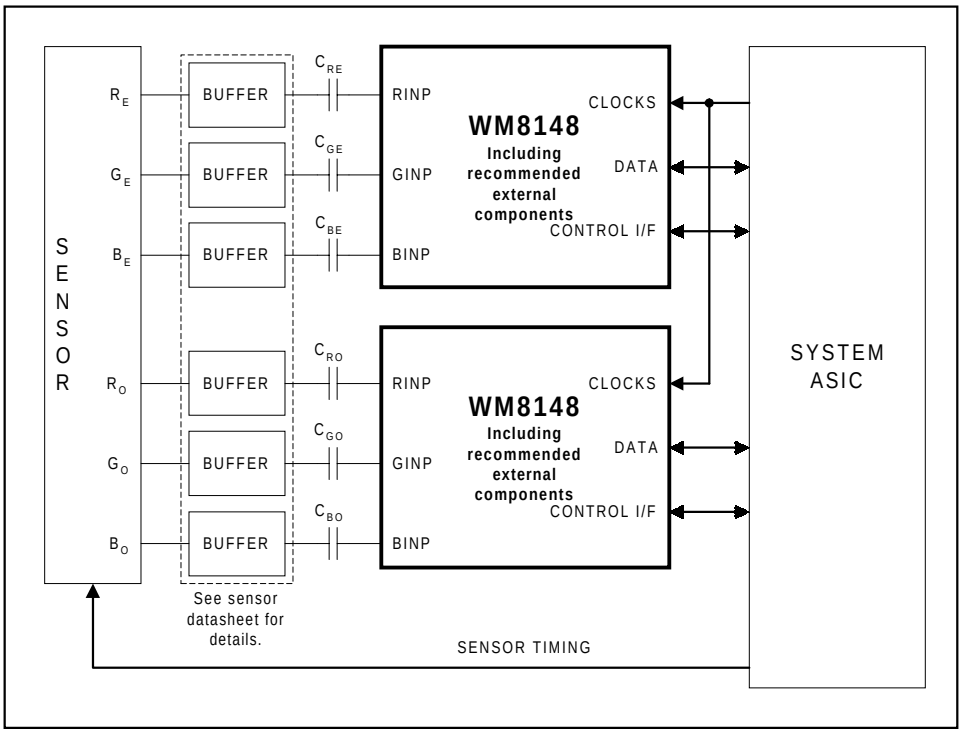


Figure 48 Block Diagram Showing Dual Architecture

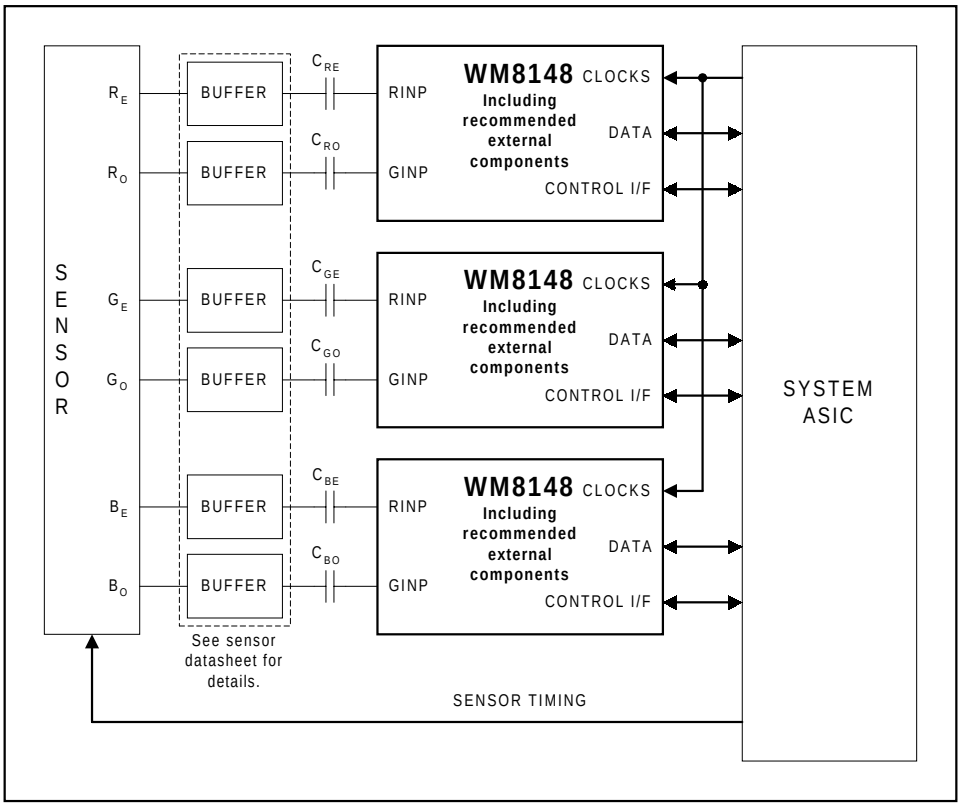
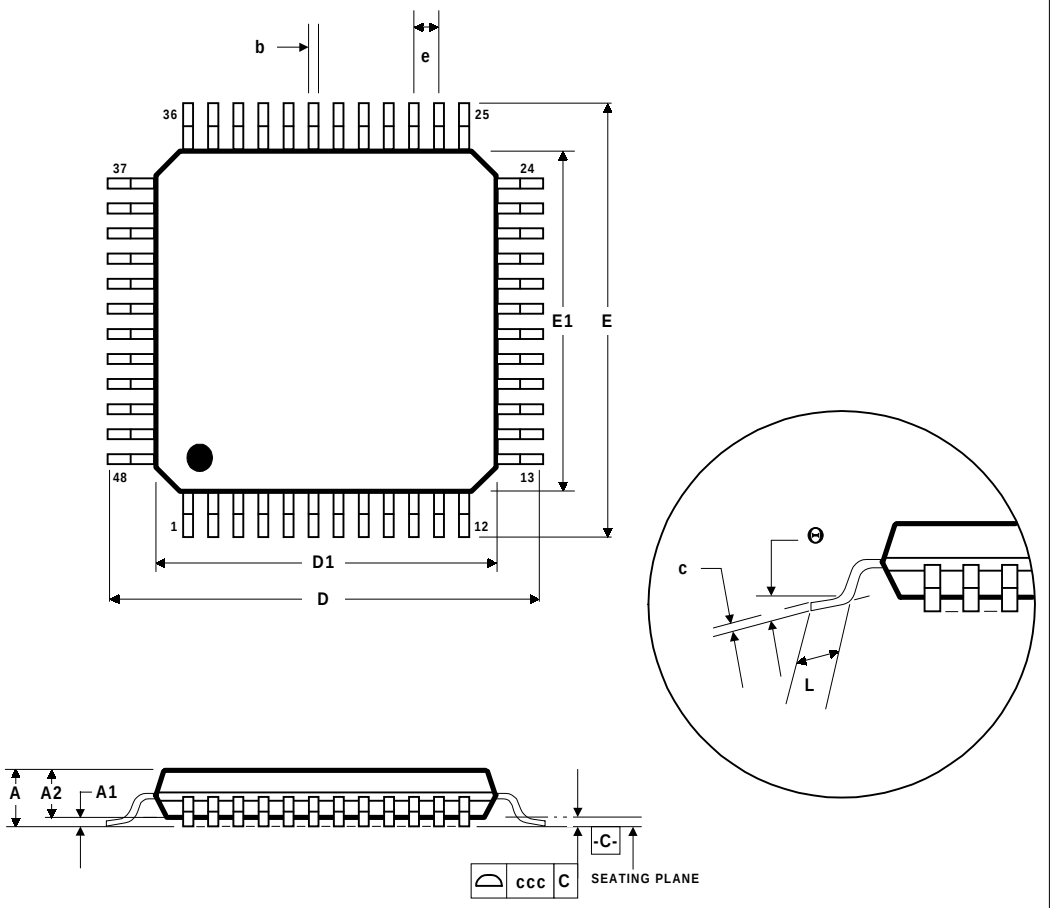


Figure 49 Block Diagram Showing Triple Architecture

PACKAGE DIMENSIONS

FT: 48 PIN TQFP (7 x 7 x 1.0 mm) **DM004.C**



Symbols	Dimensions (Millimeters)		
	MIN	NOM	MAX
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	9.00 BSC		
D_1	7.00 BSC		
E	9.00 BSC		
E_1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
Θ	0^o	3.5^o	7^o
Tolerances of Form and Position			
ccc	0.08		
REF:	JEDEC.95, MS-026		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = ABC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.