

128M-BIT CMOS MOBILE SPECIFIED RAM  
8M-WORD BY 16-BIT  
EXTENDED TEMPERATURE OPERATION**Description**

The μPD46128512-X is a high speed, low power, 134,217,728 bits (8,388,608 words by 16 bits) CMOS Mobile Specified RAM featuring asynchronous page read and random write, synchronous burst read/write function.

The μPD46128512-X is fabricated with advanced CMOS technology using one-transistor memory cell.

**Features**

- 8,388,608 words by 16 bits organization
- Asynchronous page read mode
- Synchronous read and write mode
- Burst length: 8 words / 16 words / continuous
- Clock latency: 5, 6, 7, 8, 9, 10
- Burst sequence: Linear burst
- Max clock frequency: 108/83 MHz
- Byte data control: /LB (DQ0 to DQ7), /UB (DQ8 to DQ15)
- Low voltage operation: 1.7 to 2.0 V
- Operating ambient temperature: T<sub>A</sub> = -30 to +85 °C
- Chip Enable input: /CE1 pin
- Standby Mode input: CE2 pin
- Standby Mode 1: Normal standby (Memory cell data hold valid)
- Standby Mode 2: Density of memory cell data hold is variable

μPD46128512	Clock frequency MHz (MAX.)	Asynchronous initial access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current										
					At operating mA (MAX.)	At standby μA									
						(MAX.)					(TYP.)				
						Density of data hold					Density of data hold				
						128M bits	32M bits	16M bits	8M bits	0M bits	128M bits	32M bits	16M bits	8M bits	0M bits
-E9X <sup>Note</sup>	108	70	1.7 to 2.0	-30 to +85	60	250	T.B.D.	T.B.D.	T.B.D.	65	80	T.B.D.	T.B.D.	T.B.D.	15
-E10X <sup>Note</sup>		85			50										
-E11X	83	70			60										
-E12X		85			50										

**Note** Under consideration

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**Ordering Information**

$\mu$ PD46128512-X is mainly shipping by wafer.

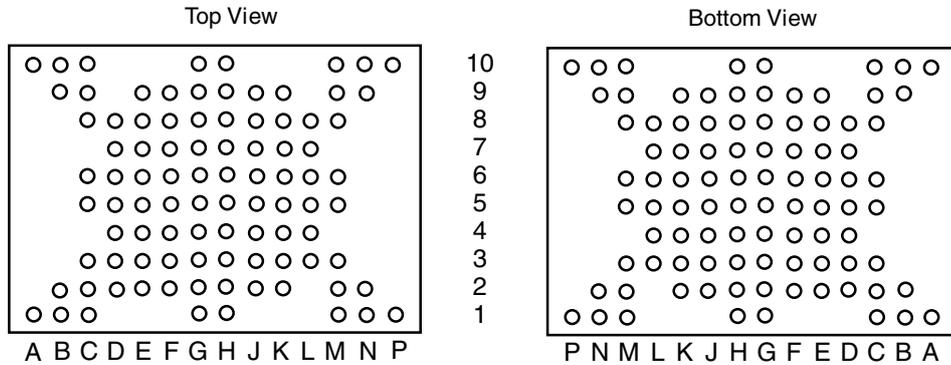
Please consult with our sales offices for package samples and ordering information.

**Pin Configuration**

The following is pin configuration of package sample.

/xxx indicates active low signal.

**93-PIN TAPE FBGA (12x9)**



		Top View													
		A	B	C	D	E	F	G	H	J	K	L	M	N	P
10		NC	NC	NC				NC	NC				NC	NC	NC
9			NC	NC		A15	A21	A22	A16	NC	V <sub>ss</sub>		NC	NC	
8				NC	A11	A12	A13	A14	NC	DQ15	DQ7	DQ14	NC		
7					A8	A19	A9	A10	DQ6	DQ13	DQ12	DQ5			
6			NC	/WE	CE2	A20	NC	NC	DQ4	V <sub>cc</sub>	NC	NC			
5			NC	CLK	/ADV	/WAIT	NC	NC	DQ3	V <sub>cc</sub>	DQ11	NC			
4				/LB	/UB	A18	A17	DQ1	DQ9	DQ10	DQ2				
3			NC	A7	A6	A5	A4	GND	/OE	DQ0	DQ8	NC			
2			NC	NC	NC	A3	A2	A1	A0	NC	/CE1		NC	NC	
1		NC	NC	NC				NC	NC				NC	NC	NC

- A0 to A22 : Address inputs
- DQ0 to DQ15 : Data inputs / outputs
- /CE1 : Chip select input
- CE2 : Standby mode input
- /WE : Write enable input
- /OE : Output enable input
- /LB, /UB : Byte data select input
- CLK : Clock input
- /ADV : Address Valid Input
- /WAIT : Wait output
- V<sub>cc</sub> : Power supply
- GND : Ground
- NC <sup>Note</sup> : No Connection

**Note** Some signals can be applied because this pin is not internally connected.

**Remark** Refer to **Package Drawing** for the index mark.



**Truth Table**  
**Asynchronous Operation**

Mode	/CE1	CE2	/ADV	/OE	/WE	/LB	/UB	DQ		/WAIT
								DQ0 to DQ7	DQ8 to DQ15	
Not selected (Standby Mode 1)	H	H	×	×	×	×	×	High-Z	High-Z	High-Z
Not selected (Standby Mode 2) <sup>Note1</sup>	×	L	×	×	×	×	×	High-Z	High-Z	High-Z
Word read	L	H	<b>Note3</b>	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	High-Z
Lower byte read						L	H	D <sub>OUT</sub>	High-Z	High-Z
Upper byte read						H	L	High-Z	D <sub>OUT</sub>	High-Z
Output disable						H	H	High-Z	High-Z	High-Z
Output disable						H	H	High-Z	High-Z	High-Z
Word write				H		×	×	High-Z	High-Z	High-Z
Lower byte write				L		L	L	D <sub>IN</sub>	D <sub>IN</sub>	High-Z
Upper byte write						L	H	D <sub>IN</sub>	High-Z	High-Z
Abort write <sup>Note2</sup>						H	L	High-Z	D <sub>IN</sub>	High-Z
						H	H	High-Z	High-Z	High-Z

- Notes**
1. CE2 pin must be fixed HIGH except Standby Mode 2 (refer to **2.3 Standby Mode Status Transition**).
  2. If /WE = LOW and /LB = /UB = HIGH, memory does not accept write data, so write operation is not available.
  3. Fixed LOW or toggle HIGH → LOW → HIGH

**Remark** H, HIGH : V<sub>IH</sub>, L, LOW : V<sub>IL</sub>, ×: V<sub>IH</sub> or V<sub>IL</sub>  
Clock pin must be fixed either LOW or HIGH.

**Burst Operation**

Mode	/CE1	CE2	CLK	/ADV	/OE	/WE	/LB	/UB	DQ		/WAIT Note8
									DQ0 to DQ7	DQ8 to DQ15	
Not selected (Standby Mode 1)	H	H	×	×	×	×	×	×	High-Z	High-Z	High-Z
Not selected (Standby Mode 2) <sup>Note1</sup>	×	L	×	×	×	×	×	×	High-Z	High-Z	High-Z
Start address latch	L	H	 Note4	L	×	×	×	×	High-Z <sup>Note5</sup>	High-Z <sup>Note5</sup>	×
Advanced burst read to next address			 Note4	H	L	H	DOUT	DOUT	Output Valid		
Burst read suspend <sup>Note2</sup>					H	HIGH					
Burst read resume <sup>Note2</sup>				L	HIGH						
Burst read termination <sup>Note3</sup>				×		×	High-Z	High-Z	High-Z		
Advanced burst write to next address			L	 Note4	H	L	DIN	DIN	Output Valid		
Burst write suspend <sup>Note2</sup>					H	HIGH					
Burst write resume <sup>Note2</sup>				L	HIGH						
Burst write termination <sup>Note3</sup>				×		×	High-Z	High-Z	High-Z		
Abort write <sup>Note6</sup>			L	×	×	×	Note10	HIGH	HIGH	High-Z	High-Z

- Notes**
- CE2 pin must be fixed HIGH except Standby Mode 2 (refer to 2.3 Standby Mode Status Transition).
  - Be sure to suspend or resume a burst read after outputting the first read access data.  
Be sure to suspend or resume a burst write after latching the first write data.  
Burst write suspend or resume is available when setting WC = 1 (/WE level control) through Mode Register Set.
  - ★** /CE1 must be fixed HIGH during t<sub>TRB</sub> specification until next read or write operation.
  - Valid clock edge shall be set either positive or negative edge through Mode Register Set.
  - If /OE = LOW and /LB = /UB = LOW, output is valid. If /OE = LOW and /LB = /UB = HIGH, output is high impedance.  
If /WE = LOW, output is high impedance. If /OE = /WE = HIGH, output is high impedance.
  - If /WE = LOW and /LB = /UB = HIGH, memory does not accept write data, so write operation is not available.
  - Both of two pins (/OE and /WE) or either of two should be connected to HIGH. It is prohibited to bring the both /OE and /WE to LOW.
  - ★** Refer to the 4.10 /WAIT.
  - For the Burst Read, the /UB, /LB setup time to CLK (t<sub>bc</sub>) must be satisfied. For the Burst Write, the /UB, /LB setup time to CLK (t<sub>bc</sub>) must be satisfied. Once /LB and /UB inputs are determined, they must not be changed until the end of burst operation.
  - ★** In case of WC = 0, /WE is HIGH.  
In case of WC = 1, /WE is LOW.  
The explanation of WC refers to Table 5-2. Mode Register Definition (5th Bus Cycle) and 5.9 /WE control.

**Remark** H, HIGH : V<sub>IH</sub>, L, LOW : V<sub>IL</sub>, ×: V<sub>IH</sub> or V<sub>IL</sub>,  : valid edge

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**1. Initialization**

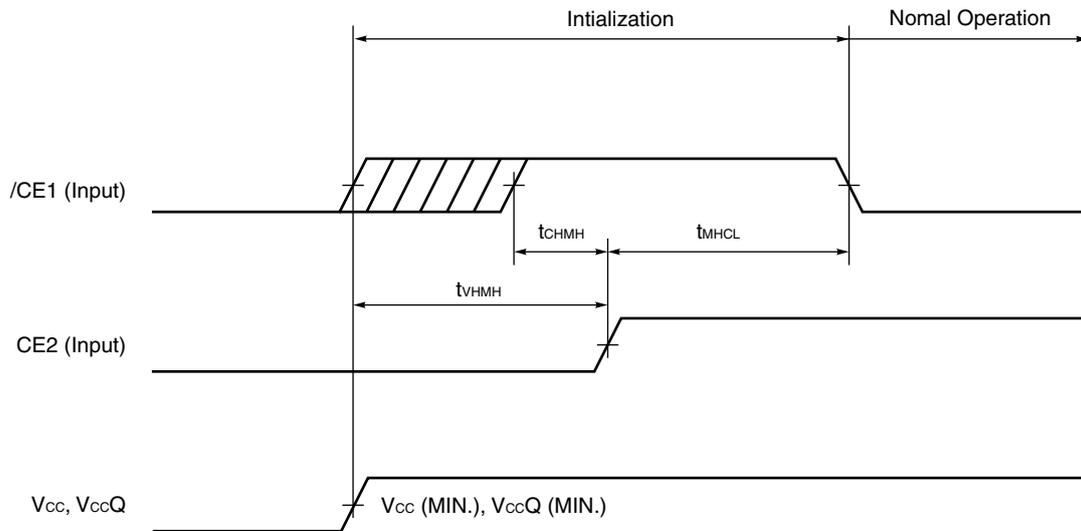
Initialize the μPD46128512-X at power application using the following sequence to stabilize internal circuits. There are 2 method of initialization.

**Initialization Timing 1**

- (1) Following power application, make CE2 HIGH after fixing CE2 to LOW for the period of  $t_{VHMH}$ . Make /CE1 HIGH before making CE2 HIGH.
- (2) /CE1 and CE2 are fixed HIGH for the period of  $t_{MHCL}$ .

Normal operation is possible after the completion of initialization.

**Figure 1-1. Initialization Timing Chart 1**



- Cautions 1. Make CE2 LOW when starting the power supply.**
- 2.  $t_{VHMH}$  is specified from when the power supply voltage reaches the prescribed minimum value ( $V_{cc} (MIN.), V_{ccQ} (MIN.)$ ).**

**Initialization Timing 1**

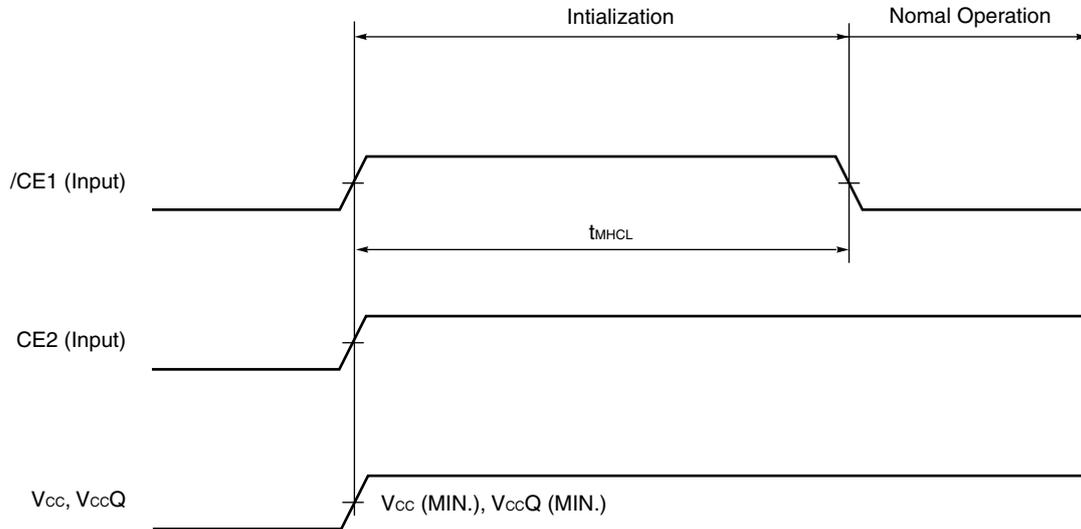
Parameter	Symbol	MIN.	MAX.	Unit
Power application to CE2 LOW hold	$t_{VHMH}$	50		μs
/CE1 HIGH to CE2 HIGH	$t_{CHMH}$	0		ns
Following power application CE2 HIGH hold to /CE1 LOW	$t_{MHCL}$	300		μs

**Initialization Timing 2**

(1) Following power application, make CE2 and /CE1 HIGH for the period of  $t_{MHCL}$ .

Normal operation is possible after the completion of initialization.

**Figure 1-2. Initialization Timing Chart 2**



- Cautions 1.**  $t_{MHCL}$  is specified from when the power supply voltage reaches the prescribed minimum value ( $V_{CC}$  (MIN.),  $V_{CCQ}$  (MIN.)).
- 2.** If the period from power supplying to value  $V_{CC}$  (MIN.),  $V_{CCQ}$  (MIN.) is beyond 10 ms or power supply is not stable rise, should be used Initialization Timing Chart 1.

**Initialization Timing 2**

Parameter	Symbol	MIN.	MAX.	Unit
Following power application /CE1, CE2 HIGH hold to /CE1 LOW	$t_{MHCL}$	300		μs

## 2. Partial Refresh

### 2.1 Standby Mode

In addition to the regular standby mode (Standby Mode 1) with a 128M bits density, Standby Mode 2, which performs partial refresh, is also provided.

### 2.2 Density Switching

In Standby Mode 2, the densities that can be selected for performing refresh are 32M bits, 16M bits, 8M bits, and 0M bit.

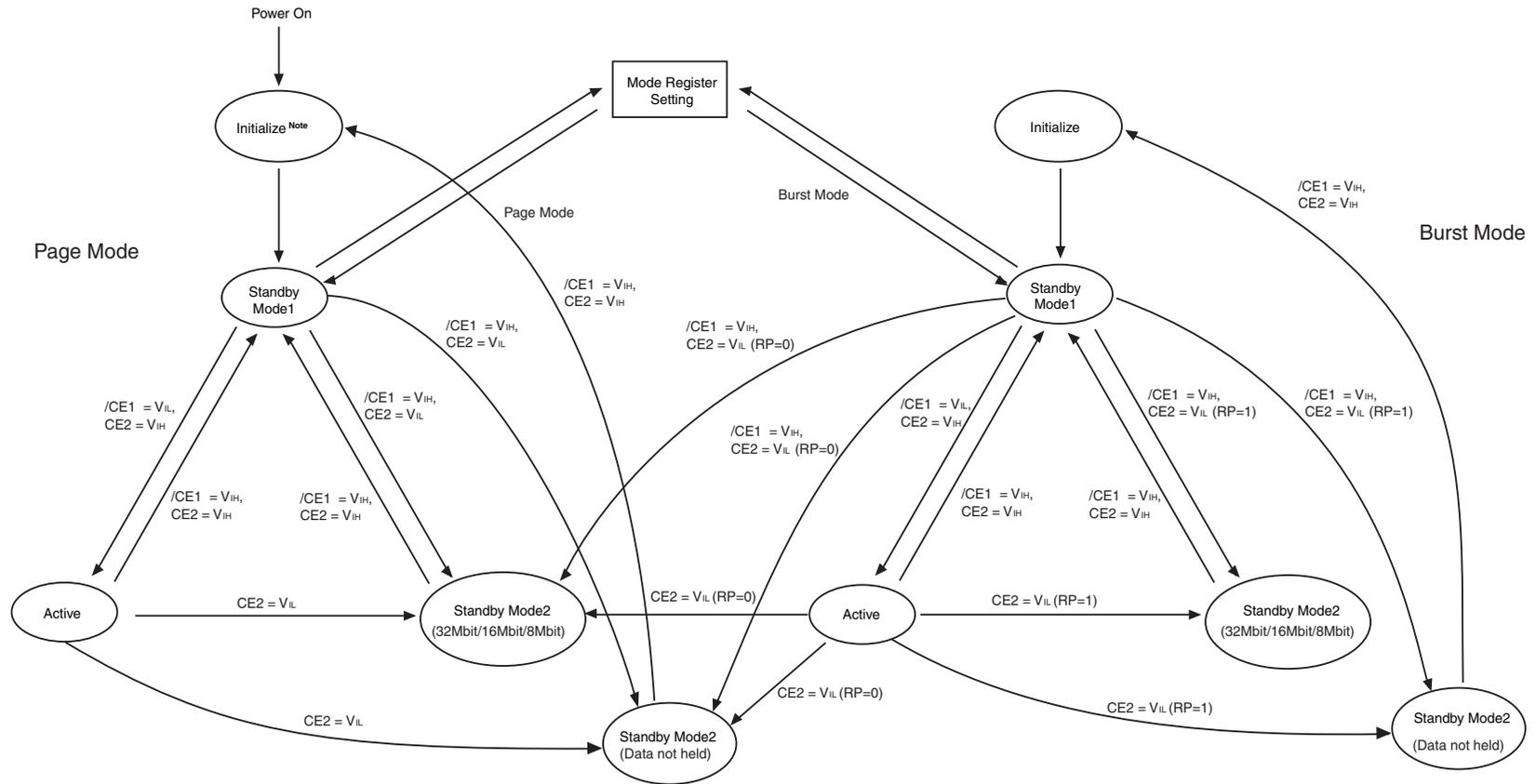
The density for performing refresh can be set with the mode register. Once the refresh density has been set in the mode register, these settings are retained until they are set again, while applying the power supply. However, the mode register setting will become undefined if the power is turned off, so set the mode register again after power application. (For how to perform mode register settings, refer to section **5. Mode Register Settings**.)

### 2.3 Standby Mode Status Transition

In Standby Mode 1, /CE1 and CE2 are HIGH. In Standby Mode 2, CE2 is LOW. In Standby Mode 2, if 0M bit is set as the density, it is necessary to perform initialization the same way as after applying power, in order to return to normal operation from Standby Mode 2. When the density has been set to 32M bits, 16M bits, or 8M bits in Standby Mode 2, it is not necessary to perform initialization to return to normal operation from Standby Mode 2.

For the timing charts, refer to **Figure 10-1. Standby Mode 2 Entry / Exit Timing Chart (Asynchronous Mode)**, **Figure 10-2. Standby Mode 2 (data not held) Entry / Exit Timing Chart (Asynchronous Mode)**.

Figure 2-1. Standby Mode State Machine



**Note** Case "Initialization Timing 2" : Following initialization, set mode register.

## 2.4 Addresses for Which Partial Refresh Is Supported

Data hold density	Correspondence address
32M bits	000000H to 1FFFFFFH
16M bits	000000H to 0FFFFFFH
8M bits	000000H to 07FFFFFFH

### 3. Page Read Operation

★ For the timing charts, refer to **Figure 7-10. Asynchronous Page Read Cycle Timing Chart.**

#### 3.1 Features of Page Read Operation

Features	Item
Page length	16 words
Page read-corresponding addresses	A3, A2, A1, A0
Page read start address	Don't care
Page direction	Don't care
Interrupt during page read operation	Enabled <sup>Note</sup>

★ **Note** /CE1 = HIGH, or any change in address A4 or higher will initiate a new read access specified as  $t_{AA}$  or  $t_{ACE}$ .

#### 3.2 Page Length

16 words is supported as the page lengths. Page length is not necessary to set through Mode Register.

#### 3.3 Page-Corresponding Addresses

The 16 words page read-enabled addresses are A3, A2, A1, and A0. Fix addresses other than A3, A2, A1, and A0 during page read operation.

#### 3.4 Page Start Address

Since random page read is supported, any address (A3, A2, A1 and A0 with the 16 words page) can be used as the page read start address.

#### 3.5 Page Direction

Since random page read is possible, there is not restriction on the page direction.

#### 3.6 Interrupt during Page Read Operation

When generating an interrupt during page read, make /CE1 HIGH or change A4 and higher addresses.

#### 3.7 When Page Read is not Used

Since random page read is supported, even when not using page read, random access is possible as usual.

#### 4. Burst Operation

Burst operation is valid when burst mode is set through mode register.

##### 4.1 Features of Burst Operation

Function	Features
Burst Length	8, 16, Continuous
Read Latency	5, 6, 7, 8, 9, 10
Write Latency	4, 5, 6, 7, 8, 9
Burst Sequence	Linear
Single Write	Single Write, Burst Write
Valid Clock Edge	Rising Edge, Falling Edge

##### 4.2 Burst Length

Burst length is the number of word to be read or written during synchronous burst read/write operation as the result of a single address latch cycle. It can be set on 8, 16words boundary or continuous for entire address through Mode Register Set sequence. Starting from initial address being latched, device internal address counter assign +1 to the previous address until reaching the end of boundary address. After completing read data out or write data latch for the set burst length, operation automatically end except for continuous burst. When continuous burst length is set, read /write is endless unless it is terminated by the rising edge of /CE1.

##### 4.3 Latency

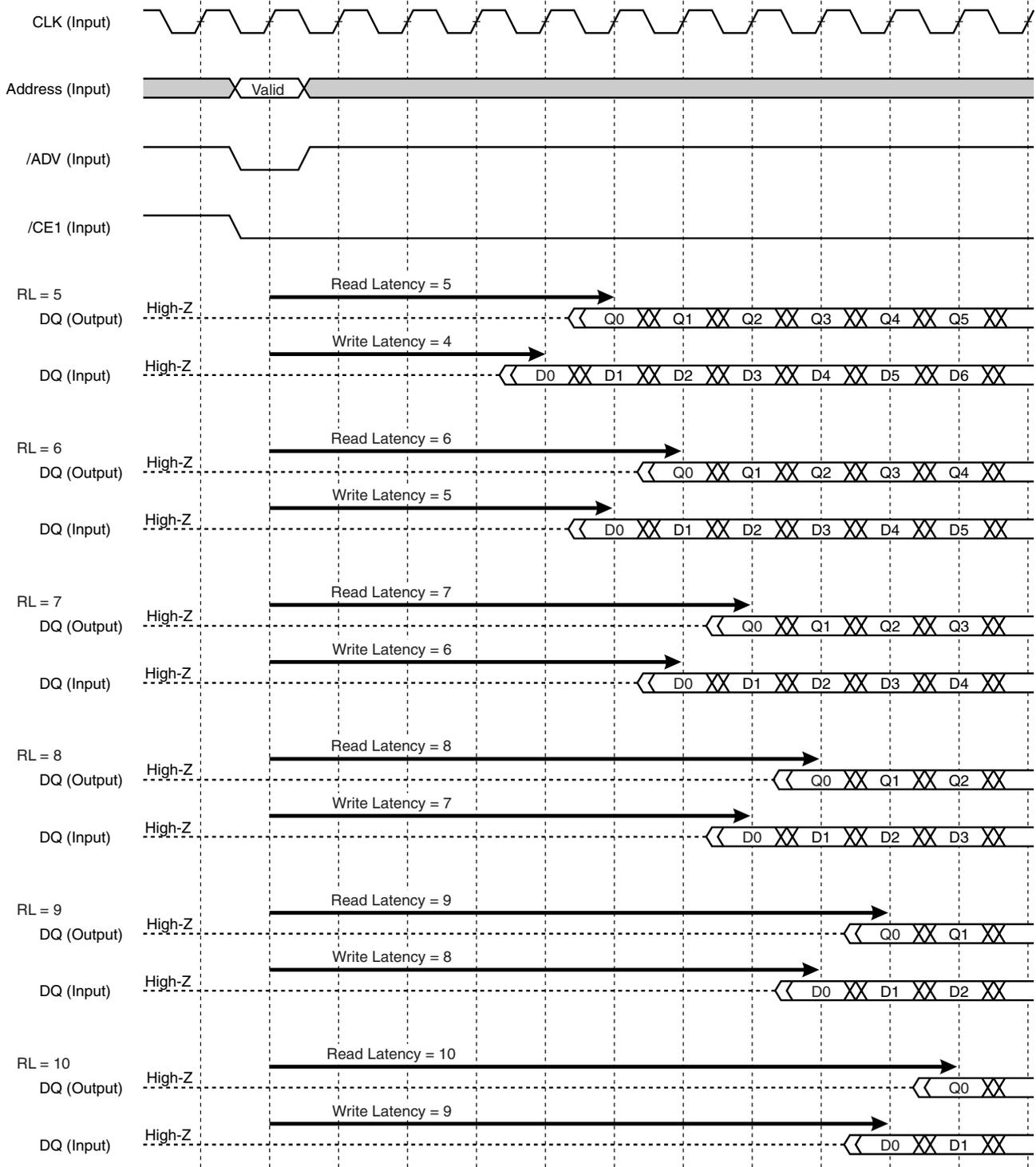
Read Latency (RL) is the number of clock cycles between the address being latched and first read data becoming available during synchronous burst read operation. It is set through Mode Register Set sequence after power application. Once RL is set through Mode Register Set sequence, write latency, that is the number of clock cycles between address being latched and first write data being latched, is automatically set to RL-1.

##### Latency Count

Grade	Clock Frequency	Asynchronous access time	Read Latency	Write Latency <sup>Note</sup>
-E9X	<108 MHz	70 ns	8, 9, 10	7, 8, 9
-E10X		85 ns	10	9
-E9X, -E11X	<83 MHz	70 ns	7, 8, 9, 10	6, 7, 8, 9
-E10X, -E12X		85 ns	8, 9, 10	7, 8, 9
-E9X, -E11X	<66 MHz	70 ns	6, 7, 8, 9, 10	5, 6, 7, 8, 9
-E10X, -E12X		85 ns	7, 8, 9, 10	6, 7, 8, 9
-E9X, -E11X	<52 MHz	70 ns	5, 6, 7, 8, 9, 10	4, 5, 6, 7, 8, 9
-E10X, -E12X		85 ns	5, 6, 7, 8, 9, 10	4, 5, 6, 7, 8, 9

**Note** Write Latency = Read Latency-1

Figure 4-1. Latency Definition



★ 4.4 Single Write

Single write operation is a single-word length synchronous write operation. The μPD46128512-X is supporting two type of synchronous write operation, “Burst Read & Single Write” and “Burst Read & Burst Write”, configurable with SW bit in the mode register. When the device set to the “Burst Read & Single Write” operation mode, the burst length at the synchronous write operation is always fixed to single word length regardless of the burst length (BL) setting in the mode register, however, BL setting is still effective in synchronous read operation (Refer to 5. Mode Register Settings).

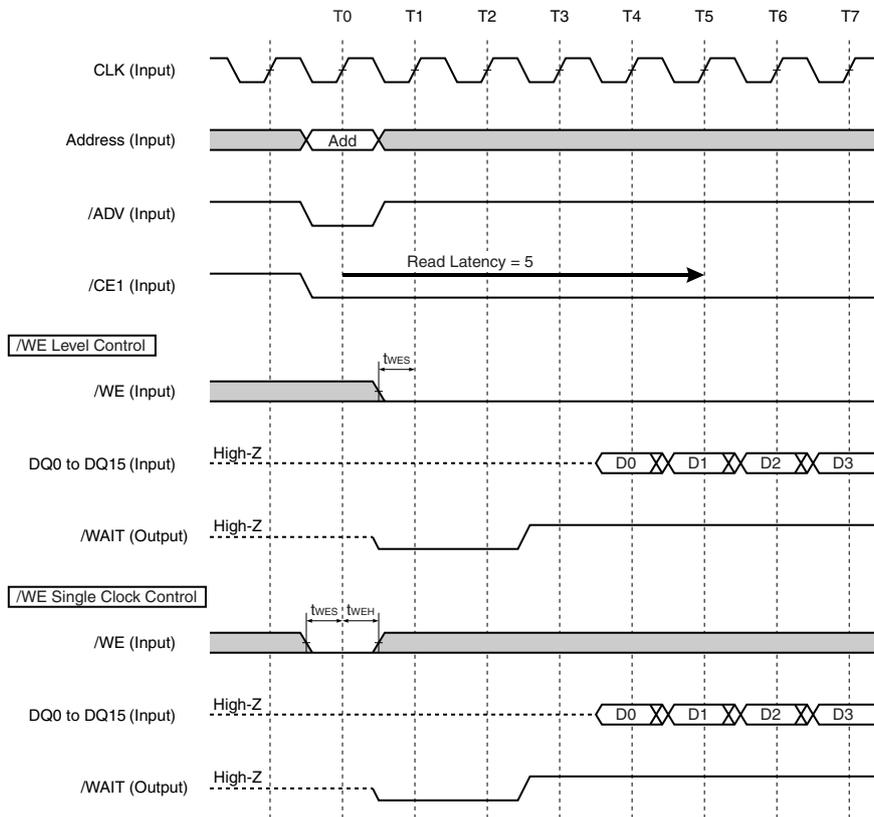
Refer to Figure 8-8. Synchronous Burst Write Cycle Timing Chart (/WE level Control), Figure 8-9. Synchronous Burst Write Cycle Timing Chart (/WE single clock control), Figure 8-10. Synchronous Single Write Timing Chart.

★ 4.5 /WE Control

The μPD46128512-X is supporting two type of timing control with /WE input signal, “/WE level control” and “/WE single clock control” configurable with WC bit in the mode register at synchronous write operation. In case of /WE level controlling, /WE must be asserted LOW before the 2nd clock input timing (T1).

Refer to Figure 8-8. Synchronous Burst Write Cycle Timing Chart (/WE level Control), Figure 8-9. Synchronous Burst Write Cycle Timing Chart (/WE single clock control).

Figure 4-2. /WE Control



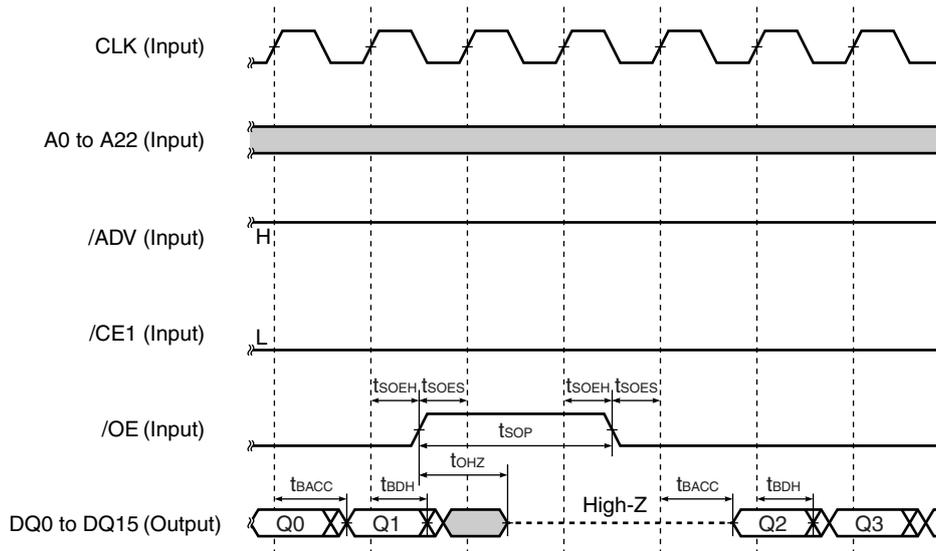
★ 4.6 Burst Read Suspend/Resume

A burst read operation can be suspended by bringing /OE signal from LOW to HIGH during the burst read operation. The /OE signal must be required to meet the specified setup / hold time to the clock which the data being suspended. Once the /OE is brought to HIGH, output data turns to be high impedance state after specific time duration.

The burst read suspend will be effective after outputting first read data, or after outputting dummy wait cycles in case of dummy wait cycling insertion at continuous burst read mode.

The burst suspend mode will be resumed by re-asserting /OE to LOW, and the first output data is from the same address location as of being suspended.

Figure 4-3. Burst Read Suspend/Resume

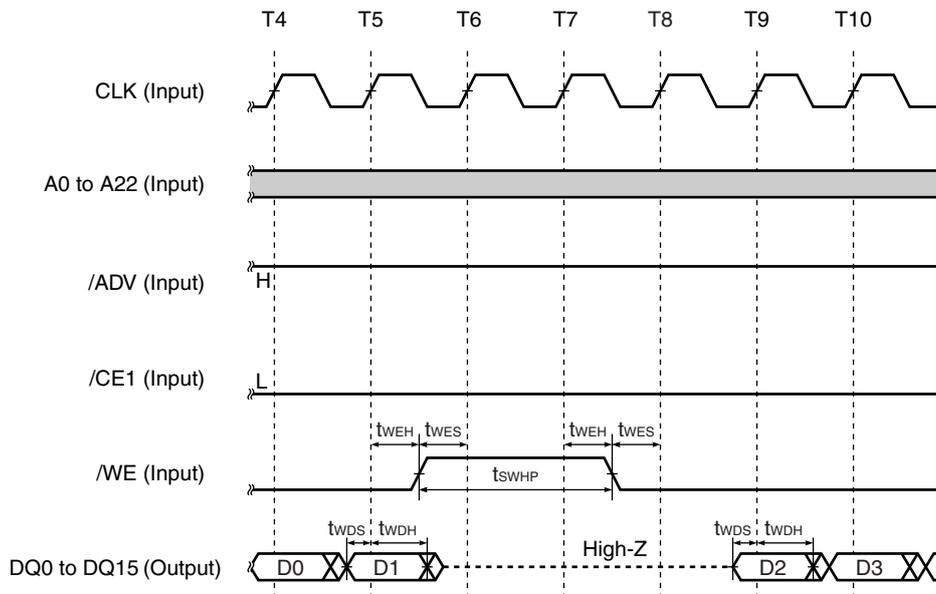


★ 4.7 Burst Write Suspend/Resume

A burst write operation can be suspended by bringing /WE signal from LOW to HIGH during the burst write operation. The /WE signal must be required to meet the specified setup / hold time to the clock which the data being suspended. The burst write suspend will be effective after inputting first write data.

The burst suspend mode will be resumed by re-asserting /WE to LOW, and the first write data is written to the same address location as of being suspended. Burst write suspend or resume is available only when WC = 1(/WE level control) is set to the mode register (refer to **Table 5-2. Mode Register Definition (5th Bus Cycle)**).

Figure 4-4. Burst Write Suspend/Resume

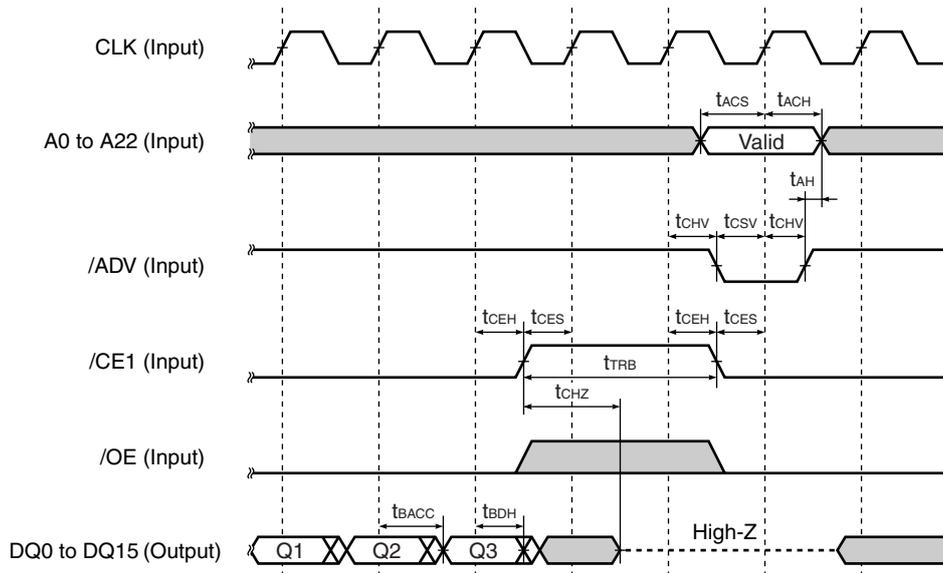


### 4.8 Burst Read Termination

Burst read termination can be performed by transferring /CE1 LOW to HIGH during the burst read. When continuous burst length is set, burst read is endless unless it is terminated. Be sure to terminate a burst read after outputting the first read access data.

In order to guarantee the last data output, the specified minimum value of /CE1 = LOW hold time ( $t_{CEH}$ ) against clock edge must be satisfied. In order to perform next operation after burst read termination, the specified minimum value of Burst Read Termination recovery time ( $t_{TRB}$ ) must be satisfied.

Figure 4-5. Burst Read Termination

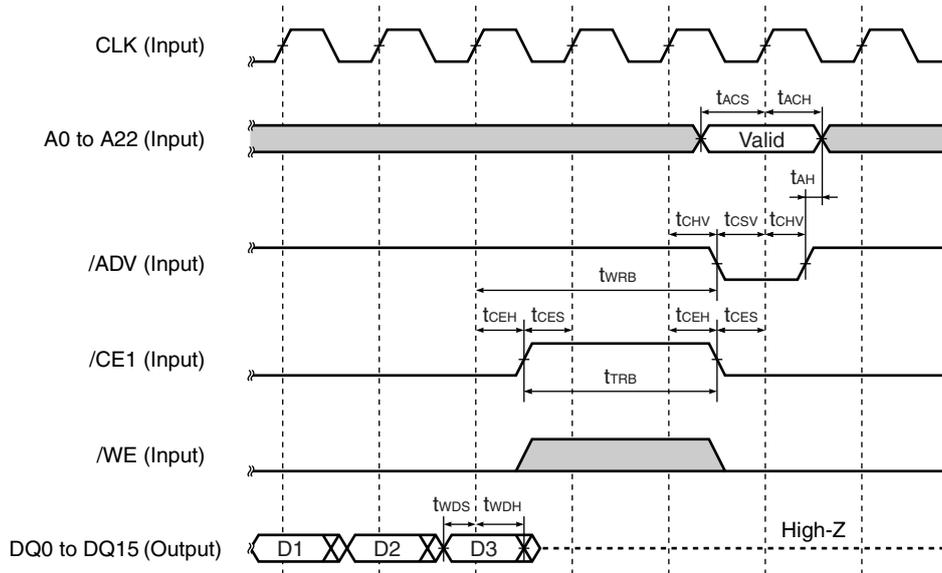


**4.9 Burst Write Termination**

Burst write termination can be performed by transferring /CE1 LOW to HIGH during the burst write. When continuous burst length is set, burst write is endless unless it is terminated. Be sure to terminate a burst write after latching the first write data.

In order to guarantee the last write data is latched, the specified minimum value of /CE1 = LOW hold time against clock edge must be satisfied. In order to perform next operation after burst write termination, the specified minimum value of Burst Write Termination recovery time ( $t_{TRB}$ ) must be satisfied.

**Figure 4-6. Burst Write Termination**



4.10 /WAIT

★ 4.10.1 Feature of /WAIT Output

The /WAIT output signal indicates the internal status, busy (LOW) or ready (HIGH), during the burst read and burst write operation.

The /WAIT output state changes depend on the /CE1 and /ADV condition. When /CE1 held entire LOW, the /WAIT output corresponds with /ADV state and turns to LOW by /ADV assertion. The /WAIT output stays high impedance at standby mode (/CE1 = HIGH) and turns to LOW at active mode brought by /CE1 assertion.

The /WAIT output will be asserted to LOW after specific time duration triggered by falling edge of /CE1, or falling edge of /ADV when /CE1 held entire LOW. When the /WAIT output LOW, it indicates the output data is not valid at the next clock cycle.

The /WAIT output asserts HIGH one clock cycle before the valid data output.

The /WAIT output retains the same state as of the clock cycle right before being suspended with /OE brought to HIGH.

Figure 4-7. Burst Read /WAIT Output (/CE1 = HIGH → LOW)

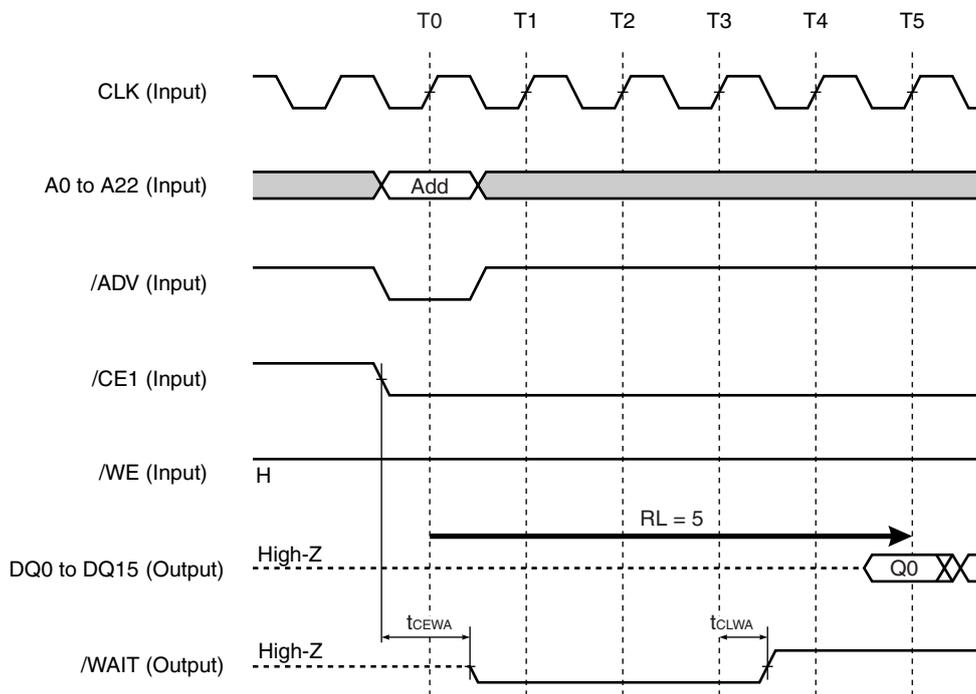
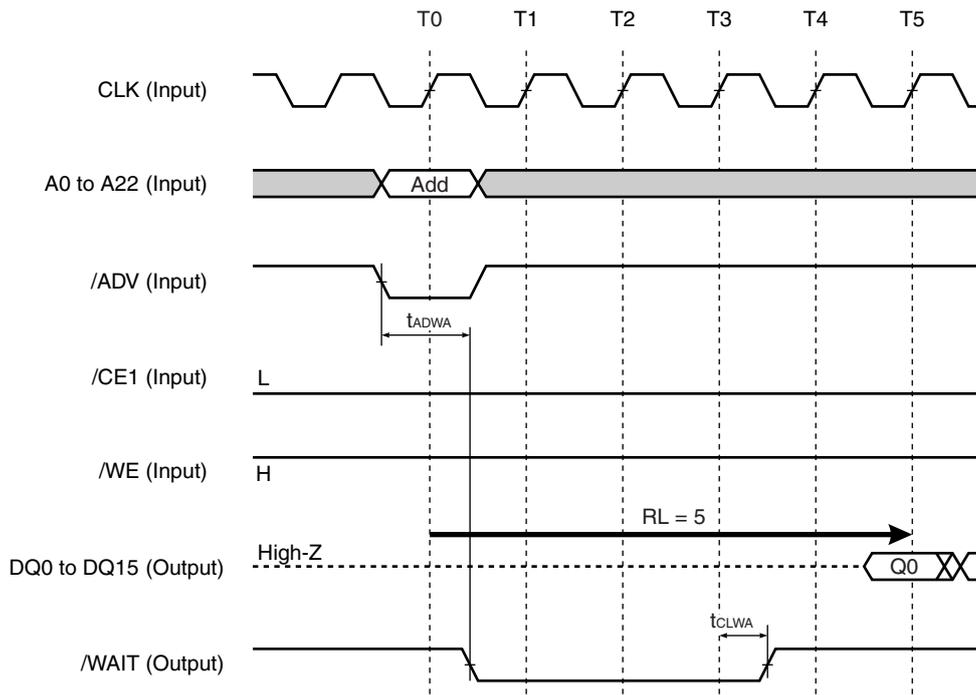


Figure 4-8. Burst Read /WAIT Output (/CE1 = LOW, /ADV = HIGH → LOW)



- ★ The /WAIT output will be asserted to LOW after specific time duration from the falling edge of the /CE1, or falling edge of the /ADV when /CE1 held LOW at burst write operation. When the /WAIT output LOW, it indicates the input data can not be accepted at the next clock cycle. The /WAIT output asserts HIGH one clock cycle before the valid data input. The /WAIT output retains the same state as of the clock cycle right before being suspended with /WE brought to HIGH. The /WAIT output always stay high impedance state under asynchronous mode setting.

Figure 4-9. Burst Write /WAIT Output (/CE1 = HIGH → LOW)

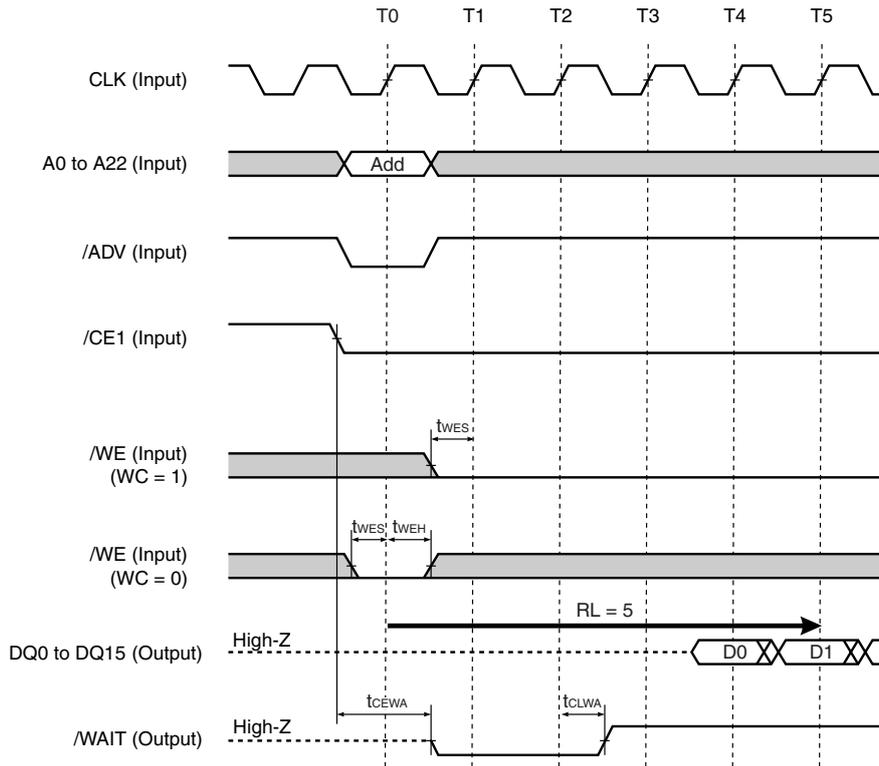
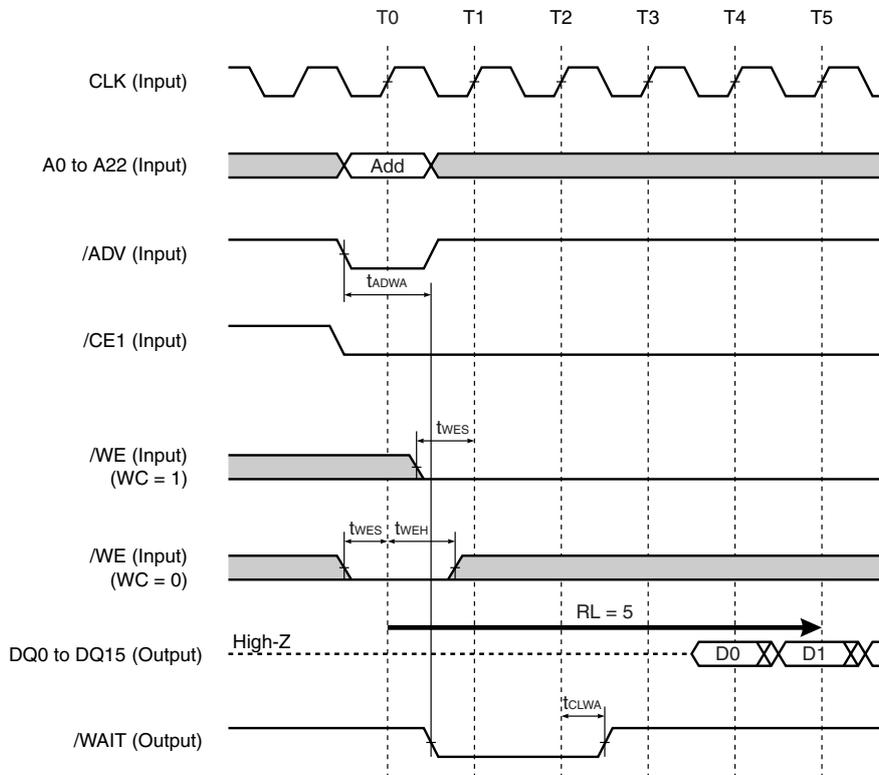


Figure 4-10. Burst Write /WAIT Output (/CE1 = LOW, /ADV = HIGH → LOW)



**4.10.2 Dummy Wait Cycles at Continuous Burst Operation**

In continuous burst operation, dummy wait cycles may be needed when a burst sequence crosses the first 16-word boundary. Whether dummy wait cycles is needed or not depends on start address and the number of dummy wait cycles depends on Read Latency (See **Table 4-1. Burst Sequence** and **4-2. Dummy Wait Cycles and Read Latency**). During the dummy cycle period, /WAIT output LOW.

**Table 4-1. Burst Sequence**

Start Address	Burst length = 8	Burst length = 16	Continuous
	Linear	Linear	Linear
xx00 H	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-...
xx01 H	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-...
xx02 H	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-...
xx03 H	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-...
xx04 H	4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19-...
xx05 H	5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-16-17-18-19-20-...
xx06 H	6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-16-17-18-19-20-21-...
xx07 H	7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-16-17-18-19-20-21-22-...
xx08 H		8-9-10-11-12-13-14-15-0-1-2-3-4-5-6-7	8-9-10-11-12-13-14-15-16-17-18-19-20-21-22-23-...
xx09 H		9-10-11-12-13-14-15-0-1-2-3-4-5-6-7-8	9-10-11-12-13-14-15-16-17-18-19-20-21-22-23-24-...
xx0A H		10-11-12-13-14-15-0-1-2-3-4-5-6-7-8-9	10-11-12-13-14-15-16-17-18-19-20-21-22-23-24-25-...
xx0B H		11-12-13-14-15-0-1-2-3-4-5-6-7-8-9-10	11-12-13-14-15- <b>W</b> -16-17-18-19-20-21-22-23-24-25-...
xx0C H		12-13-14-15-0-1-2-3-4-5-6-7-8-9-10-11	12-13-14-15- <b>W-W</b> -16-17-18-19-20-21-22-23-24-25-...
xx0D H		13-14-15-0-1-2-3-4-5-6-7-8-9-10-11-12	13-14-15- <b>W-W-W</b> -16-17-18-19-20-21-22-23-24-25-...
xx0E H		14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15- <b>W-W-W-W</b> -16-17-18-19-20-21-22-23-24-25-...
xx0F H		15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15- <b>W-W-W-W-W</b> -16-17-18-19-20-21-22-23-24-25-...
xx10 H		...	16-17-18-19-20-21-22-23-24-25-26-...
xx11 H			17-18-19-20-21-22-23-24-25-26-27-...
...	...	...	...
xxnB H			-xxnB -xxnC-xxnD-xxnE-xxnF- <b>W</b> -xx(n+1)0-xx(n+1)1-...
xxnC H			-xxnC-xxnD-xxnE-xxnF- <b>W-W</b> -xx(n+1)0-xx(n+1)1-...
xxnD H			-xxnD-xxnE-xxnF- <b>W-W-W</b> -xx(n+1)0-xx(n+1)1-...
xxnE H			-xxnE-xxnF- <b>W-W-W-W</b> -xx(n+1)0-xx(n+1)1-xx(n+1)2-...
xxnF H			-xxnF- <b>W-W-W-W-W</b> -xx(n+1)0-xx(n+1)1-xx(n+1)2-...
...	...	...	...

**Remarks 1.** The above table assumes Read Latency is set 5. **W** shows Dummy Wait Cycles.

★ **2.** Address is in HEX.

Table 4-2. Dummy Wait Cycles and Read Latency

Start Address	Read Latency = 5 (Write Latency = 4)	Read Latency = 6 (Write Latency = 5)	...	Read Latency = 9 (Write Latency = 6)	Read Latency = 10 (Write Latency = 7)	Read Latency = n (Write Latency = n-1)
xxx0 H	No wait	No wait	...	No wait	No wait	No wait
xxx1 H	No wait	No wait	...	No wait	No wait	No wait
xxx2 H	No wait	No wait	...	No wait	No wait	No wait
xxx3 H	No wait	No wait	...	No wait	No wait	No wait
xxx4 H	No wait	No wait	...	No wait	No wait	No wait
xxx5 H	No wait	No wait	...	No wait	No wait	No wait
xxx6 H	No wait	No wait	...	No wait	1 cycle	(n-9) Wait cycles are needed after boundary data output. (n = 10).
xxx7 H	No wait	No wait	...	1 cycle	2 cycle	(n-8) Wait cycles are needed after boundary data output. (n => 9)
xxx8 H	No wait	No wait	...	2 cycle	3 cycle	(n-7) Wait cycles are needed after boundary data output. (n => 8)
xxx9 H	No wait	No wait	...	3 cycle	4 cycle	(n-6) Wait cycles are needed after boundary data output. (n => 7)
xxxA H	No wait	1 cycle	...	4 cycle	5 cycle	(n-5) Wait cycles are needed after boundary data output. (n => 6)
xxxB H	1 cycle	2 cycle	...	5 cycle	6 cycle	(n-4) Wait cycles are needed after boundary data output. (n => 5)
xxxC H	2 cycle	3 cycle	...	6 cycle	7 cycle	(n-3) Wait cycles are needed after boundary data output. (n => 5)
xxxD H	3 cycle	4 cycle	...	7 cycle	8 cycle	(n-2) Wait cycles are needed after boundary data output. (n => 5)
xxxE H	4 cycle	5 cycle	...	8 cycle	9 cycle	(n-1) Wait cycles are needed after boundary data output. (n => 5)
xxxF H	5 cycle	6 cycle	...	9 cycle	10 cycle	n Wait cycles are needed after boundary data output. (n => 5)

★ Remark Address is in HEX.

**4.11 Reset Function from Synchronous Burst Mode to Asynchronous Page Mode**

Even during the burst operation mode, the μ PD46128512-X has the reset feature of changing synchronous burst mode to asynchronous page mode.

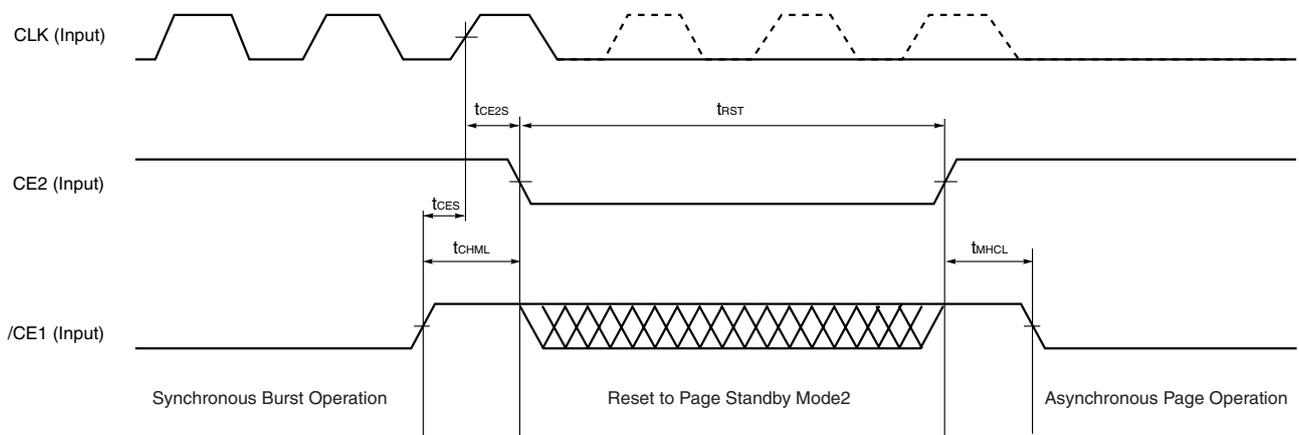
This reset is achieved by toggling CE2 signal HIGH → LOW → HIGH.

This reset to asynchronous page mode can be enable / disable with mode register setting.

Since the CE2 signal originally controls partial refresh function, the partial refresh operation can also be performed during the reset operation according to the density specified in the mode register. Please refer to the timing diagram and requirement below. Note that the timing requirement differs with the partial refresh density.

In case when the reset to asynchronous page mode is disabled in the mode register, only the partial refresh operation ★ can be performed with CE2 signal toggling. Refer to **Figure 2-1. Standby Mode State Machine.**

**Figure 4-11. Reset Entry Timing Chart to Asynchronous Page Mode**



Parameter	Symbol	MIN.	MAX.	Unit	Note
Reset to asynchronous page and standby mode2 entry /CE1 HIGH to CE2 LOW	tCHML	0		ns	
Reset to asynchronous page and standby mode2 to normal operation CE2 HIGH to /CE1 LOW	tMHCL	30		ns	1
		300		μs	2
/CE1 = HIGH setup time to CLK	tCES	5		ns	
CE2 = LOW hold time to CLK	tCE2S	1		ns	
Reset time to asynchronous page mode	tRST	70		ns	

- Notes 1.** In case the density for partial refresh are 32M bits / 16M bits / 8M bits in standby mode2
- 2.** In case the density for partial refresh is 0M bits in standby mode2

### 5. Mode Register Settings

The μPD46128512-X has several modes, Page Read mode, Burst Read mode, Burst write mode, Single Write mode, Asynchronous Write mode, Deep Power Down mode, Partial Refresh mode.

Mode Register setting defines Partial Refresh Density, Burst Length, Latency, Burst Sequence, Write mode (Burst or Single), Valid Clock Edge, Support burst write suspend/resume or not .

The several modes can be set using mode register. Since the initial value of the mode register at power application is undefined, be sure to set the mode register after initialization at power application.

#### 5.1 Mode Register Setting Method

- ★ To set each mode, write any data twice, write specific data twice, read any address in succession after the highest address (7FFFFFFH) is read (6 cycles in total).

Cycle	Operation	Address	Data
1st cycle	Read	7FFFFFFH	Read Data (RDa)
2nd cycle	Write	7FFFFFFH	RDa <sup>Note</sup> or Don't care
3rd cycle	Write	7FFFFFFH	RDa <sup>Note</sup> or Don't care
4th cycle	Write	7FFFFFFH	Code 1
5th cycle	Write	7FFFFFFH	Code 2
6th cycle	Read	Don't care	Read Data (RDb)

**Note** In order to hold the highest address (7FFFFFFH) cell data during mode register setting, be sure to set the same data with 1st cycle read data in the 2nd and 3rd cycle (write cycle).

Commands are written to the command register. The command register is used to latch the addresses and data required for executing commands, and it does not have an exclusive memory area.

For the timing chart and flow chart, refer to **Figure 9-1. Mode Register Setting Timing Chart (Asynchronous Timing + CLK fixed LOW/HIGH)**, **Figure 9-2. Mode Register Setting Timing Chart (Asynchronous Timing + toggle CLK)**, **Figure 9-3. Mode Register Setting Timing Chart (Synchronous Timing)**, **Figure 9-4. Mode Register Setting Flow Chart.** **Table 5-1, Table 5-2** shows the commands and command sequences.

#### 5.2 Cautions for Setting Mode Register

Since, for the mode register setting, the internal counter status is judged by toggling /CE1 and /OE, toggle /CE1 at every cycle during entry (one read cycle, four write cycles and one read cycle), and toggle /OE like /CE1 at the first and the 6th read cycles.

If incorrect addresses or data are written, or if addresses or data are written in the incorrect order, the setting of the mode register is not performed correctly.

Cancellation of the mode register setting must be performed before the write in the 3rd bus cycle is determined. Cancellation in the 4th bus cycle or later should not be performed. If performed, data and previous register setting are not guaranteed, so the mode register must be re-setup after the 6th bus cycle is complete.

When the highest address (7FFFFFFH) is read consecutively two or more times, the mode register setting entries are not performed correctly. Mode setting is available after power application and read or write operation other than the highest address (7FFFFFFH) are performed.

- ★ Once the several modes have been set in the mode register, these settings are retained until they are set again, while applying the power supply. However, the mode register setting will become undefined except page mode (M = 1) if the power is turned off, so set the mode register again after power application.

For the timing chart and flow chart, refer **Figure 9-1. Mode Register Setting Timing Chart (Asynchronous Timing + CLK fixed LOW/HIGH)**, **Figure 9-2. Mode Register Setting Timing Chart (Asynchronous Timing + toggle CLK)**, **Figure 9-3. Mode Register Setting Timing Chart (Synchronous Timing)**, **Figure 9-4. Mode Register Setting Flow Chart**.

**Table 5-1. Mode Register Definition (4th Bus Cycle)**

Data Code	Symbol	Function	Value	Description
DQ1, DQ0	PS	Partial Refresh Density	00	32M bit
			01	16M bit
			10	8M bit
			11	0M bit
DQ4 to DQ2	BL	Burst Length	010	8 word
			011	16 word
			111	Continuous
			Others	Reserved
DQ5	M	Function Mode	0	Burst
			1	Page
DQ6	VE	Valid Clock Edge	0	Falling Edge
			1	Rising Edge
DQ15 to DQ7	-	-	11111111	Reserved (All "1" are necessary)

**Table 5-2. Mode Register Definition (5th Bus Cycle)**

Data Code	Symbol	Function	Value	Description
DQ2 to DQ0	RL	Read Latency (Write Latency)	010	5 (Write Latency = 4)
			011	6 (5)
			100	7 (6)
			101	8 (7)
			110	9 (8)
			111	10 (9)
			Others	Reserved
DQ3	SW	Single Write	0	Burst Read & Burst Write
			1	Burst Read & Single Write
DQ4	WC	/WE Control	0	Single clock control without suspend
			1	Level control with suspend
DQ6, DQ5	-	-	11	Reserved (All "1" are necessary)
DQ7	RP	Reset to Page mode	0	Reset available to Page mode
			1	Reset not available to Page mode
DQ15 to DQ8	-	-	11111111	Reserved (All "1" are necessary)

### 5.3 Partial Refresh Density

The density for performing refresh in power down mode can be set with mode register. Setting DQ1 and DQ0 to 00 at the 4th bus cycle sets a partial refresh density of 32 M-bit hold; setting DQ1 and DQ0 to 01 at the 4th bus cycle sets a partial refresh density of 16 M-bit hold; setting DQ1 and DQ0 to 10 at the 4th bus cycle sets a partial refresh density of 8 M-bit hold; and setting DQ1 and DQ0 to 11 at the 4th bus cycle sets a partial refresh density of 0 (no hold).

Since the Partial Refresh mode is not entered unless CE2 = LOW, when partial refresh is not used, it is not necessary to set the mode register.

### 5.4 Burst Length

Sets the burst length in the burst mode. Setting DQ4 to DQ2 to 010 at the 4th bus sets 8word of burst length; setting DQ4 to DQ2 to 011 at the 4th bus cycle sets 16word of burst length; setting DQ4 to DQ2 to 111 at the 4th bus cycle sets continuous of burst length

### 5.5 Function Mode

Select function mode. Setting DQ5 to 0 at the 4th bus sets a function mode of burst and setting DQ5 to 1 at the 4th bus sets a function mode of page. After power application, page mode is set as an initial state.

### 5.6 Valid Clock Edge

Select valid clock edge (Rising edge or Falling edge) in the burst mode. Setting DQ6 to 0 at the 4th bus cycle sets clock falling edge; setting DQ6 to 1 at the 4th bus cycle sets clock rising edge.

### 5.7 Read Latency (Write Latency)

Sets the number of clock cycles (latency) between the address input and the output of the first data in the burst read mode, the address input and the write data input in the burst write mode. Setting DQ2 to DQ0 to 010 at the 5th bus cycle sets read latency of 5; setting DQ2 to DQ0 to 011 at the 5th bus sets read latency of 6; setting DQ2 to DQ0 to 100 at the 5th bus sets read latency of 7; setting DQ2 to DQ0 to 101 at the 5th bus sets read latency of 8; setting DQ2 to DQ0 to 110 at the 5th bus sets read latency of 9; setting DQ2 to DQ0 to 111 at the 5th bus sets read latency of 10. Once specific RL is set through Mode Register Setting sequence, write latency, that is the number of clock cycles between address input and first write data input, is automatically set to RL-1.

For the latency count, refer to **Figure 4-1. Latency Definition**

### 5.8 Single Write

Sets the write mode. Setting DQ3 to 0 at the 5th bus cycle sets burst write mode; setting DQ3 to 1 at the 5th bus cycle sets single write mode.

### 5.9 /WE Control

Sets the /WE timing in burst write operation and burst write suspend / resume available or not. Setting DQ4 to 0 at the 5th bus cycle sets /WE single clock control, and burst write suspend / resume are not supported. In single clock control, /WE is available at the 1st clock edge of /ADV = LOW; setting DQ4 to 1 at the 5th bus cycle sets /WE level control, and burst write suspend / resume are supported. In level control, /WE is sure to transfer LOW to HIGH after latching last write data in burst write operation.

Refer to **Figure 8-8. Synchronous Burst Write Cycle Timing Chart (/WE level Control)**, **Figure 8-9. Synchronous Burst Write Cycle Timing Chart (/WE single clock control)**, **Figure 8-11. Synchronous Burst Write Suspend Timing Chart**.

### 5.10 Reset to Page Mode

Sets the Reset function from synchronous burst mode to asynchronous page mode. Setting DQ7 to 0 at the 5th bus cycle sets reset available from synchronous burst mode to asynchronous page mode. Setting DQ7 to 1 at the 5th bus cycle sets reset unavailable.

### 5.11 Reserved Bits

Reserved bits must be 1 because reserved bits are used for internal test mode entry. Be sure to set DQ15 to DQ7 to 1 at the 4th and DQ15 to DQ8 and DQ6 and DQ5 at the 5th bus cycles.

★ 5.12 Cautions for Timing Chart of Setting Mode Register

Timing charts for setting mode register are following 3 methods.

- <Setting 1> Setting method by CLK fixed HIGH or LOW at asynchronous timing (asynchronous timing)
- <Setting 2> Setting method by toggling CLK at asynchronous timing (asynchronous timing+ toggle CLK)
- <Setting 3> Setting method at synchronous timing (synchronous timing)

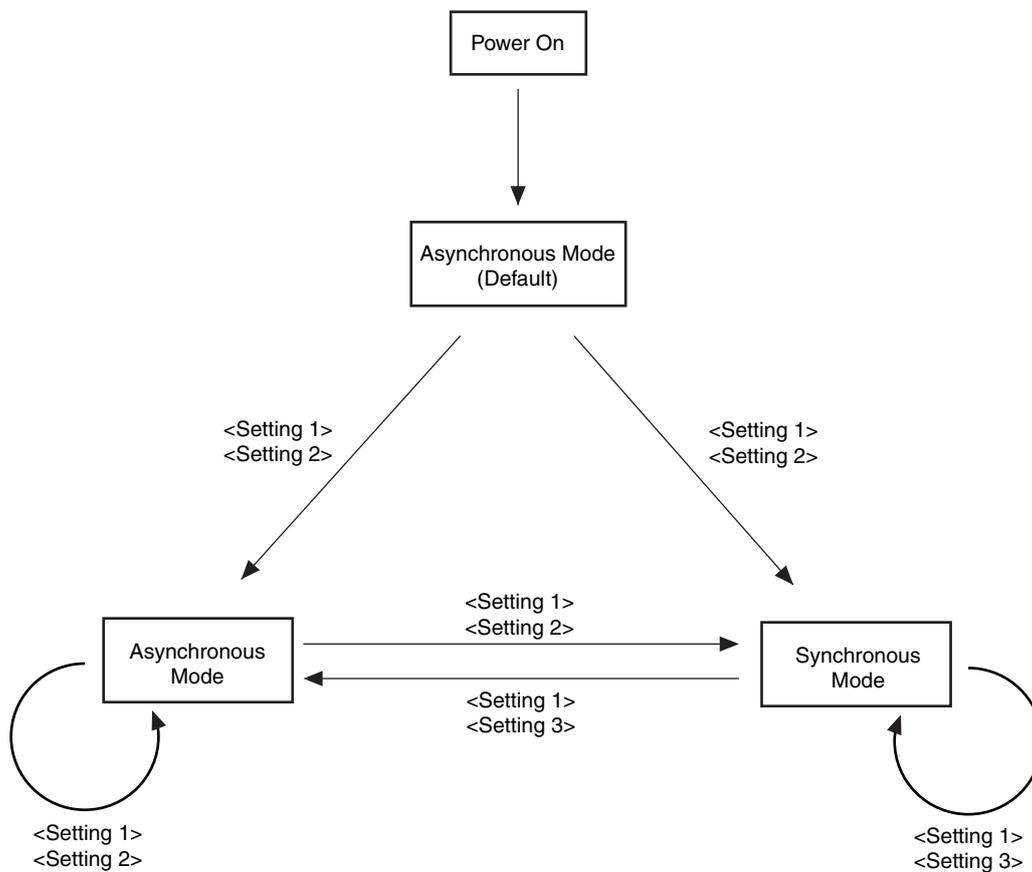
For timing chart, refer to **Figure 9-1. Mode Register Setting Timing Chart (asynchronous timing+ CLK fixed LOW/HIGH)**, **Figure 9-2. Mode Register Setting Timing Chart (asynchronous timing+ toggle CLK)**, **Figure 9-3. Mode Register Setting Timing Chart (synchronous timing)**.

It is recommended to set Mode Register contents through <Setting 1>, since <Setting 1> is used regardless of device status, asynchronous or synchronous.

<Setting 2> procedure can be performed when the device is in the asynchronous (page) mode. In case the mode register setting is possible only with <Setting 2> procedure, "reset to page" function using the CE2 signal toggling will be required in changing the operation from synchronous (burst) mode to asynchronous (page) mode. (Refer to **4.11 Reset Function from Synchronous Burst Mode to Asynchronous Page Mode**)

<Setting 3> procedure can be performed when the device is in the synchronous (burst) mode.

Figure 5-1. Mode Register Setting State Machine



## 6. Electrical Specifications

### Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V <sub>CC</sub>		-0.5 <sup>Note</sup> to +2.5	V
Supply voltage for Output	V <sub>CCQ</sub>		-0.5 <sup>Note</sup> to +2.5	V
Input / Output voltage	V <sub>T</sub>		-0.5 <sup>Note</sup> to 2.5	V
Operating ambient temperature	T <sub>A</sub>		-30 to +85	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

**Note** -1.0 V (MIN.) (Pulse width: 30 ns)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply voltage	V <sub>CC</sub> <sup>Note1</sup>		1.7	2.0	V
Supply voltage for Output	V <sub>CCQ</sub> <sup>Note1</sup>		1.7	2.0	V
Input HIGH voltage	V <sub>IH</sub>		0.8V <sub>CC</sub>	V <sub>CC</sub> +0.3	V
Input LOW voltage	V <sub>IL</sub>		-0.3 <sup>Note2</sup>	0.2V <sub>CC</sub>	V
Operating ambient temperature	T <sub>A</sub>		-30	+85	°C

**Notes 1.** Use same voltage condition (V<sub>CC</sub> = V<sub>CCQ</sub>)

**2.** -0.5 V (MIN.) (Pulse width: 30 ns)

### Capacitance (T<sub>A</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V			8	pF
Input / Output capacitance	C <sub>DQ</sub>	V <sub>DQ</sub> = 0 V			10	pF

**Remarks 1.** V<sub>IN</sub>: Input voltage, V<sub>DQ</sub>: Input / Output voltage

**2.** These parameters are not 100% tested.

**DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

Parameter	Symbol	Test condition	Density of data hold	MIN.	TYP. <sup>Note1</sup>	MAX.	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = 0 V to V <sub>CC</sub>		-1.0		+1.0	μA
DQ leakage current	I <sub>LO</sub>	V <sub>DQ</sub> = 0 V to V <sub>CCQ</sub> , /CE1 = V <sub>IH</sub> or /WE = V <sub>IL</sub> or /OE = V <sub>IH</sub>		-1.0		+1.0	μA
Operating supply current	I <sub>CCA1</sub>	/CE1 = V <sub>IL</sub> , I <sub>DQ</sub> = 0 mA, Asynchronous mode	Cycle time = 70 ns			60	mA
			Cycle time = 85 ns			50	
	I <sub>CCA2</sub>	/CE1 = V <sub>IL</sub> , Frequency = 83 MHz, RL = 7, I <sub>DQ</sub> = 0 mA, burst length = 1, Synchronous mode				50	mA
Operating supply Burst current	I <sub>CCA3</sub>	/CE1 = V <sub>IL</sub> , Frequency = 83MHz, RL = 7, I <sub>DQ</sub> = 0 mA, burst length = Continuous				30	mA
Standby supply current	I <sub>SB1</sub>	/CE1 ≥ V <sub>CC</sub> - 0.2 V, CE2 ≥ V <sub>CC</sub> - 0.2 V	128M bits <sup>Note2</sup>		80	250	μA
			32M bits <sup>Note2</sup>		T.B.D.	T.B.D.	
			16M bits <sup>Note2</sup>		T.B.D.	T.B.D.	
			8M bits <sup>Note2</sup>		T.B.D.	T.B.D.	
			0M bit		15	65	
Output HIGH voltage	V <sub>OH</sub>	I <sub>OH</sub> = -0.5 mA		0.8V <sub>CCQ</sub>			V
Output LOW voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1 mA				0.2V <sub>CCQ</sub>	V

**Notes 1.** TYP. means reference value measured at T<sub>A</sub> = 25°C. This value is not a guarantee value.

- The current measured more than 30 ms after standby mode entry (/CE1 changes from LOW to HIGH). It is specified as 2 mA (MAX.) in case of less than 30 ms after /CE1 transition.

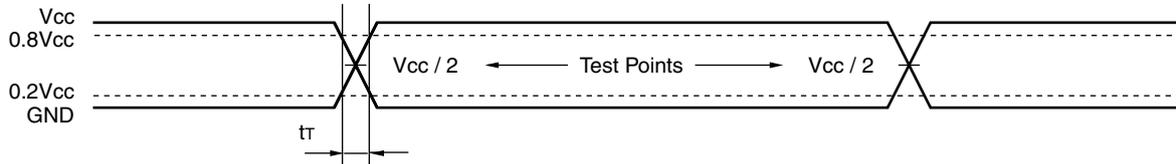
**Remark** V<sub>IN</sub>: Input voltage, V<sub>DQ</sub>: Input / Output voltage

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

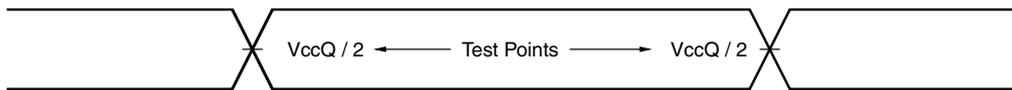
[For DQ pins]

Input Waveform (Rise and Fall Time ≤ 3 ns)



Parameter	Symbol	Test Condition	MAX.	Unit
Transition time	$t_r$	The transition time from $0.8V_{CC}$ to $0.2V_{CC}$ and from $0.2V_{CC}$ to $0.8V_{CC}$	3	ns

Output Waveform

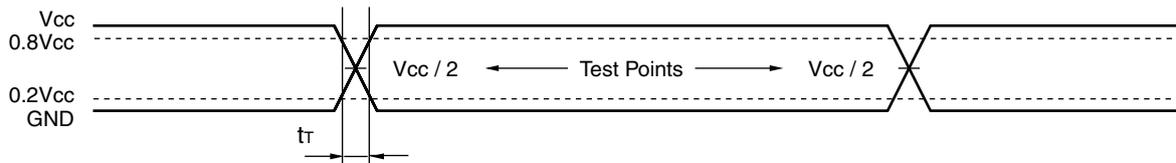


Output Load

30 pF

[For all other input pins]

Input Waveform (Rise and Fall Time ≤ 3 ns)



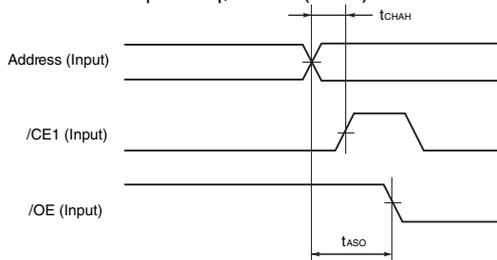
Parameter	Symbol	Test Condition	MAX.	Unit
Transition time	$t_r$	The transition time from $0.8V_{CC}$ to $0.2V_{CC}$ and from $0.2V_{CC}$ to $0.8V_{CC}$	3	ns

7. Asynchronous AC Specification, Timing Chart

Asynchronous Read Cycle

Parameter	Symbol	-E9X, -E11X		-E10X, -E12X		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t <sub>RC</sub>	70		85		ns	1
Address access time	t <sub>AA</sub>		70		85	ns	
/CE1 access time	t <sub>ACE</sub>		70		85	ns	
/OE to output valid	t <sub>OE</sub>		45		60	ns	
/LB, /UB to output valid	t <sub>BA</sub>		45		60	ns	
Output hold from address change	t <sub>OH</sub>	3		3		ns	
Page read cycle time	t <sub>PRC</sub>	20		25		ns	
Page access time	t <sub>PAA</sub>		20		25	ns	
/CE1 to output in low impedance	t <sub>CLZ</sub>	10		10		ns	2
/OE to output in low impedance	t <sub>OLZ</sub>	5		5		ns	
/LB, /UB to output in low impedance	t <sub>BLZ</sub>	5		5		ns	
/CE1 to output in high impedance	t <sub>CHZ</sub>		9		9	ns	
/OE to output in high impedance	t <sub>OHZ</sub>		9		9	ns	
/LB, /UB to output in high impedance	t <sub>BHZ</sub>		9		9	ns	
Address set to /CE1 LOW	t <sub>ASC</sub>	-15		-15		ns	
Address invalid time	t <sub>AX</sub>		15		15	ns	3
Address set to /OE LOW	t <sub>ASO</sub>	0		0		ns	
/OE HIGH to address hold	t <sub>OH AH</sub>	-5		-5		ns	
/CE1 HIGH to address hold	t <sub>CH AH</sub>	0		0		ns	4
/CE1 LOW to /OE LOW	t <sub>CLOL</sub>	-5	+10,000	-5	+10,000	ns	
/OE LOW to /CE1 HIGH	t <sub>OLCH</sub>	45		60		ns	
Address set to /ADV HIGH	t <sub>ASV</sub>	7		7		ns	
/ADV HIGH to address hold	t <sub>AH</sub>	3		3		ns	
/ADV LOW pulse width	t <sub>VPL</sub>	7		7		ns	
/CE1 HIGH pulse width	t <sub>CP</sub>	10		10		ns	
/LB, /UB HIGH pulse width	t <sub>BP</sub>	10		10		ns	
/OE HIGH pulse width	t <sub>OP</sub>	10	10,000	10	10,000	ns	5
/OE HIGH to /WE set	t <sub>OES</sub>	10	10,000	10	10,000	ns	
/WE HIGH to /OE set	t <sub>OEH</sub>	10	10,000	10	10,000	ns	

- Notes 1. Output load: 30 pF
- 2. Output load: 5 pF
- 3. t<sub>AX</sub> (MAX.) is applied while /CE1, /OE and /ADV are being hold at LOW.
- 4. When t<sub>ASO</sub> ≥ |t<sub>CH AH</sub>|, t<sub>CH AH</sub> (MIN.) is -15 ns.

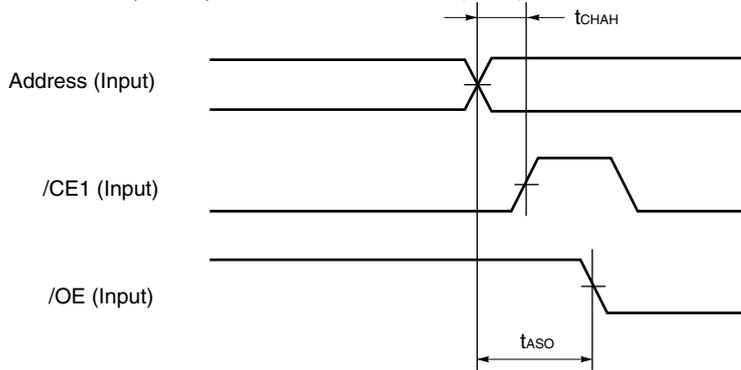


- 5. t<sub>OP</sub>, t<sub>OES</sub> and t<sub>OEH</sub> (MAX.) are applied while /CE1 is being hold at LOW.

**Asynchronous Write Cycle**

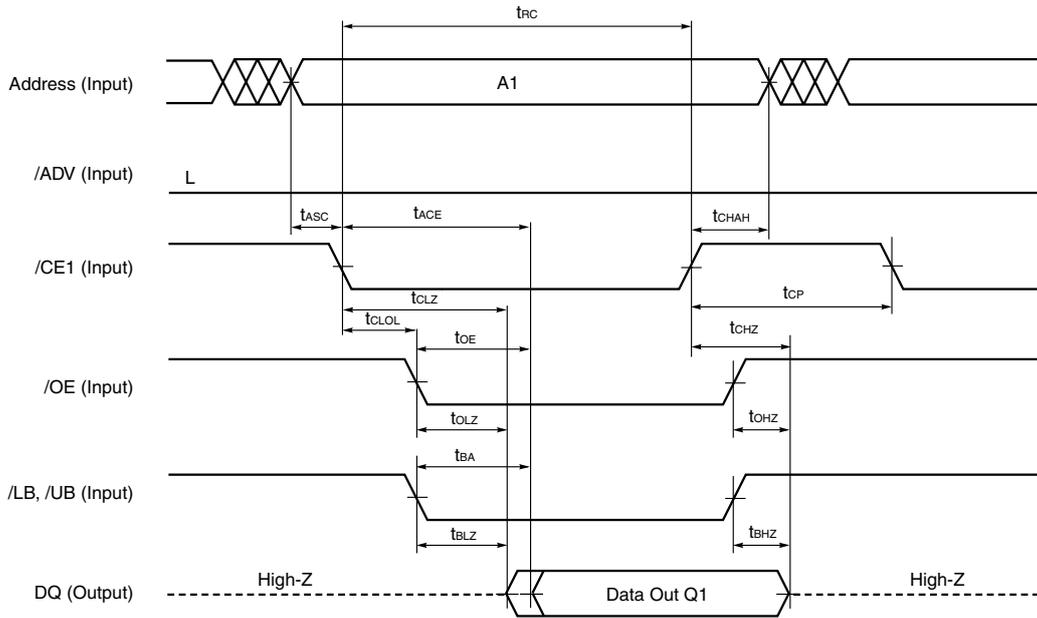
Parameter	Symbol	-E9X, -E11X		-E10X, -E12X		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t <sub>WC</sub>	70		85		ns	
/CE1 to end of write	t <sub>CW</sub>	50		60		ns	
Address valid to end of write	t <sub>AW</sub>	55		60		ns	
/LB, /UB to end of write	t <sub>BW</sub>	50		60		ns	
Write pulse width	t <sub>WP</sub>	50		55		ns	
Write recovery time	t <sub>WR</sub>	0		0		ns	
Write recovery time (/WE = HIGH → /CE1 = HIGH)	t <sub>WHCH</sub>	0	10,000	0	10,000	ns	
/CE1 pulse width	t <sub>CP</sub>	10		10		ns	
/LB, /UB HIGH pulse width	t <sub>BP</sub>	10		10		ns	
/WE HIGH pulse width	t <sub>WHP</sub>	10		10		ns	
/WE HIGH pulse width (/CE1 = LOW)	t <sub>WHP1</sub>	10	10,000	10	10,000	ns	
Address setup time	t <sub>AS</sub>	0		0		ns	
/CE1 HIGH to address hold	t <sub>CHAH</sub>	0		0		ns	1
/LB, /UB HIGH to address hold	t <sub>BHAH</sub>	0		0		ns	
/LB, /UB byte mask setup time	t <sub>BS</sub>	0		0		ns	
/LB, /UB byte mask hold time	t <sub>BH</sub>	0		0		ns	
/LB, /UB byte mask over wrap time	t <sub>BWO</sub>	30		30		ns	
Data valid to end of write	t <sub>DW</sub>	25		25		ns	
Data hold time	t <sub>DH</sub>	0		0		ns	
Address set to /ADV HIGH	t <sub>ASV</sub>	7		7		ns	
/ADV HIGH to address hold	t <sub>AH</sub>	3		3		ns	
/ADV LOW pulse width	t <sub>VPL</sub>	7		7		ns	
/OE HIGH to /WE set	t <sub>OES</sub>	10	10,000	10	10,000	ns	2
/WE HIGH to /OE set	t <sub>OEH</sub>	10	10,000	10	10,000	ns	

**Notes 1.** When t<sub>AS</sub> ≥ |t<sub>CHAH</sub>| and t<sub>CP</sub> ≥ 18 ns, t<sub>CHAH</sub> (MIN.) is -15 ns.



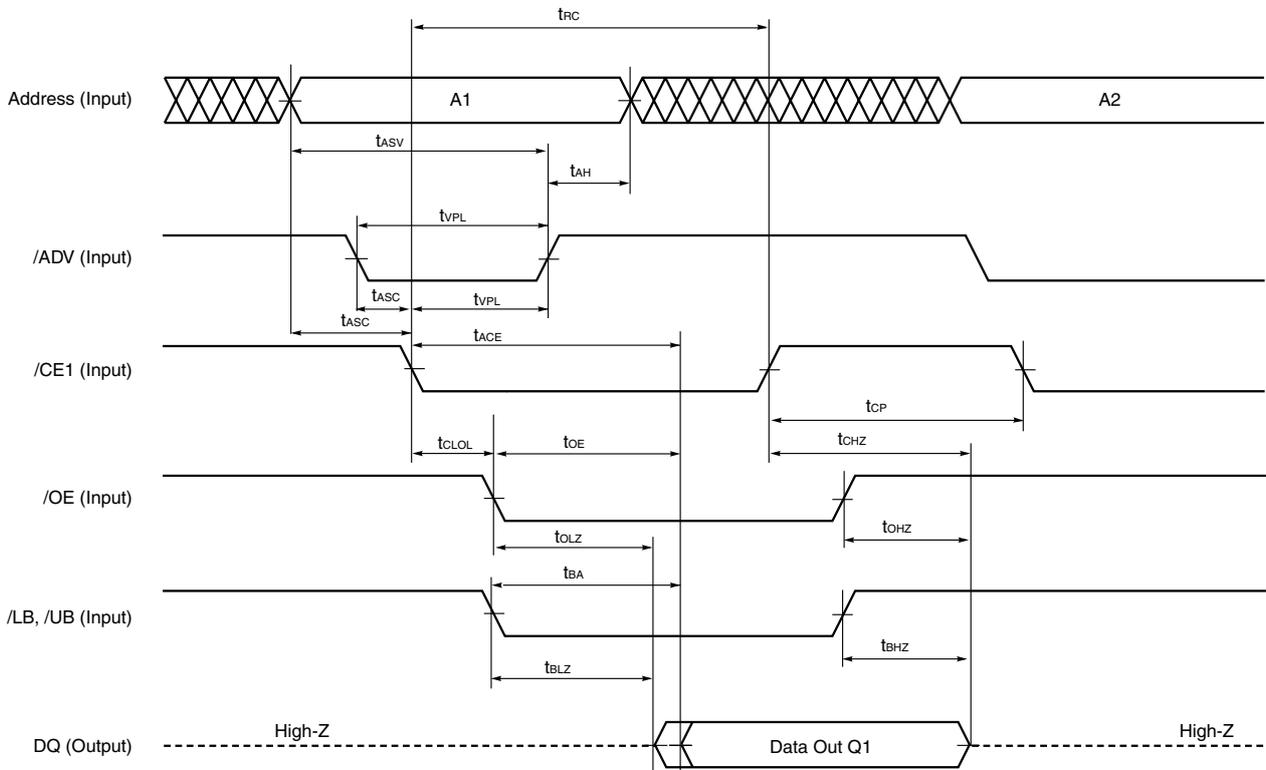
**2.** t<sub>OES</sub> and t<sub>OEH</sub> (MAX.) are applied while /CE1 is being hold at LOW.

Figure 7-1. Asynchronous Read Cycle Timing Chart 1 (Basic Timing1)



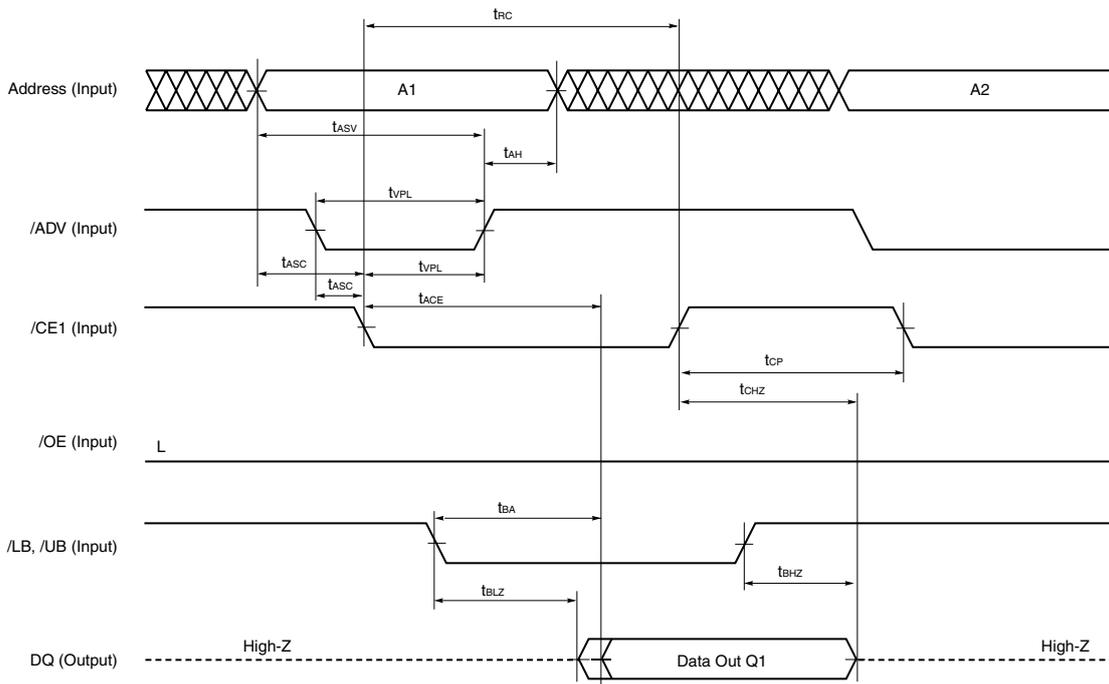
- Cautions 1. In read cycle, CE2 and /WE should be fixed HIGH.**
- 2. CLK should be fixed HIGH or LOW.**

Figure 7-2. Asynchronous Read Cycle Timing Chart 2-1 (Basic Timing2-1)



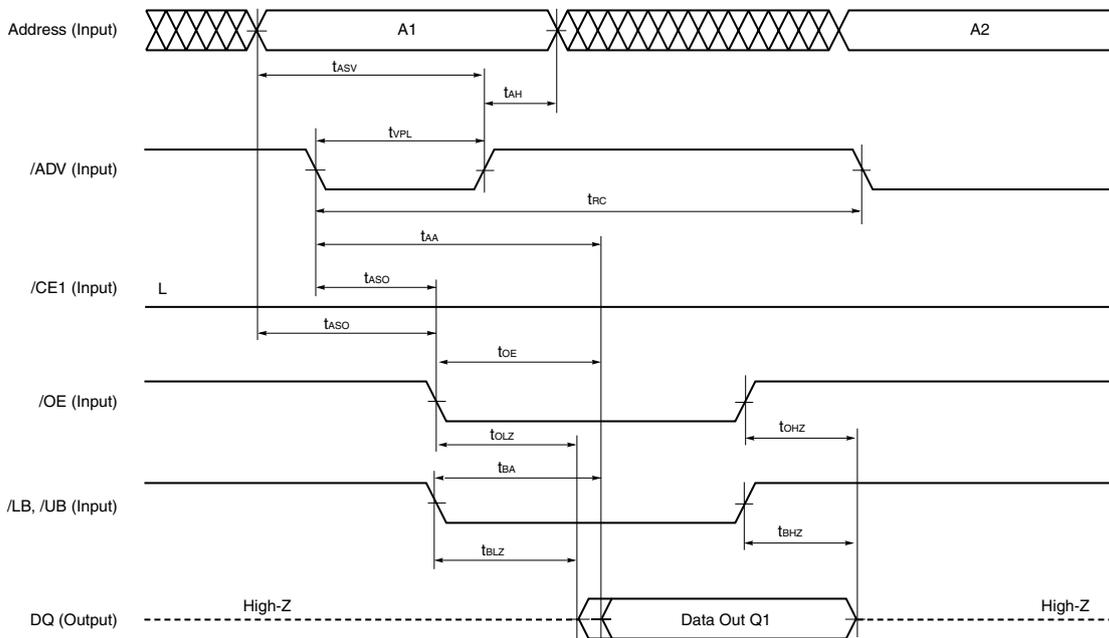
- Cautions 1. In read cycle, CE2 and /WE should be fixed HIGH.**
- 2. CLK should be fixed HIGH or LOW.**

Figure 7-3. Asynchronous Read Cycle Timing Chart 2-2 (Basic Timing2-2)



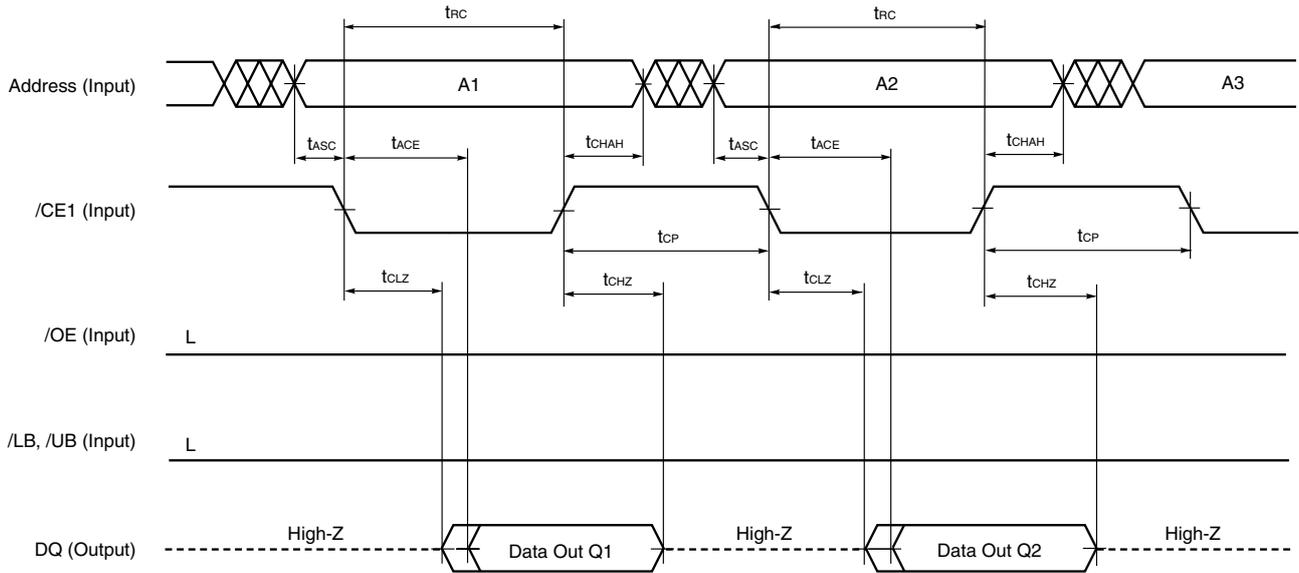
- Cautions 1. In read cycle, CE2 and /WE should be fixed HIGH.
- 2. CLK should be fixed HIGH or LOW.

Figure 7-4. Asynchronous Read Cycle Timing Chart 2-3 (Basic Timing2-3)



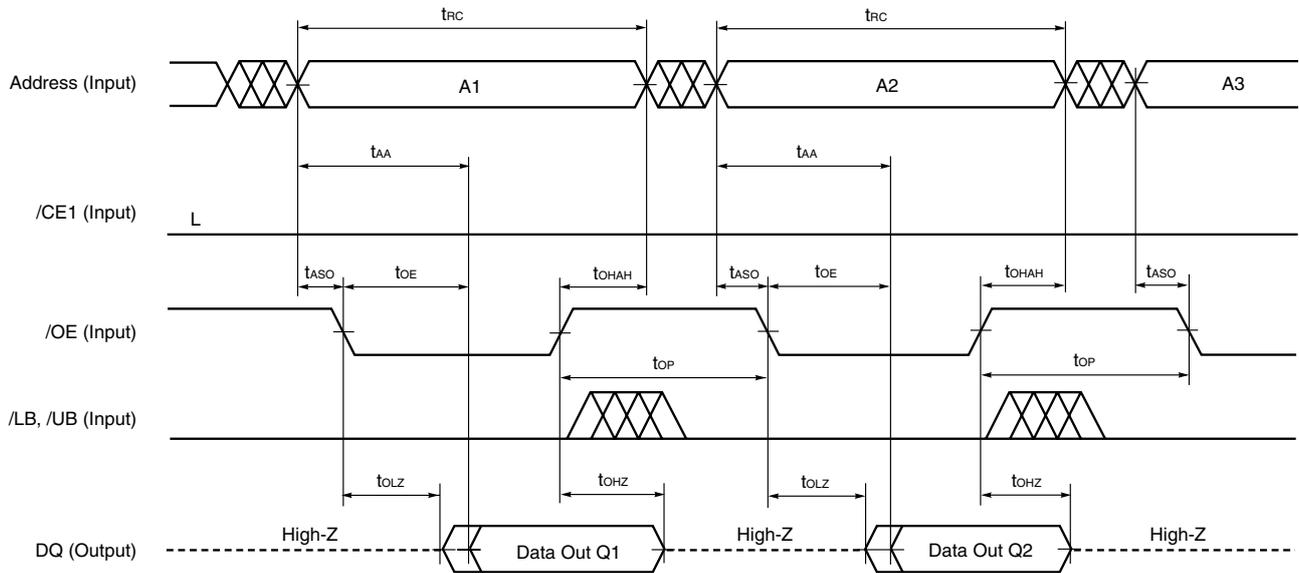
- Cautions 1. In read cycle, CE2 and /WE should be fixed HIGH.
- 2. CLK should be fixed HIGH or LOW.

Figure 7-5. Asynchronous Read Cycle Timing Chart 3 (/CE1 Controlled)



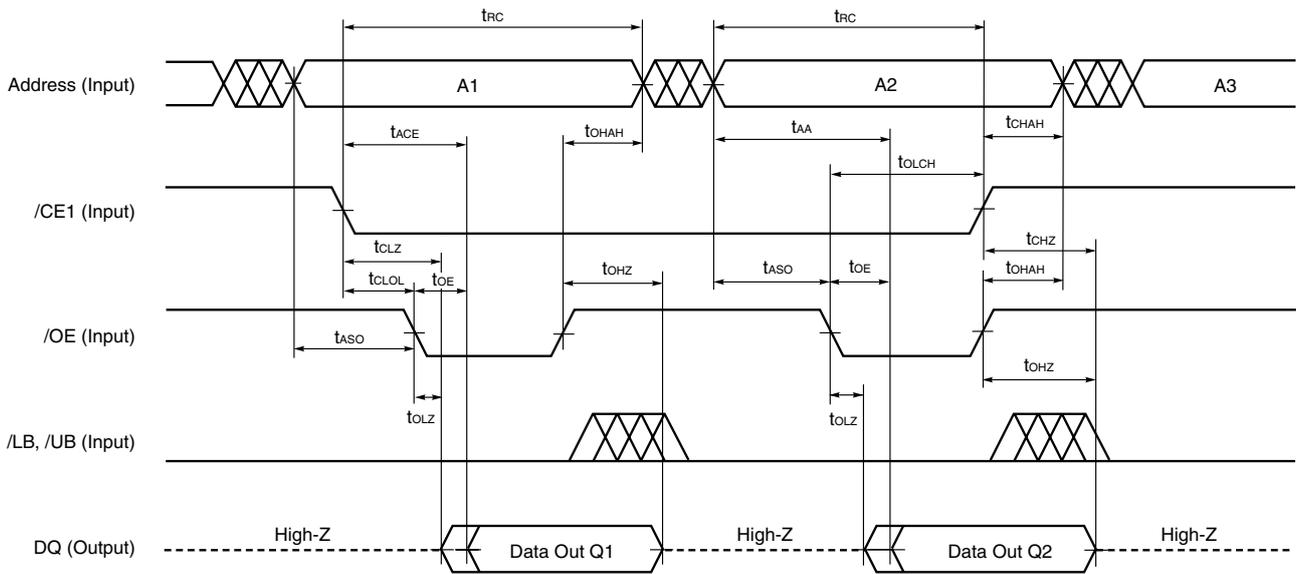
- Cautions 1. In read cycle, CE2 and /WE should be fixed HIGH.
- 2. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

Figure 7-6. Asynchronous Read Cycle Timing Chart 4 (/OE Controlled)



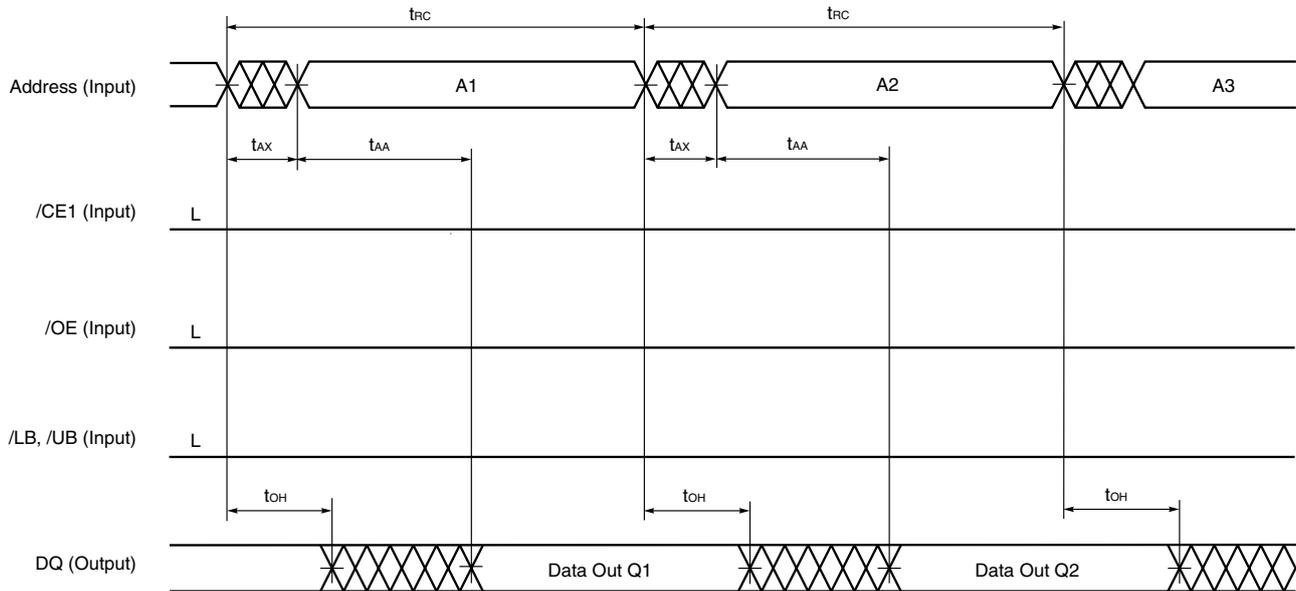
- Cautions 1. In read cycle, CE2 and /WE should be fixed HIGH.
- 2. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

Figure 7-7. Asynchronous Read Cycle Timing Chart 5 (/CE1, /OE Controlled)



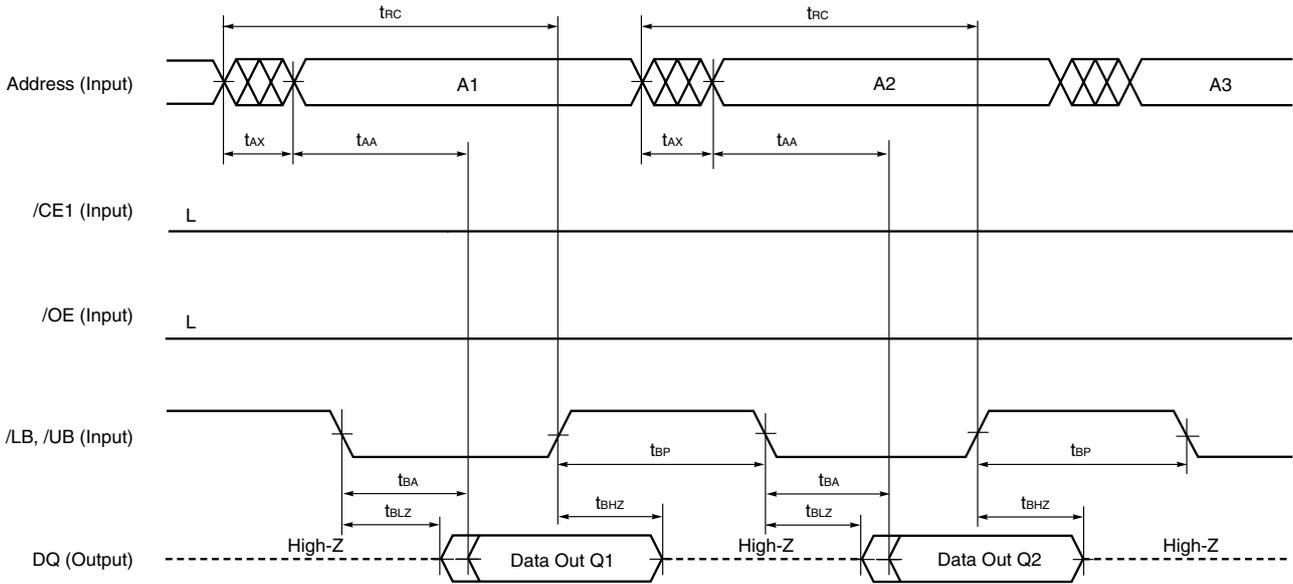
- Cautions 1. In read cycle, CE2 and /WE should be fixed HIGH.
- 2. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

Figure 7-8. Asynchronous Read Cycle Timing Chart 6 (Address Controlled)



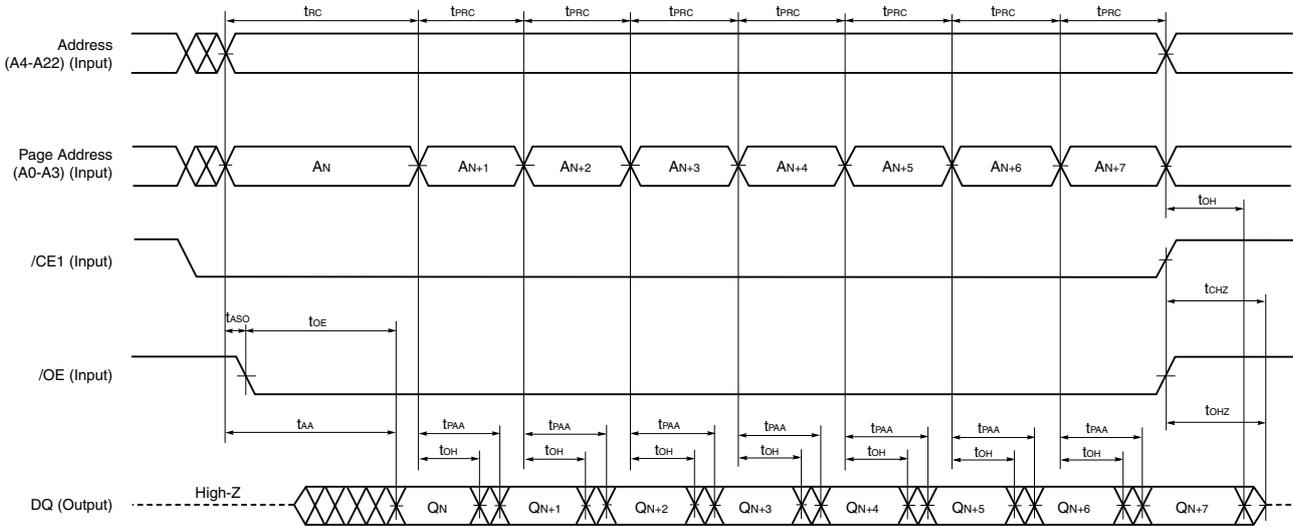
- Cautions 1. In read cycle, CE2 and /WE should be fixed HIGH.
- 2. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

Figure 7-9. Asynchronous Read Cycle Timing Chart 7 (/LB, /UB Controlled)



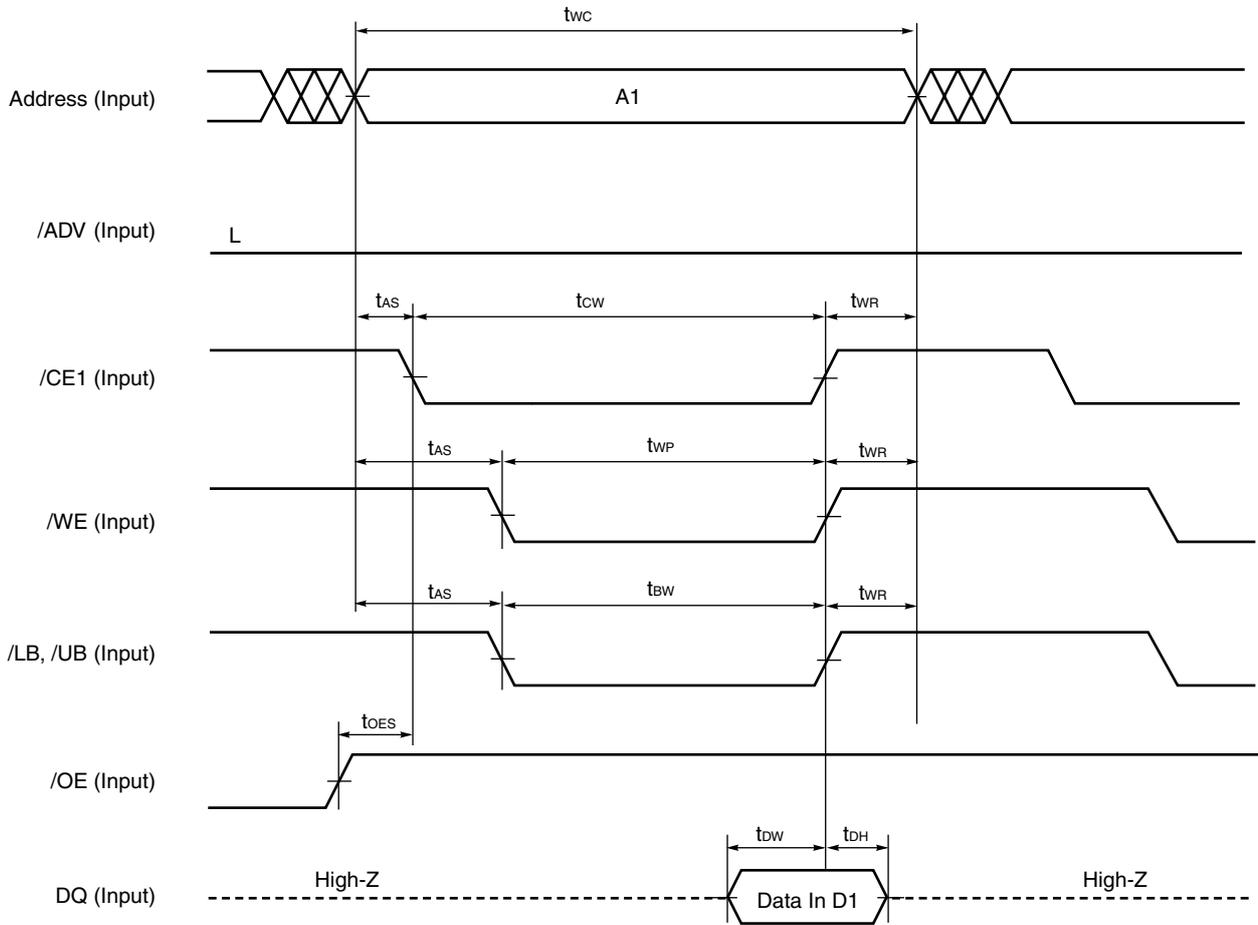
- Cautions 1.** In read cycle, CE2 and /WE should be fixed HIGH.
- 2.** /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

Figure 7-10. Asynchronous Page Read Cycle Timing Chart



- Cautions 1.** In read cycle, CE2 and /WE should be fixed HIGH.
- 2.** /LB and /UB should be fixed LOW.
- 3.** /ADV should be fixed LOW. CLK should be fixed HIGH or LOW.
- ★ **4.** Fix /CE1 and /OE to LOW throughout a page operation.
- ★ **5.** Arbitrary order and combination of A0-A3 is possible in the page operation.

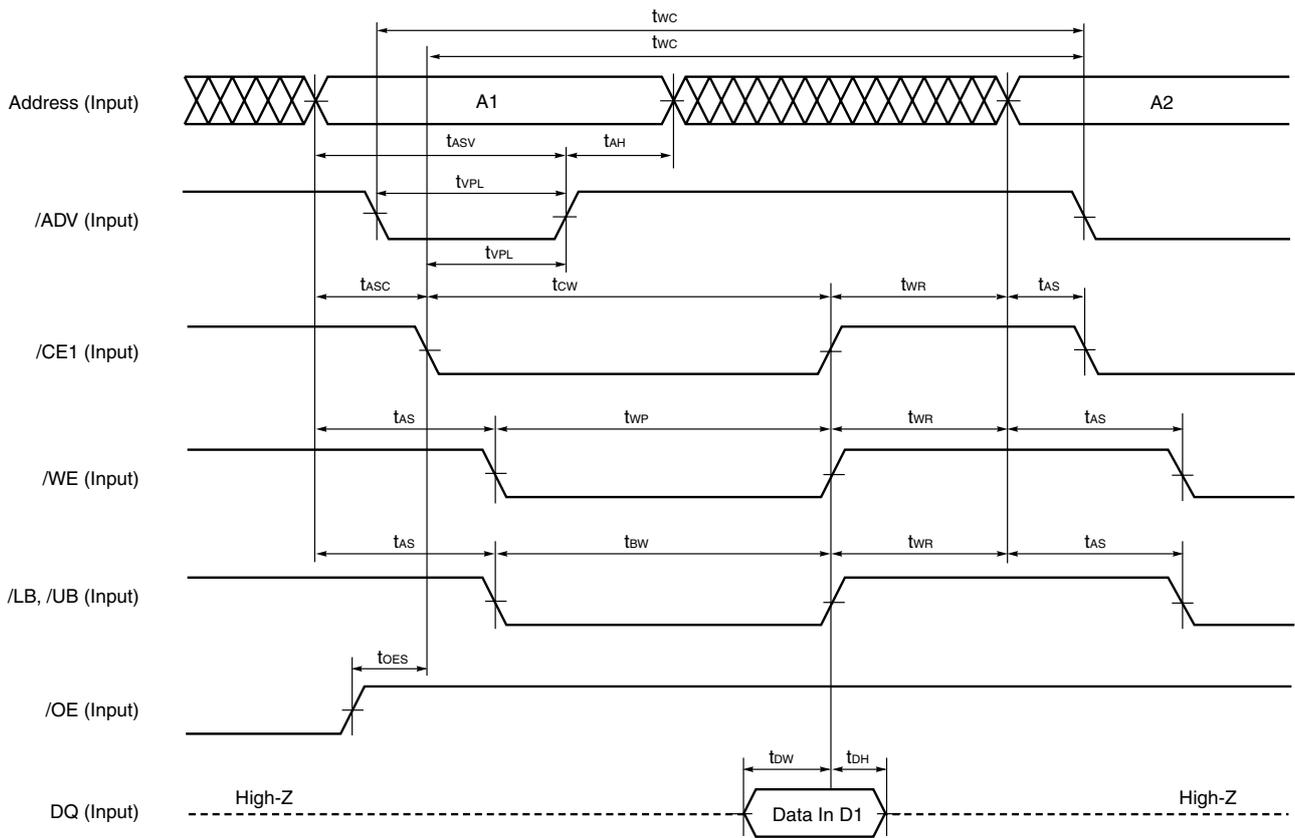
Figure 7-11. Asynchronous Write Cycle Timing Chart 1 (Basic Timing1)



- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB

Figure 7-12. Asynchronous Write Cycle Timing Chart 2 (Basic Timing2)

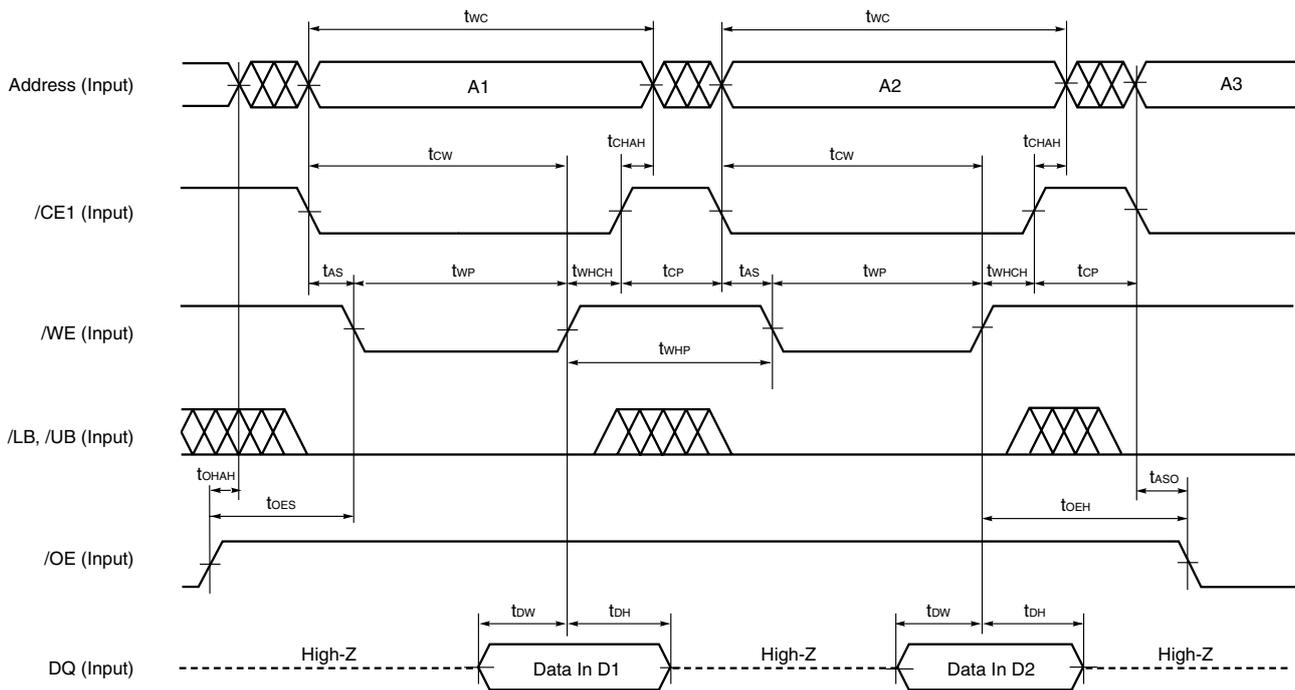


- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB



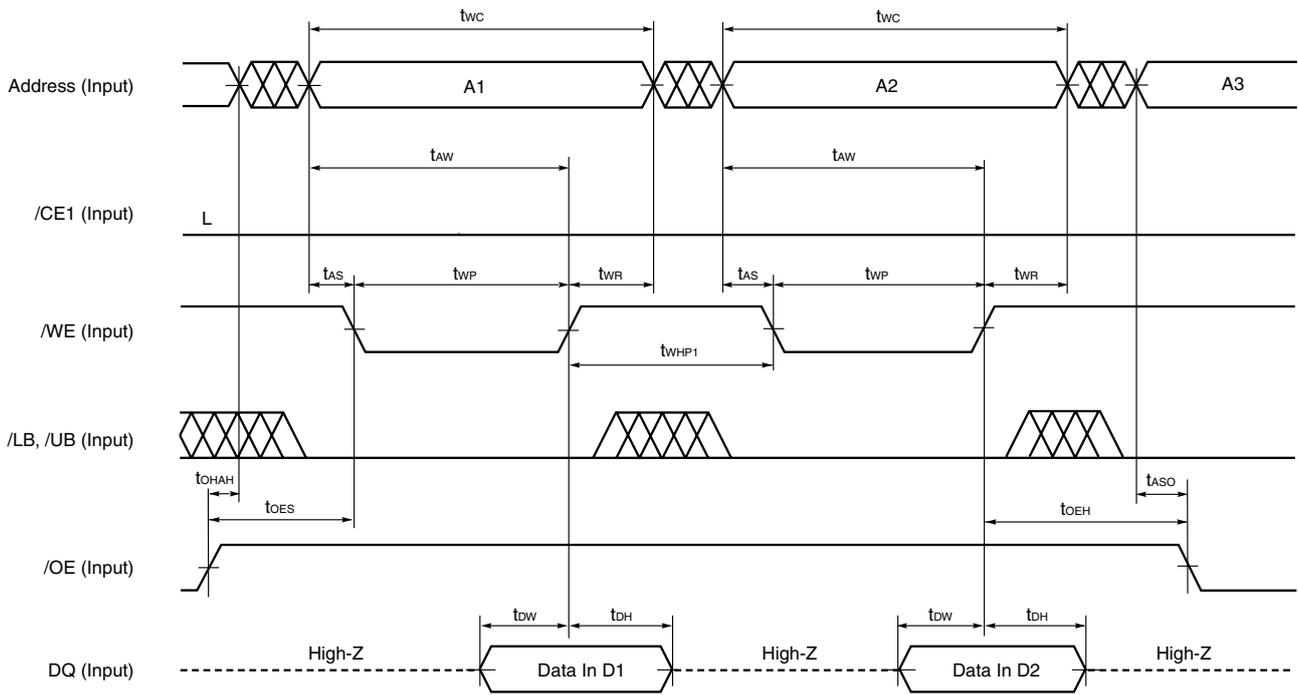
Figure 7-14. Asynchronous Write Cycle Timing Chart 4 (/WE Controlled)



- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB

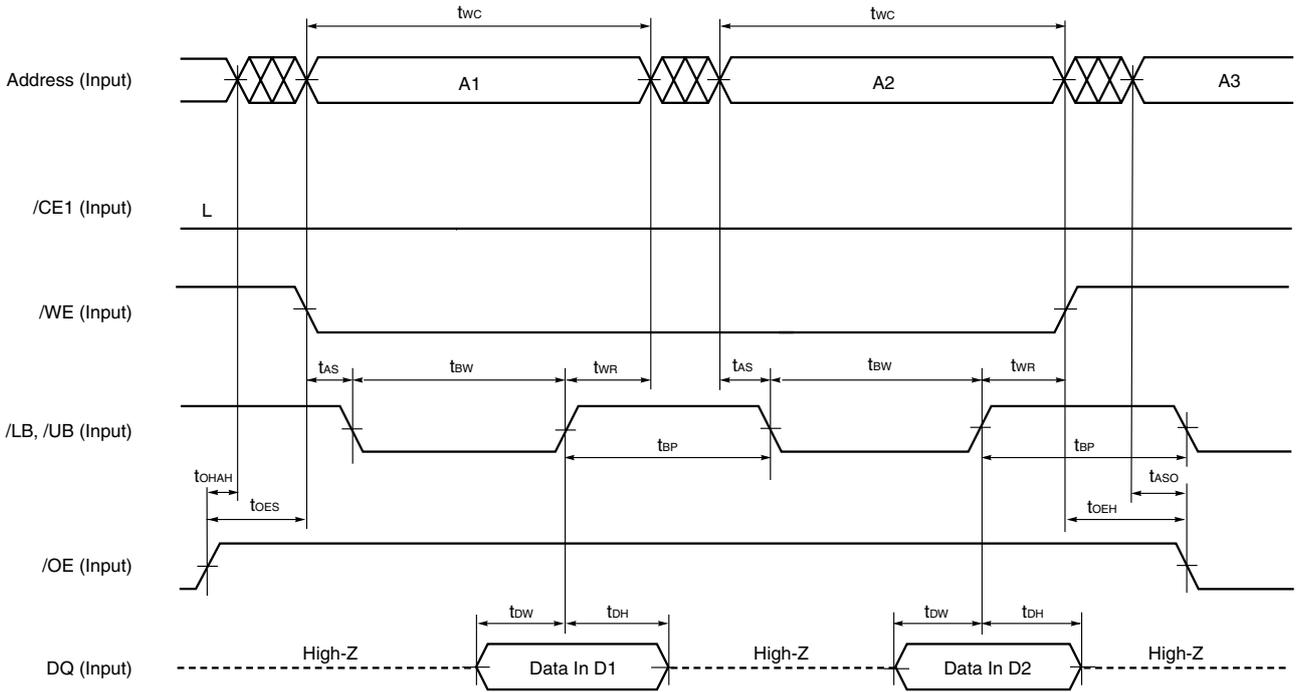
Figure 7-15. Asynchronous Write Cycle Timing Chart 5 (/WE Controlled)



- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB

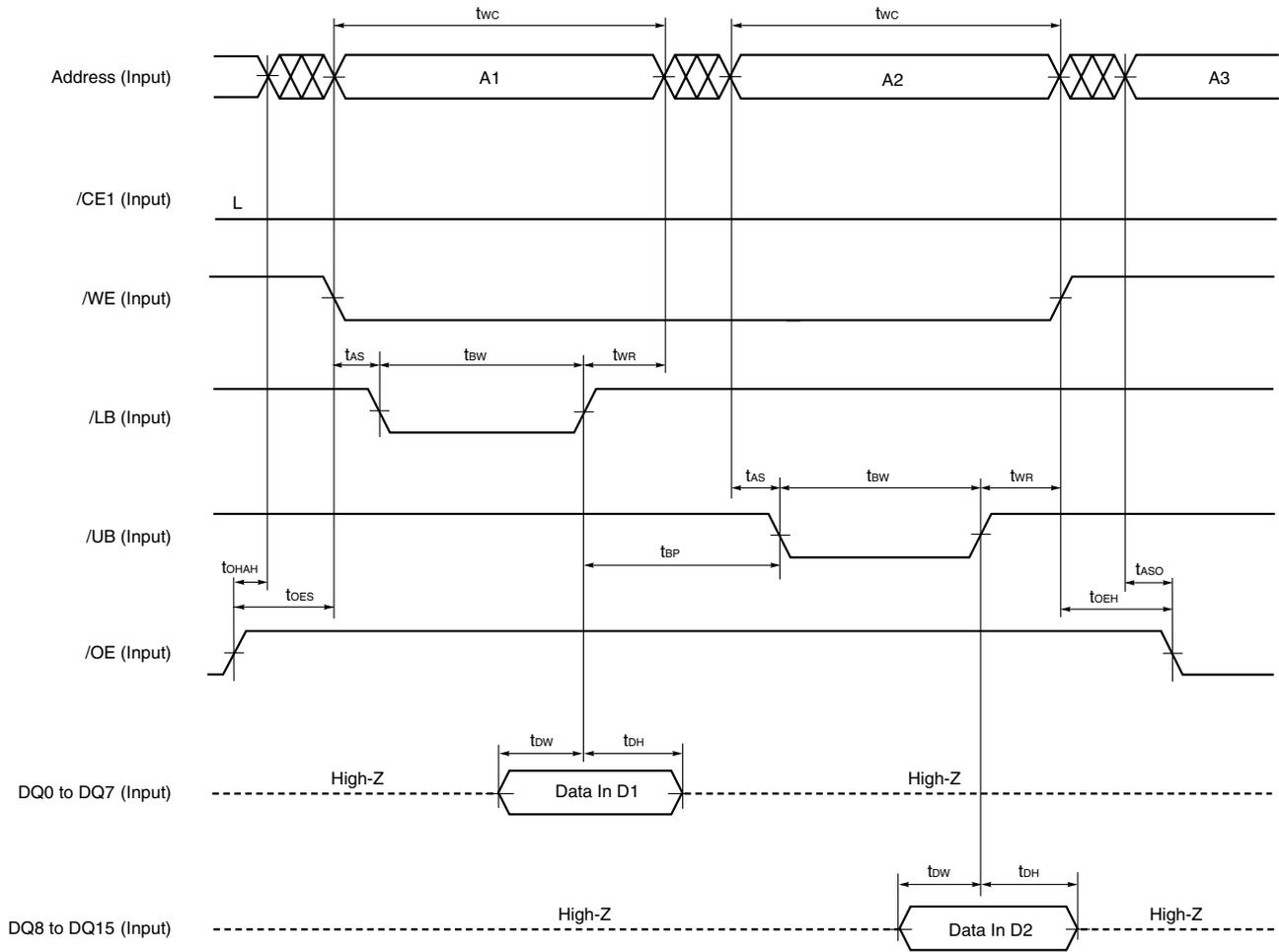
Figure 7-16. Asynchronous Write Cycle Timing Chart 6 (/LB, /UB Controlled)



- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB

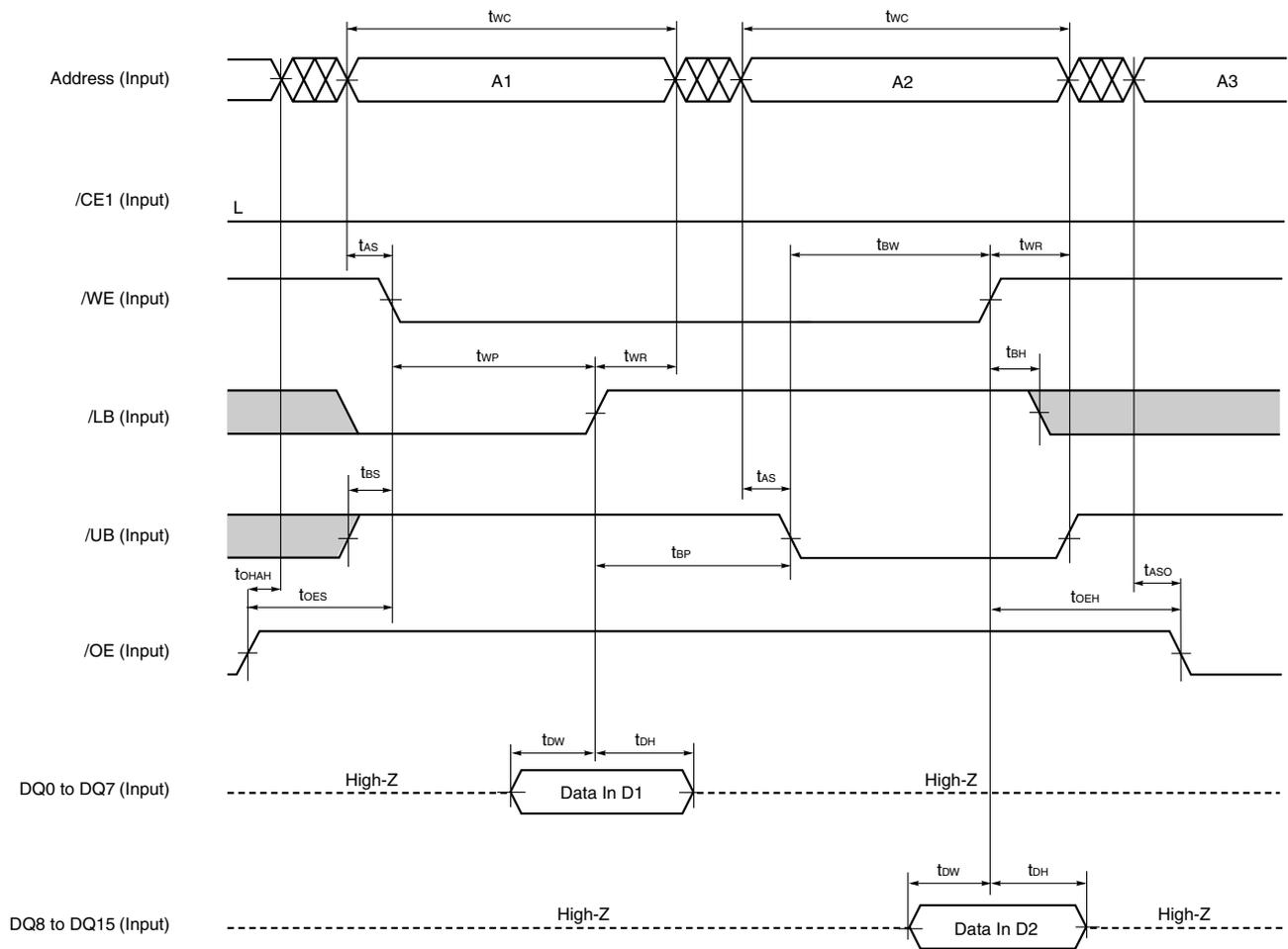
Figure 7-17. Asynchronous Write Cycle Timing Chart 7 (/LB, /UB Independent Controlled 1)



- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB

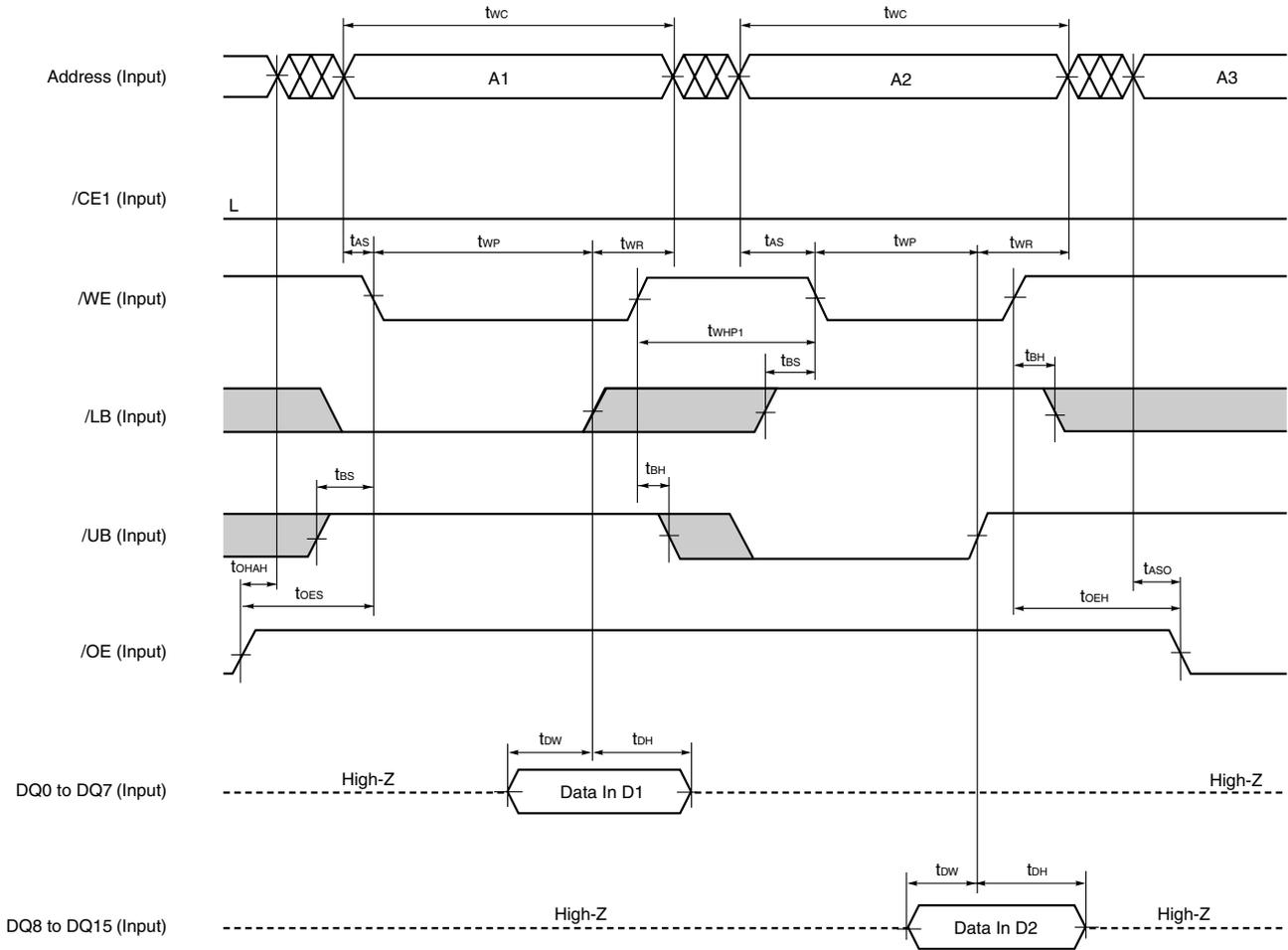
Figure 7-18. Asynchronous Write Cycle Timing Chart 8 (/LB, /UB Independent Controlled 2)



- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB

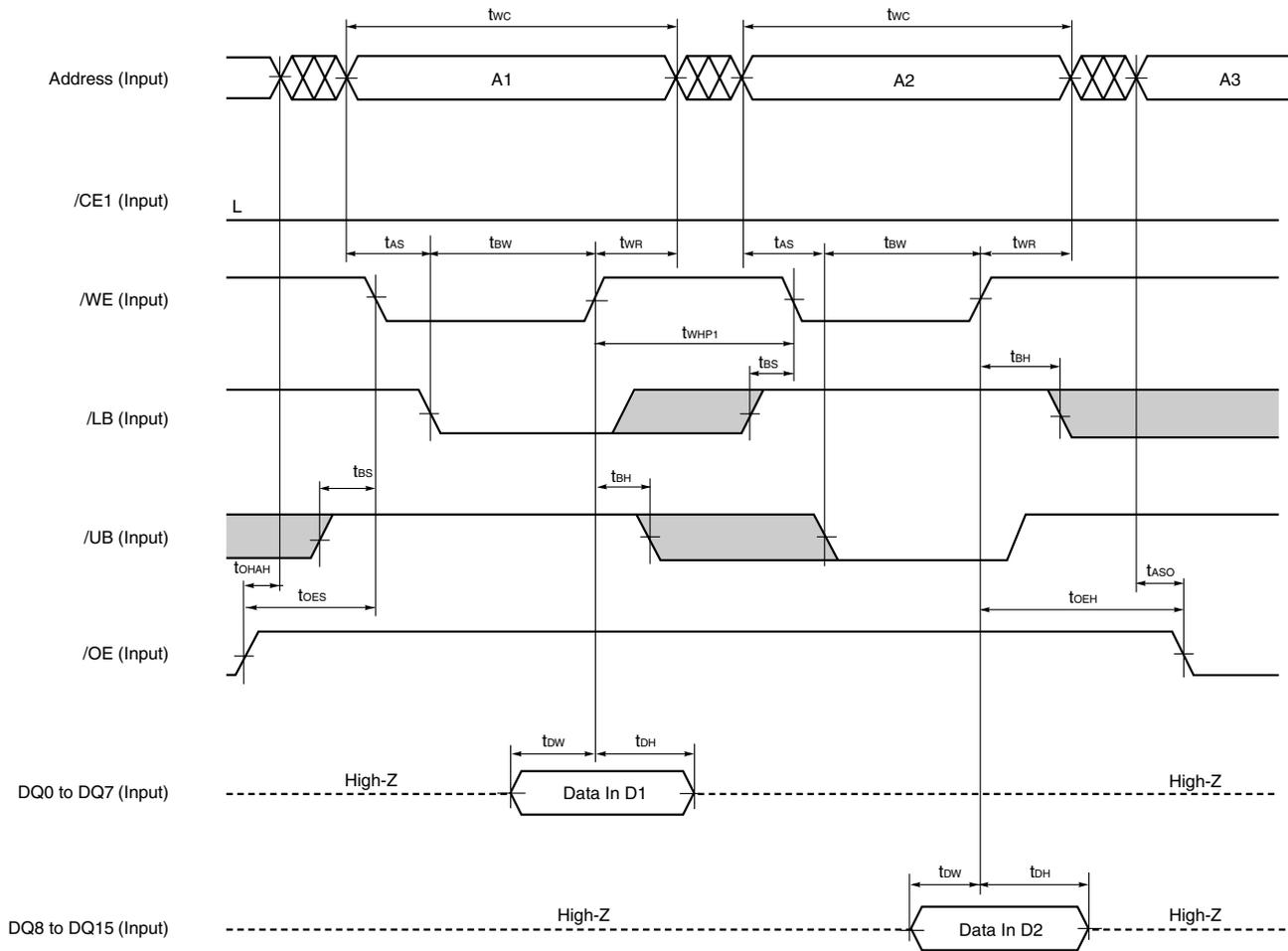
Figure 7-19. Asynchronous Write Cycle Timing Chart 9 (/LB, /UB Independent Controlled 3)



- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB

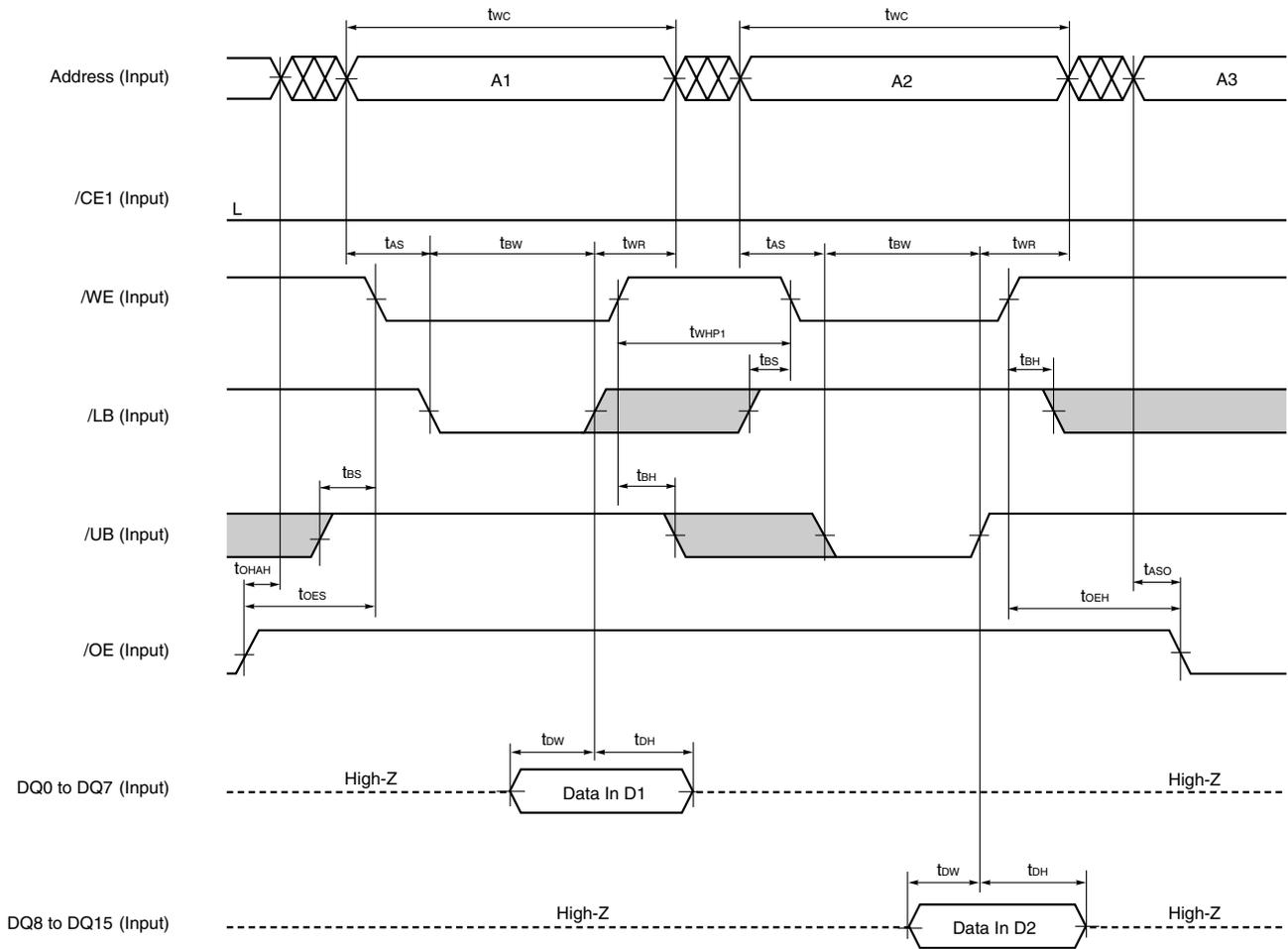
Figure 7-20. Asynchronous Write Cycle Timing Chart 10 (/LB, /UB Independent Controlled 4)



- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB

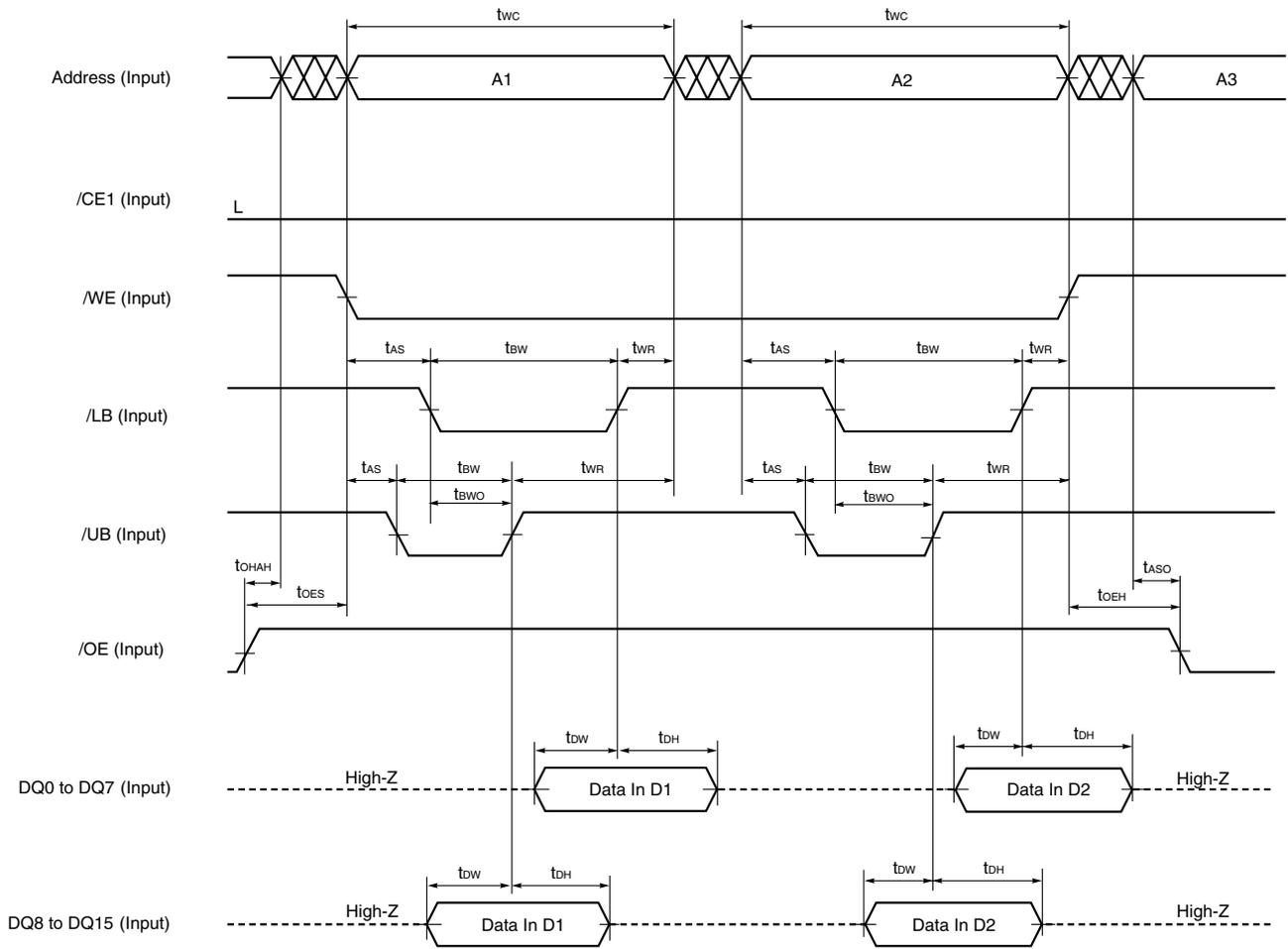
Figure 7-21. Asynchronous Write Cycle Timing Chart 11 (/LB, /UB Independent Controlled 5)



- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB

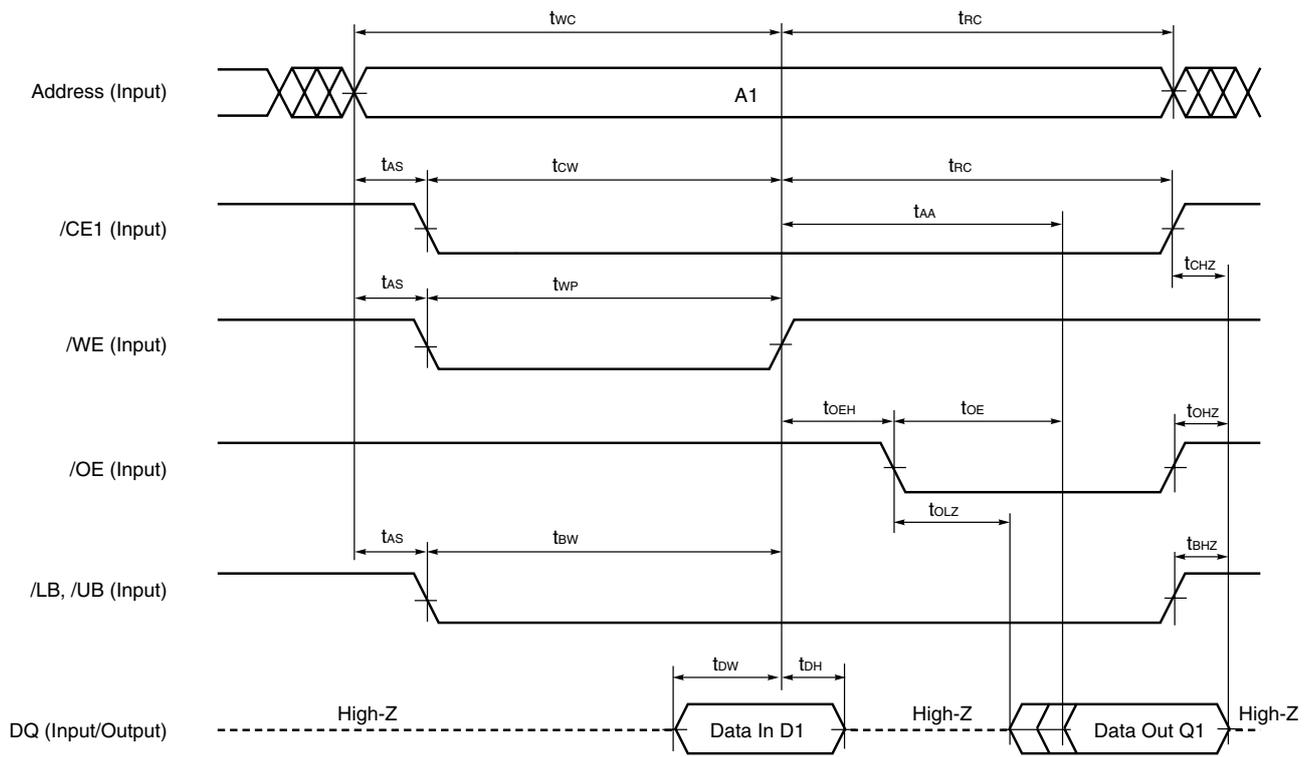
Figure 7-22. Asynchronous Write Cycle Timing Chart 12 (/LB, /UB Independent Controlled 6)



- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB

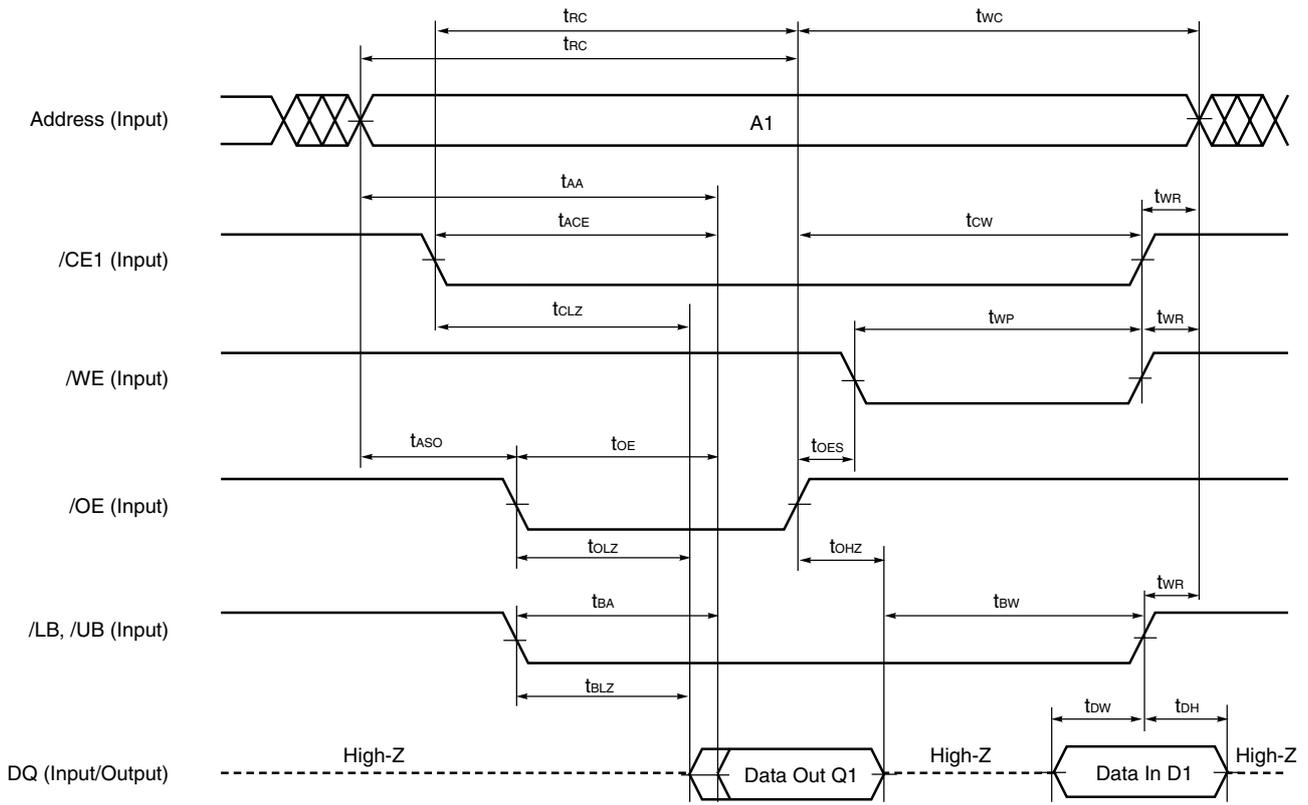
Figure 7-23. Asynchronous Write-Read Cycle Timing Chart



- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB

Figure 7-24. Asynchronous Read-Write Cycle Timing Chart



- Cautions 1.** During address transition, at least one of pins /CE1 and /WE, or both of /LB and /UB pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
  3. In write cycle, CE2 and /OE should be fixed HIGH.
  4. /ADV should be fixed LOW or toggled HIGH → LOW → HIGH. CLK should be fixed HIGH or LOW.

- ★ **Remark** Write operation is done during the overlap time of LOW of following signals.
- /CE1
  - /WE
  - /LB and/or /UB

★ 8. Synchronous AC Specification, Timing Chart

Synchronous Read / Write Common Specification

Parameter	Symbol	-E9X, -E10X		-E11X, -E12X		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
<b>Clock Specifications</b>							
Cycle frequency	t <sub>CYCLE</sub>	0.1	108	0.1	83	MHz	1
CLK HIGH width	t <sub>CH</sub>	3		3		ns	
CLK LOW width	t <sub>CL</sub>	3		3		ns	
CLK rise / fall time	t <sub>CHCL</sub>		3		3	ns	
<b>Address Latching Specifications</b>							
Address setup time to CLK	t <sub>ACS</sub>	5		5		ns	
Address hold time to CLK	t <sub>ACH</sub>	4		4		ns	
/ADV setup time to CLK	t <sub>CSV</sub>	5	10,000	5	10,000	ns	
/ADV hold time from CLK	t <sub>CHV</sub>	1		1		ns	
/ADV = LOW pulse width	t <sub>VPL</sub>	7		7		ns	
Address hold time from /ADV = HIGH	t <sub>AH</sub>	3		3		ns	
/CE1 setup time to CLK	t <sub>CES</sub>	5		5		ns	
<b>Asynchronous Specification</b>							
/CE1 to output in low impedance	t <sub>CLZ</sub>	10		10		ns	2
/OE to output in low impedance	t <sub>OLZ</sub>	5		5		ns	
/LB, /UB to output in low impedance	t <sub>BLZ</sub>	5		5		ns	
/CE1 to output in high impedance	t <sub>CHZ</sub>		9		9	ns	
/OE to output in high impedance	t <sub>OHZ</sub>		9		9	ns	
/LB, /UB to output in high impedance	t <sub>BHZ</sub>		9		9	ns	
<b>/WAIT Specification</b>							
/WAIT output time from /CE1 = LOW	t <sub>CEWA</sub>		10		13	ns	3
/WAIT output time from /ADV = LOW	t <sub>ADWA</sub>		10		13	ns	
/WAIT = HIGH output time from CLK	t <sub>CLWA</sub>		7		8	ns	
/WAIT in high impedance from /CE1 = HIGH	t <sub>CWHZ</sub>		10		10	ns	2
<b>Others</b>							
/CE1 hold time	t <sub>CEH</sub>	1		1		ns	
/LB, /UB hold time	t <sub>LUH</sub>	1		1		ns	
/CE1 HIGH pulse width	t <sub>CP</sub>	10		10		ns	

- Notes**
1. Case BL (Burst Length) = Continuous : 2 MHz (MIN.)
  2. Output load: 5 pF
  3. Output load: 30 pF

**Synchronous Burst Read Cycle**

Parameter	Symbol	-E9X, -E10X		-E11X, -E12X		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
<b>Synchronous Read Specifications</b>							
Burst access time	t <sub>BACC</sub>		7		8	ns	1
Output data hold time	t <sub>BDH</sub>	2		2		ns	
/OE setup time to CLK for data output	t <sub>OC</sub>	30		30		ns	
/LB, /UB setup time to CLK for data output	t <sub>BC</sub>	30		30		ns	
/OE setup time for burst read suspend	t <sub>SOES</sub>	5		5		ns	
/OE hold time for burst read suspend	t <sub>SOEH</sub>	1		1		ns	
Burst read suspend time (/OE = HIGH)	t <sub>SOP</sub>	9	10,000	12	10,000	ns	
Burst read termination recovery time	t <sub>TRB</sub>	18		24		ns	

**Note1.** Output load: 30 pF

**Synchronous Burst Write Cycle**

Parameter	Symbol	-E9X, -E10X		-E11X, -E12X		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
<b>Synchronous Write Specifications</b>							
/LB, /UB setup time to CLK for latching data	t <sub>BC</sub>	30		30		ns	
/WE setup time for CLK (In /WE single clock control operation) (In burst write suspend operation)	t <sub>WES</sub>	5		5		ns	
/WE hold time in the write operation (In /WE single clock control operation) (In burst write suspend operation)	t <sub>WEH</sub>	1		1		ns	
Write data setup time	t <sub>WDS</sub>	5		5		ns	
Write data hold time	t <sub>WDH</sub>	1		1		ns	
/WE HIGH pulse width	t <sub>SWHP</sub>	9	10,000	12	10,000	ns	
/ADV LOW from CLK for latching the latest data	t <sub>WRB</sub>	2		2		CLK	
Burst write termination recovery time	t <sub>TRB</sub>	18		24		ns	

Figure 8-1. Synchronous CLK Input Timing Chart

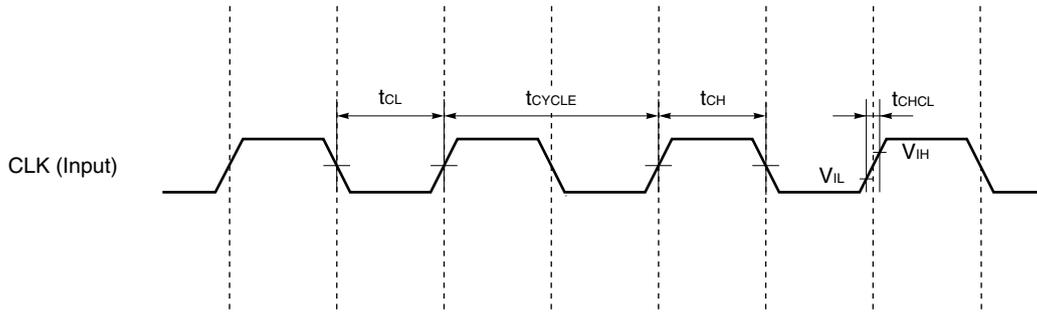
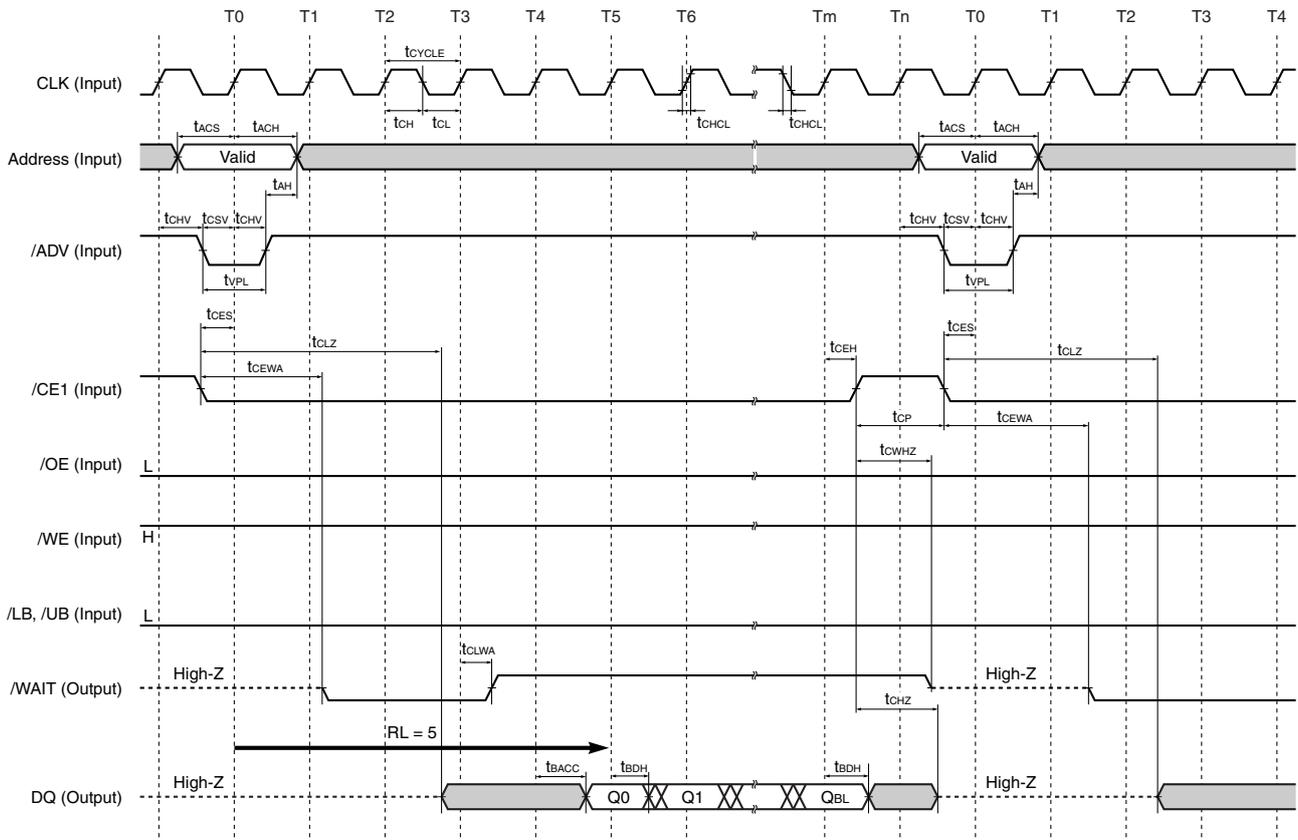
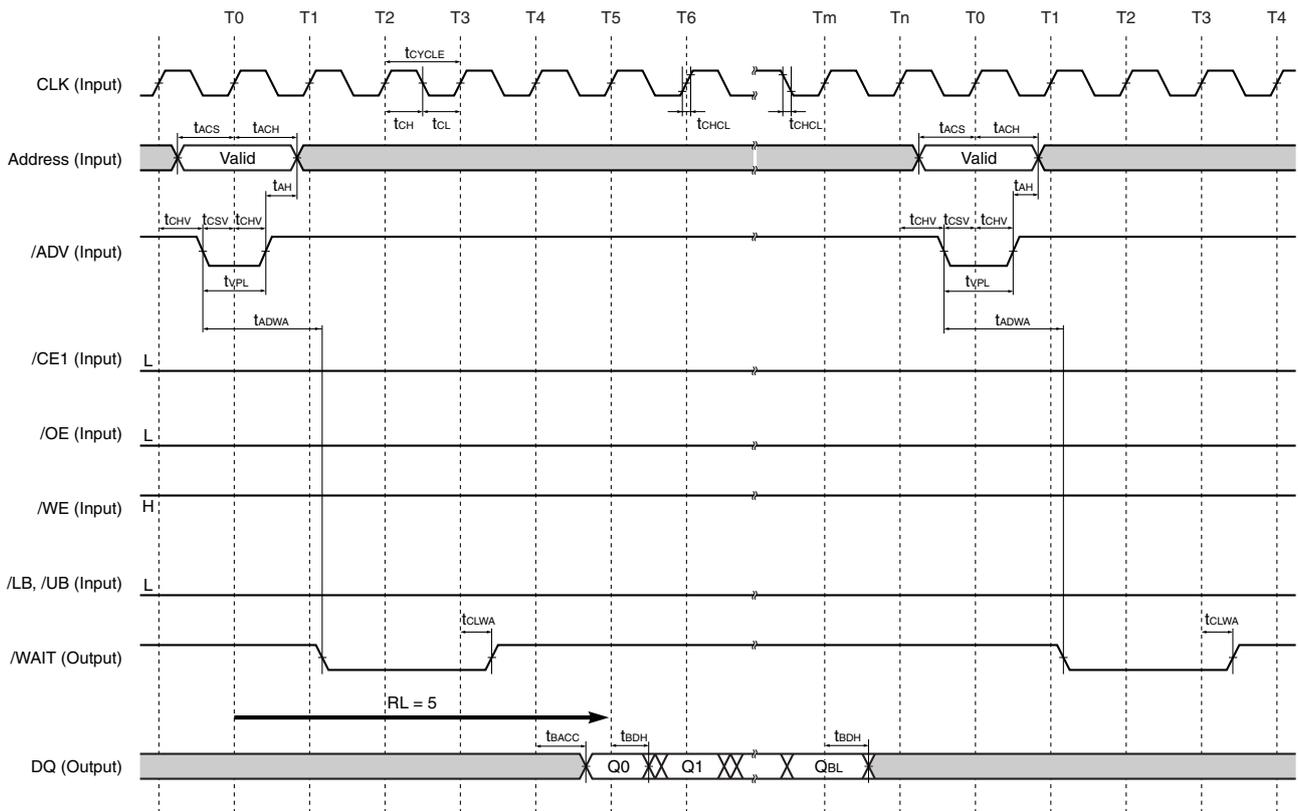


Figure 8-2. Synchronous Burst Read Cycle Timing Chart (/CE1 Control)



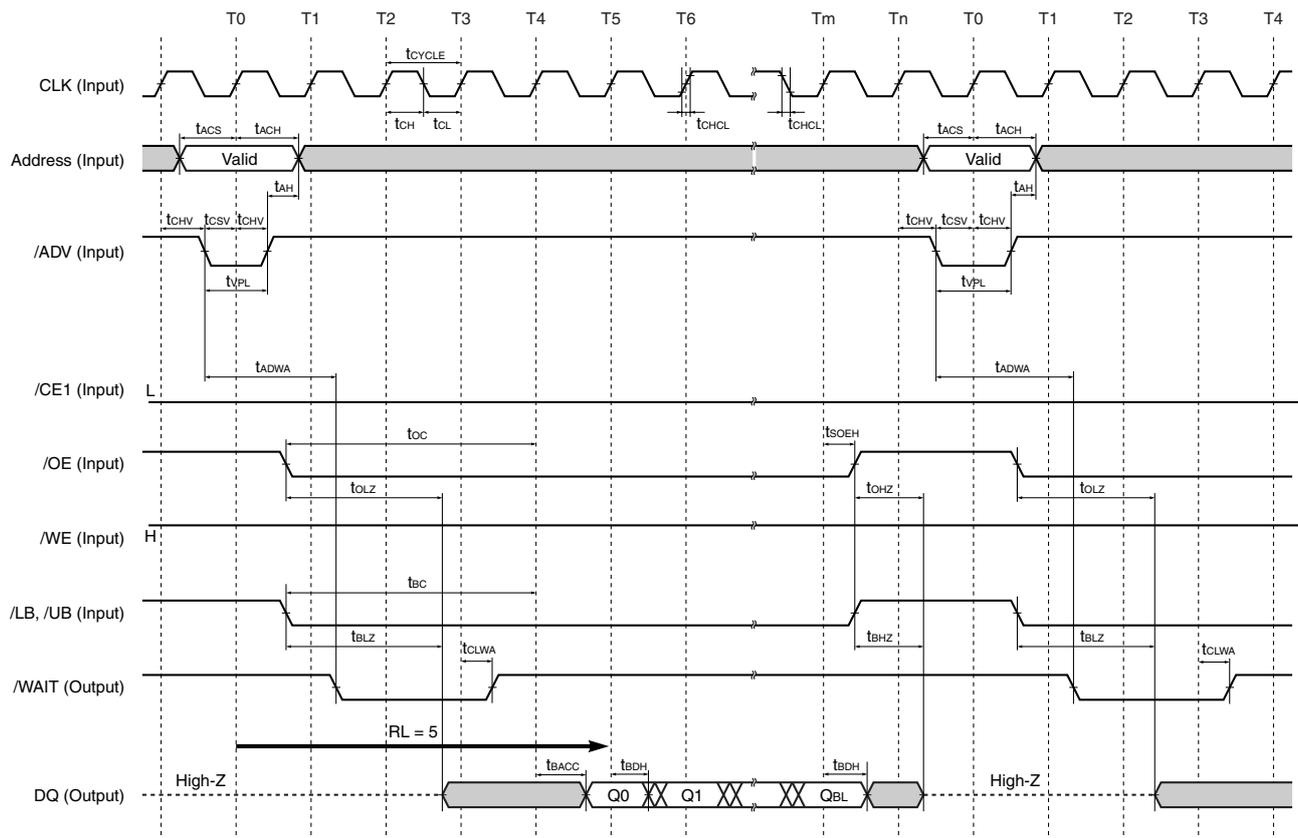
- Remarks 1.** The above timing chart assumes Read Latency is 5 and Burst Length is 8 or 16.  
**Q<sub>BL</sub>** means the latest data out of burst length.
- 2.** CE2 should be fixed HIGH.
  - 3.** Valid clock edge is the rising edge.

Figure 8-3. Synchronous Burst Read Cycle Timing Chart (/ADV Control)



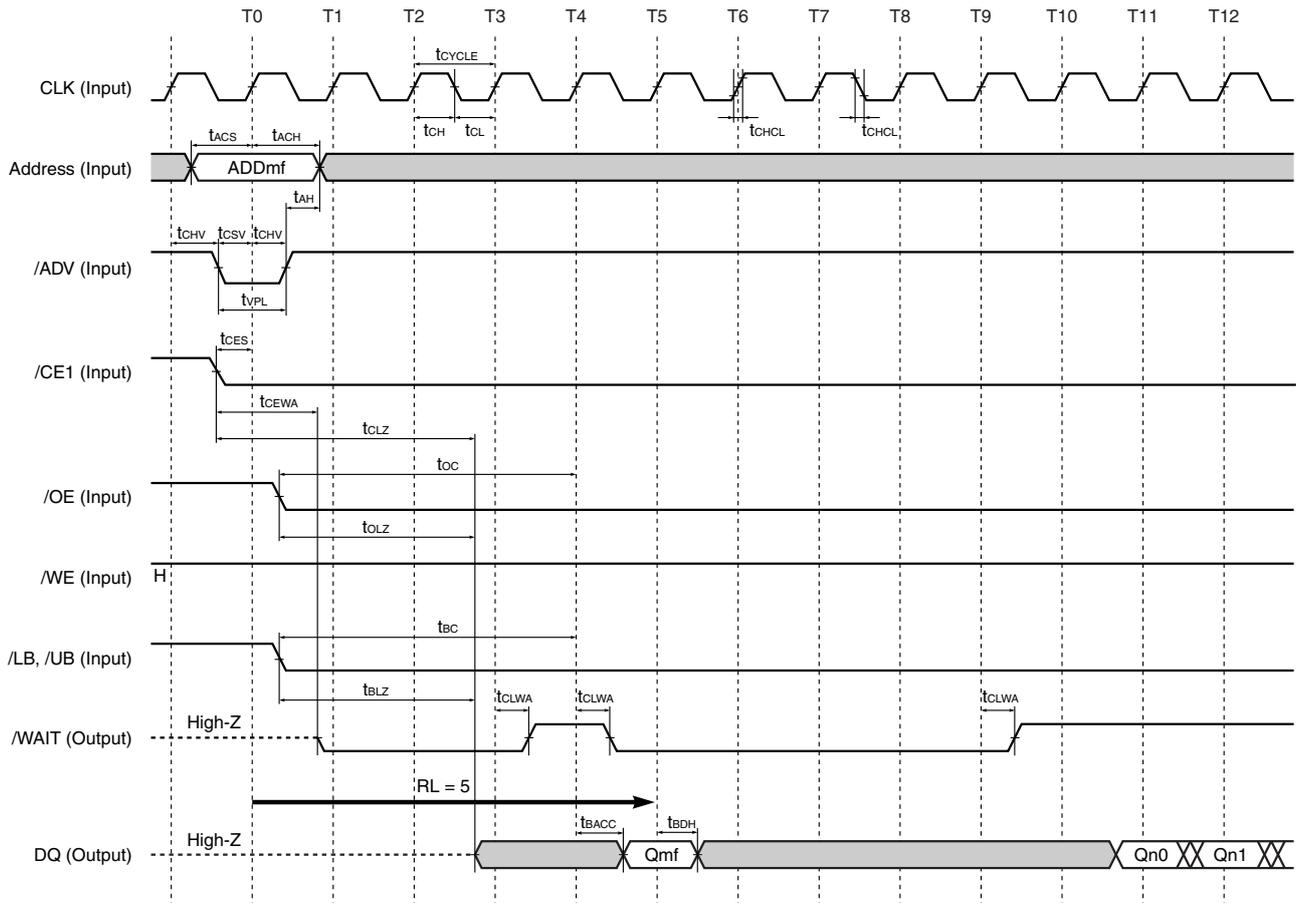
- Remarks 1.** The above timing chart assumes Read Latency is 5 and Burst Length is 8 or 16.  $Q_{BL}$  means the latest data out of burst length.
2.  $CE_2$  should be fixed HIGH.
  3. Valid clock edge is the rising edge.

Figure 8-4. Synchronous Burst Read Cycle Timing Chart (/OE Control)



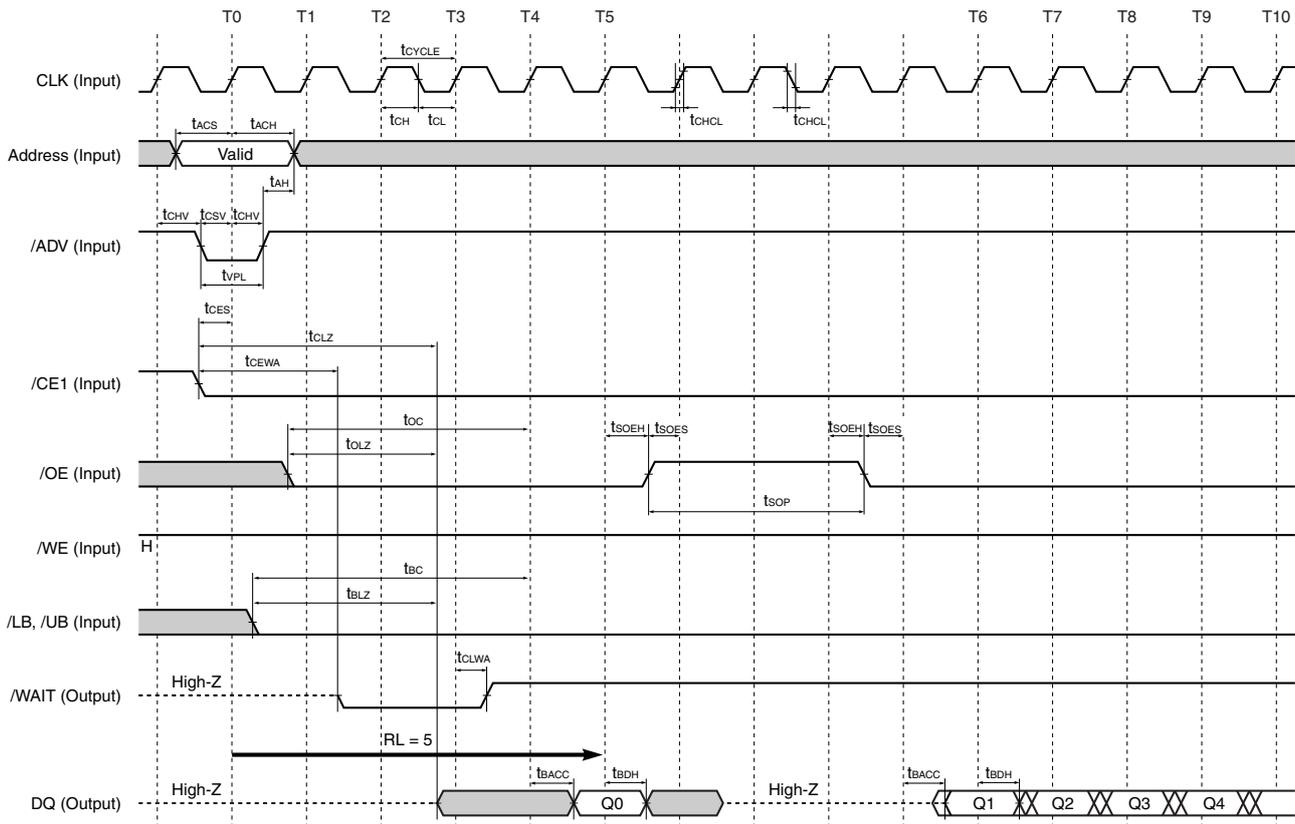
- Remarks 1.** The above timing chart assumes Read Latency is 5 and Burst Length is 8 or 16. Q<sub>BL</sub> means the latest data out of burst length.
2. CE2 should be fixed HIGH.
  3. Valid clock edge is the rising edge.
  4. t<sub>oc</sub> and t<sub>bc</sub> are defined from CLK rising edge of RL-1 to /OE = LOW, /LB and /UB = LOW.

Figure 8-5. Synchronous Burst /WAIT Timing Chart (Continuous)



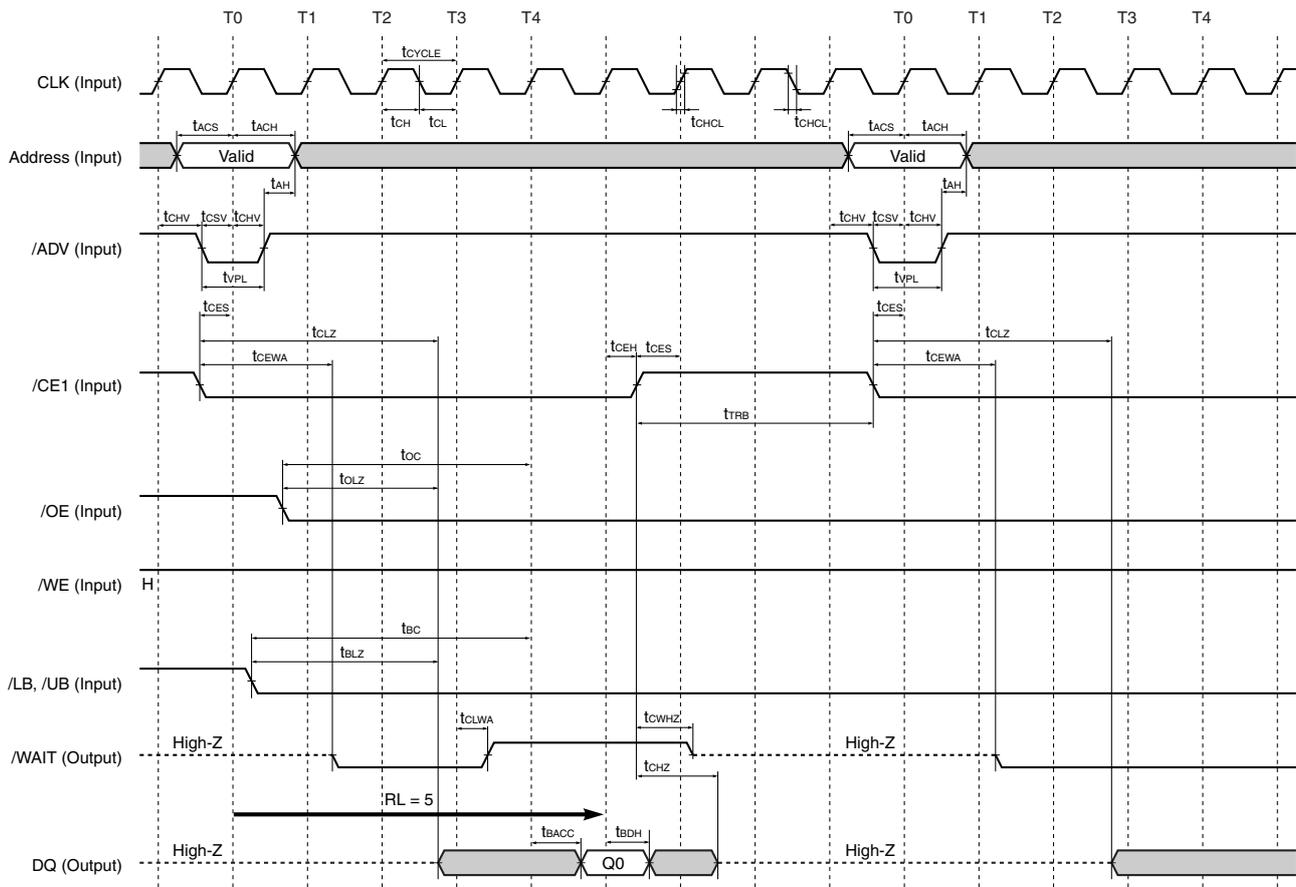
- Remarks 1.** The above timing chart assumes Burst length is continuous.
- 2.** CE2 should be fixed HIGH.
- 3.** Valid clock edge is the rising edge.
- 4.** t<sub>oc</sub> and t<sub>bc</sub> are defined from CLK rising edge of RL-1 to /OE = LOW, /LB and /UB = LOW.
- 5.** The above timing chart assumes Read Latency is 5 and start address is from xxxfH and the number of dummy wait cycles are 5 cycles.

Figure 8-6. Synchronous Burst Read Suspend Timing Chart



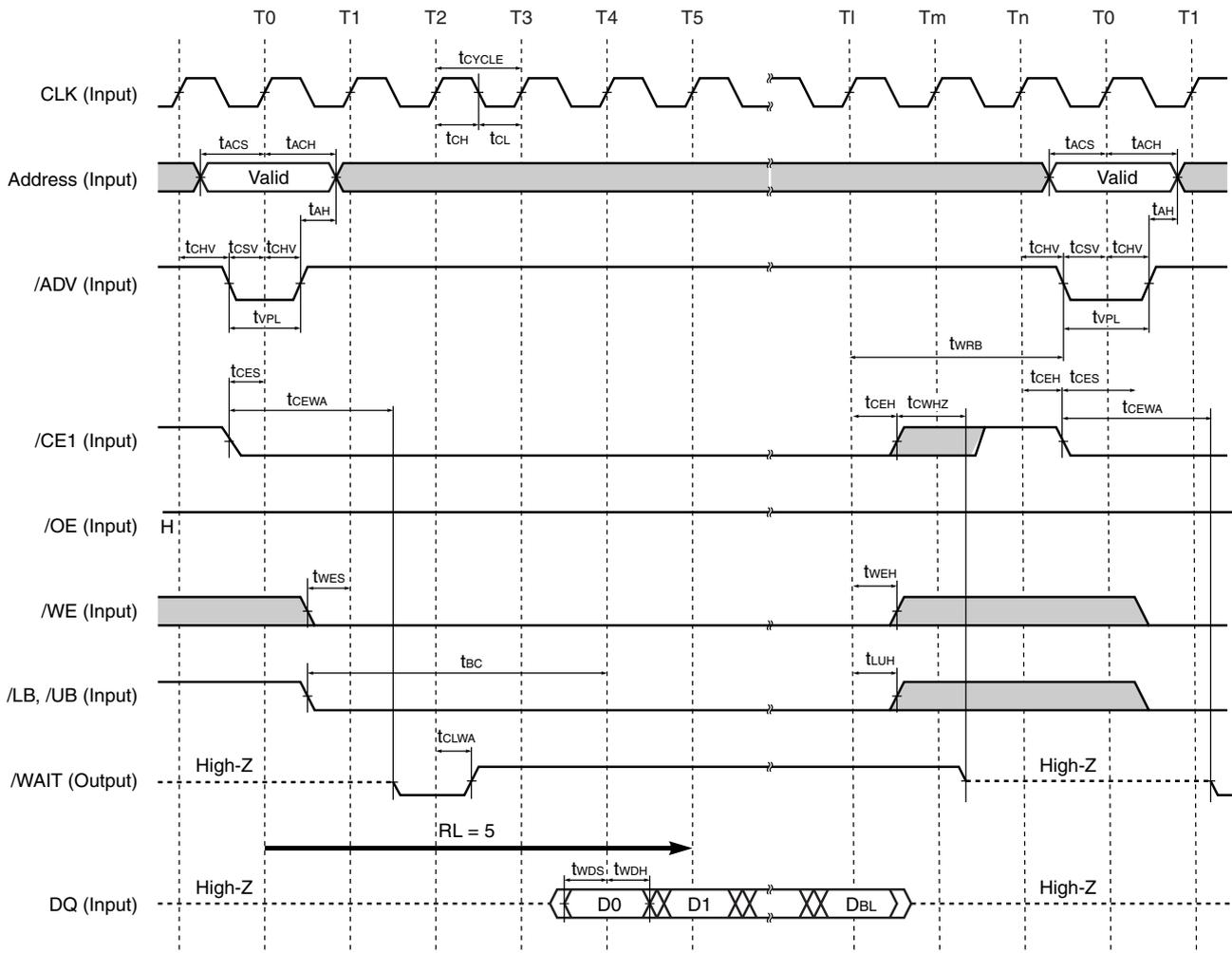
- Remarks 1.** The above timing chart assumes Read Latency is 5 and Burst Length is 8 or 16.
- 2.** CE2 should be fixed HIGH.
  - 3.** Valid clock edge is the rising edge.
  - 4.**  $t_{oc}$  and  $t_{bc}$  are defined from CLK rising edge of RL-1 to /OE = LOW, /LB and /UB = LOW.
  - 5.** Burst read suspend is valid after outputting the first read access data (Q0).

Figure 8-7. Synchronous Burst Read Termination Cycle Timing Chart



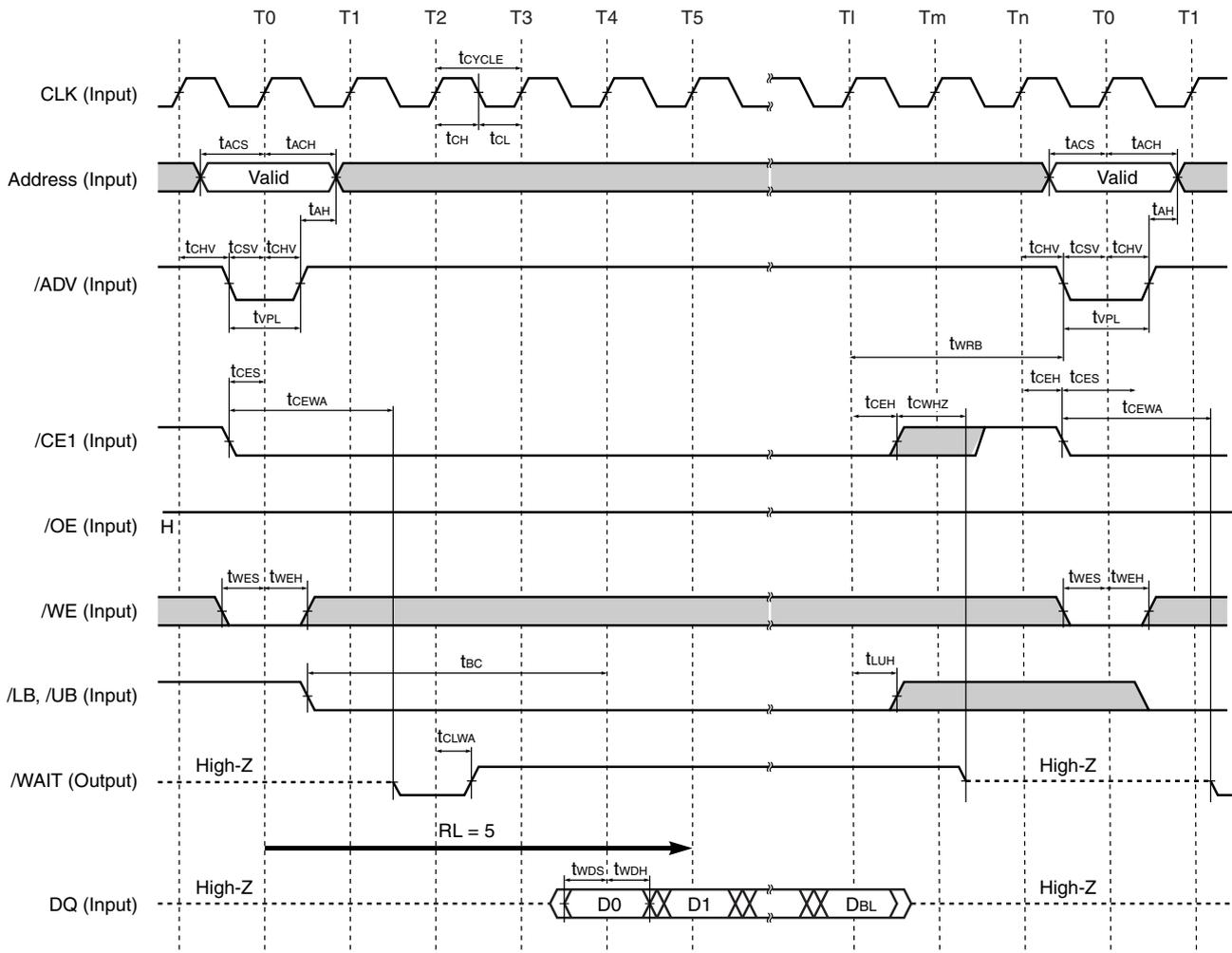
- Remarks 1.** The above timing chart assumes Read Latency is 5.
2. CE2 should be fixed HIGH.
  3. Valid clock edge is the rising edge.
  4.  $t_{oc}$  and  $t_{bc}$  are defined from CLK rising edge of  $RL-1$  to  $/OE = LOW$ ,  $/LB$  and  $/UB = LOW$ .
  5.  $t_{TRB}$  is specified from  $/CE1$  de-assert to  $/CE1$  assert for next operation.
  6. Burst read termination is valid after outputting the first read access data (Q0).
  7. In case continuous burst read is set,  $/CE1$  de-assert is needed for burst read termination.

Figure 8-8. Synchronous Burst Write Cycle Timing Chart (/WE Level Control)



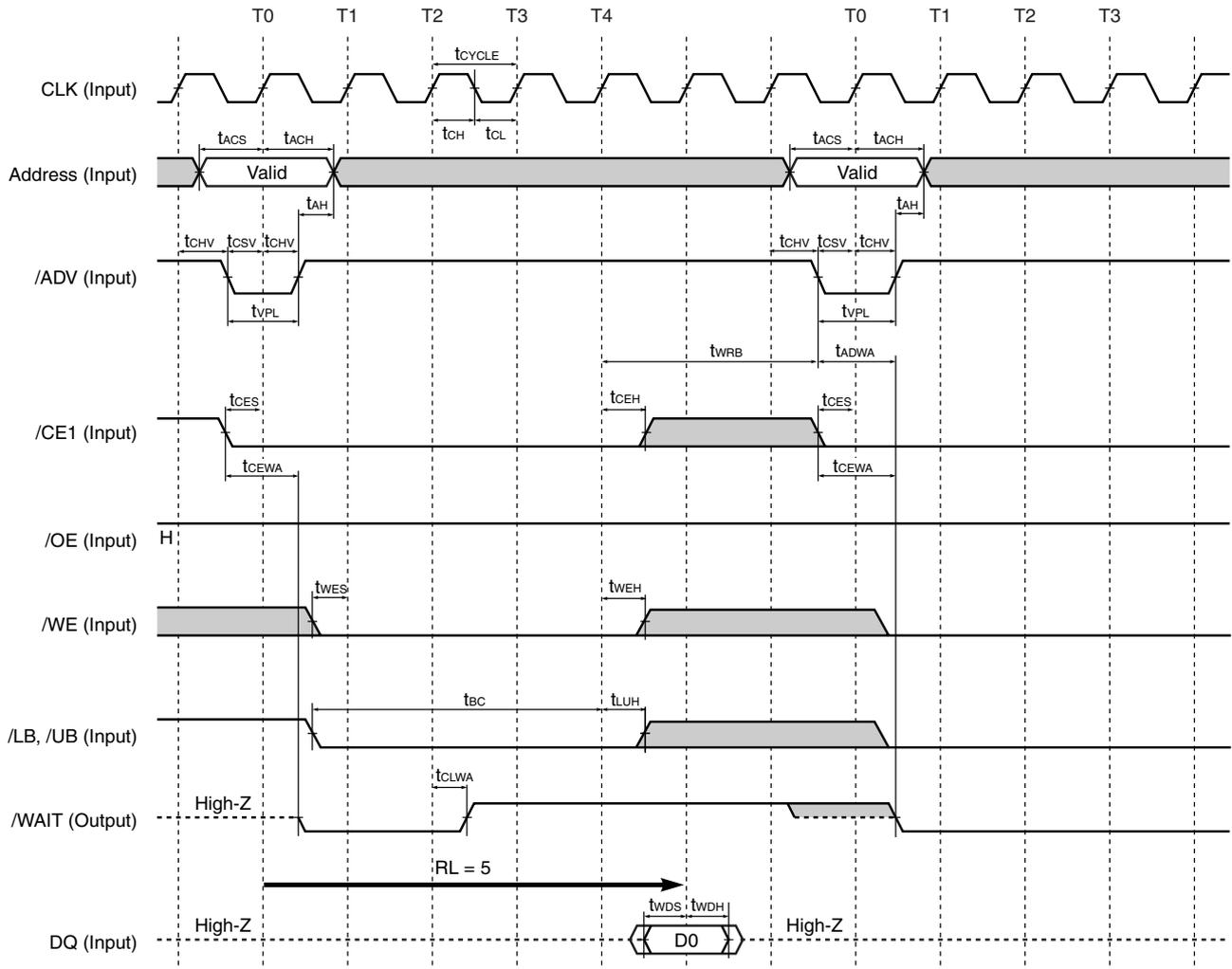
- Remarks 1.** The above timing chart assumes Read Latency is 5 and Burst Length is 8 or 16. DBL means the latest data input of burst length.
2. CE2 should be fixed HIGH.
  3. Valid clock edge is the rising edge.
  4.  $t_{bc}$  is defined from CLK rising edge of RL-1 to /LB and /UB = LOW.

Figure 8-9. Synchronous Burst Write Cycle Timing Chart (/WE Single Clock Control)



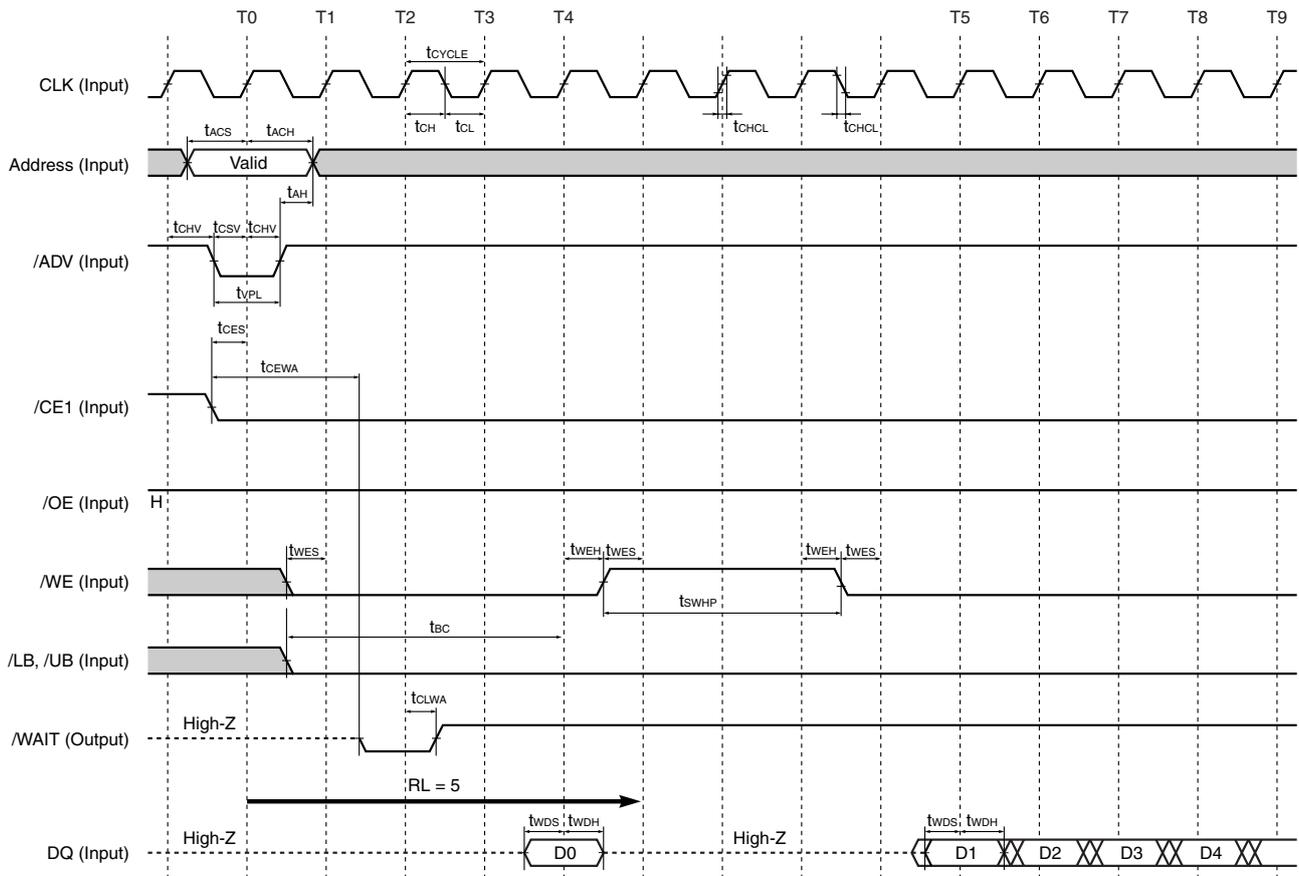
- Remarks 1.** The above timing chart assumes Read Latency is 5 and Burst Length is 8 or 16. DBL means the latest data input of burst length.
2. CE2 should be fixed HIGH.
  3. Valid clock edge is the rising edge.
  4. t<sub>bc</sub> is defined from CLK rising edge of RL-1 to /LB and /UB = LOW.

Figure 8-10. Synchronous Single Write Cycle Timing Chart (/WE level Control)



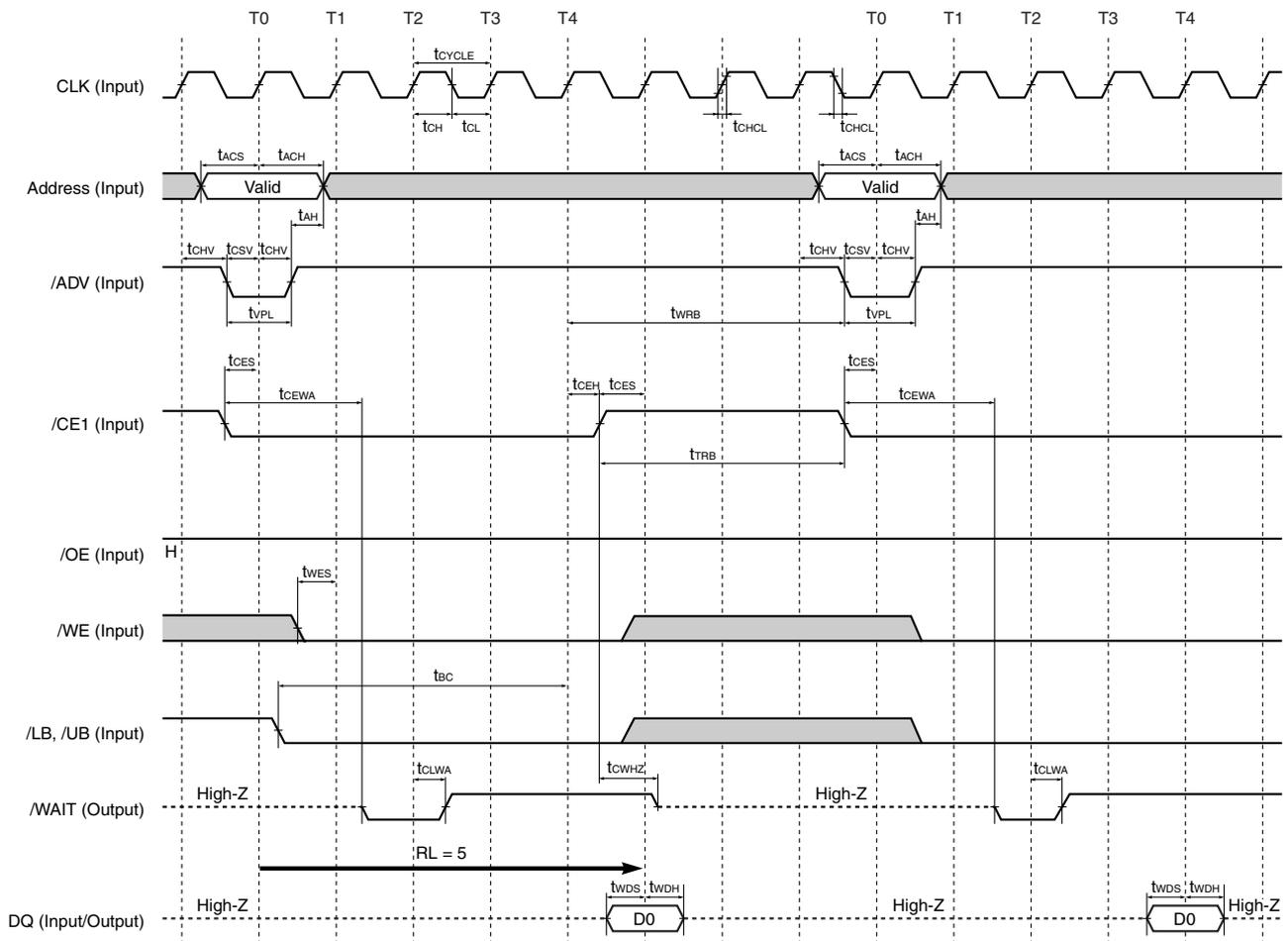
- Remarks 1.** The above timing chart assumes Read Latency is 5.
2. CE2 should be fixed HIGH.
  3. Valid clock edge is the rising edge.
  4. tbc is defined from CLK rising edge of RL-1 to /LB and /UB = LOW.

Figure 8-11. Synchronous Burst Write Suspend Timing Chart



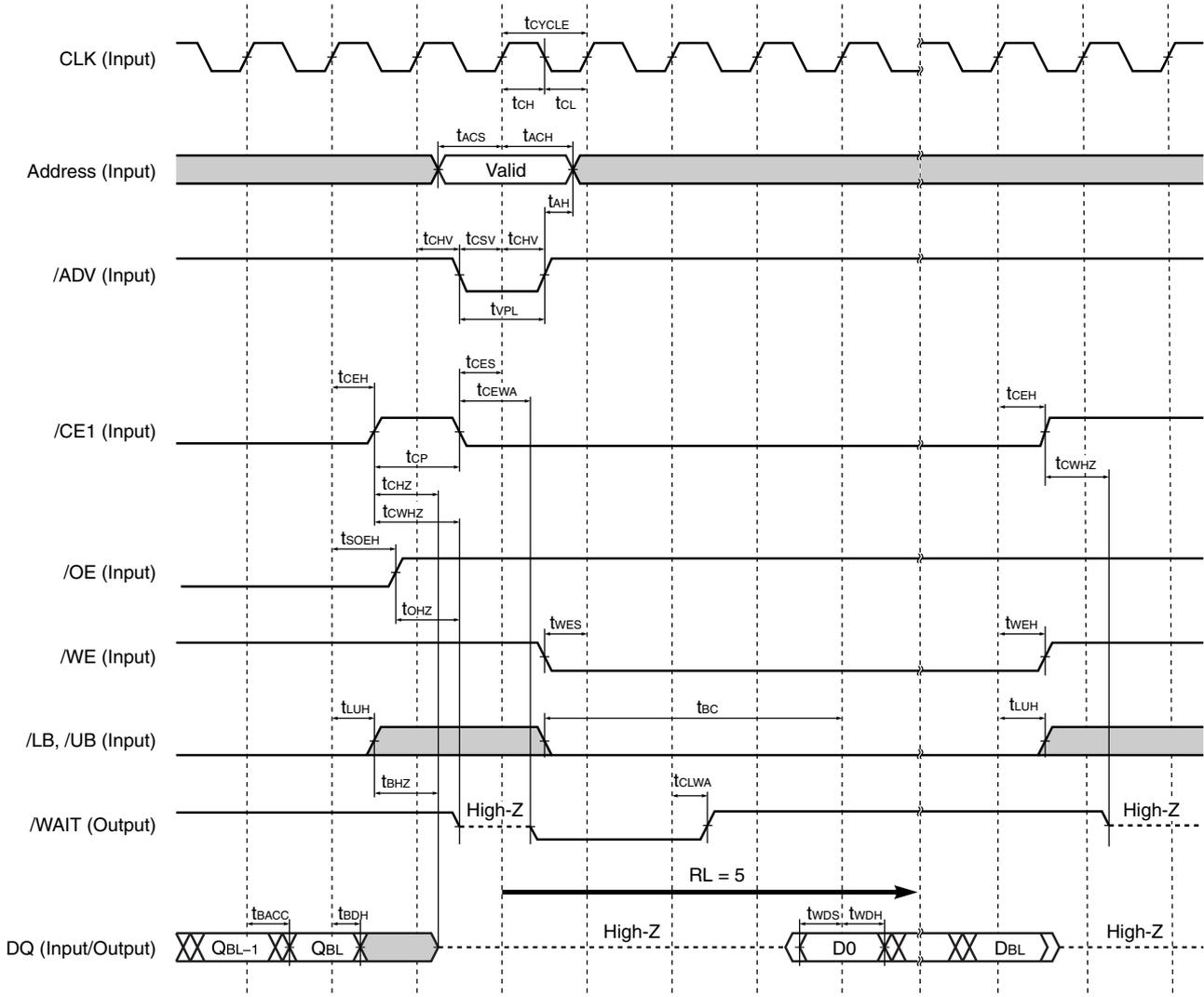
- Remarks**
1. The above timing chart assumes Read Latency is 5.
  2. CE2 should be fixed HIGH.
  3. Valid clock edge is the rising edge.
  4. tbc is defined from CLK rising edge of RL-1 to /LB and /UB = LOW.
  5. Burst write suspend is valid after latching the first write data

Figure 8-12. Synchronous Burst Write Termination Timing Chart



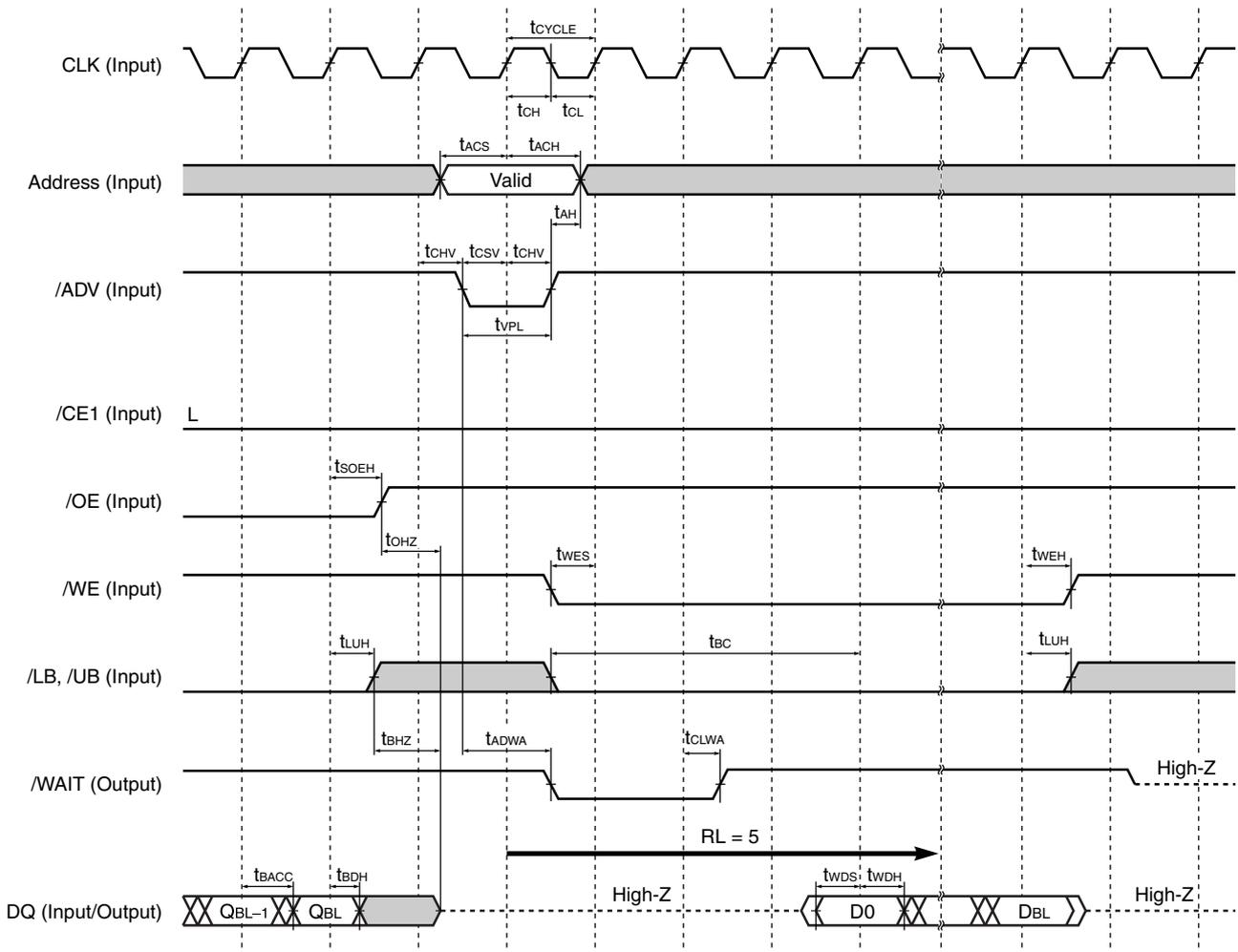
- Remarks 1.** The above timing chart assumes Read Latency is 5.
2. CE2 should be fixed HIGH.
  3. Valid clock edge is the rising edge.
  4. tbc is defined from CLK rising edge of RL-1 to /LB and /UB = LOW.
  5. Burst write suspend is valid after latching the first write data
  6. In case continuous burst write is set, /CE1 de-assert is needed for burst write termination.

Figure 8-13. Synchronous Burst Read – Burst Write Cycle Timing Chart (/CE1 Control)



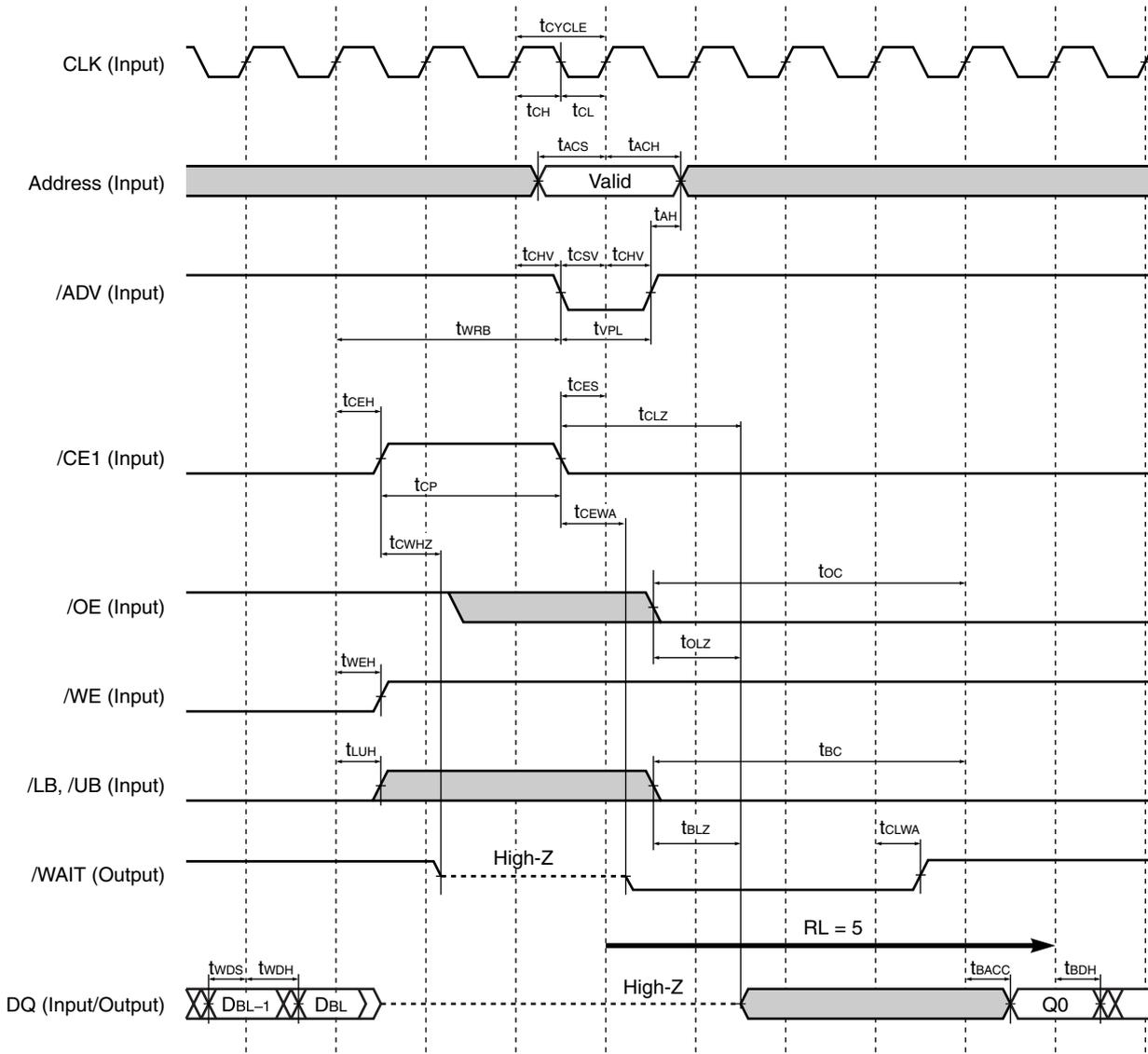
- Remarks 1.** The above timing chart assumes Read Latency is 5 and Burst Length is 8 or 16.  
 QBL means the latest data out of burst length. DBL means the latest data input of burst length.
2. CE2 should be fixed HIGH.
  3. Valid clock edge is the rising edge.
  4.  $t_{BC}$  is defined from CLK rising edge of  $RL-1$  to /LB and /UB = LOW.

Figure 8-14. Synchronous Burst Read – Burst Write Cycle Timing Chart (/ADV Control)



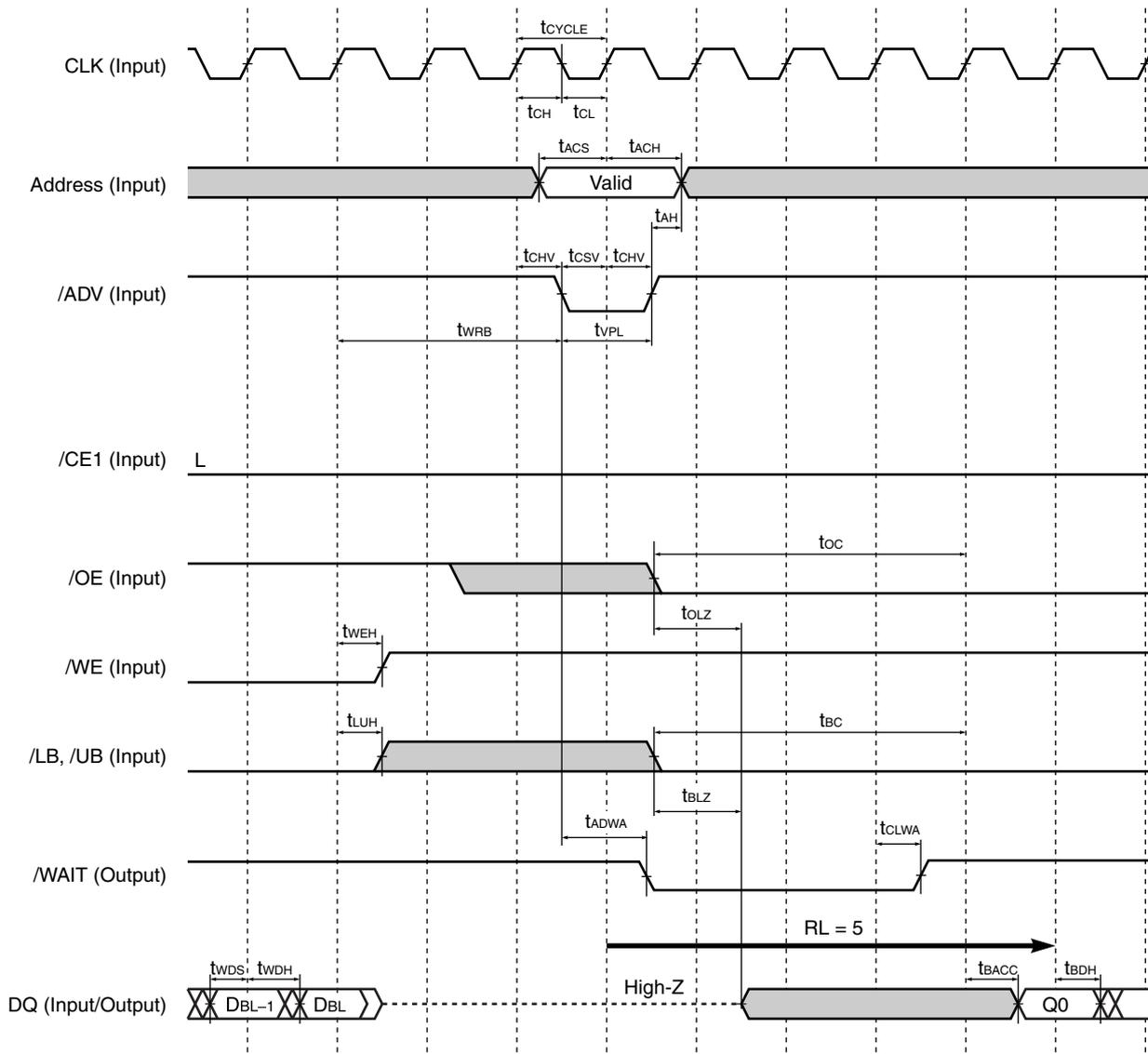
- Remarks 1.** The above timing chart assumes Read Latency is 5 and Burst Length is 8 or 16.  
 QBL means the latest data out of burst length. DBL means the latest data input of burst length.
2. CE2 should be fixed HIGH.
  3. Valid clock edge is the rising edge.
  4. tBC is defined from CLK rising edge of RL-1 to /LB and /UB = LOW.

Figure 8-15. Synchronous Burst Write – Burst Read Cycle Timing Chart (/CE1 Control)



- Remarks 1.** The above timing chart assumes Read Latency is 5 and Burst Length is 8 or 16.  
 DBL means the latest data input of burst length.
2. CE2 should be fixed HIGH.
  3. Valid clock edge is the rising edge.
  4.  $t_{oc}$  and  $t_{bc}$  are defined from CLK rising edge of RL-1 to /OE = LOW, /LB and /UB = LOW.

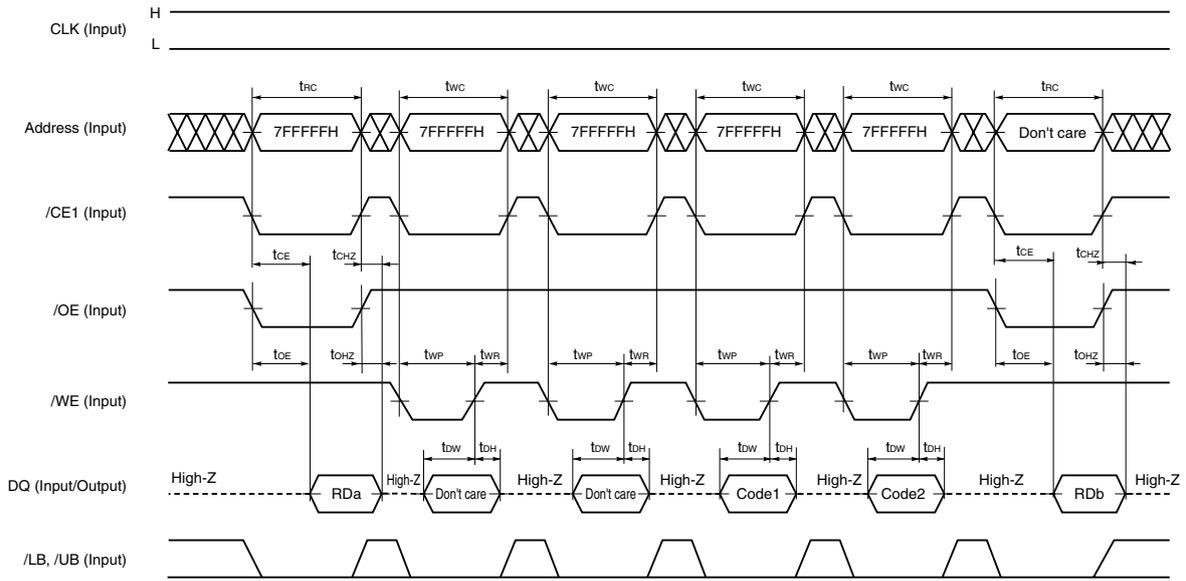
Figure 8-16. Synchronous Burst Write – Burst Read Cycle Timing Chart (/ADV Control)



- Remarks 1.** The above timing chart assumes Read Latency is 5 and Burst Length is 8 or 16.  
 $DBL$  means the latest data input of burst length.
2. CE2 should be fixed HIGH.
  3. Valid clock edge is the rising edge.
  4.  $t_{oc}$  and  $t_{bc}$  are defined from CLK rising edge of  $RL-1$  to /OE = LOW, /LB and /UB = LOW.

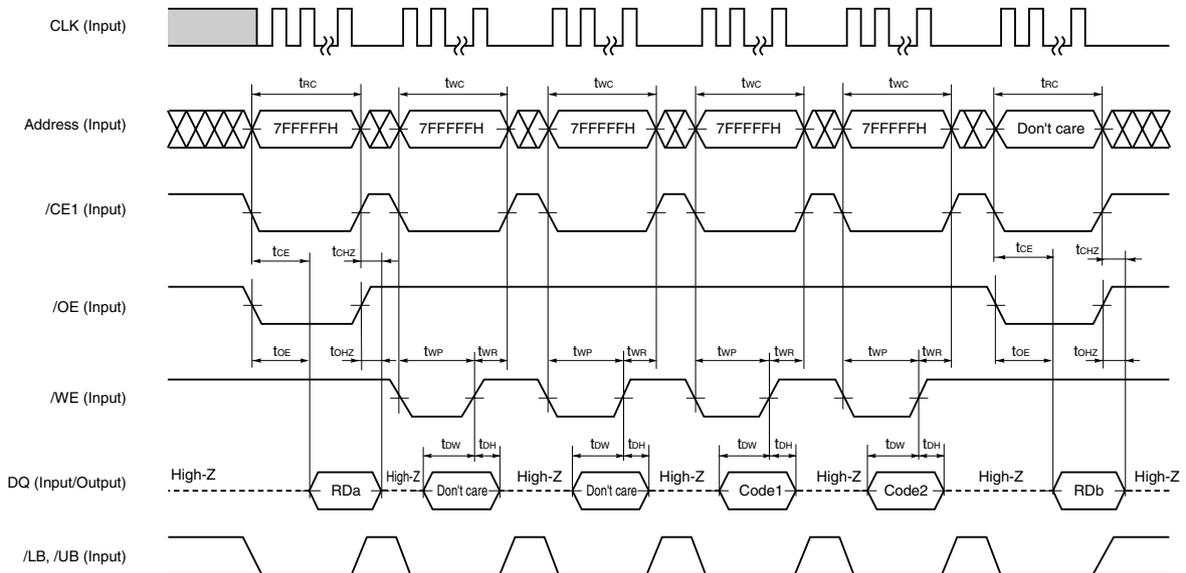
9. Mode Register Setting Timing

Figure 9-1. Mode Register Setting Timing Chart (Asynchronous Timing + CLK fixed LOW/HIGH)



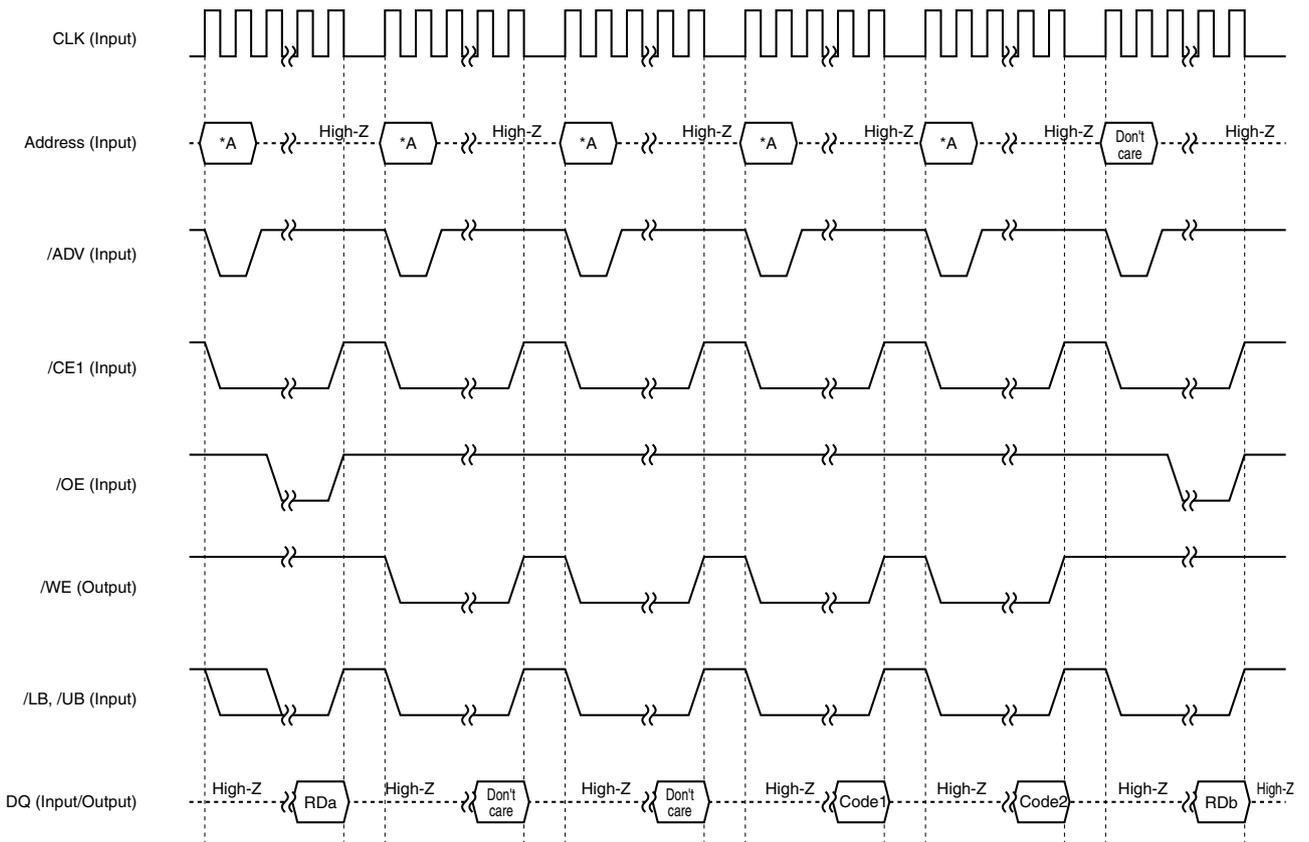
- Remarks 1.** For the data of Code1 and Code2, refer to **Table 5-1. Mode Register Definition (4th Bus Cycle)** and **Table 5-2. Mode Register Definition (5th Bus Cycle)**.
2. RDa and RDb are the output data.
  3. /ADV fixed LOW or toggle HIGH → LOW → HIGH.

Figure 9-2. Mode Register Setting Timing Chart (Asynchronous Timing + Toggle CLK)



- Remarks 1.** For the data of Code1 and Code2, refer to **Table 5-1. Mode Register Definition (4th Bus Cycle)** and **Table 5-2. Mode Register Definition (5th Bus Cycle)**.
2. RDa and RDb are the output data.
  3. /ADV fixed LOW or toggle HIGH → LOW → HIGH.

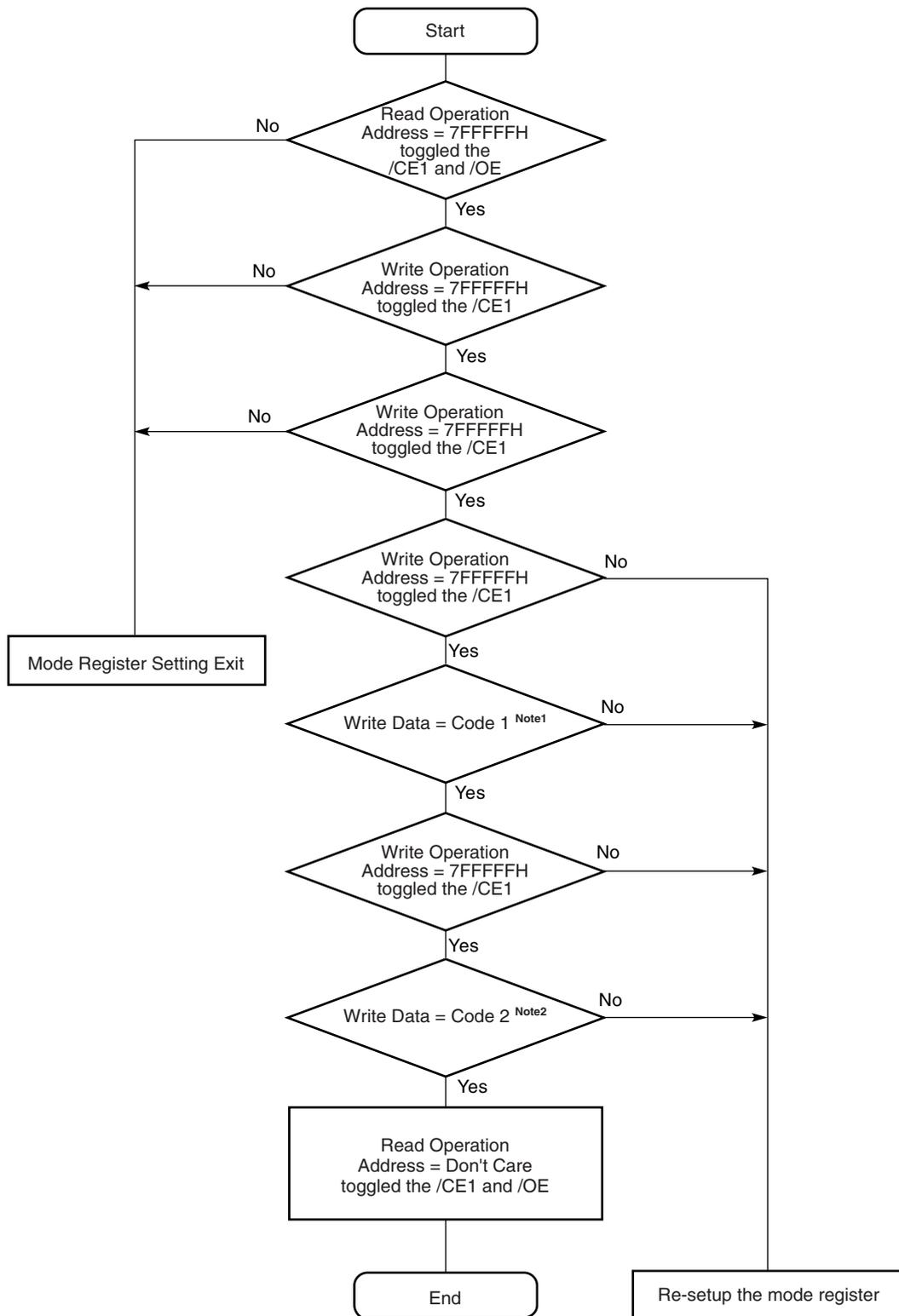
Figure 9-3. Mode Register Setting Timing Chart (Synchronous Timing)



**Caution** Refer to 8. Synchronous Read/Write specification.

- Remarks 1.** \*A means the highest address (7FFFFFFH).
2. For the data of Code1 and Code2, refer to **Table 5-1. Mode Register Definition (4th Bus Cycle)** and **Table 5-2. Mode Register Definition (5th Bus Cycle)**.
  3. RDa and RDb are the output data.

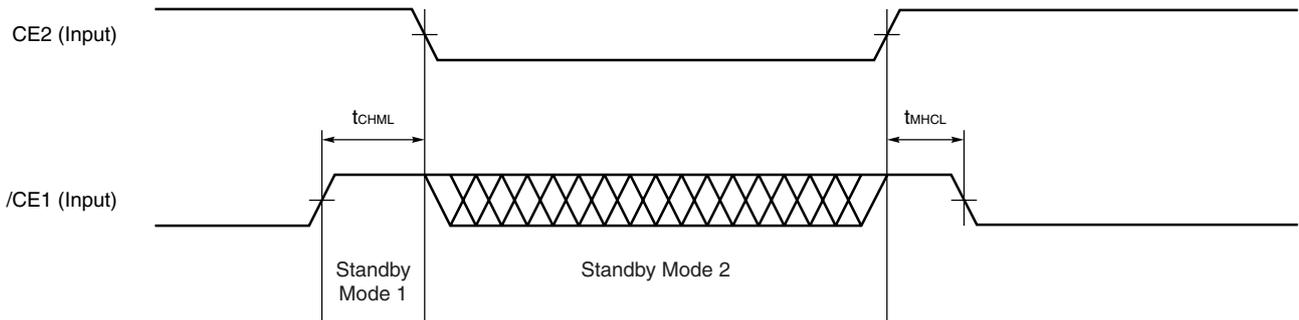
Figure 9-4. Mode Register Setting Flow Chart



- Notes 1. Refer to Table 5-1.
- 2. Refer to Table 5-2.

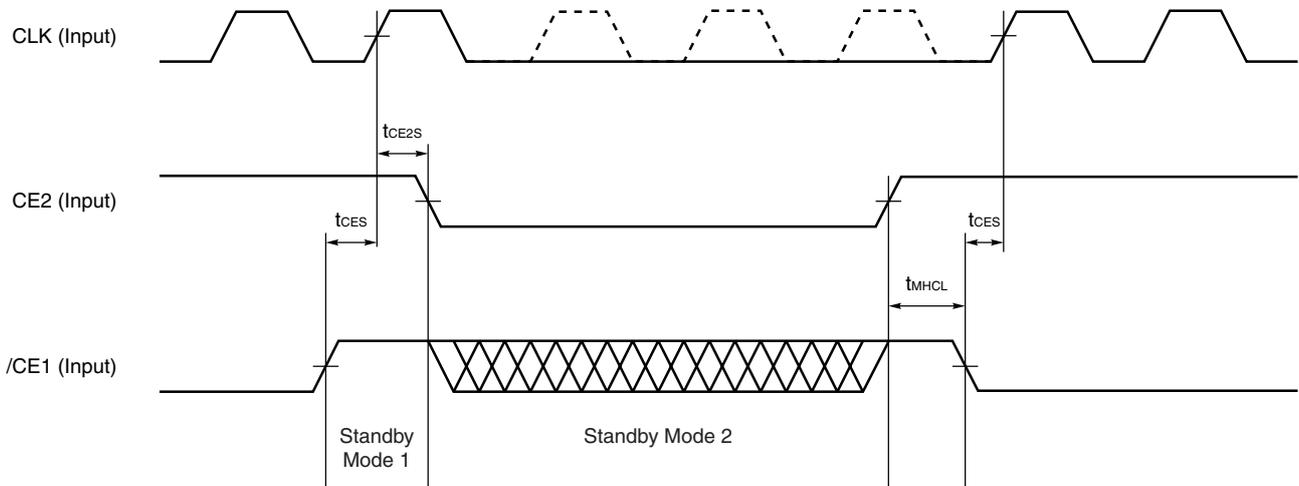
10. Standby Mode Timing Chart

Figure 10-1. Standby Mode 2 Entry / Exit Timing Chart (Asynchronous Mode)



★

Figure 10-2. Standby Mode 2 Entry / Exit Timing Chart (Synchronous Mode)



Standby Mode 2 Entry / Exit

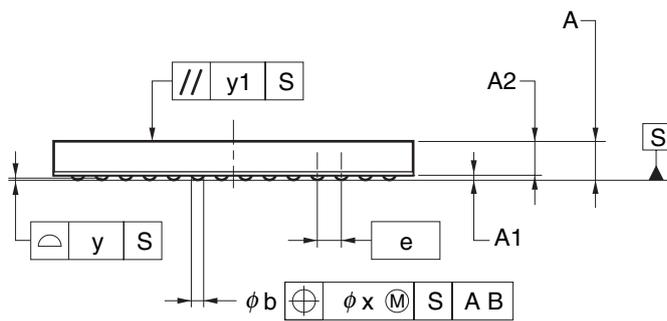
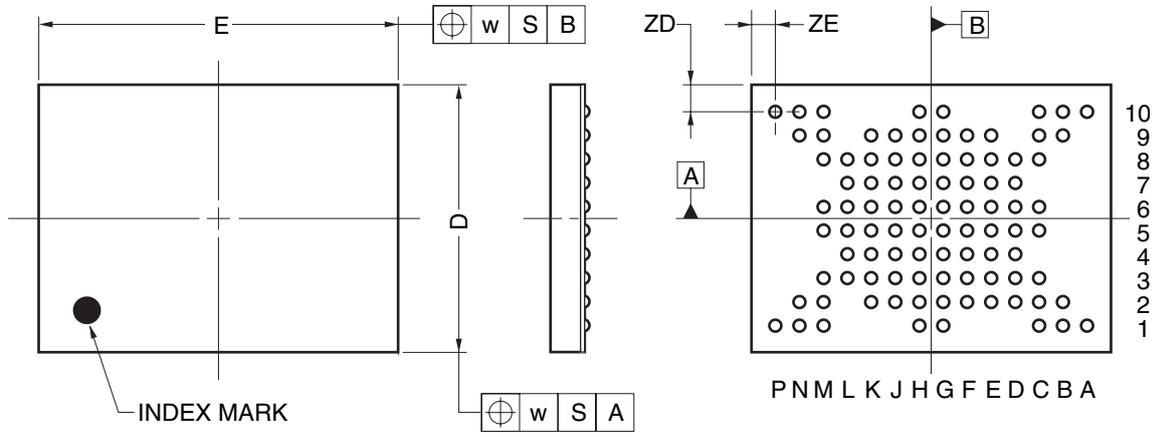
Parameter	Symbol	MIN.	MAX.	Unit	Note
Standby mode 2 entry /CE1 HIGH to CE2 LOW	$t_{CHML}$	0		ns	
Standby mode 2 exit to normal operation CE2 HIGH to /CE1 LOW	$t_{MHCL}$	30		ns	1
		300		μs	2
/CE1 = HIGH setup time to CLK	$t_{CES}$	5		ns	
CE2 = LOW hold time to CLK	$t_{CE2S}$	1		ns	

- Notes**
- This is the time it takes to return to normal operation from Standby Mode 2 (data hold: 32M bits / 16M bits / 8M bits).
  - This is the time it takes to return to normal operation from Standby Mode 2 (data not held).

11. Package Drawing

The following is a package drawing of package sample.

93-PIN TAPE FBGA (12x9)



ITEM	MILLIMETERS
D	9.0±0.1
E	12.0±0.1
w	0.2
e	0.8
A	1.3±0.1
A1	0.16±0.05
A2	1.14
b	0.40±0.05
x	0.08
y	0.1
y1	0.2
ZD	0.9
ZE	0.8
<b>P93F9-80-CR2</b>	

## 12. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the  $\mu$ PD46128512-X package sample.

### Type of Surface Mount Device

$\mu$ PD46128512F9-CR2 : 93-pin TAPE FBGA (12x9)

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
2nd edition/ Sep. 2005	p.6	p.6	Modification	Burst Operation	Notes 3 and 8 have been modified.
			Addition		Note 10 has been added.
	p.14	p.14	Modification	3. Page Read Operation	Text has been modified.
				3.1 Features of Page Read Operation	Note has been modified.
	p.17	p.17	Modification	4.4 Single Write	Text has been modified.
				4.5 /WE Control	Text has been modified.
	p.18	p.18	Modification	4.6 Burst Read Suspend/ Resume	Text has been modified.
	p.19	p.19	Modification	4.7 Burst Write Suspend/ Resume	Text has been modified.
	p.22	p.22	Modification	4.10.1 Feature of /WAIT output	Text has been modified.
	p.23	p.23	Addition	Figure 4-8. Read /WAIT Output (/CE1 = LOW, /ADV = HIGH → LOW)	Text has been added.
	p.25	p.25	Addition	Table 4-1. Burst Sequence	Remark 2 has been added.
	p.26	p.26	Addition	Table 4-2. Dummy Wait Cycles and Read Latency	“(Write Latency = n-1)” has been added in parameter of table.
			Modification		Remark has been modified.
	p.27	p.27	Addition	4.11 Reset Function from Synchronous Burst Mode to Asynchronous Page Mode	“Refer to Figure 2-1. Standby Mode State Machine.” has been added.
	p.28	p.28	Modification	5.1 Mode Register Setting Method	“read a specific address” → “read any address”
			Addition	5.2 Cautions for Setting Mode Register	“except page mode (M = 1)” has been added.
	p.32	p.32	Modification	5. 12 Caution for Timing Chart of Setting Mode	Text has been modified.
	p.42	p.42	Addition	Figure 7-10. Asynchronous Page Read Cycle Timing Chart	Cautions 4 and 5 have been added.
pp.43-56	pp.43-56	Modification	Each Figures	Remark has been modified.	
p.57	p.57	Modification	8. Synchronous AC Specification, Timing Chart	Title has been modified.	
p.77	p.77	Modification	Figure 10-2. Standby Mode 2 Entry / Exit Timing Chart (Synchronous Mode)	Title has been modified.	

## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

**⑤ POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

**⑥ INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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