FUJITSU

MOS 32768-BIT DYNAMIC RANDOM ACCESS MEMORY

Separate S2Gnls

MB 8132N/E/H-L

MB 8132N/E/H-H

March 1980

32,768-BIT DYNAMIC RANDOM ACCESS MEMORY

S-33 Orig

002481

T-2481 FUJ

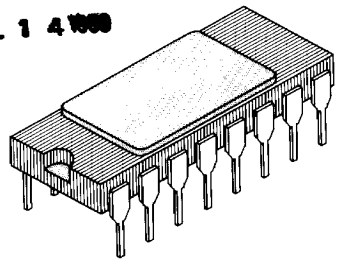
The Fujitsu MB 8132 is a fully decoded, dynamic NMOS random access memory organized as 32768 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB 8132 to be housed in a standard 16 pin DIP.

The MB 8132 comes in two types — "H" and "L". In the "L" version, A15 is externally pulled low, always. In the "H" version, A15 is externally pulled high, always. The units are marked with these designators to minimize confusion during use.

The MB 8132 is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

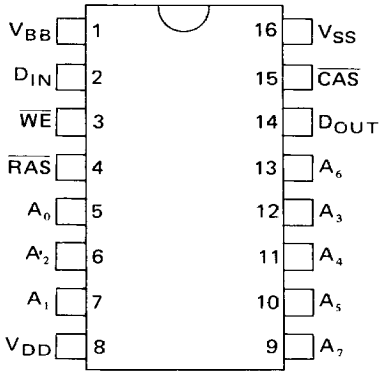
Clock timing requirements are noncritical, and power supply tolerances are very wide. All inputs are TTL compatible; the output is open drain.



CERAMIC PACKAGE
DIP-16C-A01

- 32,768 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  120 ns max (MB 8132H)
  150 ns max (MB 8132E)
  200 ns max (MB 8132N)
- Cycle time,
  320 ns min (MB 8132H)
  320 ns min (MB 8132E)
  330 ns min (MB 8132N)
- Low power: 385 mW active, 20 mW standby (max)
- ±10% tolerance on +7 volt supply
- ±0.5 volt tolerance on −2.5 volt supply
- All inputs TTL compatible, low capacitive load
- Open drain output
- "Gated" $\overline{CAS}$
- 128 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in

PIN ASSIGNMENT



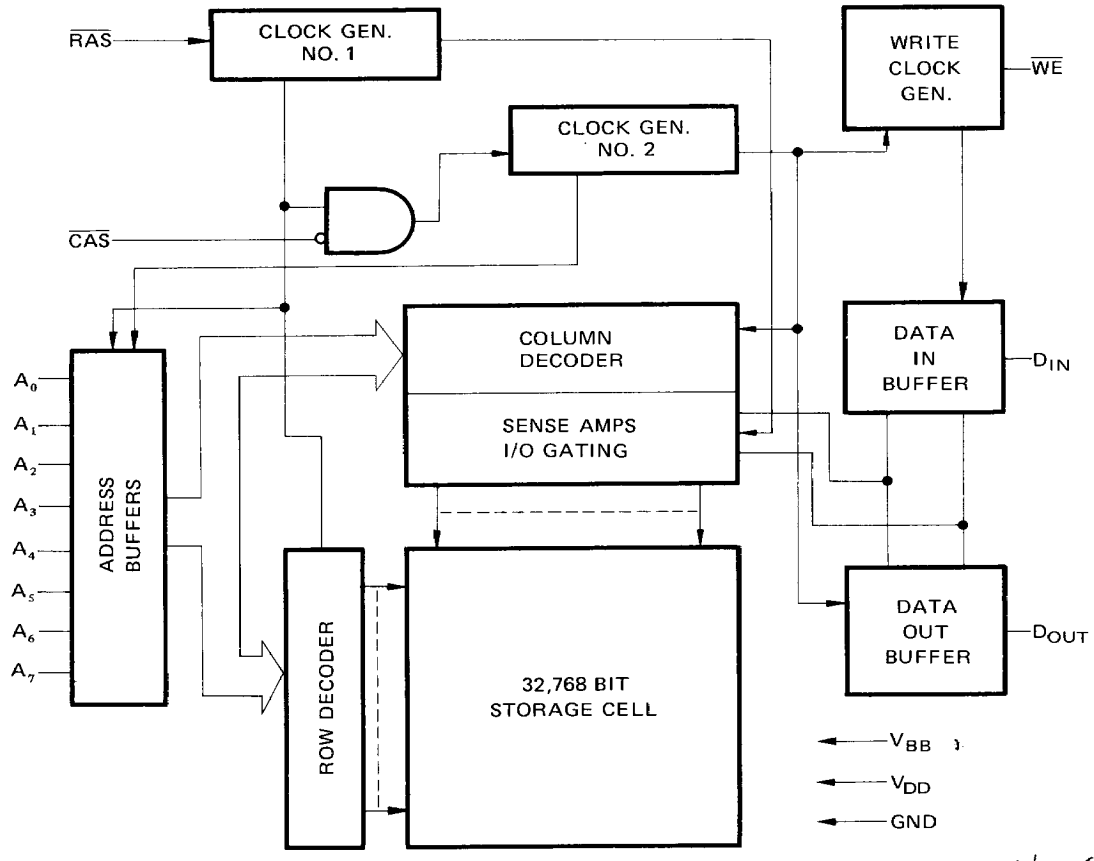
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{BB}	V_{IN}, V_{OUT}	-0.5 to +13	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 to +9	V
$V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} > 0V$)	—	0	V
Storage temperature	Tstg	-55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current	—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB 8132 BLOCK DIAGRAM



–L: A15 TIED "LOW"
–H: A15 TIED "HIGH"
NOTE: A15 IS MULTIPLEXED TO DEVICE PIN A7.

Only 15 bits required to address 32k cells
∴ A15 (16th bit) which comes in to A7 for column address is high for H version and Low for L version.
Jim Cain

CAPACITANCE (T_A = 25°C)

Put on seperate 52GN's - rgb 5-15-8

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0~A_7, D_{IN}	C_{IN1}	–	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	–	10	pF
Output Capacitance D_{OUT}	C_{OUT}	–	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	NOTES	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	1	V_{DD}	6.3	7.0	7.7	V	0°C to +70°C
	1	V_{SS}	0	0	0	V	
	1	V_{BB}	-2.0	-2.5	-3.0	V	
Input High Voltage $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	1	V_{IHC}	2.4	–	6.5	V	
Input High Voltage except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	1	V_{IH}	2.2	–	6.5	V	
Input Low Voltage, all inputs	1	V_{IL}	-1.0	–	0.8	V	

Note:

1) All voltages are referenced to V_{SS}.

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
OPERATING CURRENT	I_{DD1}		50	mA
Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	I_{BB1}		400	μA
STANDBY CURRENT	I_{DD2}		2.5	mA
Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IHC})	I_{BB2}		100	μA
REFRESH CURRENT	I_{DD3}		40	mA
Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = min)	I_{BB3}		400	μA
PAGE MODE CURRENT	I_{DD4}		30	mA
Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)	I_{BB4}		400	μA
INPUT LEAKAGE CURRENT Input leakage current, any input (V_{BB} = -2.5V, 0V≤V_{IN}≤7V, all other pins not under test = 0V)	I_{IL}	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V≤V_{OUT}≤7V)	I_{OL}	-10	10	μA
OUTPUT LEVELS Output low voltage (I_{OL} = 12 mA)	V_{OL}		0.4	V

DYNAMIC CHARACTERISTICS

NOTES 2,3,4

(Recommended operating conditions unless otherwise noted.)

Parameter	NOTES	Symbol	MB 8132N-L MB 8132N-H		MB 8132E-L MB 8132E-H		MB 8132H-L MB 8132H-H		Units
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		2		2		2	ms
Random Read/Write Cycle Time		t_{RC}	330		320		320		ns
Read-Write Cycle Time		t_{RWC}	375		375		320		ns
Page Mode Cycle Time		t_{PC}	225		170		160		ns
Access Time from $\overline{RAS}$	5 7	t_{RAC}		200		150		120	ns
Access Time from $\overline{CAS}$	6 7	t_{CAC}		135		100		80	ns
Output Buffer Turn Off Delay		t_{OFF}	0	50	0	40	0	35	ns
Transition Time		t_T	3	50	3	35	3	35	ns
$\overline{RAS}$ Precharge Time		t_{RP}	120		100		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	200	32000	150	32000	120	32000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	135		100		80		ns
$\overline{CAS}$ Precharge Time		t_{CP}	80		60		60		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	135	10000	100	10000	80	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	200		150		120		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	8 9	t_{RCD}	35	65	30	50	25	40	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0		0		0		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	25		20		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	55		45		40		ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	120		95		80		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time		t_{RCH}	0		0		0		ns
Write Command Set Up Time	10	t_{WCS}	-10		-10		0		ns
Write Command Hold Time		t_{WCH}	55		45		40		ns
Write Command Hold Time Reference to $\overline{RAS}$		t_{WCR}	120		95		80		ns
Write Command Pulse Width		t_{WP}	55		45		40		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	80		60		60		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	80		60		60		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	55		45		40		ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	120		95		80		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	10	t_{CWD}	95		70		60		ns
$\overline{RAS}$ to $\overline{WE}$ Delay	10	t_{RWD}	160		120		100		ns

Notes:

2) Several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

3) Dynamic measurements assume t_T=5ns.

4) V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

5) Assumes that $t_{RCD} \leqslant t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

6) Assumes that $t_{RCD} \geqslant t_{RCD}$ (max).

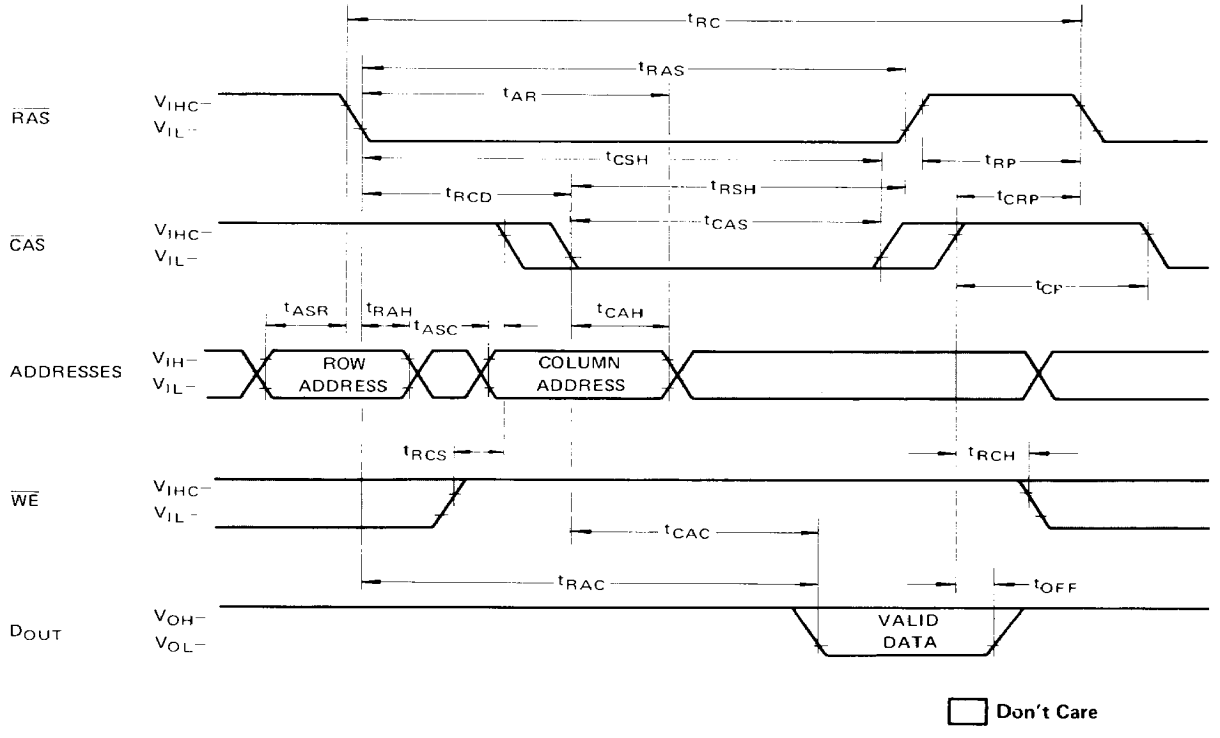
7) Refer to test conditions.

8) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

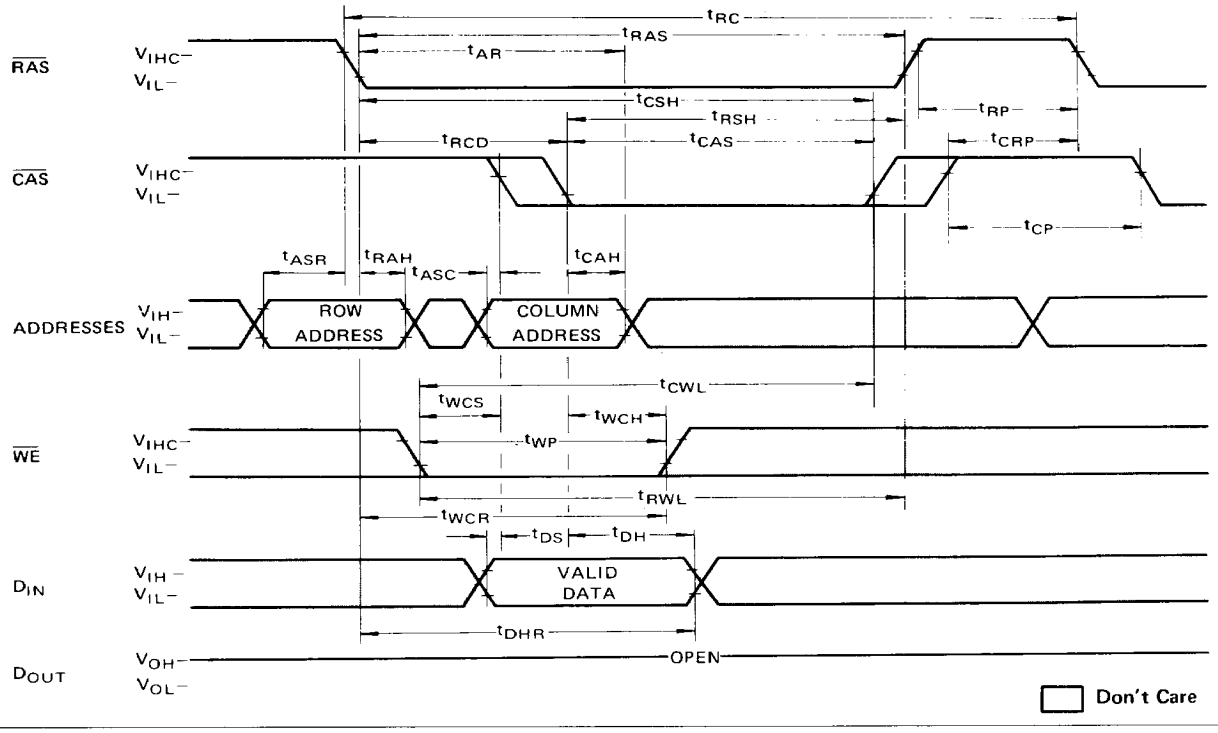
9) t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T = 5ns) + t_{ASC} (min)

10) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqslant t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
If $t_{CWD} \geqslant t_{CWD}$ (min) and $t_{RWD} \geqslant t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

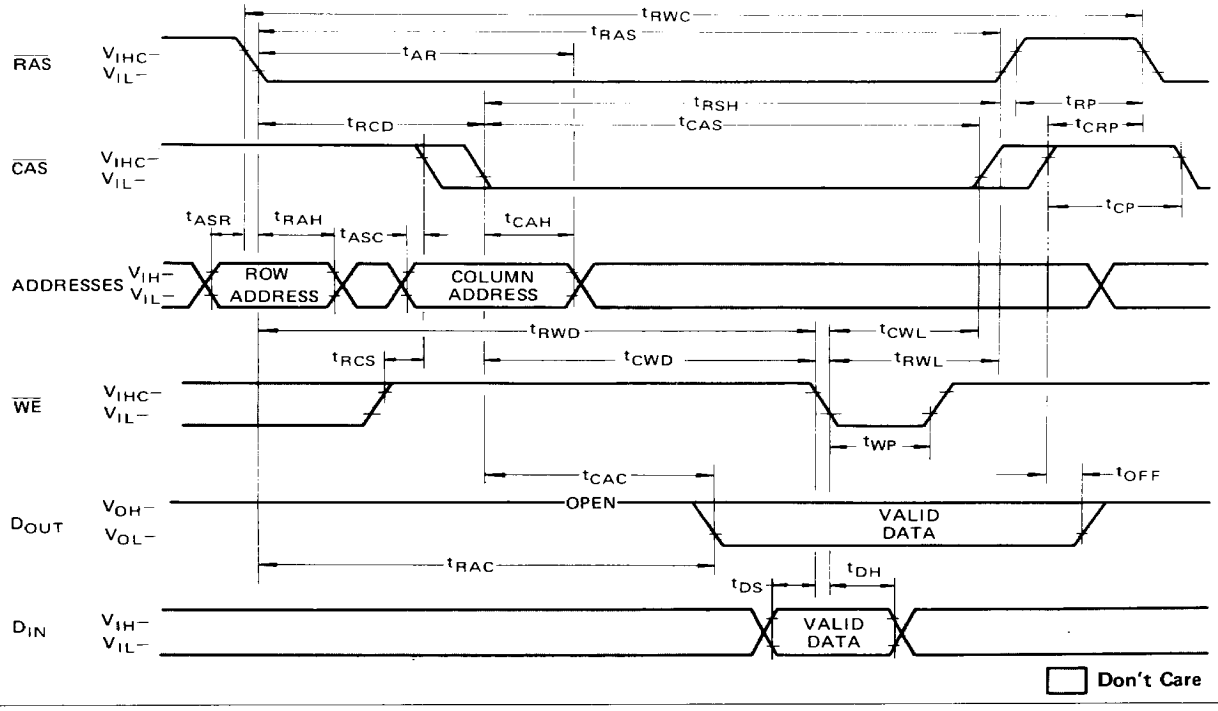
READ CYCLE TIMING DIAGRAM



WRITE CYCLE (EARLY WRITE)

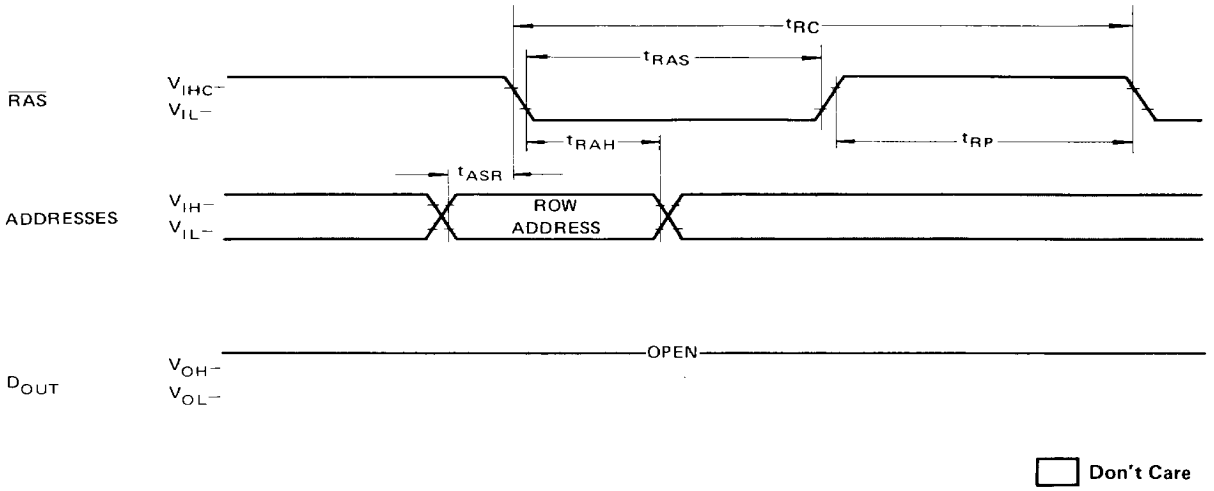


READ–WRITE/READ–MODIFY–WRITE CYCLE

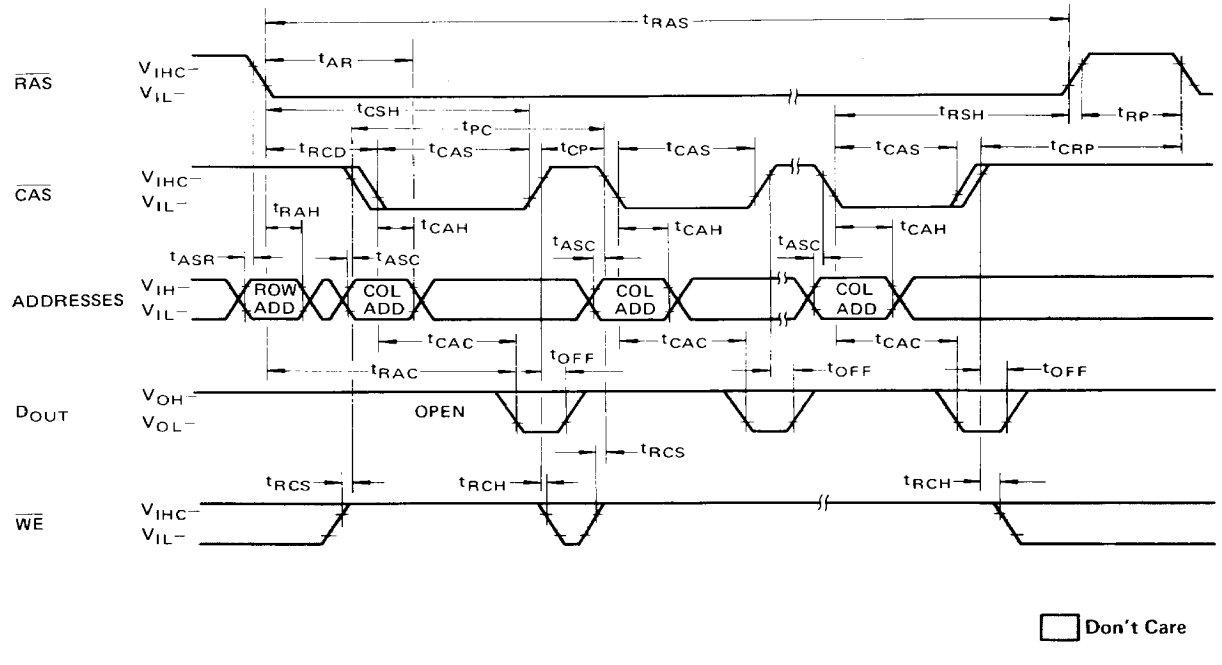


"$\overline{RAS}$–ONLY" REFRESH CYCLE

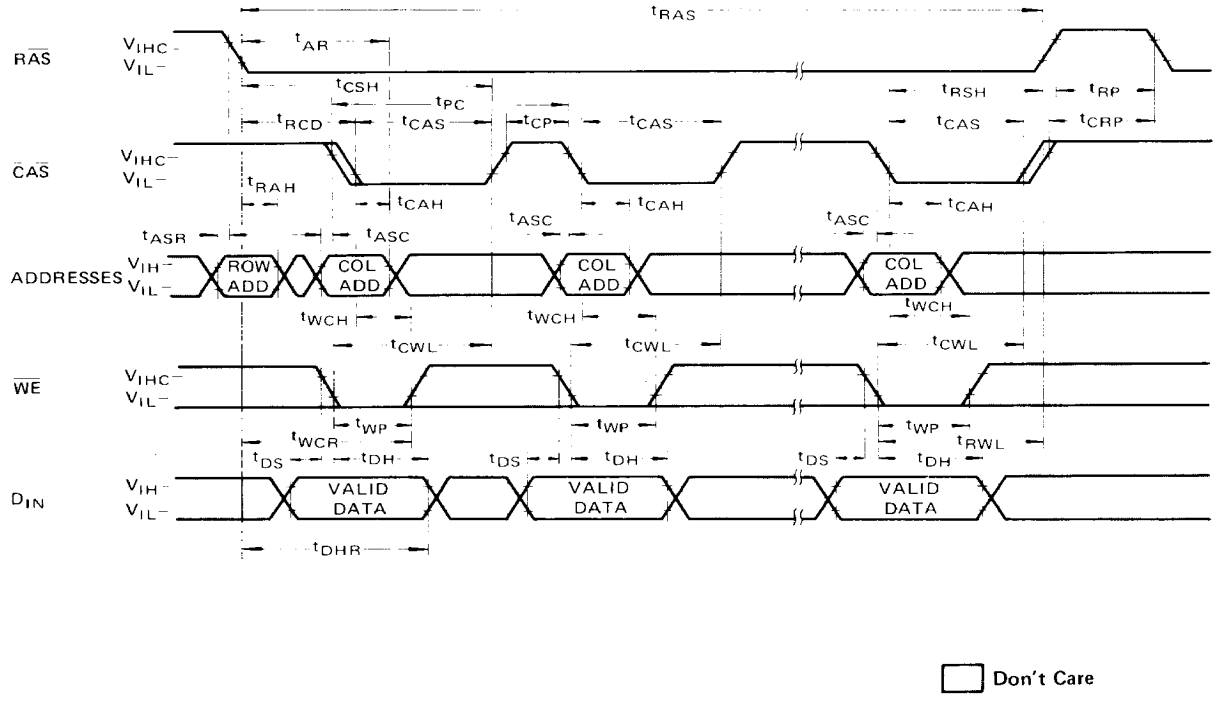
NOTE: $\overline{CAS}$ = V_{IHC}, $\overline{WE}$ = Don't care



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



DESCRIPTION

Address Inputs:
A total of sixteen binary input address bits are required to decode any 1 of 32768 storage cell locations within the MB 8132. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). A15 is always low for the "L" version and high for the "H" version. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low(0) dictates write mode. Data input is disabled when read mode is selected. $\overline{WE}$ can be driven by standard TTL circuits without a pull-up resistor.

Data Input:
Data is written into the MB 8132 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be

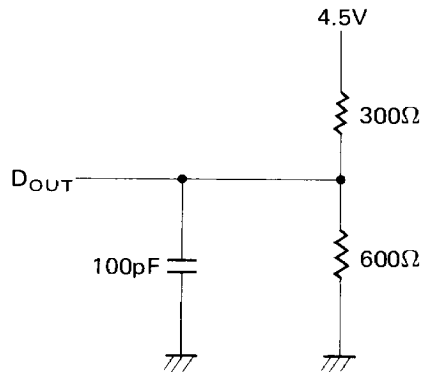
delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is open drain type. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:
Page-mode operation permits strobing the row-address into the MB 8132 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Fig. 2 – DYNAMIC TEST CONDITIONS



TYPICAL CHARACTERISTICS

Fig. 3

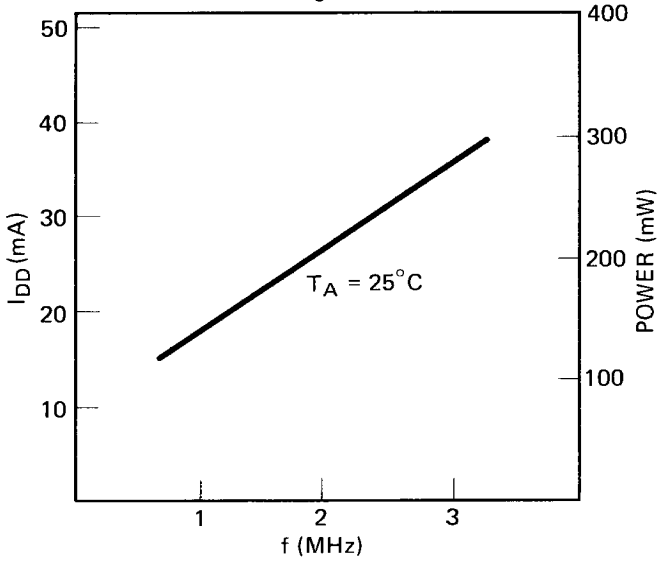


Fig. 4

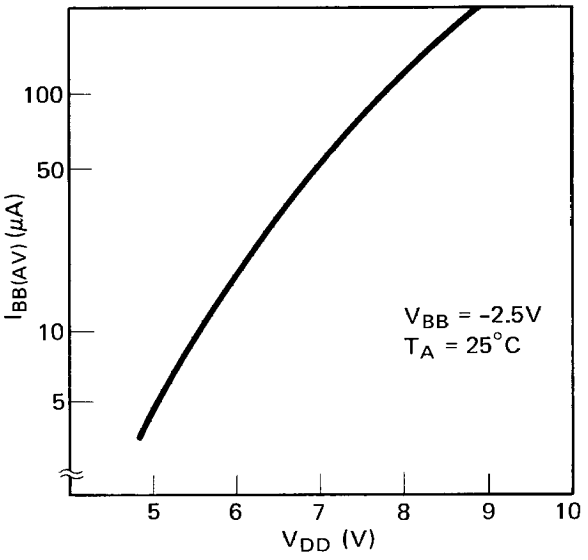


Fig. 5

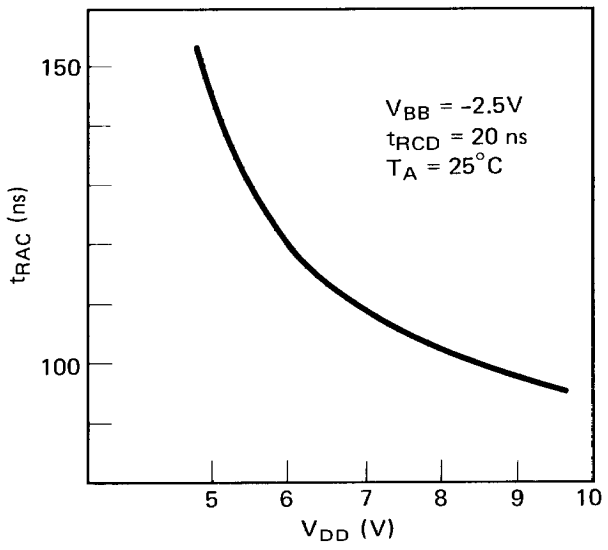
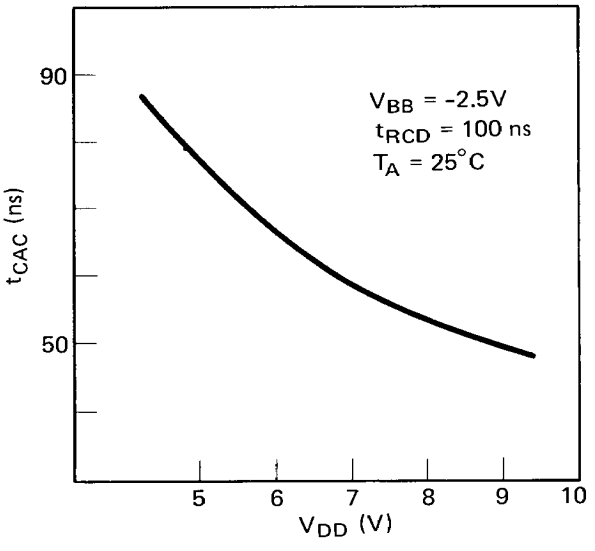
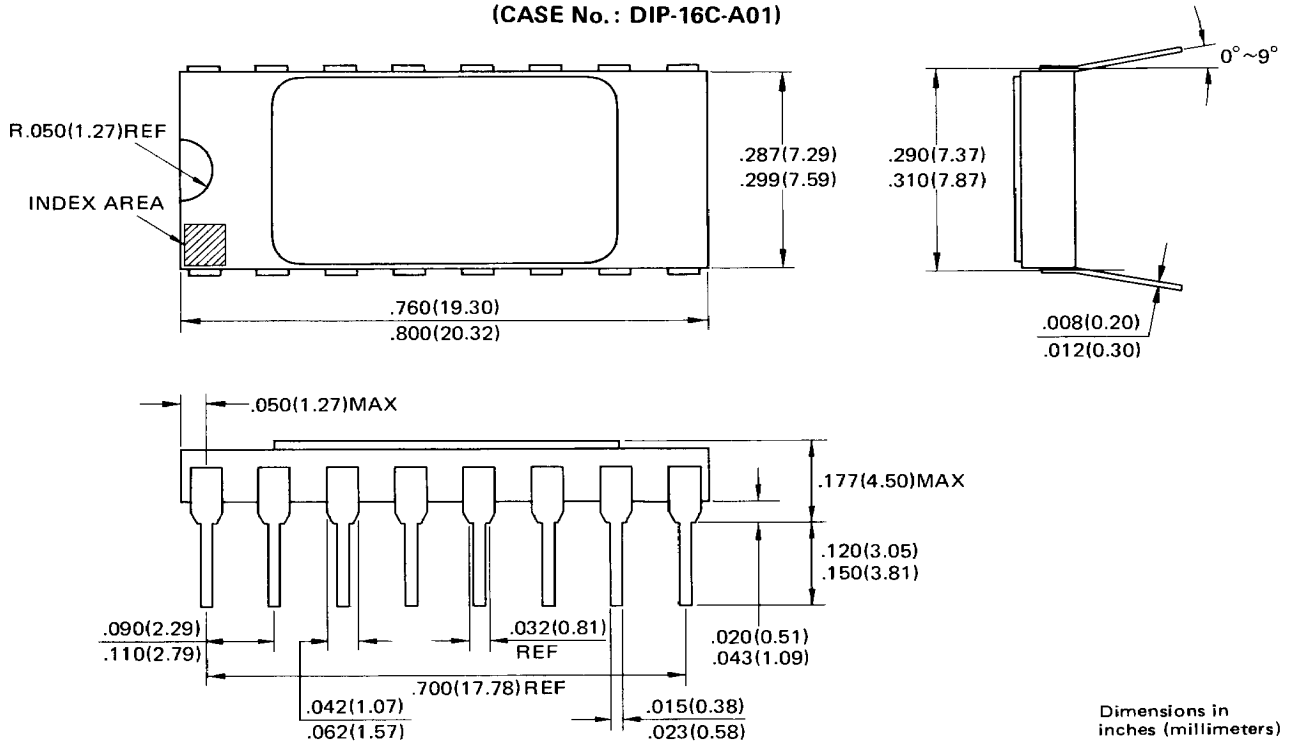


Fig. 6



PACKAGE DIMENSIONS

16-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A01)



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