ISP1123

Universal Serial Bus compound hub

Rev. 01 — 5 October 1999 **Preliminary specification**

1. General description

The ISP1123 is a compound Universal Serial Bus (USB) hub device which complies with *USB Specification Rev. 1.1*. It integrates a Serial Interface Engine (SIE), hub repeater, hub controller, USB data transceivers and a 3.3 V voltage regulator. It has a configurable number of downstream ports, ranging from 2 to 5, with one port dedicated to an embedded or non-removable function.

The ISP1123 can be bus-powered, self-powered or hybrid-powered. When it is hybrid-powered the hub functions are powered by the upstream power supply (V_{BUS}), but the downstream ports are powered by an external 5 Volt supply. The low power consumption in 'suspend' mode allows easy design of equipment that is compliant with the ACPI™, OnNow™ and USB power management requirements.

The ISP1123 has built-in overcurrent sense inputs, supporting individual and ganged mode overcurrent protection for downstream ports. All ports (including the hub) have GoodLink™ indicator outputs for easy visual monitoring of USB traffic. The ISP1123 has a serial I^2C-bus interface for external EEPROM access and a reduced frequency (6 MHz) crystal oscillator. These features allow significant cost savings in system design and easy implementation of advanced USB functionality into PC peripherals.

2. Features

- High performance USB hub device with integrated hub repeater, hub controller, Serial Interface Engine (SIE), data transceivers and 3.3 V voltage regulator
- Complies with *Universal Serial Bus Specification Rev. 1.1* and ACPI, OnNow and USB power management requirements
- Downstream port 1 dedicated to a non-removable function, correctly reported in the related descriptors
- Configurable from 2 to 5 downstream ports with automatic speed detection
- Internal power-on reset and low voltage reset circuit
- Supports bus-powered, hybrid-powered and self-powered application
- Individual or global power switching for downstream ports
- Individual or ganged port overcurrent protection with built-in sense circuits
- 6 MHz crystal oscillator with on-chip PLL for low EMI
- Visual USB traffic monitoring (GoodLink™) for hub and downstream ports
- I^2C-bus interface to read vendor ID, product ID and configuration bits from external EEPROM

- Operation over the extended USB bus voltage range (4.0 to 5.5 V)
- Operating temperature range –40 to +85 °C
- 8 kV in-circuit ESD protection for lower cost of external components
- Full-scan design with high test coverage
- Available in 32-pin SDIP, SO and LQFP packages.

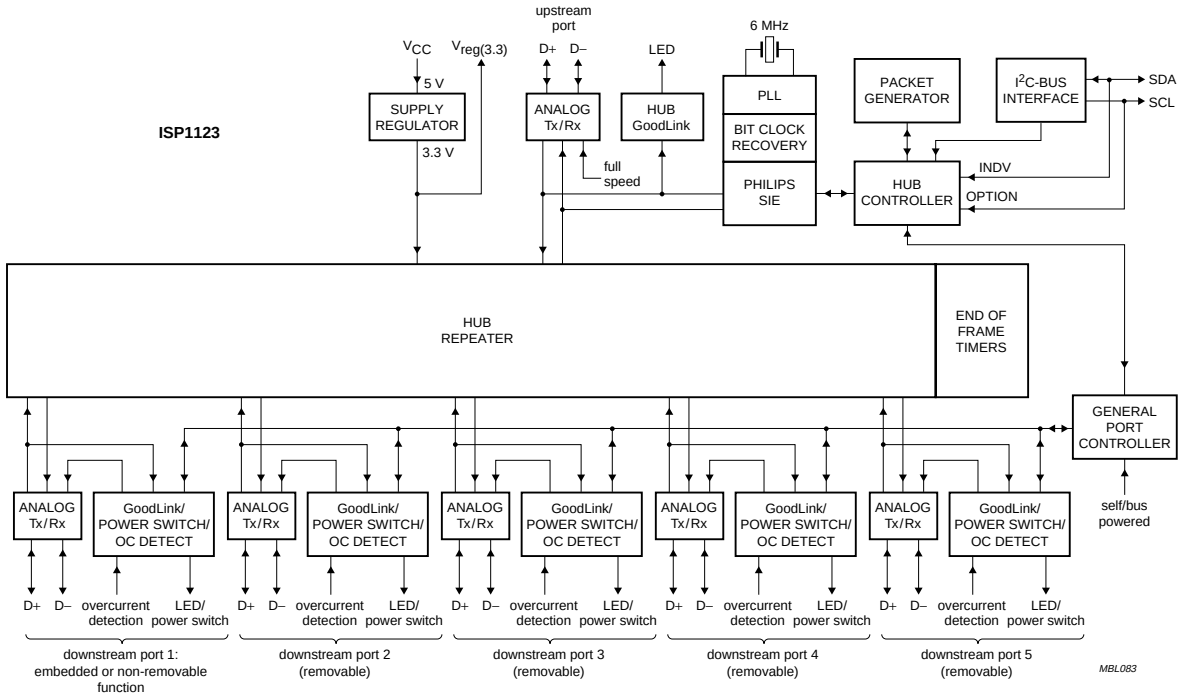
3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
ISP1123D	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1
ISP1123NB	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
ISP1123BD [1]	LQFP32	plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm	SOT358-1

[1] For the availability of the LQFP32 package please contact your local Philips Semiconductors sales office.

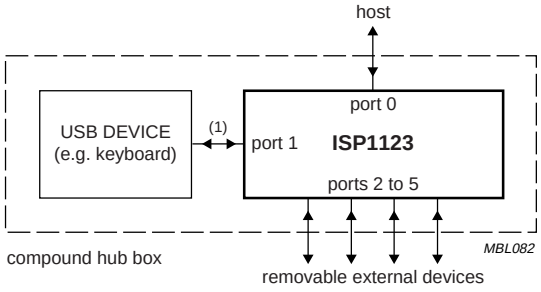
4. Block diagram



This is a conceptual block diagram and does not include each individual signal.

Fig 1. Block diagram of the ISP1123.

5. Functional diagram



(1) Downstream port 1 is non-removable.

Fig 2. A compound hub box using ISP1123.

6. Pinning information

6.1 ISP1123D (SO32) and ISP1123NB (SDIP32)

6.1.1 Pinning

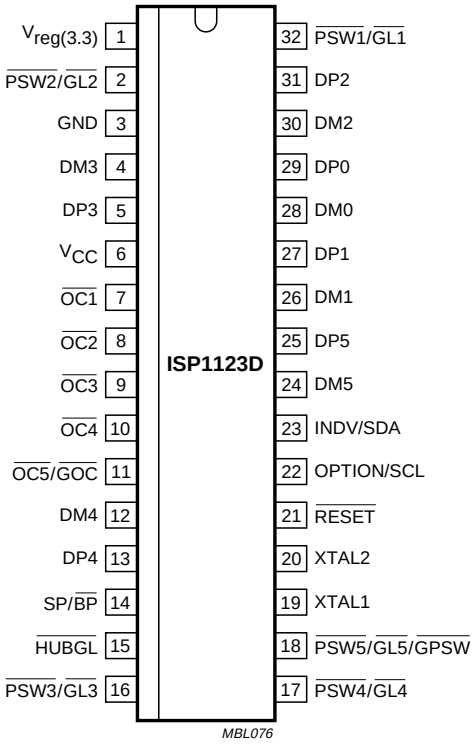


Fig 3. Pin configuration SO32.

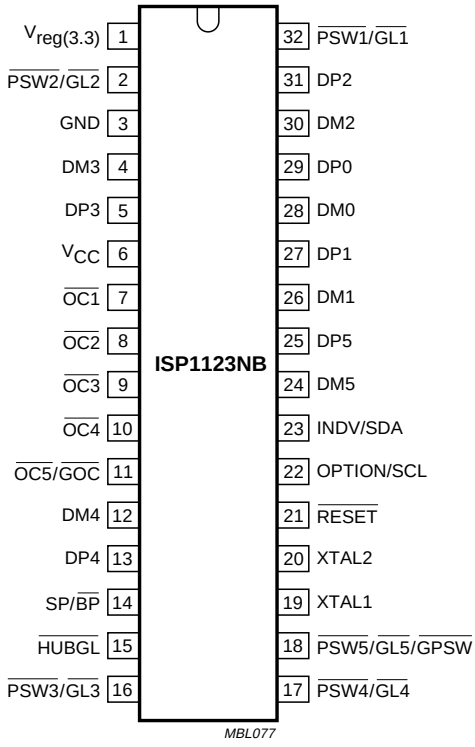


Fig 4. Pin configuration SDIP32.

6.1.2 Pin description

Table 2: Pin description for SO32 and SDIP32

Symbol [1]	Pin	Type	Description
$V_{reg(3.3)}$ [2]	1	-	regulated supply voltage (3.3 V ± 10%) from internal regulator; used to connect pull-up resistor on DP0 line
$\overline{PSW2}/\overline{GL2}$ [3]	2	O	**modes 4 to 6**: power switch control output for downstream port 2 (open-drain, 6 mA) **modes 0 to 3, 7**: GoodLink LED indicator output for downstream port 2 (open-drain, 6 mA); to connect an LED use a 330 Ω series resistor
GND	3	-	ground supply
DM3	4	AI/O	downstream port 3 D– connection (analog) [4]
DP3	5	AI/O	downstream port 3 D+ connection (analog) [4]
V_{CC}	6	-	supply voltage; connect to USB supply V_{BUS} (bus-powered or hybrid-powered) or to local supply V_{DD} (self-powered)
$\overline{OC1}$	7	AI/I	overcurrent sense input for downstream port 1 (analog [5])
$\overline{OC2}$	8	AI/I	overcurrent sense input for downstream port 2 (analog [5])
$\overline{OC3}$	9	AI/I	overcurrent sense input for downstream port 3 (analog [5])
$\overline{OC4}$	10	AI/I	overcurrent sense input for downstream port 4 (analog [5])
$\overline{OC5}/\overline{GOC}$ [3]	11	AI/I	**modes 5, 7**: overcurrent sense input for downstream port 5 (analog [5]) **modes 0, 1, 3**: global overcurrent sense input (analog [5])
DM4	12	AI/O	downstream port 4 D– connection (analog) [4]
DP4	13	AI/O	downstream port 4 D+ connection (analog) [4]
SP/$\overline{BP}$	14	I	selects power mode: **self-powered**: connect to V_{DD} (local power supply); also use this mode for hybrid-powered operation **bus-powered**: connect to GND; disable downstream port 5 to meet supply current requirements [4]
$\overline{HUBGL}$	15	O	hub GoodLink LED indicator output (open-drain, 6 mA); to connect an LED use a 330 Ω series resistor; if unused connect to V_{CC} via a 10 kΩ resistor
$\overline{PSW3}/\overline{GL3}$ [3]	16	O	**modes 4 to 6**: power switch control output for downstream port 3 (open-drain, 6 mA) **modes 0 to 3, 7**: GoodLink LED indicator output for downstream port 3 (open-drain, 6 mA); to connect an LED use a 330 Ω series resistor
$\overline{PSW4}/\overline{GL4}$ [3]	17	O	**modes 4 to 6**: power switch control output for downstream port 4 (open-drain, 6 mA) **modes 0 to 3, 7**: GoodLink LED indicator output for downstream port 4 (open-drain, 6 mA); to connect an LED use a 330 Ω series resistor

Table 2: Pin description for SO32 and SDIP32...*continued*

Symbol [1]	Pin	Type	Description
$\overline{PSW5}/\overline{GL5}/\overline{GPSW}$ [3]	18	O	**mode 5**: power switch control output for downstream port 5 (open-drain, 6 mA) **modes 3, 7**: GoodLink LED indicator output for downstream port 5 (open-drain, 6 mA); to connect an LED use a 330 Ω series resistor **modes 0 to 2**: gang mode power switch control output (open-drain, 6 mA)
XTAL1	19	I	crystal oscillator input (6 MHz)
XTAL2	20	O	crystal oscillator output (6 MHz)
$\overline{RESET}$ [2]	21	I	reset input (Schmitt trigger); a LOW level produces an asynchronous reset; connect to V_{CC} for power-on reset (internal POR circuit)
OPTION/SCL	22	I/O	mode selection input; also functions as I^2C-bus clock output (open-drain, 6 mA)
INDV/SDA	23	I/O	selects individual (HIGH) or global (LOW) power switching and overcurrent detection; also functions as bidirectional I^2C-bus data line (open-drain, 6 mA)
DM5	24	AI/O	downstream port 5 D– connection (analog) [4]
DP5	25	AI/O	downstream port 5 D+ connection (analog) [4]
DM1	26	AI/O	downstream port 1 D– connection (analog) [6]
DP1	27	AI/O	downstream port 1 D+ connection (analog) [6]
DM0	28	AI/O	upstream port D– connection (analog)
DP0	29	AI/O	upstream port D+ connection (analog)
DM2	30	AI/O	downstream port 2 D– connection (analog) [6]
DP2	31	AI/O	downstream port 2 D+ connection (analog) [6]
$\overline{PSW1}/\overline{GL1}$ [3]	32	O	**modes 4 to 6**: power switch control output for downstream port 1 (open-drain, 6 mA) **modes 0 to 3, 7**: GoodLink LED indicator output for downstream port 1 (open-drain, 6 mA); to connect an LED use a 330 Ω series resistor

[1] Symbol names with an overscore (e.g. $\overline{NAME}$) indicate active LOW signals.

[2] The voltage at pin $V_{reg(3.3)}$ is gated by the $\overline{RESET}$ pin. This allows fully self-powered operation by connecting $\overline{RESET}$ to V_{BUS} (+5 V USB supply). If V_{BUS} is lost upstream port D+ will not be driven.

[3] See Table 4 “Mode selection”.

[4] To disable a downstream port connect both D+ and D– to V_{CC} via a 1 MΩ resistor; unused ports must be disabled in reverse order starting from port 5.

[5] Analog detection circuit can be switched off using an external EEPROM, see Table 23; in this case, the pin functions as a logic input (TTL level).

[6] Downstream ports 1 and 2 cannot be disabled.

6.2 ISP1123BD (LQFP32)

6.2.1 Pinning

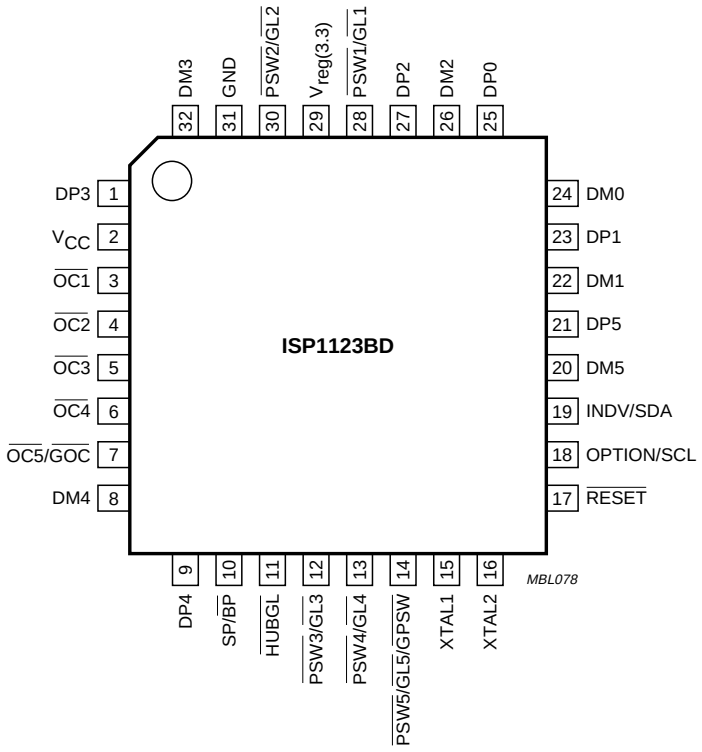


Fig 5. Pin configuration LQFP32.

6.2.2 Pin description

Table 3: Pin description for LQFP32

Symbol [1]	Pin	Type	Description
$V_{reg(3.3)}$ [2]	29	-	regulated supply voltage (3.3 V ± 10%) from internal regulator; used to connect pull-up resistor on DP0 line
$\overline{PSW2}/\overline{GL2}$ [3]	30	O	**modes 4 to 6**: power switch control output for downstream port 2 (open-drain, 6 mA) **modes 0 to 3, 7**: GoodLink LED indicator output for downstream port 2 (open-drain, 6 mA); to connect an LED use a 330 Ω series resistor
GND	31	-	ground supply
DM3	32	AI/O	downstream port 3 D– connection (analog) [4]
DP3	1	AI/O	downstream port 3 D+ connection (analog) [4]
V_{CC}	2	-	supply voltage; connect to USB supply V_{BUS} (bus-powered or hybrid-powered) or to local supply V_{DD} (self-powered)
$\overline{OC1}$	3	AI/I	overcurrent sense input for downstream port 1 (analog [5])
$\overline{OC2}$	4	AI/I	overcurrent sense input for downstream port 2 (analog [5])
$\overline{OC3}$	5	AI/I	overcurrent sense input for downstream port 3 (analog [5])
$\overline{OC4}$	6	AI/I	overcurrent sense input for downstream port 4 (analog [5])

Table 3: Pin description for LQFP32...*continued*

Symbol [1]	Pin	Type	Description
$\overline{OC5}/\overline{GOC}$ [3]	7	AI/I	**modes 5, 7**: overcurrent sense input for downstream port 5 (analog [5]) **modes 0, 1, 3**: global overcurrent sense input (analog [5])
DM4	8	AI/O	downstream port 4 D– connection (analog) [4]
DP4	9	AI/O	downstream port 4 D+ connection (analog) [4]
SP/$\overline{BP}$	10	I	selects power mode: **self-powered**: connect to V_{DD} (local power supply); also use this mode for hybrid-powered operation **bus-powered**: connect to GND; disable downstream port 5 to meet supply current requirements [4]
$\overline{HUBGL}$	11	O	hub GoodLink LED indicator output (open-drain, 6 mA); to connect an LED use a 330 Ω series resistor; if unused connect to V_{CC} via a 10 kΩ resistor
$\overline{PSW3}/\overline{GL3}$ [3]	12	O	**modes 4 to 6**: power switch control output for downstream port 3 (open-drain, 6 mA) **modes 0 to 3, 7**: GoodLink LED indicator output for downstream port 3 (open-drain, 6 mA); to connect an LED use a 330 Ω series resistor
$\overline{PSW4}/\overline{GL4}$ [3]	13	O	**modes 4 to 6**: power switch control output for downstream port 4 (open-drain, 6 mA) **modes 0 to 3, 7**: GoodLink LED indicator output for downstream port 4 (open-drain, 6 mA); to connect an LED use a 330 Ω series resistor
$\overline{PSW5}/\overline{GL5}/\overline{GPSW}$ [3]	14	O	**mode 5**: power switch control output for downstream port 5 (open-drain, 6 mA) **modes 3, 7**: GoodLink LED indicator output for downstream port 5 (open-drain, 6 mA); to connect an LED use a 330 Ω series resistor **modes 0 to 2**: gang mode power switch control output (open-drain, 6 mA)
XTAL1	15	I	crystal oscillator input (6 MHz)
XTAL2	16	O	crystal oscillator output (6 MHz)
$\overline{RESET}$ [2]	17	I	reset input (Schmitt trigger); a LOW level produces an asynchronous reset; connect to V_{CC} for power-on reset (internal POR circuit)
OPTION/SCL	18	I/O	mode selection input; also functions as I^2C-bus clock output (open-drain, 6 mA)
INDV/SDA	19	I/O	selects individual (HIGH) or global (LOW) power switching and overcurrent detection; also functions as bidirectional I^2C-bus data line (open-drain, 6 mA)
DM5	20	AI/O	downstream port 5 D– connection (analog) [4]
DP5	21	AI/O	downstream port 5 D+ connection (analog) [4]
DM1	22	AI/O	downstream port 1 D– connection (analog) [6]
DP1	23	AI/O	downstream port 1 D+ connection (analog) [6]
DM0	24	AI/O	upstream port D– connection (analog)
DP0	25	AI/O	upstream port D+ connection (analog)

Table 3: Pin description for LQFP32…*continued*

Symbol [1]	Pin	Type	Description
DM2	26	AI/O	downstream port 2 D– connection (analog) [6]
DP2	27	AI/O	downstream port 2 D+ connection (analog) [6]
$\overline{PSW1}/\overline{GL1}$ [3]	28	O	**modes 4 to 6**: power switch control output for downstream port 1 (open-drain, 6 mA) **modes 0 to 3, 7**: GoodLink LED indicator output for downstream port 1 (open-drain, 6 mA); to connect an LED use a 330 Ω series resistor

[1] Symbol names with an overscore (e.g. $\overline{NAME}$) indicate active LOW signals.

[2] The voltage at pin $V_{reg(3.3)}$ is gated by the $\overline{RESET}$ pin. This allows fully self-powered operation by connecting $\overline{RESET}$ to V_{BUS} (+5 V USB supply). If V_{BUS} is lost upstream port D+ will not be driven.

[3] See Table 4 “Mode selection”.

[4] To disable a downstream port connect both D+ and D– to V_{CC} via a 1 MΩ resistor; unused ports must be disabled in reverse order starting from port 5.

[5] Analog detection circuit can be switched off using an external EEPROM, see Table 23; in this case, the pin functions as a logic input (TTL level).

[6] Downstream ports 1 and 2 cannot be disabled.

7. Functional description

The ISP1123 is a compound USB hub with up to 5 downstream ports. The number of ports can be configured between 2 and 5. The downstream ports can be used to connect low-speed or full-speed USB peripherals. Downstream port 1 is dedicated to an embedded or non-removable function, the other ports are removable.

All standard USB requests from the host are handled by the hardware without the need for firmware intervention. The block diagram is shown in Figure 1 and the basic architecture of a compound hub in Figure 2.

The ISP1123 requires only a single supply voltage. An internal 3.3 V regulator provides the supply voltage for the analog USB data transceivers.

The ISP1123 supports both bus-powered and self-powered hub operation. When using bus-powered operation a downstream port cannot supply more than 100 mA to a peripheral. In case of self-powered operation an external supply is used to power the downstream ports, allowing a current consumption of max. 500 mA per port.

A basic I^2C-bus interface is provided for reading vendor ID, product ID and configuration bits from an external EEPROM upon a reset.

7.1 Analog transceivers

The integrated transceiver interfaces directly to the USB cables through external termination resistors. They are capable of transmitting and receiving serial data at both ‘full-speed’ (12 Mbit/s) and ‘low-speed’ (1.5 Mbit/s) data rates. The slew rates are adjusted according to the speed of the device connected and lie within the range mentioned in the *USB Specification Rev. 1.1*.

7.2 Philips Serial Interface Engine (SIE)

The Philips SIE implements the full USB protocol layer. It is completely hardwired for speed and needs no firmware intervention. The functions of this block include: synchronization pattern recognition, parallel/serial conversion, bit (de-)stuffing, CRC checking/generation, Packet IDentifier (PID) verification/generation, address recognition, handshake evaluation/generation.

7.3 Hub repeater

The hub repeater is responsible for managing connectivity on a ‘per packet’ basis. It implements ‘packet signalling’ and ‘resume’ connectivity. Low-speed devices can be connected to downstream ports. If a low-speed device is detected the repeater will not propagate upstream packets to the corresponding port, unless they are preceded by a PREAMBLE PID.

7.4 End-of-frame timers

This block contains the specified EOF1 and EOF2 timers which are used to detect ‘loss-of-activity’ and ‘babble’ error conditions in the hub repeater. The timers also maintain the low-speed keep-alive strobe which is sent at the beginning of a frame.

7.5 General and individual port controller

The general and individual port controllers together provide status and control of individual downstream ports. Any port status change will be reported to the host via the hub status change (interrupt) endpoint.

7.6 GoodLink

Indication of a good USB connection is provided through GoodLink technology. An LED can be directly connected via an external 330 Ω resistor.

During enumeration the LED blinks on momentarily. After successful configuration of the ISP1123, the LED is permanently on. The LED blinks off for 100 ms upon each successful packet transfer (with ACK). The hub GoodLink indicator blinks when the hub receives a packet addressed to it. Downstream GoodLink indicators blink upon an acknowledgment from the associated port. In ‘suspend’ mode the LED is off.

This feature provides a user-friendly indication of the status of the hub, the connected downstream devices and the USB traffic. It is a useful diagnostics tool to isolate faulty USB equipment and helps to reduce field support and hotline costs.

7.7 Bit clock recovery

The bit clock recovery circuit recovers the clock from the incoming USB data stream using a 4× oversampling principle. It is able to track jitter and frequency drift as specified by the *USB Specification Rev. 1.1*.

7.8 Voltage regulator

A 5 to 3.3 V DC-DC regulator is integrated on-chip to supply the analog transceiver and internal logic. This can also be used to supply the terminal 1.5 kΩ pull-up resistor on the D+ line of the upstream connection.

7.9 PLL clock multiplier

A 6 to 48 MHz clock multiplier Phase-Locked Loop (PLL) is integrated on-chip. This allows for the use of low-cost 6 MHz crystals. The low crystal frequency also minimizes Electro-Magnetic Interference (EMI). The PLL requires no external components.

7.10 Overcurrent detection

An overcurrent detection circuit for downstream ports has been integrated on-chip. It is self-reporting, resets automatically, has a low trip time and requires no external components. Both individual and ganged mode overcurrent detection are supported.

7.11 I^2C-bus interface

A basic serial I^2C-bus interface (single master, 100 kHz) is provided to read VID, PID and configuration bits from an external I^2C-bus EEPROM (e.g. Philips PCF8582 or equivalent). At reset the ISP1123 reads 6 bytes of data from the external memory.

The I^2C-bus interface timing complies with the standard mode of operation as described in *The I^2C-bus and how to use it*, order number 9398 393 40011.

8. Modes of operation

The ISP1123 has several modes of operation, each corresponding with a different pin configuration. Modes are selected by means of pins INDV, OPTION and SP/$\overline{BP}$, as shown in Table 4.

Table 4: Mode selection

Mode	INDV [1]	OPTION	SP/$\overline{BP}$ [2]	$\overline{PSWn}$/$\overline{GLn}$ (n = 1 to 4)	$\overline{PSW5}$/$\overline{GL5}$/GPSW	$\overline{OCn}$ (n = 1 to 4)	$\overline{OC5}$/$\overline{GOC}$
0	0	0	0	GoodLink	ganged power	inactive	global overcurrent
1	0	0	1	GoodLink	ganged power	inactive	global overcurrent
2	0	1	0	GoodLink	ganged power	inactive [3]	inactive [3]
3	0	1	1	GoodLink [4]	GoodLink [4]	inactive	global overcurrent
4	1	0	0	individual power	inactive	individual overcurrent	inactive
5	1	0	1	individual power	individual power	individual overcurrent	individual overcurrent
6	1	1	0	individual power	inactive	inactive [3]	inactive [3]
7	1	1	1	GoodLink [4]	GoodLink [4]	individual overcurrent	individual overcurrent

[1] Port power switching: logic 0 = ganged, logic 1 = individual.

[2] Power mode: logic 0 = bus-powered, logic 1 = self-powered (or hybrid-powered).

[3] No overcurrent detection.

[4] No power switching.

9. Endpoint descriptions

Each USB device is logically composed of several independent endpoints. An endpoint acts as a terminus of a communication flow between the host and the device. At design time each endpoint is assigned a unique number (endpoint identifier, see Table 5). The combination of the device address (given by the host during enumeration), the endpoint number and the transfer direction allows each endpoint to be uniquely referenced.

The ISP1123 has two endpoints, endpoint 0 (control) and endpoint 1 (interrupt).

Table 5: Hub endpoints

Function	Ports	Endpoint identifier	Transfer type	Direction [1]	Max. packet size (bytes)
Hub	0: upstream 1 to 5: downstream	0	control	OUT	64
				IN	64
		1	interrupt	IN	1

[1] IN: input for the USB host; OUT: output from the USB host.

9.1 Hub endpoint 0 (control)

All USB devices and functions must implement a default control endpoint (ID = 0). This endpoint is used by the host to configure the device and to perform generic USB status and control access.

The ISP1123 hub supports the following USB descriptor information through its control endpoint 0, which can handle transfers of 64 bytes maximum:

- Device descriptor
- Configuration descriptor
- Interface descriptor
- Endpoint descriptor
- Hub descriptor
- String descriptor.

9.2 Hub endpoint 1 (interrupt)

Endpoint 1 is used by the ISP1123 hub to provide status change information to the host. This endpoint can be accessed only after the hub has been configured by the host (by sending the Set Configuration command).

Endpoint 1 is an interrupt endpoint: the host polls it once every 255 ms by sending an IN token. If the hub has detected no change in the port status it returns a NAK (Not AcKnowledge) response to this request, otherwise it sends the Status Change byte (see Table 6).

Table 6: Status Change byte: bit allocation

Bit	Symbol	Description
0	Hub SC	a logic 1 indicates a status change on the hub's upstream port
1	Port 1 SC	a logic 1 indicates a status change on downstream port 1
2	Port 2 SC	a logic 1 indicates a status change on downstream port 2
3	Port 3 SC	a logic 1 indicates a status change on downstream port 3
4	Port 4 SC	a logic 1 indicates a status change on downstream port 4
5	Port 5 SC	a logic 1 indicates a status change on downstream port 5
6	reserved	not used
7	reserved	not used

10. Host requests

The ISP1123 handles all standard USB requests from the host via control endpoint 0. The control endpoint can handle a maximum of 64 bytes per transfer.

Remark: Please note that the USB data transmission order is Least Significant Bit (LSB) first. In the following tables multi-byte variables are displayed least significant byte first.

10.1 Standard requests

Table 7 shows the supported standard USB requests. Some requests are explicitly unsupported. All other requests will be responded with a STALL packet.

Table 7: Standard USB requests

Request name	bmRequestType byte 0 [7:0] (Bin)	bRequest byte 1 (Hex)	wValue byte 2, 3 (Hex)	wIndex byte 4, 5 (Hex)	wLength byte 6, 7 (Hex)	Data
Address						
Set Address	X000 0000	05	address [1]	00, 00	00, 00	none
Configuration						
Get Configuration	1000 0000	08	00, 00	00, 00	01, 00	configuration value = 01H
Set Configuration (0)	X000 0000	09	00, 00	00, 00	00, 00	none
Set Configuration (1)	X000 0000	09	01, 00	00, 00	00, 00	none
Descriptor						
Get Configuration Descriptor	1000 0000	06	00, 02	00, 00	length [2]	configuration, interface and endpoint descriptors
Get Device Descriptor	1000 0000	06	00, 01	00, 00	length [2]	device descriptor
Get String Descriptor (0)	1000 0000	06	03, 00	00, 00	length [2]	language ID string
Get String Descriptor (1)	1000 0000	06	03, 01	00, 00	length [2]	manufacturer string
Get String Descriptor (2)	1000 0000	06	03, 02	00, 00	length [2]	product string

Table 7: Standard USB requests...*continued*

Request name	bmRequestType byte 0 [7:0] (Bin)	bRequest byte 1 (Hex)	wValue byte 2, 3 (Hex)	wIndex byte 4, 5 (Hex)	wLength byte 6, 7 (Hex)	Data
Feature						
Clear Device Feature (REMOTE_WAKEUP)	X000 0000	01	01, 00	00, 00	00, 00	none
Clear Endpoint (1) Feature (HALT/STALL)	X000 0010	01	00, 00	81, 00	00, 00	none
Set Device Feature (REMOTE_WAKEUP)	X000 0000	03	01, 00	00, 00	00, 00	none
Set Endpoint (1) Feature (HALT/STALL)	X000 0010	03	00, 00	81, 00	00, 00	none
Status						
Get Device Status	1000 0000	00	00, 00	00, 00	02, 00	device status
Get Interface Status	1000 0001	00	00, 00	00, 00	02, 00	zero
Get Endpoint (0) Status	1000 0010	00	00, 00	00/80 [3], 00	02, 00	endpoint 0 status
Get Endpoint (1) Status	1000 0010	00	00, 00	81, 00	02, 00	endpoint 1 status
Unsupported						
Set Descriptor	0000 0000	07	XX, XX	XX, XX	XX, XX	descriptor; STALL
Get Interface	1000 0001	0A	00, 00	XX, XX	01, 00	STALL
Set Interface	X000 0001	0B	XX, XX	XX, XX	00, 00	STALL
Synch Frame	1000 0010	0C	00, 00	XX, XX	02, 00	STALL

[1] Device address: 0 to 127.

[2] Returned value in bytes.

[3] MSB specifies endpoint direction: 0 = OUT, 1 = IN. The ISP1123 accepts either value.

10.2 Hub specific requests

In Table 8 the supported hub specific requests are listed, as well as some unsupported requests. Table 9 provides the feature selectors for setting or clearing port features.

Table 8: Hub specific requests

Request name	bmRequestType byte 0 [7:0] (Bin)	bRequest byte 1 (Hex)	wValue byte 2, 3 (Hex)	wIndex byte 4, 5 (Hex)	wLength byte 6, 7 (Hex)	Data
Descriptor						
Get Hub Descriptor	1010 0000	06	00, 00/29 [1]	00, 00	length [2], 00	hub descriptor
Feature						
Clear Hub Feature (C_LOCAL_POWER)	X010 0000	01	00, 00	00, 00	00, 00	none
Clear Port Feature (feature selectors)	X010 0011	01	feature [3], 00	port [4], 00	00, 00	none
Set Port Feature (feature selectors)	X010 0011	03	feature [3], 00	port [4], 00	00, 00	none

Table 8: Hub specific requests *...continued*

Request name	bmRequestType byte 0 [7:0] (Bin)	bRequest byte 1 (Hex)	wValue byte 2, 3 (Hex)	wIndex byte 4, 5 (Hex)	wLength byte 6, 7 (Hex)	Data
Status						
Get Hub Status	1010 0000	00	00, 00	00, 00	04, 00	hub status and status change field
Get Port Status	1010 0011	00	00, 00	port [4], 00	04, 00	port status
Unsupported						
Get Bus Status	1010 0011	02	00, 00	port [4], 00	01, 00	STALL
Clear Hub Feature (C_OVER_CURRENT)	X010 0000	01	01, 00	00, 00	00, 00	STALL
Set Hub Descriptor	0010 0000	07	XX, XX	00, 00	3E, 00	STALL
Set Hub Feature (C_LOCAL_POWER)	X010 0000	03	00, 00	00, 00	00, 00	STALL
Set Hub Feature (C_OVER_CURRENT)	X010 0000	03	01, 00	00, 00	00, 00	STALL

[1] *USB Specification Rev. 1.0* uses 00H, *USB Specification Rev. 1.1* specifies 29H.

[2] Returned value in bytes.

[3] Feature selector value, see Table 9.

[4] Downstream port identifier: 1 to N with N = number of enabled ports (2 to 5).

Table 9: Port feature selectors

Feature selector name	Value (Hex)	Set feature	Clear feature
PORT_CONNECTION	00	not used	not used
PORT_ENABLE	01	not used	disables a port
PORT_SUSPEND	02	suspends a port	resumes a port
PORT_OVERCURRENT	03	not used	not used
PORT_RESET	04	resets and enables a port	not used
PORT_POWER	08	powers on a port	powers off a port
PORT_LOW_SPEED	09	not used	not used
C_PORT_CONNECTION	10	not used	clears port connection change bit
C_PORT_ENABLE	11	not used	clears port enable change bit
C_PORT_SUSPEND	12	not used	clears port suspend change bit
C_PORT_OVERCURRENT	13	not used	clears port overcurrent change bit
C_PORT_RESET	14	not used	clears port reset change bit

10.3 Descriptors

The ISP1123 hub controller supports the following standard USB descriptors:

- Device
- Configuration
- Interface
- Endpoint
- Hub
- String.

Table 10: Device descriptor

Values in square brackets are optional.

Offset (bytes)	Field name	Size (bytes)	Value (Hex)	Comments
0	bLength	1	12	descriptor length = 18 bytes
1	bDescriptorType	1	01	type = DEVICE
2	bcdUSB	2	10, 01	*USB Specification Rev. 1.1*
4	bDeviceClass	1	09	HUB_CLASSCODE
5	bDeviceSubClass	1	00	-
6	bDeviceProtocol	1	00	-
7	bMaxPacketSize0	1	40	packet size = 64 bytes
8	idVendor	2	CC, 04	Philips Semiconductors vendor ID (04CC); can be customized using an external EEPROM (see Table 23)
10	idProduct	2	23, 11	ISP1123 product ID; can be customized using an external EEPROM (see Table 23)
12	bcdDevice	2	00, 01	device release 1.0; silicon revision increments this value
14	iManufacturer	1	00	no manufacturer string (default)
			[01]	manufacturer string enabled (using an external EEPROM)
15	iProduct	1	00	no product string (default)
			[02]	product string enabled (using an external EEPROM)
16	iSerialNumber	1	00	no serial number string
17	bNumConfigurations	1	01	one configuration

Table 11: Configuration descriptor

Values in square brackets are optional.

Offset (bytes)	Field name	Size (bytes)	Value (Hex)	Comments
0	bLength	1	09	descriptor length = 9 bytes
1	bDescriptorType	1	02	type = CONFIGURATION
2	wTotalLength	2	19, 00	total length of configuration, interface and endpoint descriptors (25 bytes)
4	bNumInterfaces	1	01	one interface
5	bConfigurationValue	1	01	configuration value = 1
6	iConfiguration	1	00	no configuration string
7	bmAttributes	1	E0	self-powered with remote wake-up [1]
			A0	bus-powered with remote wake-up [1]
8	MaxPower [2]	1	32	100 mA (default)
			[00]	0 mA (using an external EEPROM)
			[FA]	500 mA (using an external EEPROM)

[1] Selected by input SP/$\overline{BP}$.

[2] Value in units of 2 mA.

Table 12: Interface descriptor

Offset (bytes)	Field name	Size (bytes)	Value (Hex)	Comments
0	bLength	1	09	descriptor length = 9 bytes
1	bDescriptorType	1	04	type = INTERFACE
2	bInterfaceNumber	1	00	-
3	bAlternateSetting	1	01	no alternate setting
4	bNumEndpoints	1	01	status change (interrupt) endpoint
5	bInterfaceClass	1	09	HUB_CLASSCODE
6	bInterfaceSubClass	1	00	-
7	bInterfaceProtocol	1	00	no class-specific protocol
8	bInterface	1	00	no interface string

Table 13: Endpoint descriptor

Offset (bytes)	Field name	Size (bytes)	Value (Hex)	Comments
0	bLength	1	07	descriptor length = 7 bytes
1	bDescriptorType	1	05	type = ENDPOINT
2	bEndpointAddress	1	81	endpoint 1, direction: IN
3	bmAttributes	1	03	interrupt endpoint
4	wMaxPacketSize	2	01, 00	packet size = 1 byte
6	bInterval	1	FF	polling interval (255 ms)

Table 14: Hub descriptor

Values in square brackets are optional.

Offset (bytes)	Field name	Size (bytes)	Value (Hex)	Comments
0	bDescLength	1	09	descriptor length = 9 bytes
1	bDescriptorType	1	29	type = HUB
2	bNbrPorts	1	05 to 02	number of enabled downstream ports; selectable by DP/DM strapping
3	wHubCharacteristics	2	0D, 00	individual power switching [1], overcurrent protection active (modes 0, 1, 3, 4, 5, 7), hub is part of a compound device
			15, 00	individual power switching [1], no overcurrent protection (modes 2, 6) [2], hub is part of a compound device
5	bPwrOn2PwrGood [3]	1	32	100 ms (default; modes 0, 1, 2, 4, 5, 6)
			00	0 ms (default; modes 3, 7)
			[FA]	500 ms (using an external EEPROM; modes 0, 1, 2, 4, 5, 6); see Table 23
6	bHubContrCurrent	1	64	maximum hub controller current (100 mA)
7	DeviceRemovable	1	02	port 1 is non-removable
8	PortPwrCtrlMask	1	FF	must be all ones for compatibility with *USB Specification Rev. 1.0*

[1] ISP1123 always reports power management status on an individual basis, even for ganged/global modes. This is compliant with *USB Specification Rev. 1.1*.

[2] Condition with no overcurrent detection is reported to the host.

[3] Value in units of 2 ms.

Table 15: String descriptors

String descriptors are optional and therefore disabled by default; they can be enabled through an external EEPROM.

Offset (bytes)	Field name	Size (bytes)	Value (Hex)	Comments
String descriptor (0): language ID string				
0	bLength	1	04	descriptor length = 4 bytes
1	bDescriptorType	1	03	type = STRING
2	bString	2	09, 04	LANGID code zero
String descriptor (1): manufacturer string				
0	bLength	1	2E	descriptor length = 46 bytes
1	bDescriptorType	1	03	type = STRING
2	bString	44	UC [1]	“Philips Semiconductors”

Table 15: String descriptors *...continued*

String descriptors are optional and therefore disabled by default; they can be enabled through an external EEPROM.

Offset (bytes)	Field name	Size (bytes)	Value (Hex)	Comments
String descriptor (2): product string				
0	bLength	1	10	descriptor length = 16 bytes
1	bDescriptorType	1	03	type = STRING
2	bString	14	UC [1]	“ISP1122”

[1] Unicode encoded string.

10.4 Hub responses

This section describes the hub responses to requests from the USB host.

10.4.1 Get device status

The hub returns 2 bytes, see Table 16.

Table 16: Get device status response

Bit #	Function	Value	Description
0	self-powered	0	bus-powered
		1	self-powered
1	remote wake-up	0	no remote wake-up
		1	remote wake-up enabled
2 to 15	reserved	0	-

10.4.2 Get configuration

The hub returns 1 byte, see Table 17.

Table 17: Get configuration response

Bit #	Function	Value	Description
0	configuration value	0	device not configured
		1	device configured
1 to 7	reserved	0	-

10.4.3 Get interface status

The hub returns 2 bytes, see Table 18.

Table 18: Get interface status response

Bit #	Function	Value	Description
0 to 15	reserved	0	-

10.4.4 Get hub status

The hub returns 4 bytes, see Table 19.

Table 19: Get hub status response

Bit #	Function	Value	Description
0	local power source	0	local power supply good
		1	local power supply lost
1	overcurrent indicator	0	no overcurrent condition
		1	hub overcurrent condition detected
2 to 15	reserved	0	-
16	local power status change	0	no change in local power status
		1	local power status changed
17	overcurrent indicator change	0	no change in overcurrent condition
		1	overcurrent condition changed
18 to 31	reserved	0	-

10.4.5 Get port status

The hub returns 4 bytes. The first 2 bytes contain the port status bits (wPortStatus, see Table 20). The last 2 bytes hold the port status change bits (wPortChange, see Table 21).

Table 20: Get port status response (wPortStatus)

Bit #	Function	Value	Description
0	current connect status	0	no device present
		1	device present on this port
1	port enabled/disabled	0	port disabled
		1	port enabled
2	suspend	0	port not suspended
		1	port suspended
3	overcurrent indicator	0	no overcurrent condition
		1	overcurrent condition detected
4	reset	0	reset not asserted
		1	reset asserted
5 to 7	reserved	0	-
8	port power	0	port powered off
		1	port power on
9	low-speed device attached	0	full-speed device attached
		1	low-speed device attached
10 to 15	reserved	0	-

Table 21: Get port status response (wPortChange)

Bit #	Function	Value	Description
0	connect status change	0	no change in current connect status
		1	current connect status changed
1	port enabled/disabled change	0	no port error
		1	port disabled by a port error
2	suspend change	0	no change in suspend status
		1	resume complete
3	overcurrent indicator change	0	no change in overcurrent status
		1	overcurrent indicator changed
4	reset change	0	no change in reset status
		1	reset complete
5 to 15	reserved	0	-

10.4.6 Get configuration descriptor

The hub returns 25 bytes containing the configuration descriptor (9 bytes, see Table 11), the interface descriptor (9 bytes, see Table 12) and the endpoint descriptor (7 bytes, see Table 13).

10.4.7 Get device descriptor

The hub returns 18 bytes containing the device descriptor, see Table 10.

10.4.8 Get hub descriptor

The hub returns 9 bytes containing the hub descriptor, see Table 14.

10.4.9 Get string descriptor (0)

The hub returns 4 bytes containing the language ID, see Table 15.

10.4.10 Get string descriptor (1)

The hub returns 46 bytes containing the manufacturer name, see Table 15.

10.4.11 Get string descriptor (2)

The hub returns 16 bytes containing the product name, see Table 15.

11. I²C-bus interface

A simple I²C-bus interface is provided in the ISP1123 to read customized vendor ID, product ID and some other configuration bits from an external EEPROM. The interface supports single master operation at a nominal bus speed of 93.75 kHz.

The I²C-bus interface is intended for bidirectional communication between ICs via two serial bus wires, SDA (data) and SCL (clock). Both lines are driven by open-drain circuits and must be connected to the positive supply voltage via pull-up resistors.

11.1 Protocol

The I²C-bus protocol defines the following conditions:

- **Bus free**: both SDA and SCL are HIGH
- **START**: a HIGH-to-LOW transition on SDA, while SCL is HIGH
- **STOP**: a LOW-to-HIGH transition on SDA, while SCL is HIGH
- **Data valid**: after a START condition, data on SDA are stable during the HIGH period of SCL; data on SDA may only change while SCL is LOW.

Each device on the I²C-bus has a unique slave address, which the master uses to select a device for access.

The master starts a data transfer using a START condition and ends it by generating a STOP condition. Transfers can only be initiated when the bus is free. The receiver must acknowledge each byte by means of a LOW level on SDA during the ninth clock pulse on SCL.

For detailed information please consult *The I²C-bus and how to use it.*, order number 9398 393 40011.

11.2 Hardware connections

Via the I²C-bus interface the ISP1123 can be connected to an external EEPROM (PCF8582 or equivalent). The hardware connections are shown in Figure 6.

The SCL and SDA pins are multiplexed with pins OPTION and INDV respectively.

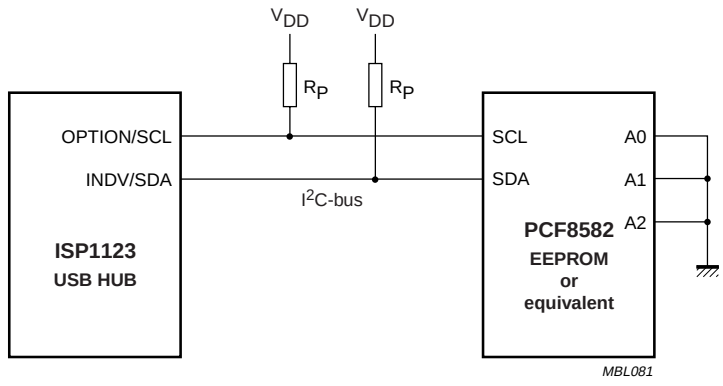


Fig 6. EEPROM connection diagram.

The slave address which ISP1123 uses to access the EEPROM is 1010000B. Page mode addressing is not supported, so pins A0, A1 and A2 of the EEPROM must be connected to GND (logic 0).

11.3 Data transfer

When the ISP1123 is reset, the I^2C-bus interface tries to read 6 bytes of configuration data from an external EEPROM. If no response is detected, the levels on inputs SDA and SCL are interpreted as INDV and OPTION to select the operating mode (see Table 4).

The data in the EEPROM memory are organized as shown in Table 22.

Table 22: EEPROM organization

Address (Hex)	Default value (Hex)	Contents
00	CC	idVendor [1] (lower byte)
01	04	idVendor [1] (upper byte)
02	23	idProduct [2] (lower byte)
03	11	idProduct [2] (upper byte)
04	-	configuration bits C7 to C0; see Table 23
05	AA	signature

[1] Vendor ID code in the Device descriptor, see Table 10.

[2] Product ID code in the Device descriptor, see Table 10.

Table 23: Configuration bits

Bit	Function	Value (Bin)	Description
C0	OPTION	see Table 4 “Mode selection”	
C1	INDV	see Table 4 “Mode selection”	
C2	reserved	0 [1]	must always be programmed to logic 0
C3	PwrOn2PwrGood [2]	0 [1]	100 ms (bPwrOn2PwrGood = 32H)
		1	500 ms (bPwrOn2PwrGood = FAH)
C4	string descriptor enable	0 [1]	string descriptors disabled
		1	string descriptors enabled (strings: “Philips Semiconductors”, “ISP1122”)
C5	internal analog overcurrent detection enable	0	internal analog overcurrent detection circuit disabled; overcurrent pins $\overline{OCn}$ function as digital inputs (TTL level)
		1 [1]	internal analog overcurrent detection circuit enabled
C7, C6	MaxPower [3]	00 [1]	100 mA (MaxPower = 32H)
		01	500 mA (MaxPower = FAH)
		1X	0 mA (MaxPower = 00H)

[1] Default value at reset if no external EEPROM is present.

[2] Modifies the Hub Descriptor field ‘bPwrOn2PwrGood’, see Table 14.

[3] Modifies the Hub Descriptor field ‘MaxPower’, see Table 14.

12. Hub power modes

USB hubs can either be self-powered or bus-powered.

Self-powered — Self-powered hubs have a 5 V local power supply on board which provide power to the hub and the downstream ports. The *USB Specification Rev. 1.1* requires that these hubs limit the current to 500 mA per downstream port and report overcurrent conditions to the host. The hub may optionally draw 100 mA from the USB supply (V_{BUS}) to power the interface functions (**hybrid-powered**).

Bus-powered — Bus-powered hubs obtain all power from the host or an upstream self-powered hub. The maximum current is 100 mA per downstream port. Current limiting and reporting of overcurrent conditions are both optional.

Power switching of downstream ports can be done **individually** or **ganged**, where all ports are switched simultaneously with one power switch. The ISP1123 supports both modes, which can be selected using input INDV (see Table 4).

12.1 Voltage drop requirements

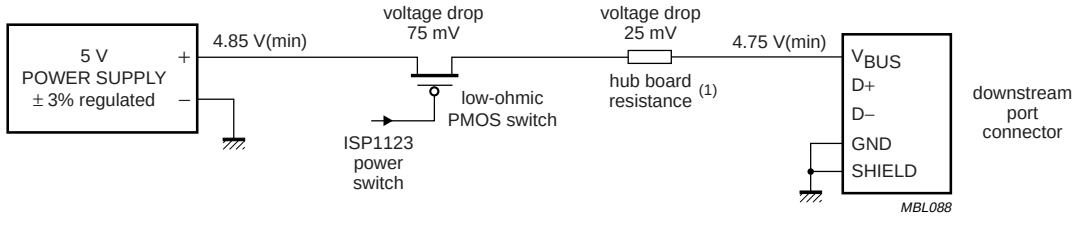
12.1.1 Self-powered hubs

Self-powered hubs are required to provide a minimum of 4.75 V to its output port connectors at all legal load conditions. To comply with Underwriters Laboratory Inc. (UL) safety requirements, the power from any port must be limited to 25 W (5 A at 5 V). Overcurrent protection may be implemented on a global or individual basis.

Assuming a 5 V ± 3% power supply the worst case supply voltage is 4.85 V. This only allows a voltage drop of 100 mV across the hub printed-circuit board (PCB) to each downstream connector. This includes a voltage drop across:

- Power supply connector
- Hub PCB (power and ground traces, ferrite beads)
- Power switch (FET on-resistance)
- Overcurrent sense device.

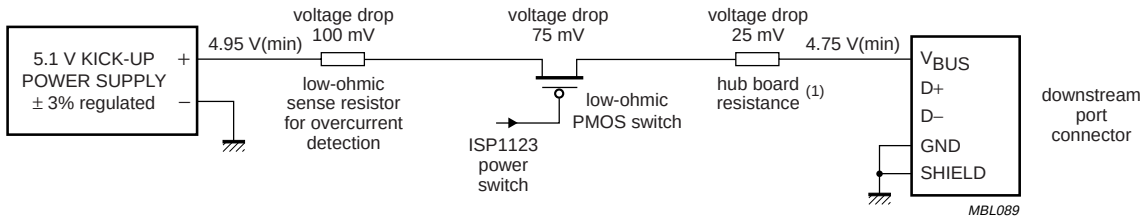
PCB resistance and power supply connector resistance may cause a drop of 25 mV, leaving only 75 mV as the voltage drop allowed across the power switch and overcurrent sense device. The individual voltage drop components are shown in Figure 7.



(1) Includes PCB traces, ferrite beads, etc.

Fig 7. Typical voltage drop components in self-powered mode using individual overcurrent detection.

In case of global overcurrent detection an increased voltage drop is needed for the overcurrent sense device (in this case a low-ohmic resistor). This can be realized by using a special power supply of 5.1 V ± 3%, as shown in Figure 8.



(1) Includes PCB traces, ferrite beads, etc.

Fig 8. Typical voltage drop components in self-powered mode using global overcurrent detection.

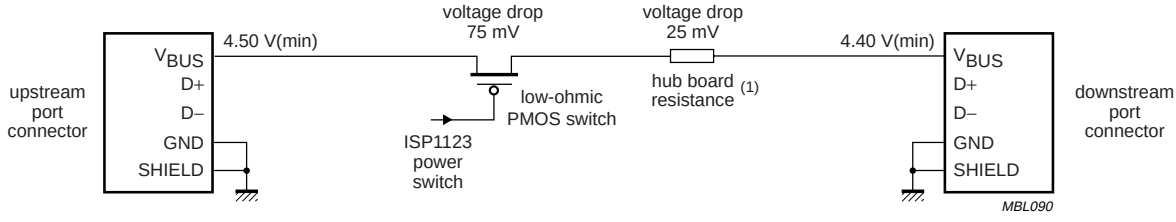
12.1.2 Bus-powered hubs

Bus-powered hubs are guaranteed to receive a supply voltage of 4.5 V at the upstream port connector and must provide a minimum of 4.4 V to the downstream port connectors. The voltage drop of 100 mV across bus-powered hubs includes:

- Hub PCB (power and ground traces, ferrite beads)
- Power switch (FET on-resistance)
- Overcurrent sense device.

The PCB resistance may cause a drop of 25 mV, which leaves 75 mV for the power switch and overcurrent sense device. The voltage drop components are shown in Figure 9.

For bus-powered hubs overcurrent protection is optional. It may be implemented for all downstream ports on a global or individual basis.



(1) Includes PCB traces, ferrite beads, etc.

Fig 9. Typical voltage drop components in bus-powered mode (no overcurrent detection).

13. Overcurrent detection

The ISP1123 has an analog overcurrent detection circuit for monitoring downstream port lines. This circuit automatically reports an overcurrent condition to the host and turns off the power to the faulty port. The host must reset the condition flag.

Pins $\overline{OC1}$ to $\overline{OC5}/\overline{GOC}$ are used for individual port overcurrent detection. Pin $\overline{OC5}/\overline{GOC}$ can also be used for global overcurrent detection. This is controlled by input INDV (see Table 4).

The overcurrent detection circuit can be switched off using an external EEPROM (see Table 23). In this case, the overcurrent pins $\overline{OCn}$ function as logic inputs (TTL level).

13.1 Overcurrent circuit description

The integrated overcurrent detection circuit of ISP1123 senses the voltage drop across the power switch or an extra low-ohmic sense resistor. When the port draws too much current, the voltage drop across the power switch exceeds the trip voltage threshold (ΔV_{trip}). The overcurrent circuit detects this and switches off the power switch control signal after a delay of 15 ms (t_{trip}). This delay acts as a 'debounce' period to minimize false tripping, especially during the inrush current produced by 'hot plugging' of a USB device.

13.2 Power switch selection

From the voltage drop analysis given in Figure 7, Figure 8 and Figure 9, the power switch has a voltage drop budget of 75 mV. For individual self-powered mode, the current drawn per port can be up to 500 mA. Thus the power switch should have maximum on-resistance of 150 mΩ.

If the voltage drop due to the hub board resistance can be minimized, the power switch can have more voltage drop budget and therefore a higher on-resistance. Power switches with a typical on-resistance of around 100 mΩ fit into this application.

The ISP1123 overcurrent detection circuit has been designed with a nominal trip voltage (ΔV_{trip}) of 85 mV. This gives a typical trip current of approximately 850 mA for a power switch with an on-resistance of 100 mΩ[1].

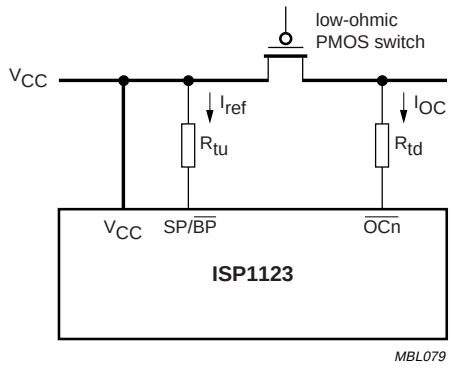
13.3 Tuning the overcurrent trip voltage

The ISP1123 trip voltage can optionally be adjusted through external components to set the desired trip current. This is done by inserting tuning resistors at pins SP/$\overline{BP}$ or $\overline{OCn}$ (see Figure 10). R_{tu} tunes up the trip voltage ΔV_{trip} and R_{td} tunes it down according to Equation 1.

$$\Delta V_{trip} = \Delta V_{trip(intrinsic)} + I_{ref} \cdot R_{tu} - I_{OC} \cdot R_{td} \quad (1)$$

with $I_{ref(nom)}$ = 5 µA and $I_{OC(nom)}$ = 0.5 µA.

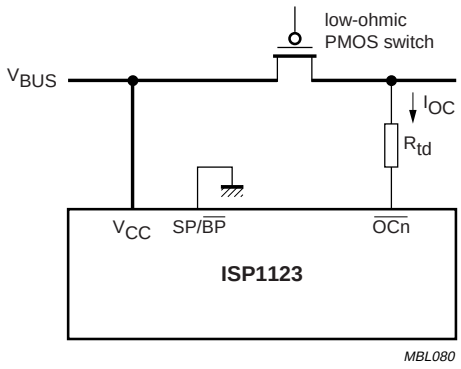
1. The following PMOS power switches have been tested to work well with the ISP1123: Philips PHP109, Vishay Siliconix Si2301DS, Fairchild FDN338P.



$I_{ref(nom)}$ = 5 μA

$I_{OC(nom)}$ = 0.5 μA

a. Self-powered mode.



$I_{OC(nom)}$ = 0.5 μA

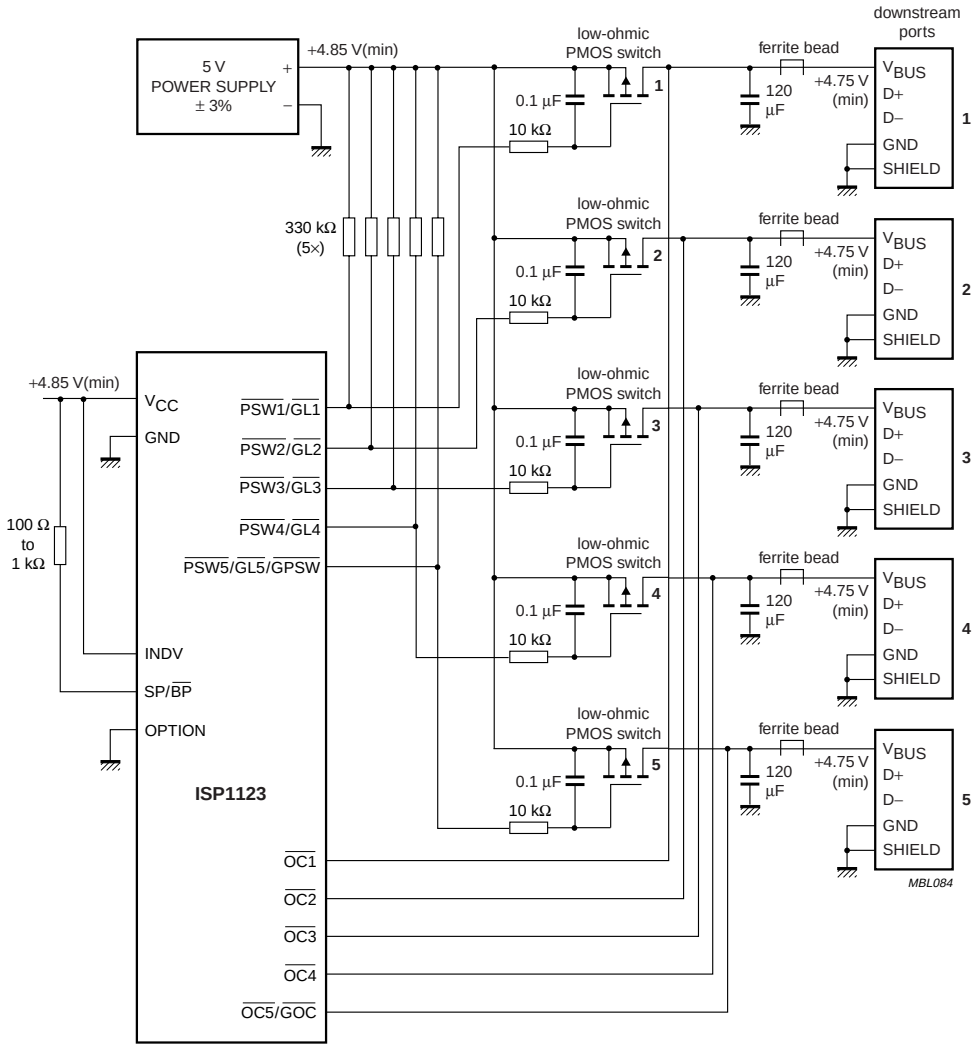
b. Bus-powered mode.

Fig 10. Tuning the overcurrent trip voltage.

13.4 Reference circuits

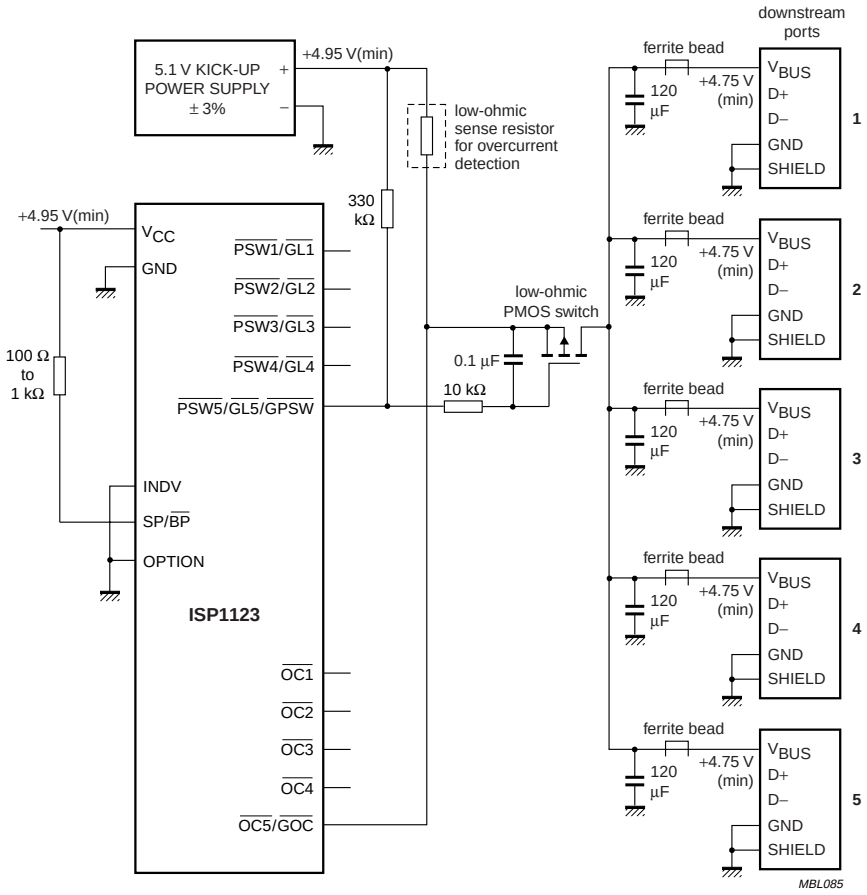
Some typical examples of port power switching and overcurrent detection modes are given in Figure 11 to Figure 14.

The RC circuit (10 kΩ and 0.1 μF) around the PMOS switch provides for soft turn-on. The series resistor connecting the SP/$\overline{BP}$ pin to V_{CC} tunes up the overcurrent trip voltage slightly (see Figure 10). In the schematic diagram the resistor separates the net names for pins V_{CC} and SP/$\overline{BP}$. This allows an automatic router to use a wide trace for V_{CC} and a narrow trace to connect pin SP/$\overline{BP}$.



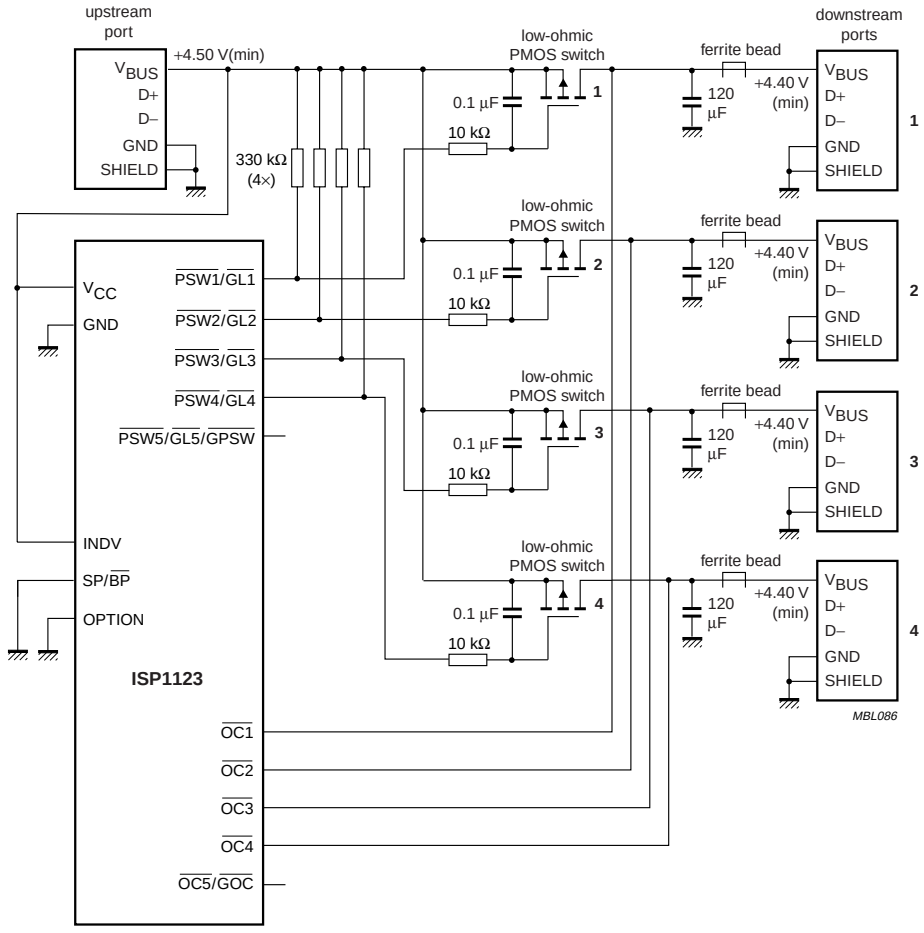
Power switches 1 to 5 are low-ohmic PMOS devices as specified in Section 13.2.

Fig 11. Mode 5: self-powered hub; individual port power switching; individual overcurrent detection.



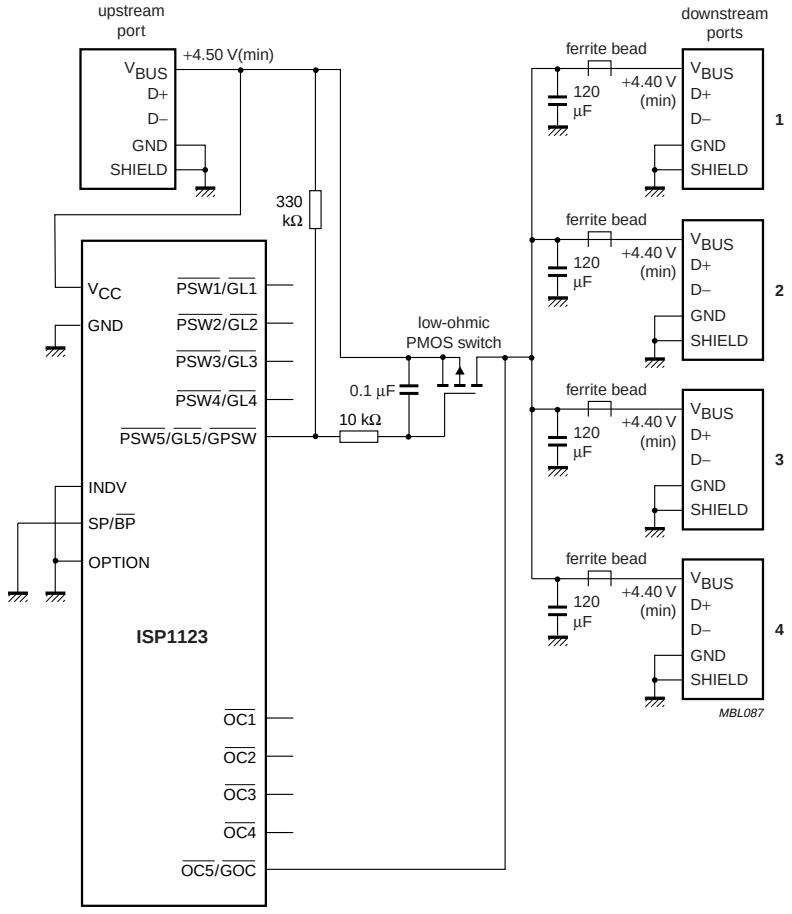
Power switch is low-ohmic PMOS device as specified in Section 13.2.

Fig 12. Mode 1: self-powered hub; ganged port power switching; global overcurrent detection.



Power switches 1 to 4 are low-ohmic PMOS devices as specified in Section 13.2.

Fig 13. Mode 4: bus-powered hub; individual port power switching; individual overcurrent detection.



Power switch is low-ohmic PMOS device as specified in Section 13.2.

Fig 14. Mode 0: bus-powered hub; ganged port power switching; global overcurrent detection.

14. Limiting values

Table 24: Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+6.0	V
V_I	input voltage		–0.5	V_{CC} + 0.5	V
$I_{latchup}$	latchup current	$V_I < 0$ or $V_I > V_{CC}$	-	200	mA
V_{esd}	electrostatic discharge voltage	$I_{LI} < 15$ µA [1] [2]	-	±4000 [3]	V
T_{stg}	storage temperature		–60	+150	°C
P_{tot}	total power dissipation		-	95	mW

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor (Human Body Model).

[2] Values are given for device only; in-circuit $V_{esd(max)}$ = ±8000 V.

[3] For open-drain pins $V_{esd(max)}$ = ±2000 V.

Table 25: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.0	5.5	V
V_I	input voltage		0	5.5	V
$V_{I(AI/O)}$	input voltage on analog I/O pins (D+/D–)		0	3.6	V
$V_{O(od)}$	open-drain output pull-up voltage		0	5.5	V
T_{amb}	operating ambient temperature		–40	+85	°C

15. Static characteristics

Table 26: Static characteristics; supply pins

V_{CC} = 4.0 to 5.5 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{reg(3.3)}$	regulated supply voltage		3.0 [1]	3.3	3.6	V
I_{CC}	operating supply current		-	18	-	mA
$I_{CC(susp)}$	suspend supply current	1.5 kΩ pull-up on upstream port D+ (pin DP0)	-	-	270	µA
		no pull-up on upstream port D+ (pin DP0)	-	-	80	µA

[1] In ‘suspend’ mode the minimum voltage is 2.7 V.

Table 27: Static characteristics: digital pins

V_{CC} = 4.0 to 5.5 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
Schmitt trigger inputs						
$V_{th(LH)}$	positive-going threshold voltage		1.4	-	1.9	V
$V_{th(HL)}$	negative-going threshold voltage		0.9	-	1.5	V
V_{hys}	hysteresis voltage		0.4	-	0.7	V
Output levels						
V_{OL}	LOW-level output voltage (open drain outputs)	I_{OL} = 6 mA	-	-	0.4	V
		I_{OL} = 20 µA	-	-	0.1	V
Leakage current						
I_{LI}	input leakage current		-	-	±1	µA
Open-drain outputs						
I_{OZ}	OFF-state output current		-	-	±1	µA

Table 28: Static characteristics: overcurrent sense pins

V_{CC} = 4.0 to 5.5 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔV_{trip}	overcurrent detection trip voltage on $\overline{OCn}$ pins	$\Delta V = V_{CC} - V_{\overline{OCn}}$	[1]	65	85	105	mV
		$\Delta V = V_{SP/\overline{BP}} - V_{\overline{OCn}}$	[2]				

[1] Bus-powered mode.

[2] Self-powered or hybrid-powered mode.

Table 29: Static characteristics: analog I/O pins (D+, D–) [1]

V_{CC} = 4.0 to 5.5 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{DI}	differential input sensitivity	$\|V_{I(D+)} - V_{I(D-)}\|$	0.2	-	-	V
V_{CM}	differential common mode voltage	includes V_{DI} range	0.8	-	2.5	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	R_L = 1.5 kΩ to +3.6V	-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L = 15 kΩ to GND	2.8	-	3.6	V
Leakage current						
I_{LZ}	OFF-state leakage current		-	-	±10	µA
Capacitance						
C_{IN}	transceiver capacitance	pin to GND	-	-	20	pF
Resistance						
Z_{DRV} [2]	driver output impedance	steady-state drive	28	-	44	Ω
Z_{INP}	input impedance		10	-	-	MΩ
Termination						
V_{TERM} [3]	termination voltage for upstream port pull-up (R_{PU})		3.0 [4]	-	3.6	V

[1] D+ is the USB positive data pin (DPn); D– is the USB negative data pin (DMn).

[2] Includes external resistors of 20 Ω ±1% on both D+ and D–.

[3] This voltage is available at pin $V_{reg(3.3)}$.

[4] In 'suspend' mode the minimum voltage is 2.7 V.

16. Dynamic characteristics

Table 30: Dynamic characteristics

V_{CC} = 4.0 to 5.5 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reset						
$t_{W(\overline{RESET})}$	pulse width on input $\overline{RESET}$	crystal oscillator running	10	-	-	µs
		crystal oscillator stopped	-	2 [1]	-	ms
Crystal oscillator						
f_{XTAL}	crystal frequency		-	6	-	MHz

[1] Dependent on the crystal oscillator start-up time.

Table 31: Dynamic characteristics: overcurrent sense pins

V_{CC} = 4.0 to 5.5 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{trip}	overcurrent trip response time from $\overline{OCn}$ LOW to $\overline{PSWn}$ HIGH	see Figure 15	[1]	-	-	15	ms

[1] Operating modes 0, 1, 4 and 5; see Table 4.

Table 32: Dynamic characteristics: analog I/O pins (D+, D−); full-speed mode [1]

V_{CC} = 4.0 to 5.5 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; C_L = 50 pF; R_{PU} = 1.5 kΩ on D+ to V_{TERM}.; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics							
t_{FR}	rise time	C_L = 50 pF; 10 to 90% of $\lvert V_{OH} - V_{OL}\rvert$		4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 10 to 90% of $\lvert V_{OH} - V_{OL}\rvert$		4	-	20	ns
FRFM	differential rise/fall time matching (t_{FR}/t_{FF})		[2]	90	-	111.11	%
V_{CRS}	output signal crossover voltage		[2] [3]	1.3	-	2.0	V
Data source timing							
t_{DJ1}	source differential jitter for consecutive transitions	see Figure 16	[2] [3]	−3.5	-	+3.5	ns
t_{DJ2}	source differential jitter for paired transitions	see Figure 16	[2] [3]	−4	-	+4	ns
t_{FEOPT}	source EOP width	see Figure 17	[3]	160	-	175	ns
t_{FDEOP}	source differential data-to-EOP transition skew	see Figure 17	[3]	−2	-	+5	ns
Receiver timing							
t_{JR1}	receiver data jitter tolerance for consecutive transitions	see Figure 18	[3]	−18.5	-	+18.5	ns
t_{JR2}	receiver data jitter tolerance for paired transitions	see Figure 18	[3]	−9	-	+9	ns
t_{FEOPR}	receiver SE0 width	accepted as EOP; see Figure 17	[3]	82	-	-	ns
t_{FST}	width of SE0 during differential transition	rejected as EOP; see Figure 19	[3]	-	-	14	ns
Hub timing (downstream ports configured as full-speed)							
t_{FHDD}	hub differential data delay (without cable)	see Figure 20; C_L = 0 pF	[3]	-	-	44	ns
t_{FSOP}	data bit width distortion after SOP	see Figure 20	[3]	−5	-	+5	ns
t_{FEOPD}	hub EOP delay relative to t_{HDD}	see Figure 21	[3]	0	-	15	ns
t_{FHESK}	hub EOP output width skew	see Figure 21	[3]	−15	-	+15	ns

[1] Test circuit; see Figure 23.

[2] Excluding the first transition from Idle state.

[3] Characterized only, not tested. Limits guaranteed by design.

Table 33: Dynamic characteristics: analog I/O pins (D+, D–); low-speed mode [1]

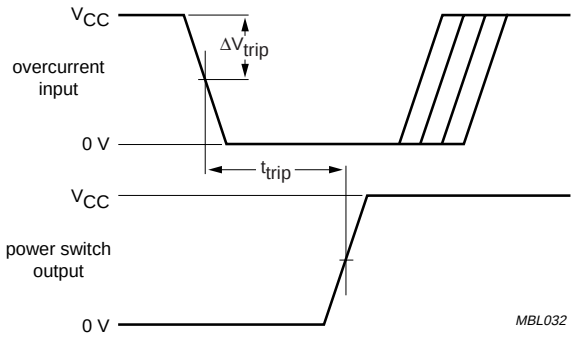
V_{CC} = 4.0 to 5.5 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; C_L = 50 pF; R_{PU} = 1.5 kΩ on D– to V_{TERM}; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics							
t_{LR}	rise time	C_L = 200 to 600 pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$		75	-	300	ns
t_{LF}	fall time	C_L = 200 to 600 pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$		75	-	300	ns
LRFM	differential rise/fall time matching (t_{LR}/t_{LF})		[2]	80	-	125	%
V_{CRS}	output signal crossover voltage		[2] [3]	1.3	-	2.0	V
Hub timing (downstream ports configured as low-speed)							
t_{LHDD}	hub differential data delay	see Figure 20		-	-	300	ns
t_{LSOP}	data bit width distortion after SOP	see Figure 20	[3]	–60	-	+60	ns
t_{LEOPD}	hub EOP delay relative to t_{HDD}	see Figure 21	[3]	0	-	200	ns
t_{LHESK}	hub EOP output width skew	see Figure 21	[3]	–300	-	+300	ns

[1] Test circuit: see Figure 23.

[2] Excluding the first transition from Idle state.

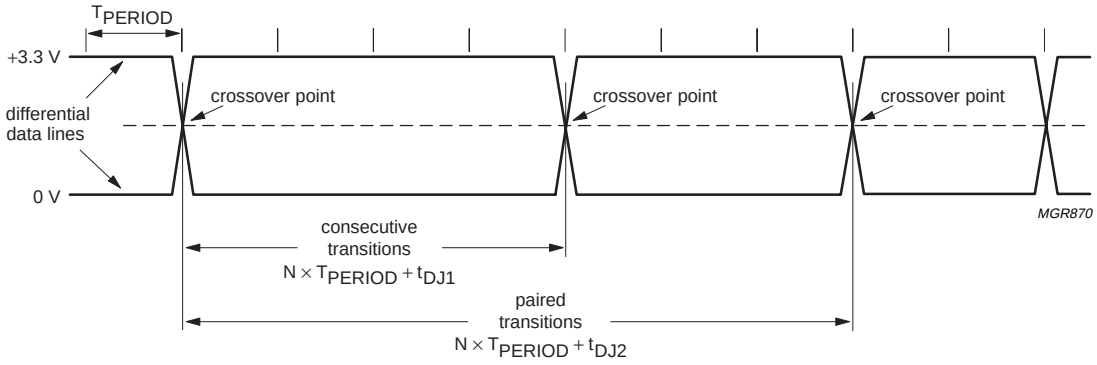
[3] Characterized only, not tested. Limits guaranteed by design.



Overcurrent input: $\overline{OCn}$; power switch output: $\overline{PSWn}$.

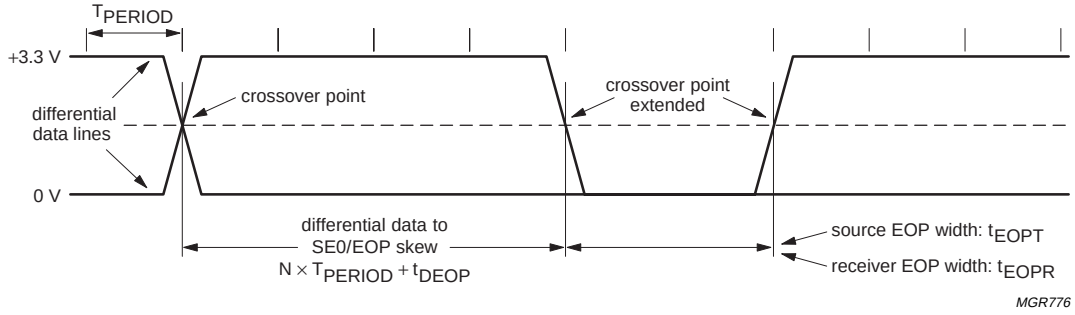
Reference voltage for overcurrent sensing: V_{CC} (bus-powered mode) or $V_{SP/\overline{BP}}$ (self-powered mode).

Fig 15. Overcurrent trip response timing.



T_{PERIOD} is the bit duration corresponding with the USB data rate.

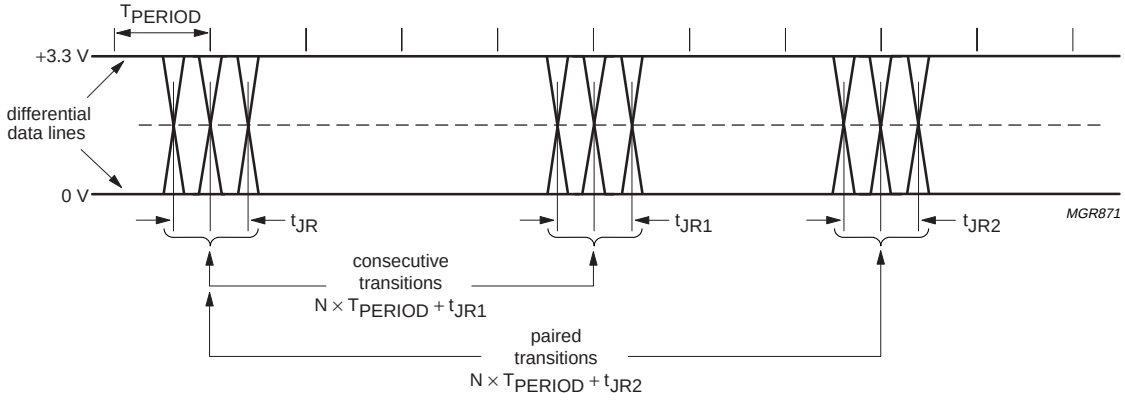
Fig 16. Source differential data jitter.



T_{PERIOD} is the bit duration corresponding with the USB data rate.

Full-speed timing symbols have a subscript prefix ‘F’, low-speed timings a prefix ‘L’.

Fig 17. Source differential data-to-EOP transition skew and EOP width.



T_{PERIOD} is the bit duration corresponding with the USB data rate.

Fig 18. Receiver differential data jitter.

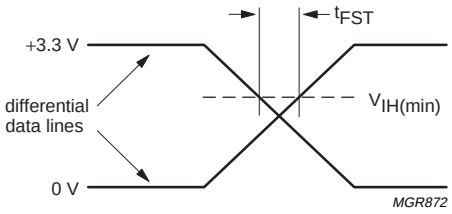
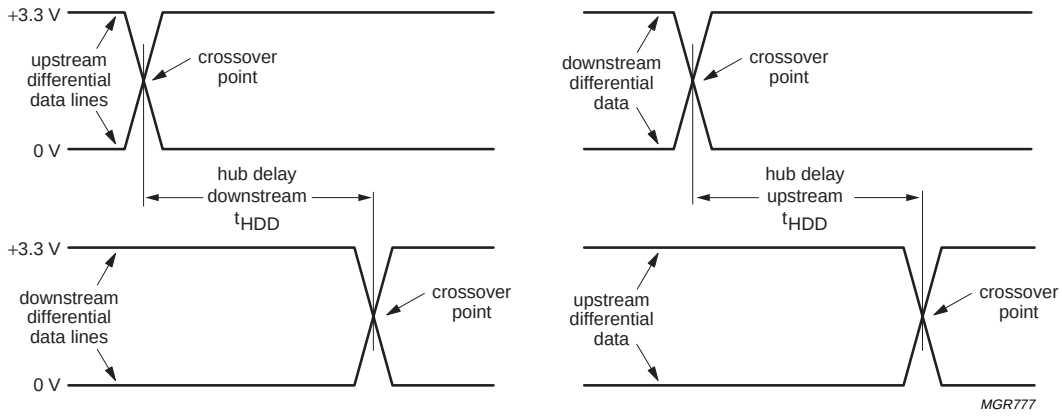


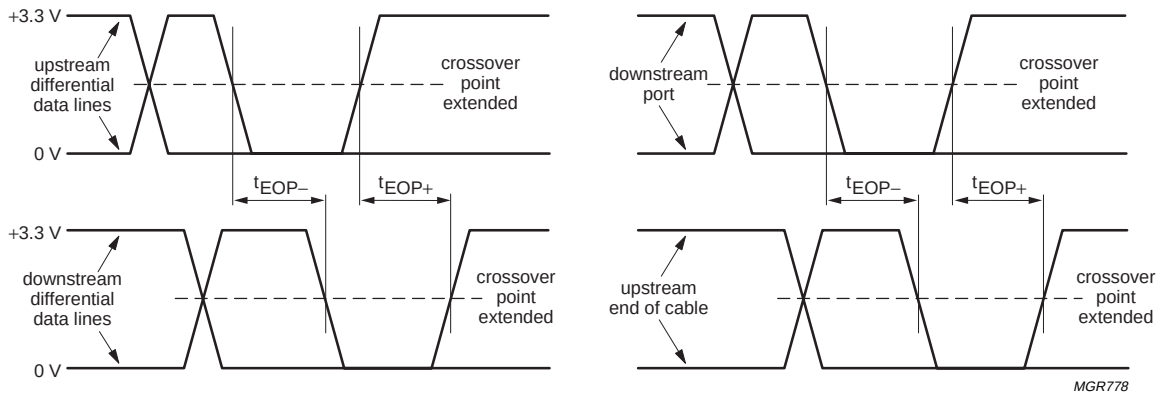
Fig 19. Receiver SE0 width tolerance.



SOP distortion:
$t_{SOP} = t_{HDD\ (next\ J)} - t_{HDD(SOP)}$

Full-speed timing symbols have a subscript prefix ‘F’, low-speed timings a prefix ‘L’.

Fig 20. Hub differential data delay and SOP distortion.



EOP delay:
$t_{EOP} = \max(t_{EOP-}, t_{EOP+})$

EOP delay relative to t_{HDD}:
$t_{EOPD} = t_{EOP} - t_{HDD}$

EOP skew:
$t_{HESK} = t_{EOP+} - t_{EOP-}$

Full-speed timing symbols have a subscript prefix ‘F’, low-speed timings a prefix ‘L’.

Fig 21. Hub EOP delay and EOP skew.

Table 34: Dynamic characteristics: I²C-bus pins (SDA, SCL)

V_{CC} and T_{amb} within recommended operating range; V_{DD} = +5 V; V_{SS} = V_{GND} ; V_{IL} and V_{IH} between V_{SS} and V_{DD}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	f_{XTAL} = 6 MHz	0	93.75 [1]	100	kHz
t_{BUF}	bus free time		4.7	-	-	µs
$t_{SU;STA}$	START condition set-up time		250	-	-	ns
$t_{HD;STA}$	hold time START condition		4.0	-	-	µs
t_{LOW}	SCL LOW time		4.7	-	-	µs
t_{HIGH}	SCL HIGH time		4.0	-	-	µs
t_r	SCL and SDA rise time	[2]	-	-	1000	ns
t_f	SCL and SDA fall time		-	-	300	ns
$t_{SU;DAT}$	data set-up time		250	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	µs
$t_{VD;DAT}$	SCL LOW to data out valid time		-	-	0.4	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	-	-	µs
C_b	capacitive load for each bus line		-	-	400	pF

[1] $f_{SCL} = {}^{1}/_{64} f_{XTAL}$.

[2] Rise time is determined by C_b and pull-up resistor value R_p (typ. 4.7 kΩ).

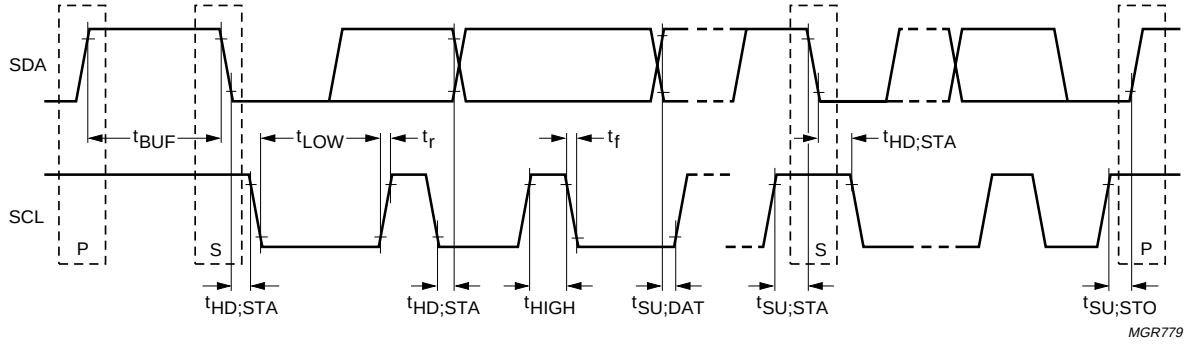
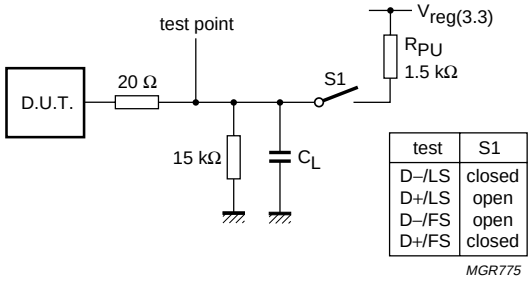


Fig 22. I²C-bus timing.

17. Test information

The dynamic characteristics of the analog I/O ports (D+ and D–) as listed in Table 32 and Table 33, were determined using the circuit shown in Figure 23.



Load capacitance:

C_L = 50 pF (full-speed mode)

C_L = 200 pF or 600 pF (low-speed mode, minimum or maximum timing).

Speed selection:

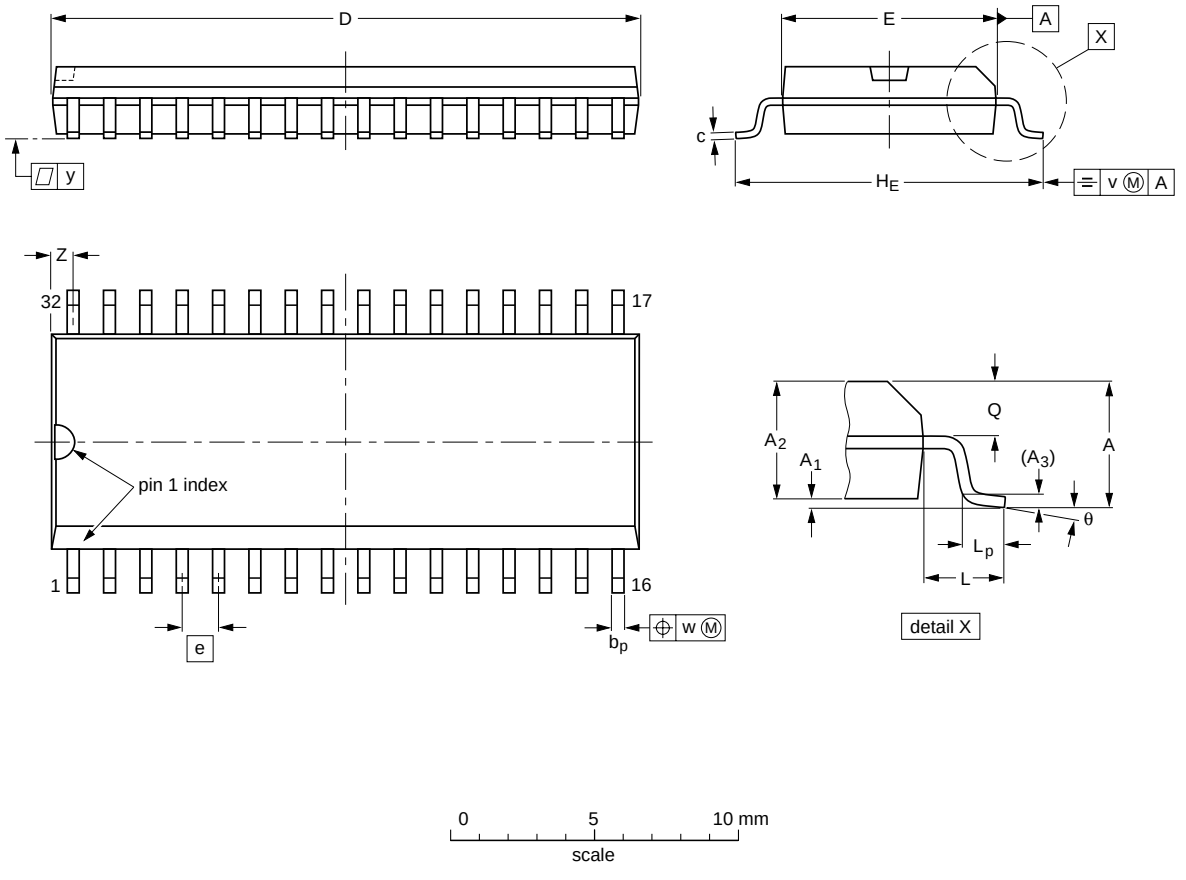
full-speed mode (FS): 1.5 kΩ pull-up resistor on D+

low-speed mode (LS): 1.5 kΩ pull-up resistor on D–.

Fig 23. Load impedance for D+ and D- pins.

18. Package outline

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

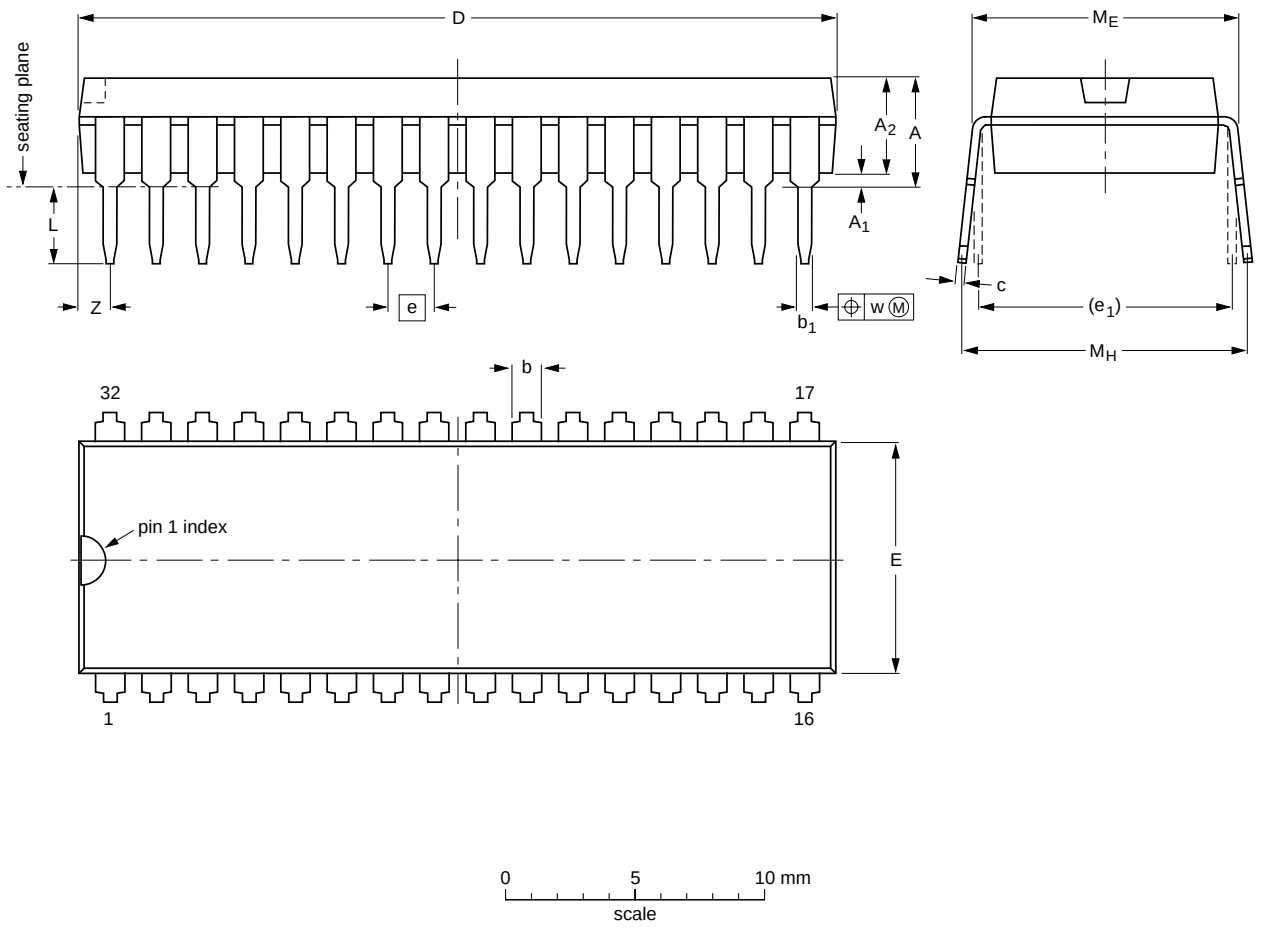
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~95-01-25~~ 97-05-22

Fig 24. SO32 package outline.

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

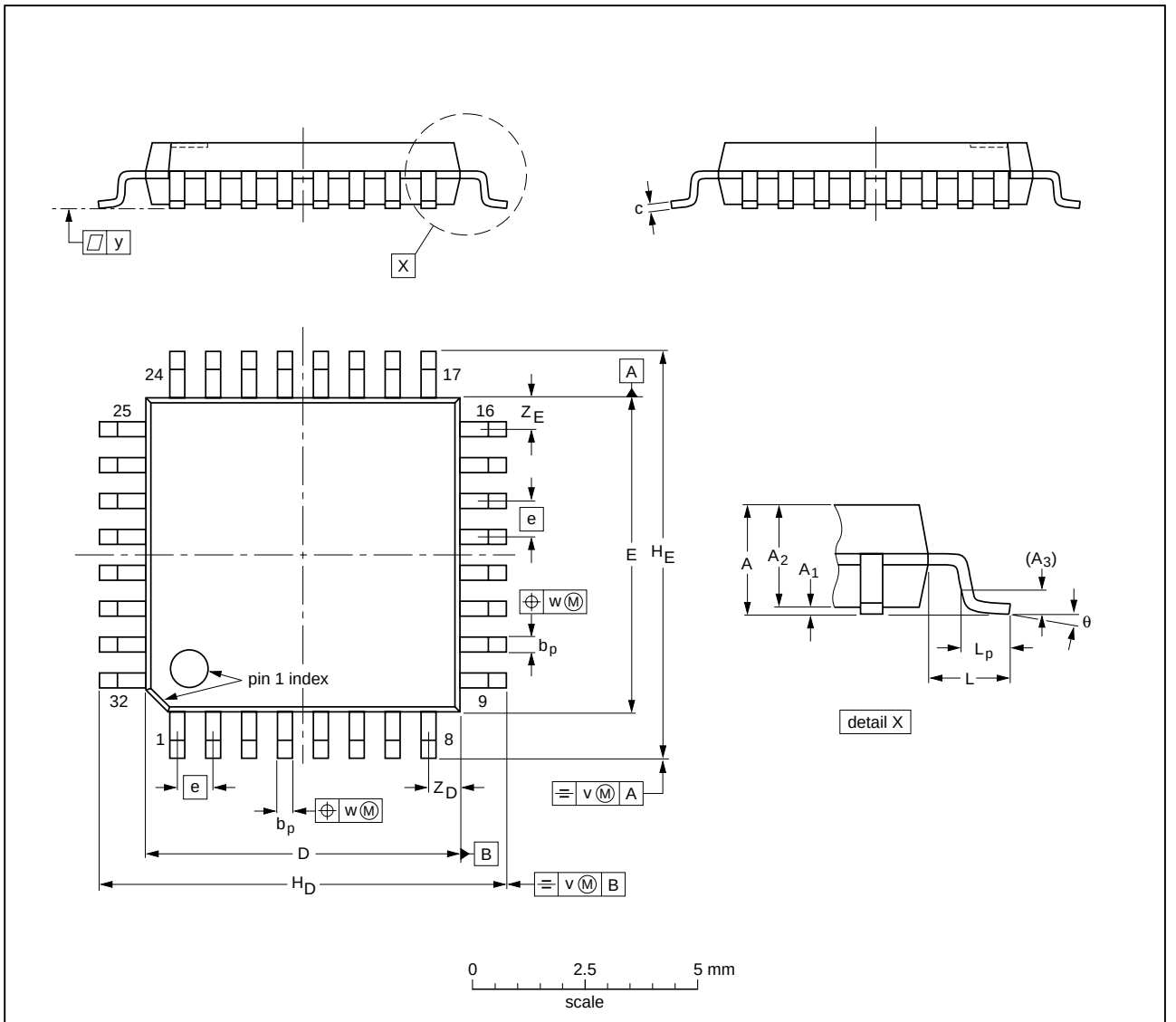
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

Fig 25. SDIP32 package outline.

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1						~~95-12-19~~ 97-08-04

Fig 26. LQFP32 package outline.

19. Soldering

19.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

19.2 Surface mount packages

19.2.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

19.2.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

19.2.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19.3 Through-hole mount packages

19.3.1 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

19.3.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

19.4 Package related soldering information

Table 35: Suitability of IC packages for wave, reflow and dipping soldering methods

Mounting	Package	Soldering method		
		Wave	Reflow [1]	Dipping
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable [2]	–	suitable
Surface mount	BGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable [3]	suitable	–
	PLCC [4], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended [4] [5]	suitable	–
	SSOP, TSSOP, VSO	not recommended [6]	suitable	–

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[3] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[4] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[5] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[6] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

20. Revision history

Table 36: Revision history

Rev	Date	CPCN	Description
01	19991005		Preliminary specification; initial version.

21. Data sheet status

Datasheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

22. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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