

HN58C256 Series

256K (32K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58C256 is a 256-Kilobit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 32,768 x 8-bits. The HN58C256 is capable of in-system electrical Byte and Page reprogrammability.

The HN58C256 achieves fast address access, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58C256 has a 64-Byte Page Programming function to make its erase and write operations faster. The HN58C256 features Data Polling to indicate completion of erase and programming operations.

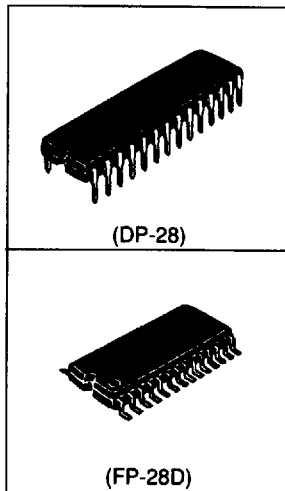
The HN58C256 provides several levels of data protection. Hardware data protection is provided with noise protection on the WE signal and write inhibit on power on and off.

The HN58C256 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

The Hitachi HN58C256 is offered in JEDEC-Standard Byte-Wide EEPROM pinouts in 28-pin Plastic DIP and 28-lead SOP packages.

■ FEATURES

- Single Power Supply:
 $V_{cc} = 5V \pm 10\%$
- Fast Access Time:
200 ns (max)
- Low Power Dissipation:
Active Current: 20 mW/MHz (typ)
Standby Current: 200 μ W (typ)
- Automatic Programming:
Automatic Page Write: 10 ms (max)
64 Byte Page Size
Automatic Byte Write: 10 ms (max)
- Data Polling
- Data Protection Circuitry on Power On/Off
- Data Retention: 10 years
- Erase/Write Endurance:
100,000 cycles in Page Mode
- Pin Arrangement:
JEDEC Standard Byte-Wide EEPROM
- Packages:
28-pin Plastic DIP
28-lead Plastic SOP

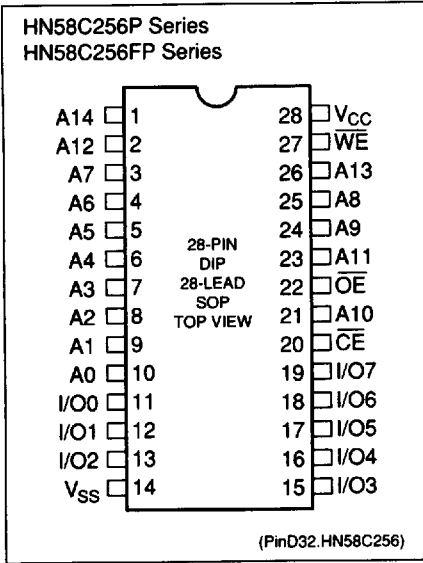


HN58C256 Series

ORDERING INFORMATION

| Type No. | Access Time | Package |
|---------------|-------------|---------------------------------|
| HN58C256P-20 | 200 ns | 28-pin Plastic DIP (DP-28) |
| HN58C256FP-20 | 200 ns | 28-lead Plastic SOP (FP-28D) |

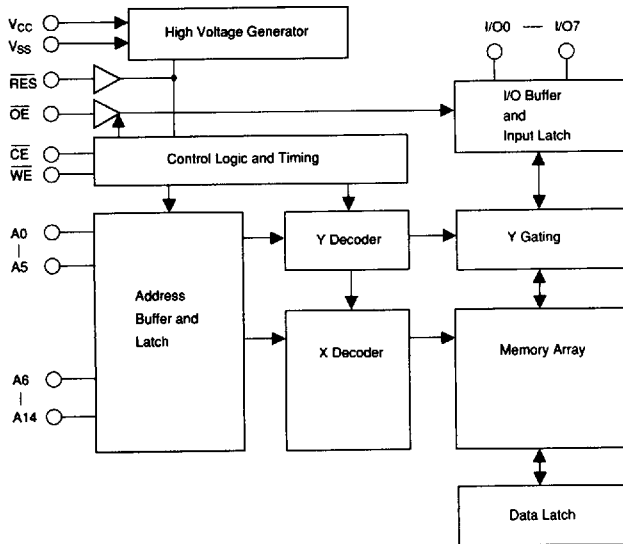
PIN ARRANGEMENT



PIN DESCRIPTION

| Pin Name | Function |
|-----------------|---------------|
| $A_0 - A_{14}$ | Address |
| $I/O_0 - I/O_7$ | Input/Output |
| \overline{OE} | Output Enable |
| \overline{CE} | Chip Enable |
| \overline{WE} | Write Enable |
| V_{CC} | Power Supply |
| V_{SS} | Ground |

BLOCK DIAGRAM



■ **MODE SELECTION**

| | | | | |
|---------------|-----------------|-----------------|-----------------|----------------------|
| Mode | \overline{CE} | \overline{OE} | \overline{WE} | I/O |
| Read | V_{IL} | V_{IL} | V_{IH} | D_{OUT} |
| Standby | V_{IH} | X | X | High-Z |
| Write | V_{IL} | V_{IH} | V_{IL} | D_{IN} |
| Deselect | V_{IL} | V_{IH} | V_{IH} | High-Z |
| Write Inhibit | X | X | V_{IH} | - |
| | X | V_{IL} | X | - |
| Data Polling | V_{IL} | V_{IL} | V_{IH} | Data Out (I/O_7) |

Note: 1. X = Don't Care

■ **ABSOLUTE MAXIMUM RATINGS**

| Item | Symbol | Value | Unit |
|--|-----------|---------------------------|------|
| Supply Voltage ¹ | V_{CC} | -0.6 to +7.0 | V |
| Input Voltage ¹ | V_{IN} | -0.5 ² to +7.0 | V |
| Operating Temperature Range ³ | T_{OPR} | 0 to +70 | °C |
| Storage Temperature Range | T_{STG} | -55 to +125 | °C |

- Notes: 1. Relative to V_{SS} .
 2. V_{IN} min = -3.0V for pulse width \leq 50 ns.
 3. Including electrical characteristics and data retention.

■ **CAPACITANCE** ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Condition |
|--------------------|-----------|------|------|------|------|----------------|
| Input Capacitance | C_{IN} | - | - | 6 | pF | $V_{IN} = 0V$ |
| Output Capacitance | C_{OUT} | - | - | 12 | pF | $V_{OUT} = 0V$ |

HN58C256 Series

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to 70°C)

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Condition |
|----------------------------|-----------|-------------------|------|--------------|---------------|---|
| Input Leakage Current | I_{LI} | - | - | 2 | μA | $V_{CC} = 5.5\text{ V}$, $V_{IN} = 5.5\text{ V}$ |
| Output Leakage Current | I_{LO} | - | - | 2 | μA | $V_{CC} = 5.5\text{ V}$, $V_{OUT} = 5.5\text{ V}/0.4\text{ V}$ |
| Standby V_{CC} Current | I_{CC1} | - | - | 200 | μA | $\overline{CE} = V_{CC}$ |
| | I_{CC2} | - | - | 1 | mA | $\overline{CE} = V_{IH}$ |
| Operating V_{CC} Current | I_{CC3} | - | - | 12 | mA | $I_{OUT} = 0\text{ mA}$, Duty = 100%, Cycle = 1 μs |
| | | - | - | 30 | mA | $I_{OUT} = 0\text{ mA}$, Duty = 100%, Cycle = 200 ns |
| Input Voltage | V_{LL} | -0.3 ¹ | - | 0.8 | V | |
| | V_{IH} | 2.2 | - | $V_{CC} + 1$ | V | |
| Output Voltage | V_{OL} | - | - | 0.4 | V | $I_{OL} = 2.1\text{ mA}$ |
| | V_{OH} | 2.4 | - | - | V | $I_{OH} = -400\text{ }\mu\text{A}$ |

Notes: 1. V_{LL} min = -3.0 V for pulse width ≤ 50 ns.

AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

($T_a = 0$ to 70°C , $V_{CC} = 5V \pm 10\%$)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

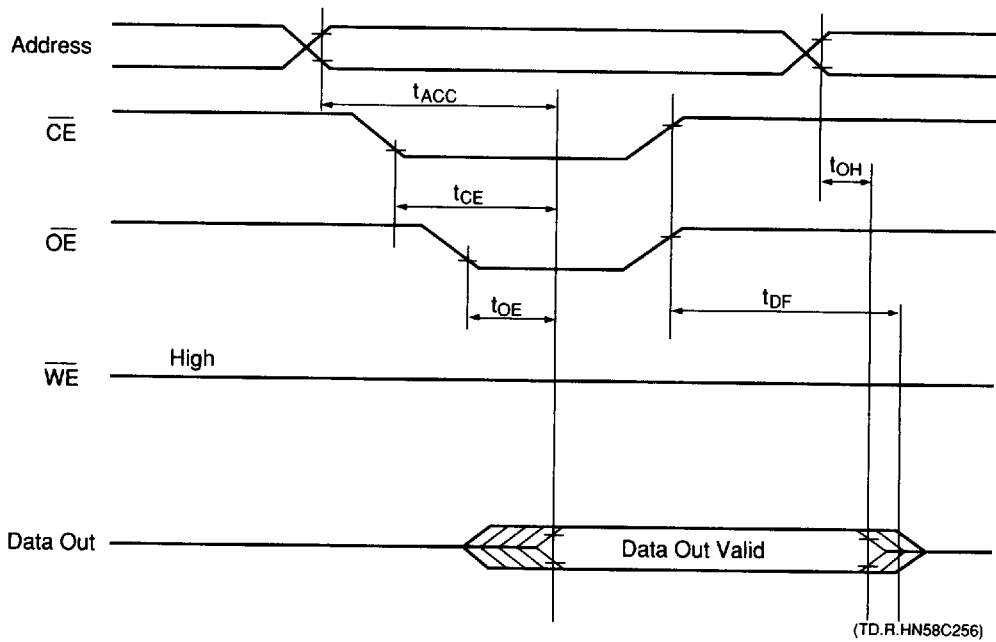
| Item | Symbol | HN58C256-20 | | Unit | Test Condition |
|---------------------------------------|-----------|-------------|------|------|---|
| | | Min. | Max. | | |
| Address Access Time | t_{ACC} | - | 200 | ns | $\overline{CE} = \overline{OE} = V_{LL}$, $\overline{WE} = V_{IH}$ |
| Chip Enable Access Time | t_{CE} | - | 200 | ns | $\overline{OE} = V_{LL}$, $\overline{WE} = V_{IH}$ |
| Output Enable Access Time | t_{OE} | 10 | 90 | ns | $\overline{CE} = V_{LL}$, $\overline{WE} = V_{IH}$ |
| Output Hold to Address Change | t_{OH} | 0 | - | ns | $\overline{CE} = \overline{OE} = V_{LL}$, $\overline{WE} = V_{IH}$ |
| Output Disable to High-Z ¹ | t_{DF} | 0 | 60 | ns | $\overline{CE} = V_{LL}$, $\overline{WE} = V_{IH}$ |

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

4496203 0025510 3T8

HITACHI

■ READ TIMING WAVEFORM



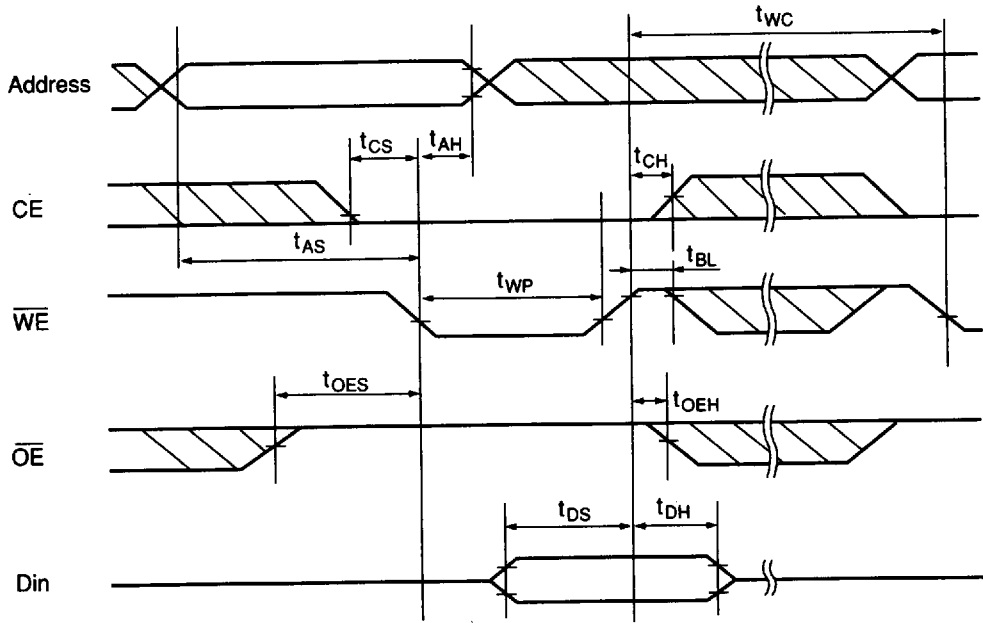
■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

| Item | Symbol | Min. ¹ | Typ. | Max. | Unit | Test Condition |
|-----------------------------------|------------|-------------------|------|------|---------|----------------|
| Address Setup Time | t_{AS} | 0 | - | - | ns | |
| Write Enable to Write Setup Time | t_{WS}^3 | 0 | - | - | ns | |
| Chip Enable to Write Setup Time | t_{CS}^2 | 0 | - | - | ns | |
| Write Pulse Width | t_{CW}^3 | 150 | - | - | ns | |
| | t_{WP}^2 | 150 | - | - | ns | |
| Address Hold Time | t_{AH} | 150 | - | - | ns | |
| Data Setup Time | t_{DS} | 100 | - | - | ns | |
| Data Hold Time | t_{DH} | 0 | - | - | ns | |
| Write Enable Hold Time | t_{WH}^3 | 0 | - | - | ns | |
| Chip Enable Hold Time | t_{CH}^2 | 0 | - | - | ns | |
| Output Enable to Write Setup Time | t_{OES} | 0 | - | - | ns | |
| Output Enable Hold Time | t_{OEH} | 0 | - | - | ns | |
| Write Cycle Time | t_{WC} | 10 | - | - | ms | |
| Byte Load Window | t_{BL} | 100 | - | - | μ s | |

- Note:
1. Use this device in a longer cycle than this value.
 2. Write Enable controlled operation.
 3. Chip Enable controlled operation.

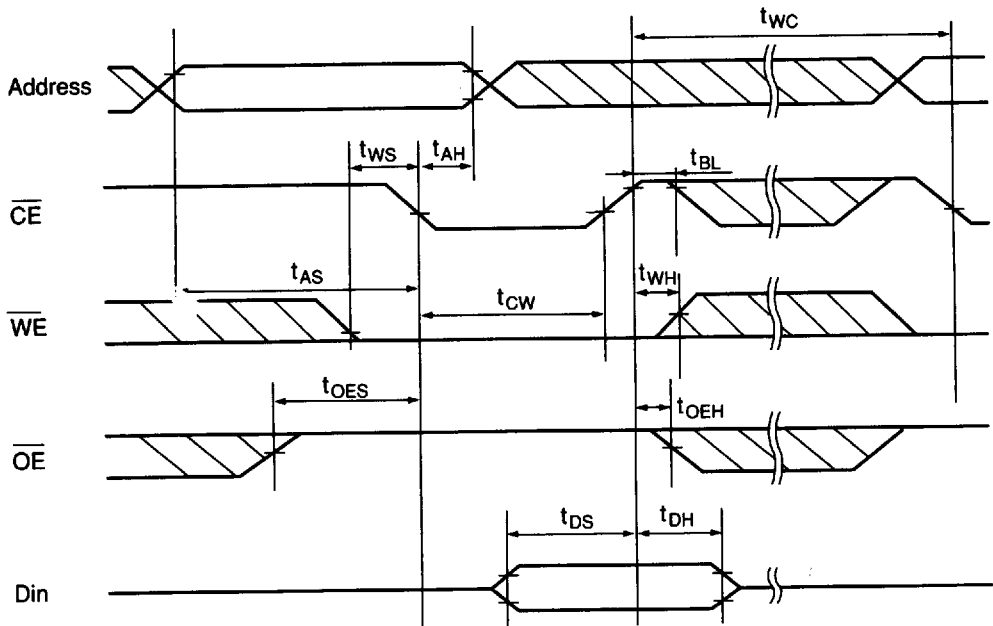


■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{\text{WE}}$ Controlled)



(TD.BE1.HN58C256)

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{\text{CE}}$ Controlled)



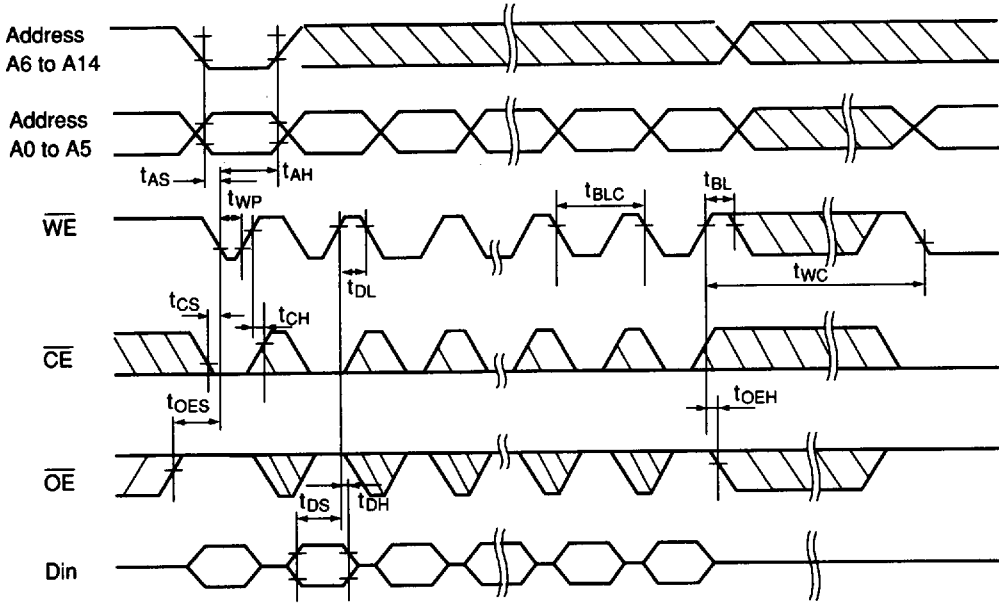
(TD.BE2.HN58C256)

■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

| Item | Symbol | Min. ¹ | Typ. | Max. | Unit | Test Condition |
|-----------------------------------|------------|-------------------|------|------|---------|----------------|
| Address Setup Time | t_{AS} | 0 | - | - | ns | |
| Write Enable to Write Setup Time | t_{WS}^3 | 0 | - | - | ns | |
| Chip Enable to Write Setup Time | t_{CS}^2 | 0 | - | - | ns | |
| Write Pulse Width | t_{WP}^2 | 150 | - | - | ns | |
| | t_{CW}^3 | 150 | - | - | ns | |
| Address Hold Time | t_{AH} | 150 | - | - | ns | |
| Data Setup Time | t_{DS} | 100 | - | - | ns | |
| Data Hold Time | t_{DH} | 0 | - | - | ns | |
| Write Enable Hold Time | t_{WH}^3 | 0 | - | - | ns | |
| Chip Enable Hold Time | t_{CH}^2 | 0 | - | - | ns | |
| Output Enable to Write Setup Time | t_{OES} | 0 | - | - | ns | |
| Output Enable Hold Time | t_{OEH} | 0 | - | - | ns | |
| Data Latch Time | t_{DL} | 200 | - | - | ns | |
| Write Cycle Time | t_{WC} | 10 | - | - | ms | |
| Byte Load Window | t_{BL} | 100 | - | - | μ s | |
| Byte Load Cycle | t_{BLC} | 0.3 | - | 30 | μ s | |

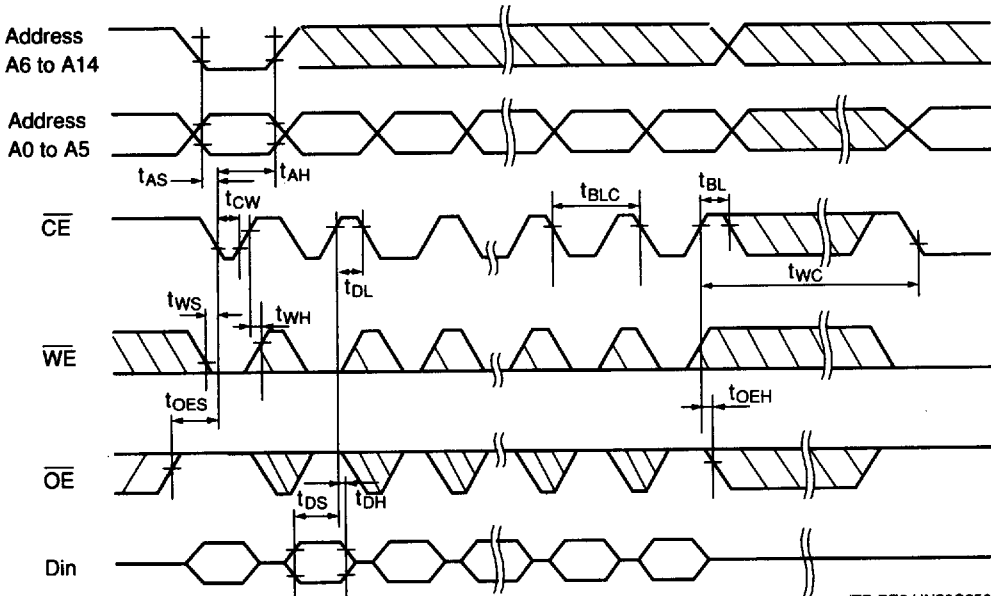
- Notes:
1. Use this device in longer cycle than this value.
 2. Write Enable controlled operation.
 3. Chip Enable controlled operation.

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM (\overline{WE} Controlled)



(TD.PE1.HN58C256)

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM (\overline{CE} Controlled)

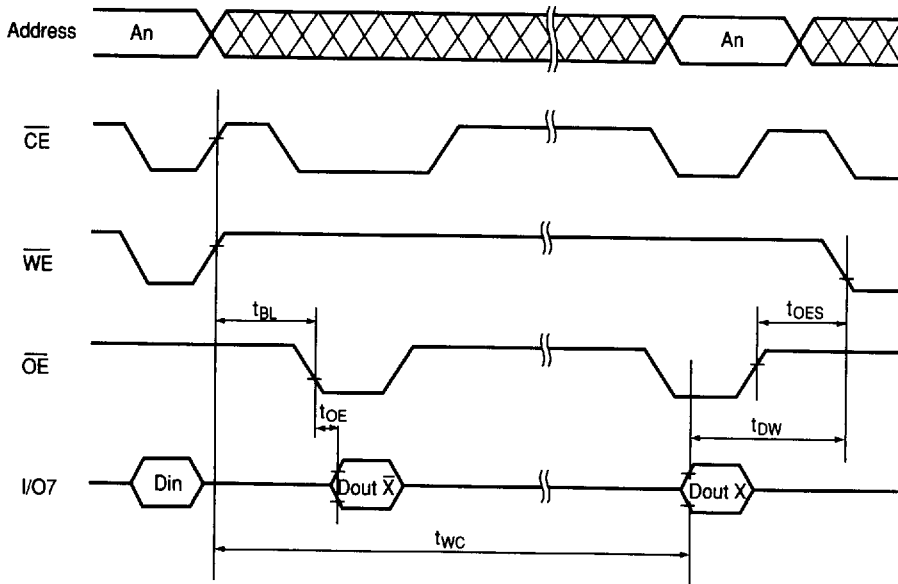


(TD.PE2.HN58C256)

■ AC ELECTRICAL CHARACTERISTICS FOR DATA POLLING OPERATION

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Condition |
|-----------------------------------|-----------|------|------|------|---------------|----------------|
| Byte Load Window | t_{BL} | 100 | - | - | μs | |
| Output Enable to Output Delay | t_{OE} | 10 | - | 90 | ns | |
| Output Enable to Write Setup Time | t_{OES} | 0 | - | - | ns | |
| Write Start Time | t_{DW} | 150 | - | - | ns | |
| Write Cycle Time | t_{WC} | - | - | 10 | ms | |

■ DATA POLLING TIMING WAVEFORM



(TD.DP.EE)

FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 64 Bytes of data to be written into the EEPROM in a single write cycle. Following the initial Byte cycle, an additional 1 to 63 Bytes can be written in the same manner. Each additional Byte load cycle must be started within 30 μ s from the preceding falling edge of \overline{WE} or \overline{CE} . When \overline{WE} or \overline{CE} is high for 100 μ s after data input, the EEPROM enters erase and write mode automatically and only the input data is written into the EEPROM. Data can be written and accessed 10^5 times in 64 Byte units.

Data Polling

Data Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 , to indicate that the EEPROM is performing a Write operation.

\overline{WE} and \overline{CE} Pin Operation

During a write cycle, addresses are latched by the falling edge of \overline{WE} or \overline{CE} , and data is latched by the rising edge of \overline{WE} or \overline{CE} .

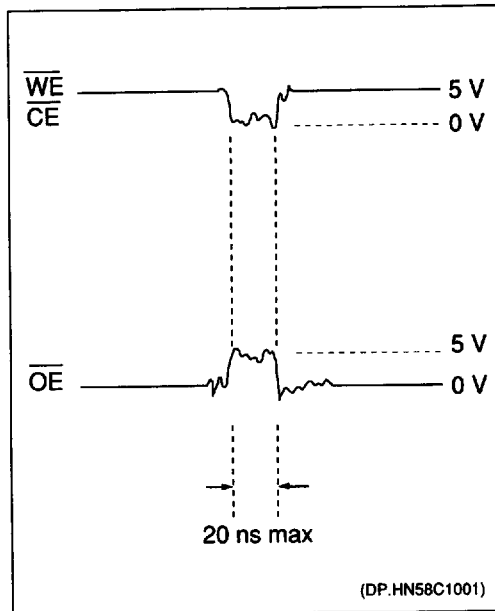
Write/Erase Endurance and Data Retention

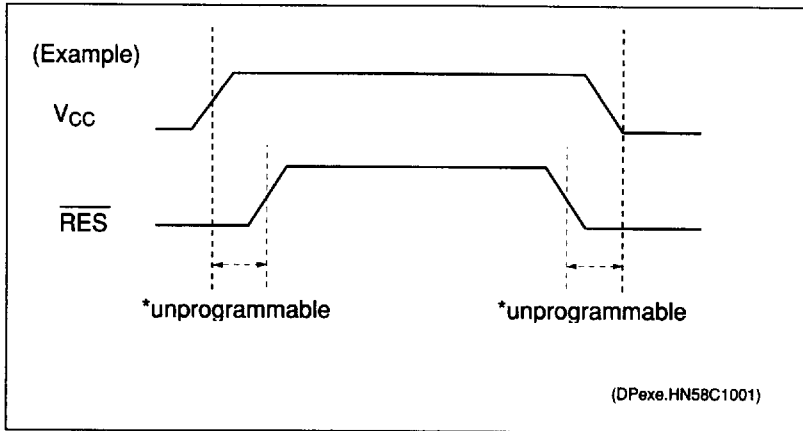
The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58C256 has:

1. Data protection against Noise on Control Pins (\overline{CE} , \overline{OE} , \overline{WE}) during Operation.
During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58C256 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.





■ **FUNCTIONAL DESCRIPTION (continued)**

Data Protection (continued)

2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

In addition, when V_{CC} is turned on or off, the input level of the control pins (\overline{CE} , \overline{OE} , \overline{WE}) must be held as $\overline{CE}=V_{CC}$ or $\overline{OE}=\text{Low}$ or $\overline{WE}=V_{CC}$ level.