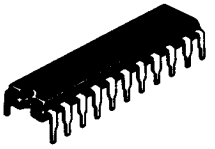
HM6288 Series

16384-word×4-bit High Speed CMOS Static RAM

The Hitachi HM6288 is a high speed 64k static RAM organized as 16-kword x 4-bit. It realizes high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6288, packaged in a 300 mil plastic DIP and SOJ, is available for high density mounting. Low power version retains the data with battery back up.



(DP-22NB)

(CP-24D)

■FEATURES

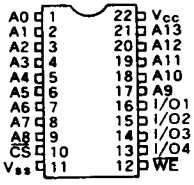
- Single 5V Supply and High Density Plastic Package.
- High Speed: Fast Access Time 25/35/45 ns (max.)
- Low Power dissipation
  - Active mode 300mW (typ.)
  - Standby mode 100μW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required.
- Equal Access and Cycle Times.
- Directly TTL Compatible – All Inputs and Outputs.

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6288P-25 HM6288P-35	25ns 35ns	300 mil 22-pin Plastic DIP (DP-22NB)
HM6288LP-25 HM6288LP-35	25ns 35ns	
HM6288JP-25 HM6288JP-35	25ns 35ns	300 mil 24-pin SOJ (CP-24D)
HM6288LJP-25 HM6288LJP-35	25ns 35ns	

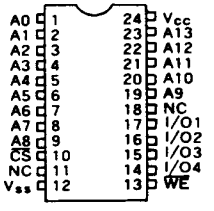
■PIN ARRANGEMENT

- HM6288P Series



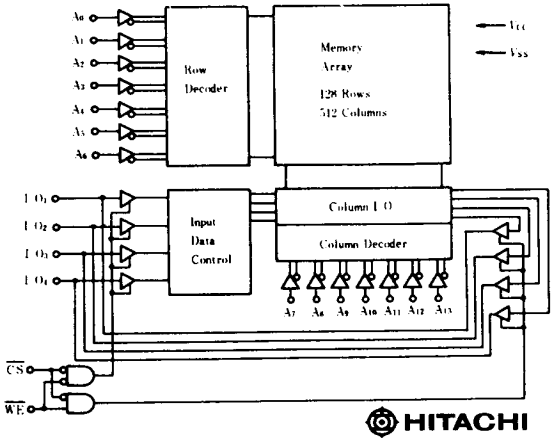
(Top View)

- HM6288JP Series



(Top View)

■BLOCK DIAGRAM



■Pin Description

Pin Name	Function
A0 – A13	Address
I/O1 – I/O4	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

HITACHI

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5^{*1} to $+7.0$	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note: *1. V_T min. = −2.0V for pulse width ≦ 10ns

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read'Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-0.5^{*1}	–	0.8	V

Note: *1. V_{IL} min. = −2.0V for pulse width ≦ 10ns

■DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=MAX. V_{IN}=V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$=V_{IH}, $V_{I/O}$=V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, min. cycle	–	60	120	mA
Standby V_{CC} Current	I_{SB}	$\overline{CS}$=V_{IH}, min. cycle	–	15	30	mA
Standby V_{CC} Current 1	I_{SB1}*2	$\overline{CS}$ ≧ V_{CC} −0.2V	–	0.02	2.0	mA
	I_{SB1}*3	0V ≦ V_{IN} ≦ 0.2V or V_{CC} −0.2V ≦ V_{IN}	–	0.02	0.1	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA	2.4	–	–	V

Notes: *1. Typical limits are at V_{CC}=5.0V, Ta=+25°C and specified loading.
*2. P version
*3. LP version

■CAPACITANCE (Ta=25°C, f=1.0MHz)

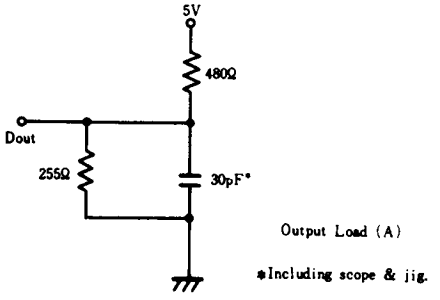
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note: This parameter is sampled and not 100% tested

■ AC CHARACTERISTICS

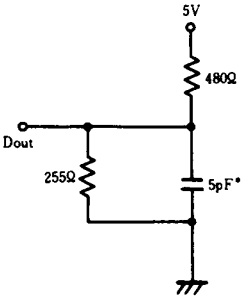
- **AC Test Conditions**

Input pulse levels: 0V to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure



Output Load (A)

*Including scope & jig.



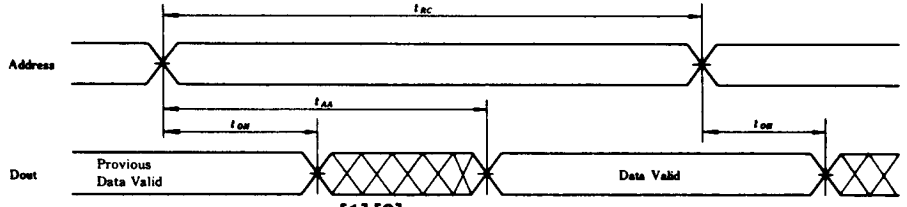
Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

■ READ CYCLE

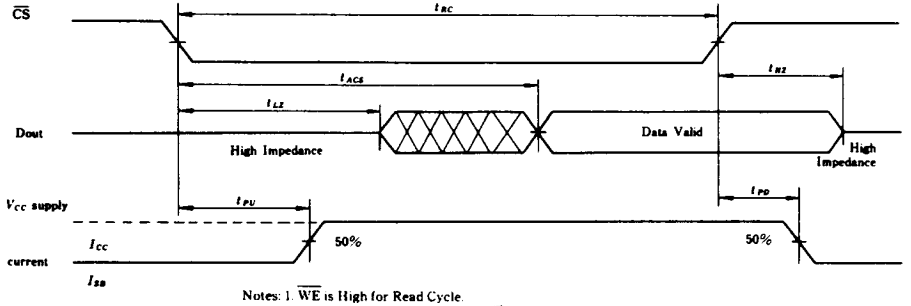
Parameter	Symbol	HM6288-25		HM6288-35		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	35	–	ns
Address Access Time	t_{AA}	–	25	–	35	ns
Chip Select Access Time	t_{ACS}	–	25	–	35	ns
Output Hold from Address Change	t_{OH}	3	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}*	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{HZ}*	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Seselection to Power Down Time	t_{PD}	–	25	–	30	ns

* Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No.1 [1] [2]



● Timing Waveform of Read Cycle No.2 [1] [3]



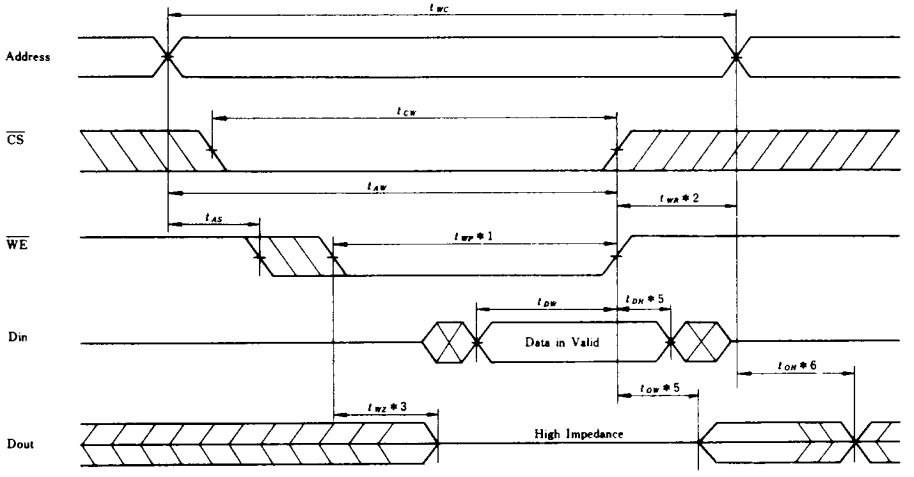
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

■ WRITE CYCLE

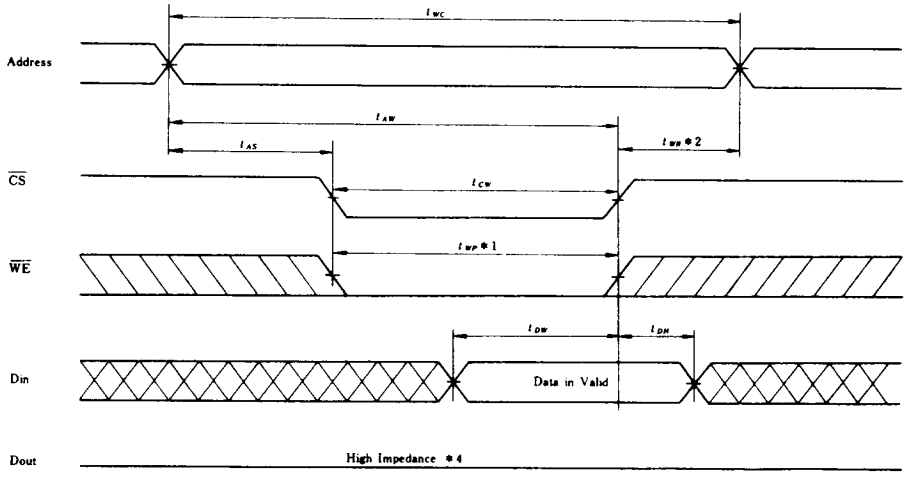
Parameter	Symbol	HM6288-25		HM6288-35		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	35	–	ns
Chip Selection to End of Write	t_{CW}	20	–	30	–	ns
Address Valid to End of Write	t_{AW}	20	–	30	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Write Pulse Width	t_{WP}	20	–	30	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Date Valid to End of Write	t_{DW}	12	–	20	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Write Enabled to Output in High Z	t_{WZ}*	0	8	0	10	ns
Output Active from End of Write	t_{OW}*	5	–	5	–	ns

* Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Write Cycle No.1 ($\overline{WE}$ Controlled)



● Timing Waveform of Write Cycle No.2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tow. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

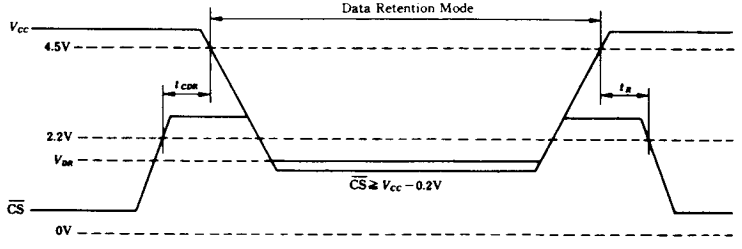
● Low *Vcc* Data Retention Characteristics ($Ta = 0$ to $+70°C$)

(This Characteristics is guaranteed only for L-version.)

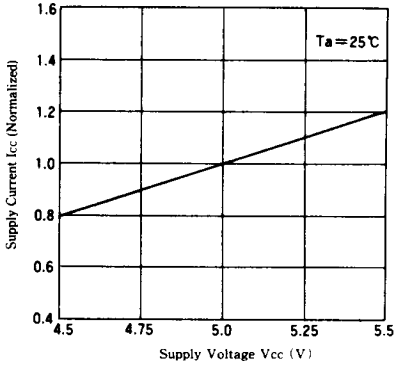
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geq V_{CC} - 0.2V$
Data retention current	I_{CCDR}	–	–	$50^{2)}$ $35^{3)}$	μA	$V_{in} \geq V_{CC} - 0.2V$ or $0V \leq V_{in} \leq 0.2V$
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	See retention waveform
Operation recovery time	t_R	$t_{RC}^{1)}$	–	–	ns	

NOTE : 1. t_{RC} = Read cycle time
2. $V_{CC} = 3.0V$
3. $V_{CC} = 2.0V$

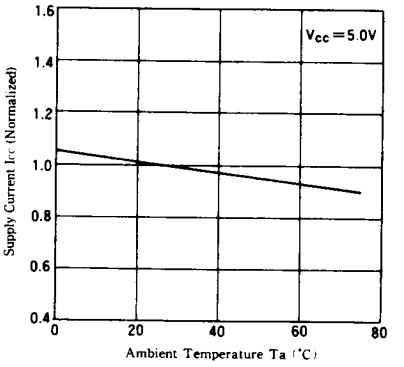
Low *Vcc* Data Retention Waveform



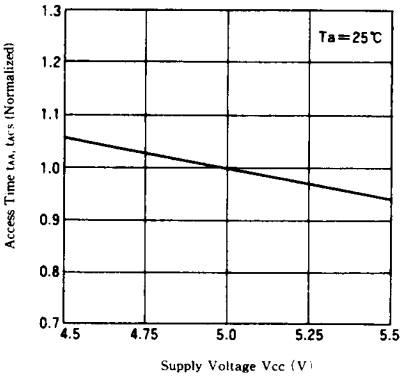
SUPPLY CURRENT VS. SUPPLY VOLTAGE



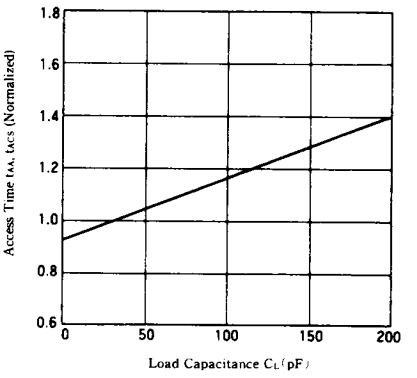
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



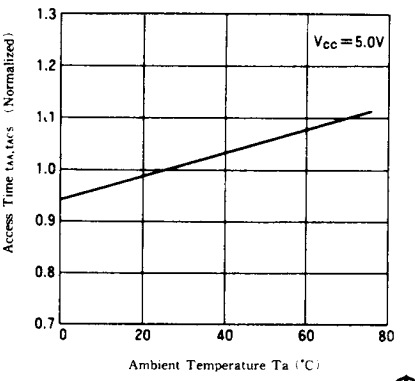
ACCESS TIME VS. SUPPLY VOLTAGE



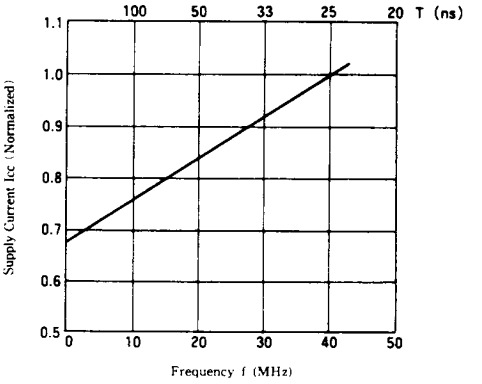
ACCESS TIME VS. LOAD CAPACITANCE



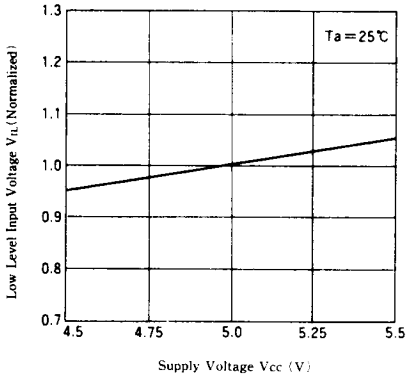
ACCESS TIME VS. AMBIENT TEMPERATURE



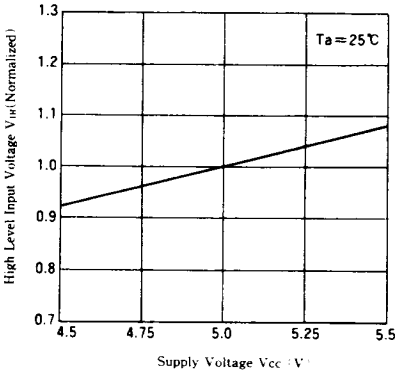
SUPPLY CURRENT VS. FREQUENCY



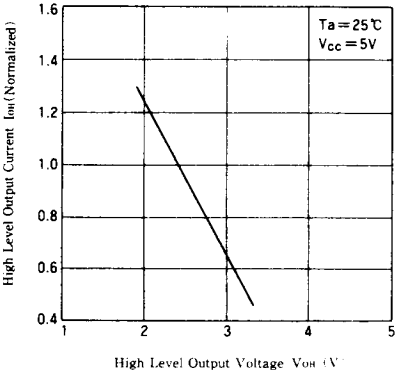
LOW LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



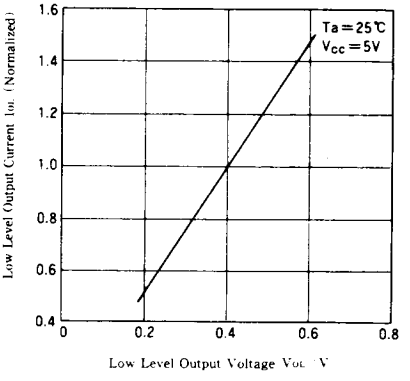
HIGH LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



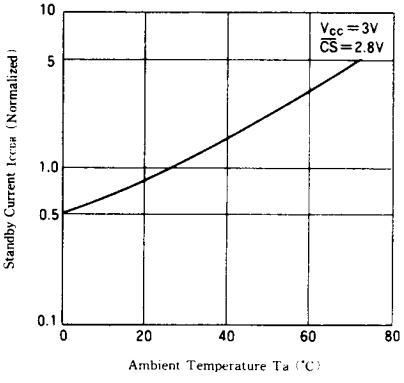
OUTPUT CURRENT VS. OUTPUT VOLTAGE(1)



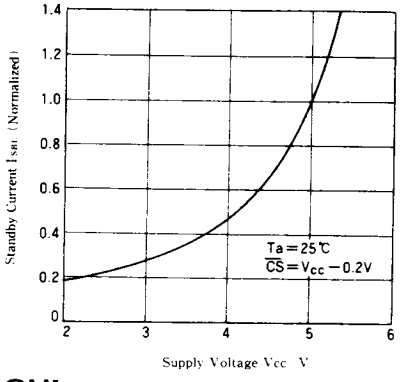
OUTPUT CURRENT VS. OUTPUT VOLTAGE(2)



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



STANDBY CURRENT VS. INPUT VOLTAGE