

# NTR3162P

## Power MOSFET

-20 V, -3.6 A, Single P-Channel, SOT-23

### Features

- Low  $R_{DS(on)}$  at Low Gate Voltage
- -0.3 V Low Threshold Voltage
- Fast Switching Speed
- This is a Pb-Free Device

### Applications

- Battery Management
- Load Switch in PWM
- Battery Protection

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	-20	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 8$	V	
Continuous Drain Current (Note 1)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	-2.2	A
			$T_A = 85^\circ\text{C}$	-1.6	
	$t \leq 5$ s	$T_A = 25^\circ\text{C}$	-3.6		
Power Dissipation (Note 1)	Steady State	$P_D$	$T_A = 25^\circ\text{C}$	0.48	W
	$t \leq 5$ s			1.25	
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	-10.7	A	
Operating Junction and Storage Temperature		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	-0.6	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		$T_L$	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	260	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - $t < 10$ s (Note 1)	$R_{\theta JA}$	100	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

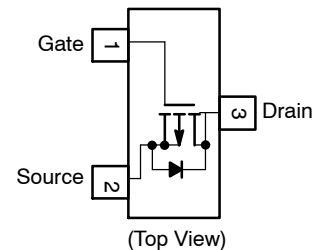


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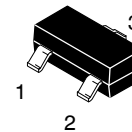
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
-20 V	70 m $\Omega$ @ -4.5 V	-2.2 A
	95 m $\Omega$ @ -2.5 V	-1.9 A
	120 m $\Omega$ @ -1.8 V	-1.7 A

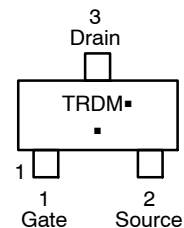
### SIMPLIFIED SCHEMATIC



### MARKING DIAGRAM/ PIN ASSIGNMENT



SOT-23  
CASE 318  
STYLE 21



TRD = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTR3162PT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
NTR3162PT3G	SOT-23 (Pb-Free)	10000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\ \mu\text{A}$ , Reference to $25^\circ\text{C}$		14.5		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}, T_J = 25^\circ\text{C}$ $V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}, T_J = 85^\circ\text{C}$			-1.0 -5.0	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			$\pm 100$	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-0.3	-0.6	-1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			2.5		mV/ $^\circ\text{C}$
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -2.2\text{ A}$		48	70	m $\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -1.9\text{ A}$		57	95	
		$V_{GS} = -1.8\text{ V}, I_D = -1.7\text{ A}$		72	120	
		$V_{GS} = -1.5\text{ V}, I_D = -1.0\text{ A}$		88		
Forward Transconductance	$g_{FS}$	$V_{DS} = -5.0\text{ V}, I_D = -2.2\text{ A}$		9.0		S

## CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -10\text{ V}$		940		pF
Output Capacitance	$C_{oss}$			140		
Reverse Transfer Capacitance	$C_{rss}$			100		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -3.6\text{ A}$		10.3		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.5		
Gate-to-Source Charge	$Q_{GS}$			1.4		
Gate-to-Drain Charge	$Q_{GD}$			2.7		
Gate Resistance	$R_G$			6.0		

## SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -10\text{ V}, I_D = -3.6\text{ A}, R_G = 6\ \Omega$		8.0		ns
Rise Time	$t_r$			15		
Turn-Off Delay Time	$t_{d(off)}$			31		
Fall Time	$t_f$			50		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}, T_J = 25^\circ\text{C}$		0.7	1.2	V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, I_D = -1.0\text{ A}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}$		25		ns
Charge Time	$t_a$			8.0		
Discharge Time	$t_b$			17		
Reverse Recovery Charge	$Q_{RR}$			11		

2. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

4. Switching characteristics are independent of operating junction temperatures.

P-CHANNEL TYPICAL CHARACTERISTICS

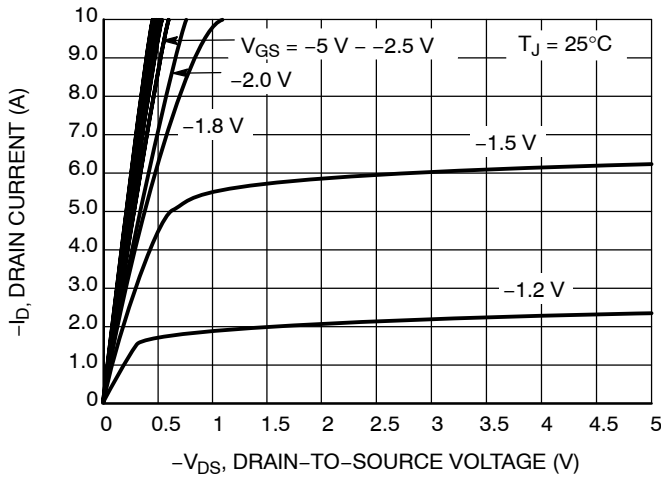


Figure 1. On-Region Characteristics

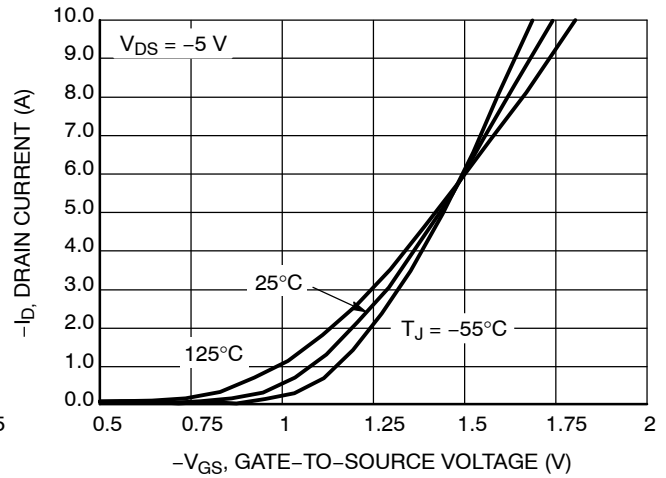


Figure 2. Transfer Characteristics

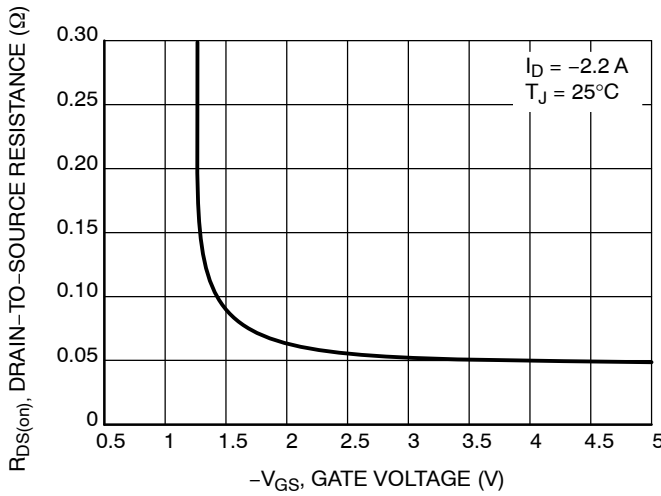


Figure 3. On-Resistance vs. Gate-to-Source Voltage

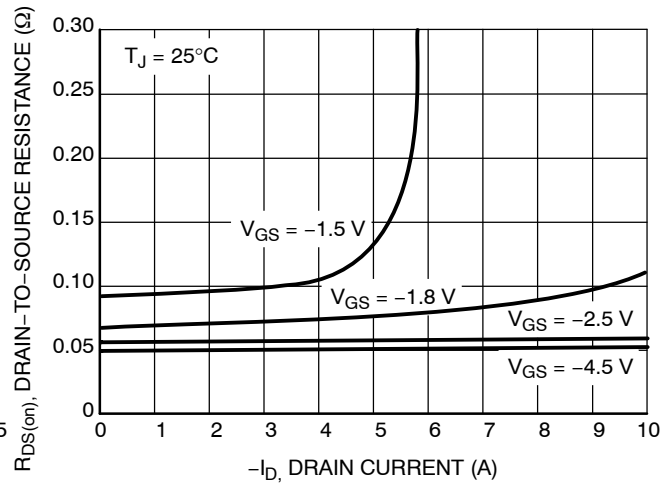


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

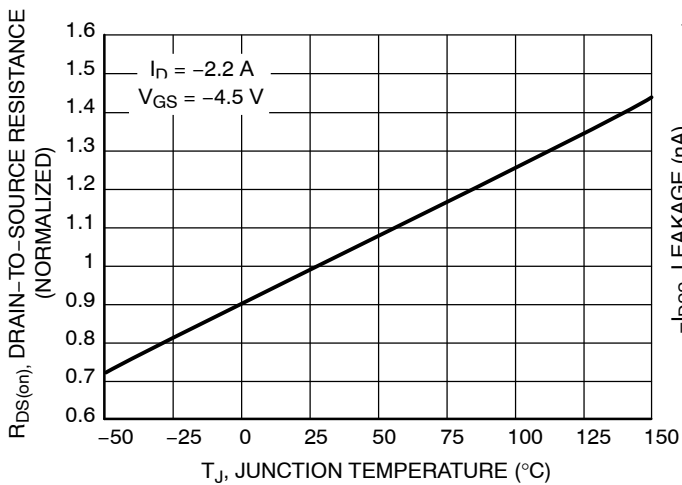


Figure 5. On-Resistance Variation with Temperature

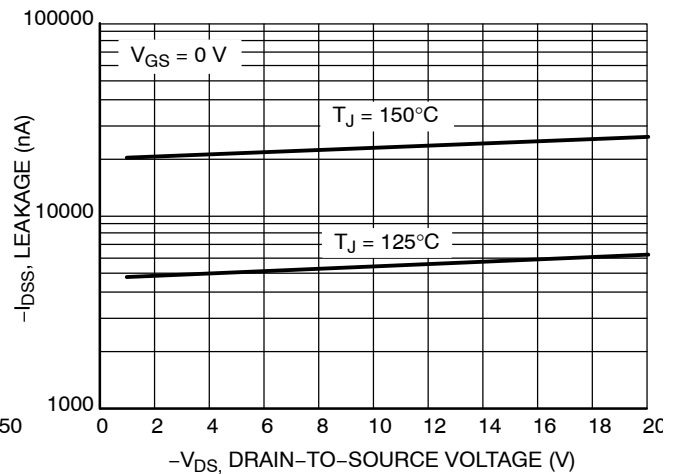
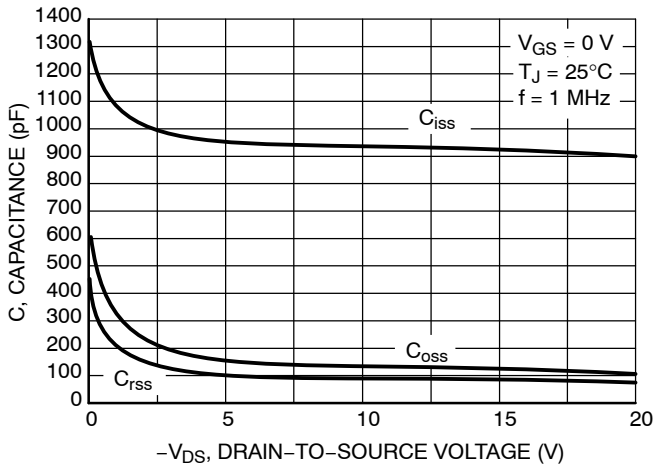
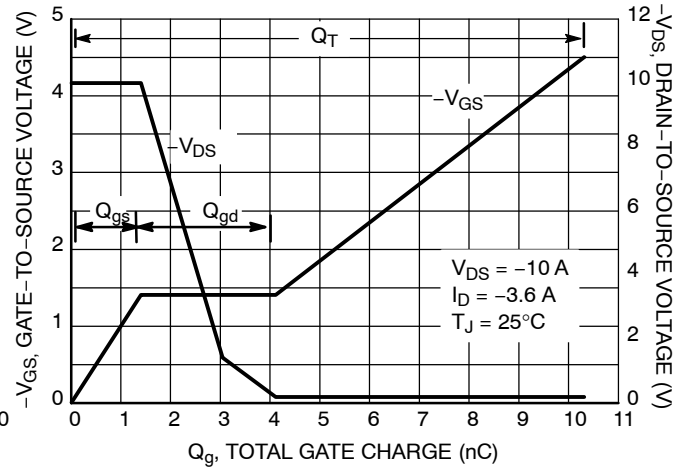


Figure 6. Drain-to-Source Leakage Current vs. Voltage

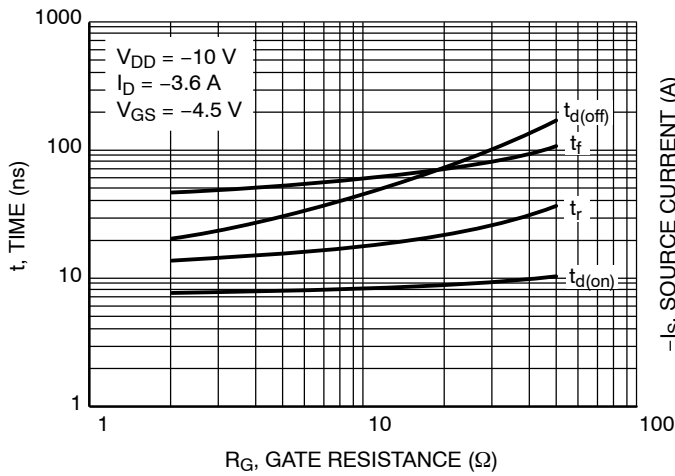
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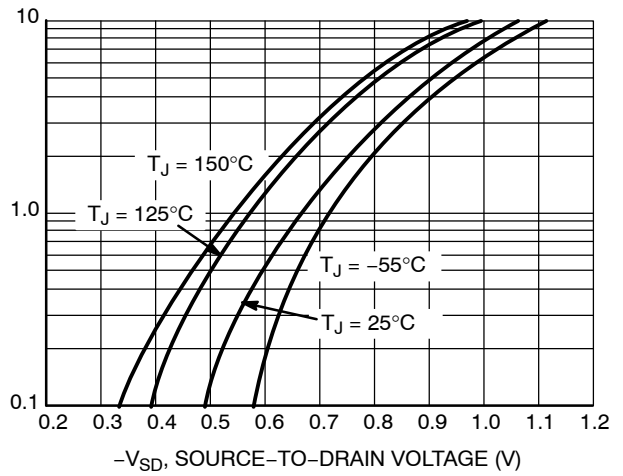
**Figure 7. Capacitance Variation**



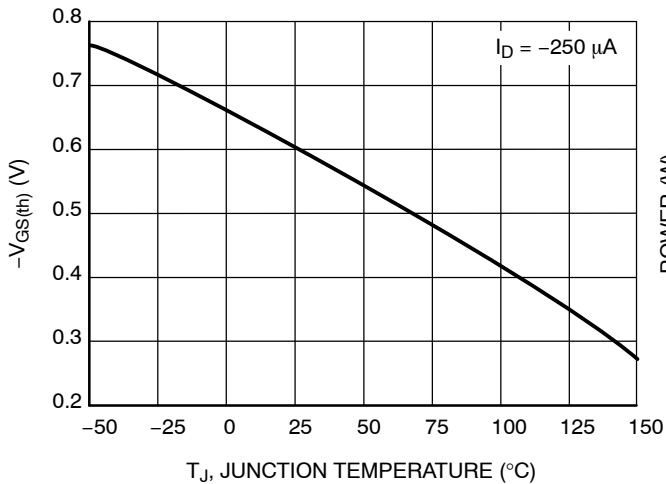
**Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Gate Charge**



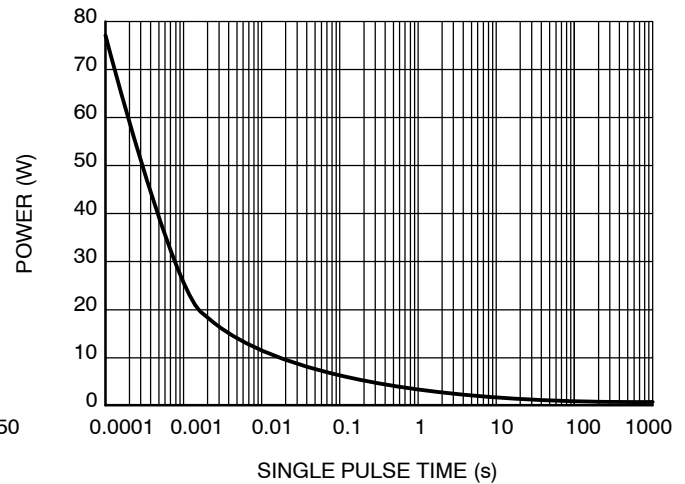
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**

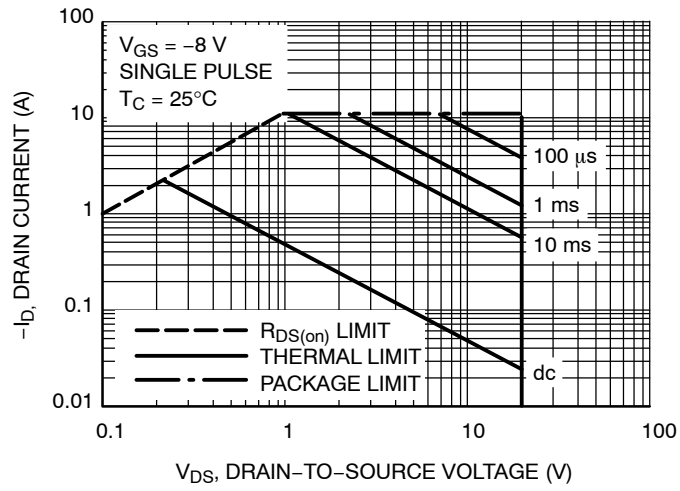


**Figure 11. Threshold Voltage**

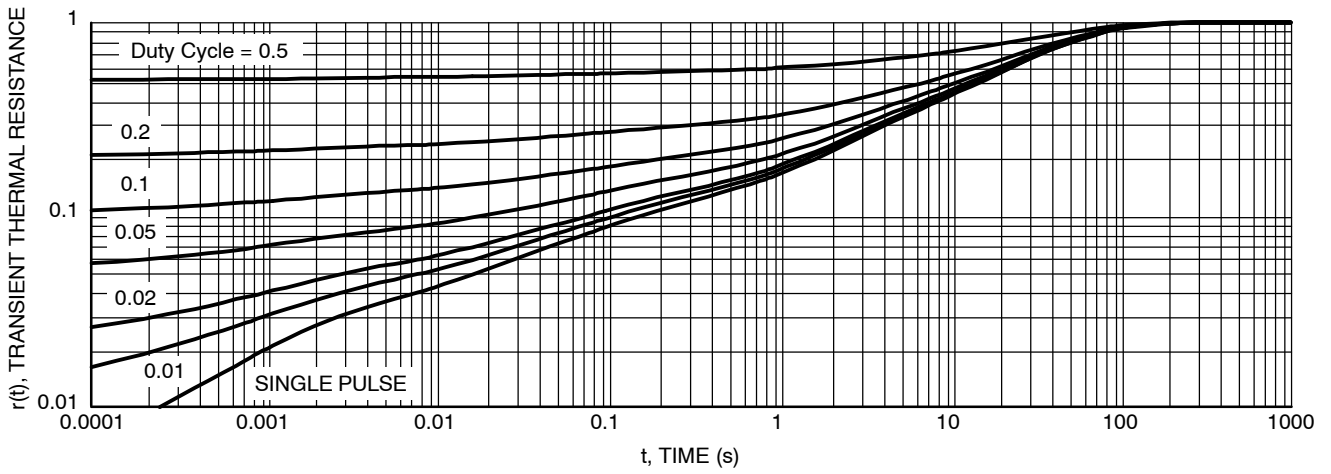


**Figure 12. Single Pulse Maximum Power Dissipation**

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**Figure 13. Maximum Rated Forward Biased Safe Operating Area**

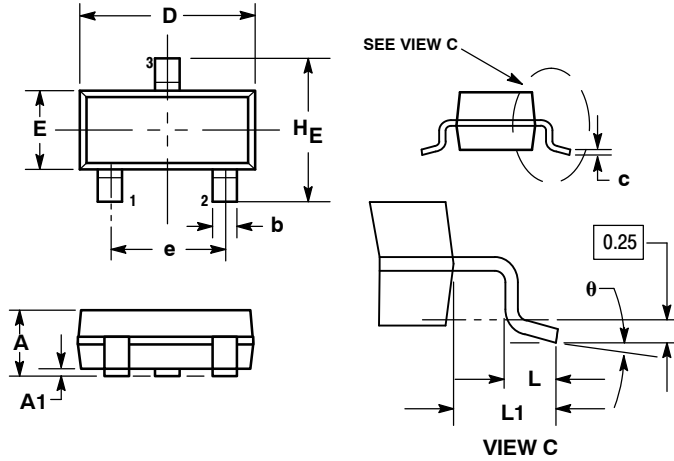


**Figure 14. Thermal Response**

# NTR3162P

## PACKAGE DIMENSIONS

### SOT-23 (TO-236) CASE 318-08 ISSUE AN

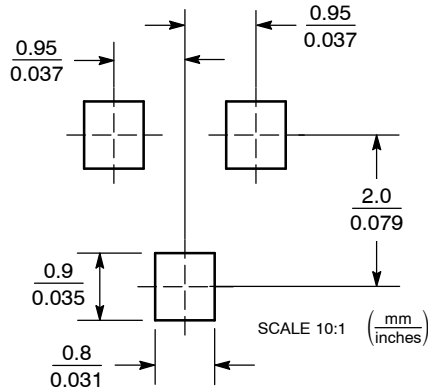


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
  4. 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104

- STYLE 21:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

### SOLDERING FOOTPRINT



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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