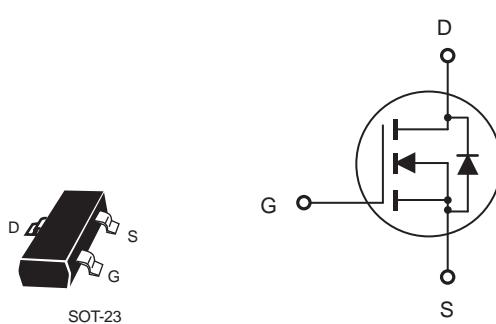


N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- 30V, 4.8A, $R_{DS(ON)} = 34m\Omega$ @ $V_{GS} = 10V$.
 $R_{DS(ON)} = 50m\Omega$ @ $V_{GS} = 4.5V$.
- High dense cell design for extremely low $R_{DS(ON)}$.
- Lead free product is acquired.
- Rugged and reliable.
- SOT-23 package.



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	4.8	A
Drain Current-Pulsed ^a	I_{DM}	20	A
Maximum Power Dissipation	P_D	1.25	W
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient ^b	$R_{\theta JA}$	100	$^\circ C/W$



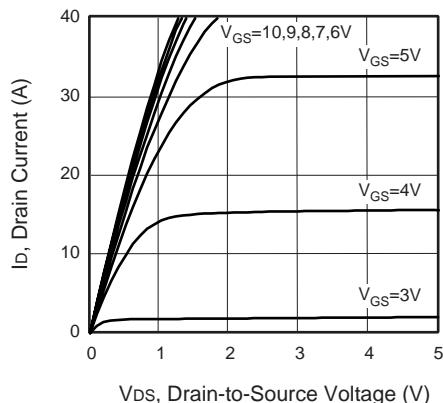
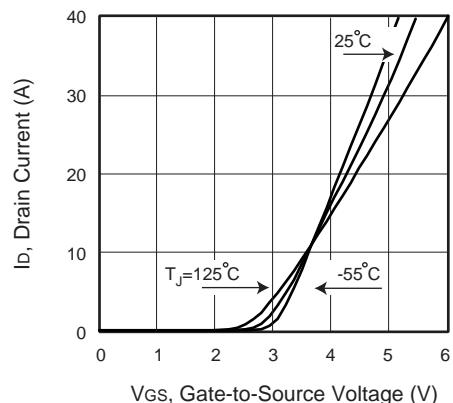
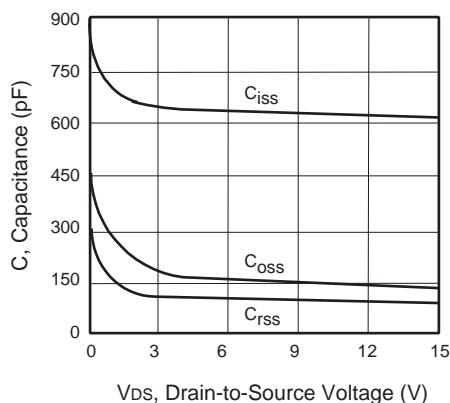
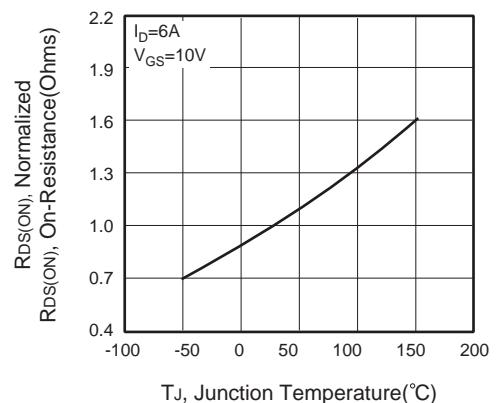
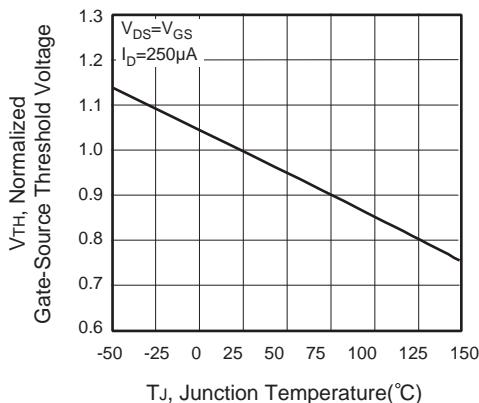
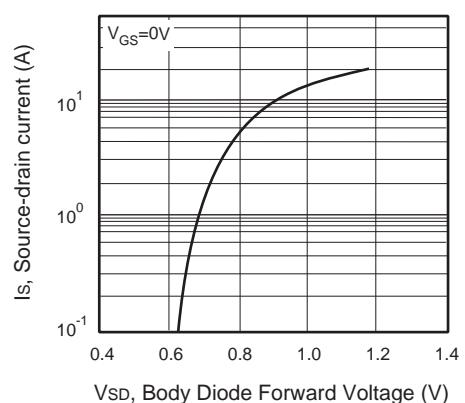
CES2316

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 30\text{V}, V_{\text{GS}} = 0\text{V}$		1		μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{\text{GS}} = 20\text{V}, V_{\text{DS}} = 0\text{V}$		100		nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{\text{GS}} = 20\text{V}, V_{\text{DS}} = 0\text{V}$		-100		nA
On Characteristics						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250\mu\text{A}$	1.0		3.0	V
Static Drain-Source On-Resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}} = 10\text{V}, I_D = 6\text{A}$		27	34	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 4.9\text{A}$		36	50	$\text{m}\Omega$
Dynamic Characteristics^d						
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 15\text{V}, I_D = 6\text{A}$		8		S
Input Capacitance	C_{iss}	$V_{\text{DS}} = 15\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		610		pF
Output Capacitance	C_{oss}			145		pF
Reverse Transfer Capacitance	C_{rss}			95		pF
Switching Characteristics^d						
Turn-On Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}} = 15\text{V}, I_D = 5.5\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 3\Omega$		9	20	ns
Turn-On Rise Time	t_r			3	8	ns
Turn-Off Delay Time	$t_{\text{d(off)}}$			24	50	ns
Turn-Off Fall Time	t_f			4	10	ns
Total Gate Charge	Q_g	$V_{\text{DS}} = 15\text{V}, I_D = 6\text{A}, V_{\text{GS}} = 10\text{V}$		12.3	16	nC
Gate-Source Charge	Q_{gs}			1.5		nC
Gate-Drain Charge	Q_{gd}			2.5		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^b	I_S				1.7	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{\text{GS}} = 0\text{V}, I_S = 1.7\text{A}$			1.2	V

Notes :

- a.Repetitive Rating : Pulse width limited by maximum junction temperature.
- b.Surface Mounted on FR4 Board, $t \leq 5 \text{ sec}$.
- c.Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- d.Guaranteed by design, not subject to production testing.

**Figure 1. Output Characteristics****Figure 2. Transfer Characteristics****Figure 3. Capacitance****Figure 4. On-Resistance Variation with Temperature****Figure 5. Gate Threshold Variation with Temperature****Figure 6. Body Diode Forward Voltage Variation with Source Current**

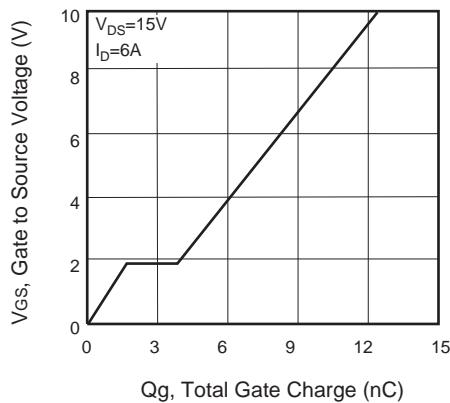


Figure 7. Gate Charge

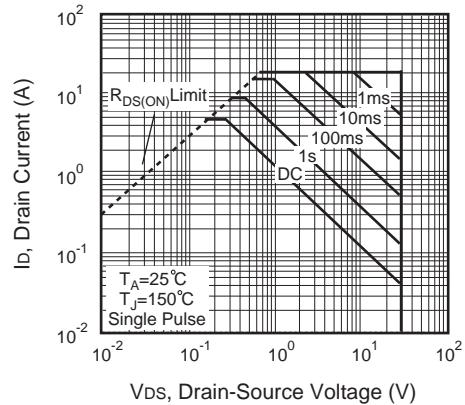


Figure 8. Maximum Safe Operating Area

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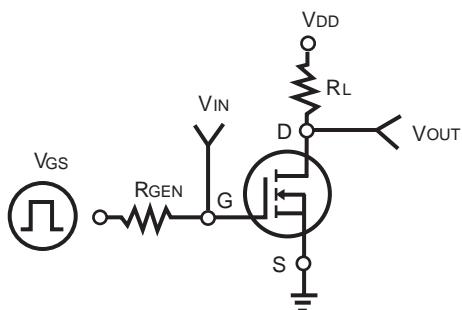


Figure 9. Switching Test Circuit

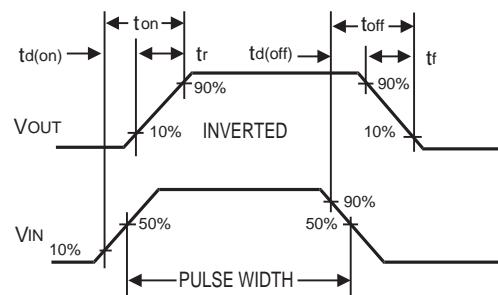


Figure 10. Switching Waveforms

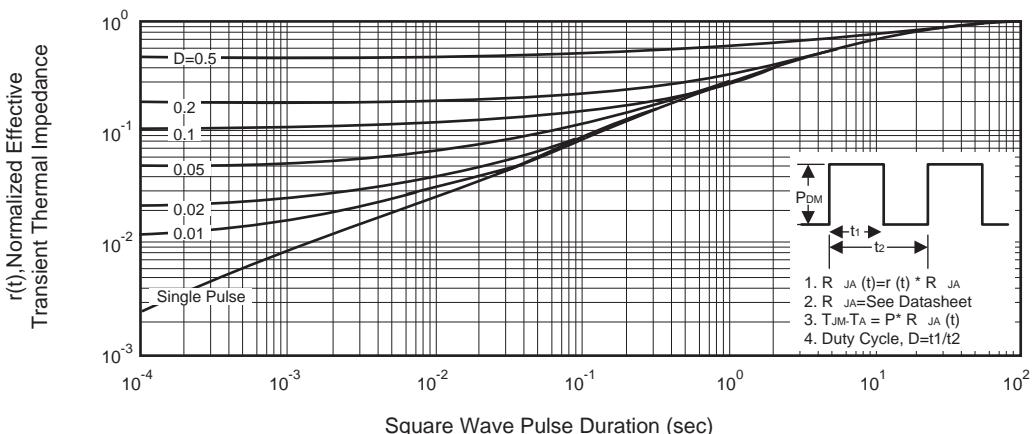


Figure 11. Normalized Thermal Transient Impedance Curve