For Home Electronics and Security Devices Camera Image Processor Series

Camera Image Processor with ADPCM / MIDI / MP3 / AAC / HE-AAC Audio

BU6569GVW

No.09061EAT04

●Description

BU6569GVW is a camera image processor with ADPCM/MIDI/MP3/AAC/HE-AAC Audio.

●Features

1)Built-in Camera Module Interface

UXGA size (1600×1200) for input of image data up to 7.5 fps, SXGA size (1280×1024) for input of image data up to 15fps and VGA size (640×480) for input of image data up to 30fps (zooming function available).
Input data format for YUV=4:2:2, RGB=4:4:4 (8 bits for each RGB).
Filter processing (image processing) to input images (2 gradations / gray scale / sepia / emboss / edge enhancement / negative).
Multi-step size reduction down to 1/16 in X- and Y-direction possible, cutting out into an arbitrary size after resizing.
Cut images to be stored into an arbitrary position in frame memory in YUV=4:2:2 format or RGB=5:6:5 format (16bit/pixel).

2) Built-in frame memory / JPEG code memory

Built in image frame memory (160KB to store 1 frame of 320×240@16bit/pixel).
Data to be stored into image frame memory in YUV=4:2:2 format or RGB=5:6:5 format (16bit/pixel).
An arbitrary position of frame memory to be updated to camera image according to mask frame memory.
Mask data to be stored into mask frame memory in 1bit/2pixels in YUV=4:2:2 format or 1bit/1pixels in RGB=5:6:5 format.
Rectangular writing function and rectangular reading function as transparent color to image frame memory.
Frame memory is usable as JPEG code memory (192KB) to store JPEG compressed images.
Frame memory is usable as a ring buffer for JPEG code of 192KB or more.

3) Built-in LCD controller interface

Built-in input/output interface which type is CPU I/F, to LCD controller
For display colors of 262144 colors / 65536 colors / 4096 colors.
Up to 2 LCD module controllers, MAIN and SUB, controllable.
Arbitrary rectangular selection in frame memory to be transferred to LCD controller.
Multi-step scaling process in the range of 1/4× to 2× in X- and Y-direction is available to display images from frame memory to the LCD.

4) Extended overlay function

Supporting overlay of icon-data up to two icons with LCD data transfer.
Icon-data corresponding to 65536 display colors. Possible to setting transparent colors.

5) Built-in TV encoder interface

Connection to ROHM-made BU9972GU or BU9969KN. Optional rectangular area of frame memory transferable to TV encoder IC. Multi-step scaling process in the range of 1× to 8× in X- and Y-direction is available for display images from frame memory to the TV encoder IC.

6) Built-in JPEG CODEC

ISO/IEC10918 conforming base line method.

・Compression

For YUV=4:2:2 format only.

Quantization table selectable from 32 built-in tables.

・Decompression

For YUV=4:4:4, 4:2:2(horizontal sub-sampling), 4:2:0, 4:1:1(horizontal sub-sampling), and gray scale.

7) Built-in HOST CPU interface

Adaptable to 16bit bus interface.

Read/Write access to/from frame memory.

Read/Write access to/from internal registers (Indirect access with a index register as the address).

Read/Write access to/from the LCD controller: Parallel/Serial (Direct access available via the LCD interface).

8) Built-in USB interface

USB 2.0 FS adaptable to mass storage class.

9) Built-in NAND Flash memory interface

Adaptable to 8bit and 16bit width for data bus.

ECC calculation by BU6569GVW.

10) Built-in SD card interface

Built-in host controller block of SD card interface, MMC interface.

11) AAC Decode

Supporting Advanced Audio Coding, Low complexity (AAC-LC)

Supporting High Efficiency Advanced Audio Coding (HE-AAC)

12) MP3 Decode

ISO/IEC 11172-3 (32, 44.1 or 48 KHz)

13) Melody source

Simultaneous generation of up to 64 polyphonic tones out of a tone palette of 128 sounds plus 47 drum set sounds, 15 electric drum set sounds, and 32 effect sounds. Up to 8 user customized sound can be used to create original sounds.

Supporting 12-bit pitch bending and modulation support.

Plays up to four songs simultaneously and supports real-time modification of tempo, key, volume, and pan pot.

14) ADPCM CODEC

Built-in ADPCM decoder/PCM player (2 channels), enables mixing with melody.

Built-in ADPCM encoder/PCM recorder (1 channel).

15) IIS, PCM interface

Digital input

・IIS interface (IIS, Standard Left Justified format, and Standard Right Justified format)

・PCM interface (G711.1 u-Law, G711.1 A-Law, Linear (negative number is expressed as 2's-complement.))

Digital output

・IIS interface (IIS, Standard Left Justified format)

16) Stereo DAC block

Built-in a stereo digital-analog converter.

The DAC block's dynamic range is 1.98 Vpp (typ.)

LPF is included as a smoothing filter subsequent to DAC output, which can eliminate the high-frequency components of the generated analog waveform.

17) Auto Play

AAC/HE-AAC/MP3 music can be played automatically in SD card or Flash memory of 512B/page and 2KB/page by using auto play file list (link information of page address) written into Play List RAM by HOST CPU.

18) Clock generation, power management function

Two oscillation circuits configuration by XIN1, 2 and XOUT1, 2 terminals, or clock input available from the XIN1, 2 terminal. Built-in two PLL circuits enable clock multiplication.

Clock control of BU6569GVW inside in unit of block (suspend mode available.)

∗ Data is prepared separately about each register setup. Please refer to the Development Scheme on page 14.

System1 (VDDIO1)	P2-P6(D8-D4),P8-P27(D3-D0,ADVB,CSB, WRB,RDB,INT,RESETB,LED0,VIB0,DIGLR, DIGCK,DACMCK,DIGDIN,DIGDOUT,FSYNC, PCMDIN,DCLK) ,P112-P120(A2,A1,D15-D9)
System 2 (VDDIO2)	P42-P43(SD_CLK,SD_CMD),P45-P61(SD_DAT0,FL_CEB,FL_RB,LCDCS1B, LCDCS2B,LCDWRB,LCDRDB,LCDA0,TEST,LCDD0-LCDD7), P63-P72(LCDD8-LCDD17),P74-P80(CAMRST,SDA,SDC,CAMCKI,CAMCKO,CAMVS,CAMHS), P82-P89(CAMD0-CAMD7),P92-P102(TE_VSYNC, TE_HSYNC,TE_PIXCLK,TED0-TED7)
System 3 (VDDIO3)	P37-P39(USB_DM,USB_DP,USB_RDY)
System 4 (VDDIO4)	P105-P109(XIN1,XOUT1,PLL_FILTER,XIN2,XOUT2)
System 5 (AVDD)	P29-P30(L_OUT,R_OUT),P34-P35(VREF,MONO_OUT)

●Application

Security camera, Intercom with camera, Drive recorder and Web camera etc.

●Lineup

Parameter	Power source voltage IO1:HOSTI/F IO2:Camera, LCD	Camera interface	HOST CPU interface	LCD interface	Codec	[Image] / [Sound /Music]	Multimedia interface	Package
BU6569GVW	1.7-3.6V(VDDIO1) 2.7-3.6V(VDDIO2) *1 3.0-3.6V(VDDUSB) *2 1.45-1.55V(VDD Core)	Supported up to 2M pixels. (1600×1200)	16bit bus 80 systems CPU Interface	Supported up to QVGA (320×240)	2M pixels JPEG Codec Motion-JPEG		USB2.0 FS I/F, SDC / MMC I/F, TV encoder I/F, NAND Flash, Memory I/F	SBGA120W080
					64MIDI/MP3/AAC / HE-AAC decode ADPCM Codec			

*1 VDDIO2, VDDIO4, and AVDD can be used by the same source voltage.

*2 VDDUSB is the same as VDDIO3.

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Applied power source voltage 1 (IO1)	VDDIO1	-0.3～+4.2	V
Applied power source voltage 2 (IO2)	VDDIO2	-0.3～+4.2	V
Applied power source voltage 3 (USB)	VDDIO3	-0.3～+4.2	V
Applied power source voltage 4 (PLL)	VDDIO4	-0.3～+4.2	V
Applied power source voltage 5 (DAC)	AVDD	-0.3～+4.2	V
Applied power source voltage 6 (CORE)	VDD	-0.3～+2.1	V
Input voltage	VIN	-0.3～VDDIO+0.3	V
Storage temperature range	Tstg	-40～+150	℃
Power dissipation	PD	380	mW

∗ Power dissipation is IC only.
In the case exceeding 25ºC, 3.8mW should be reduced at the rating 1ºC.

●Recommended operating range

Parameter	Symbol	Rating	Unit
Applied power source voltage 1 (IO1)	VDDIO1	1.70～3.60 (Typ:3.30V)	V
Applied power source voltage 2 (IO2)	VDDIO2	2.70～3.60 (Typ: 3.30V)	V
Applied power source voltage 3 (USB)	VDDIO3	3.00～3.60 (Typ:3.30V)	V
Applied power source voltage 4 (PLL)	VDDIO4	2.70～3.60 (Typ: 3.30V)	V
Applied power source voltage 5 (DAC)	AVDD	2.70～3.60 (Typ: 3.30V)	V
Applied power source voltage 6 (CORE)	VDD	1.45～1.55 (Typ:1.50V)	V
Input voltage range	VIN	0～VDDIO	V
Operating temperature range	Topr	-30～+85	℃

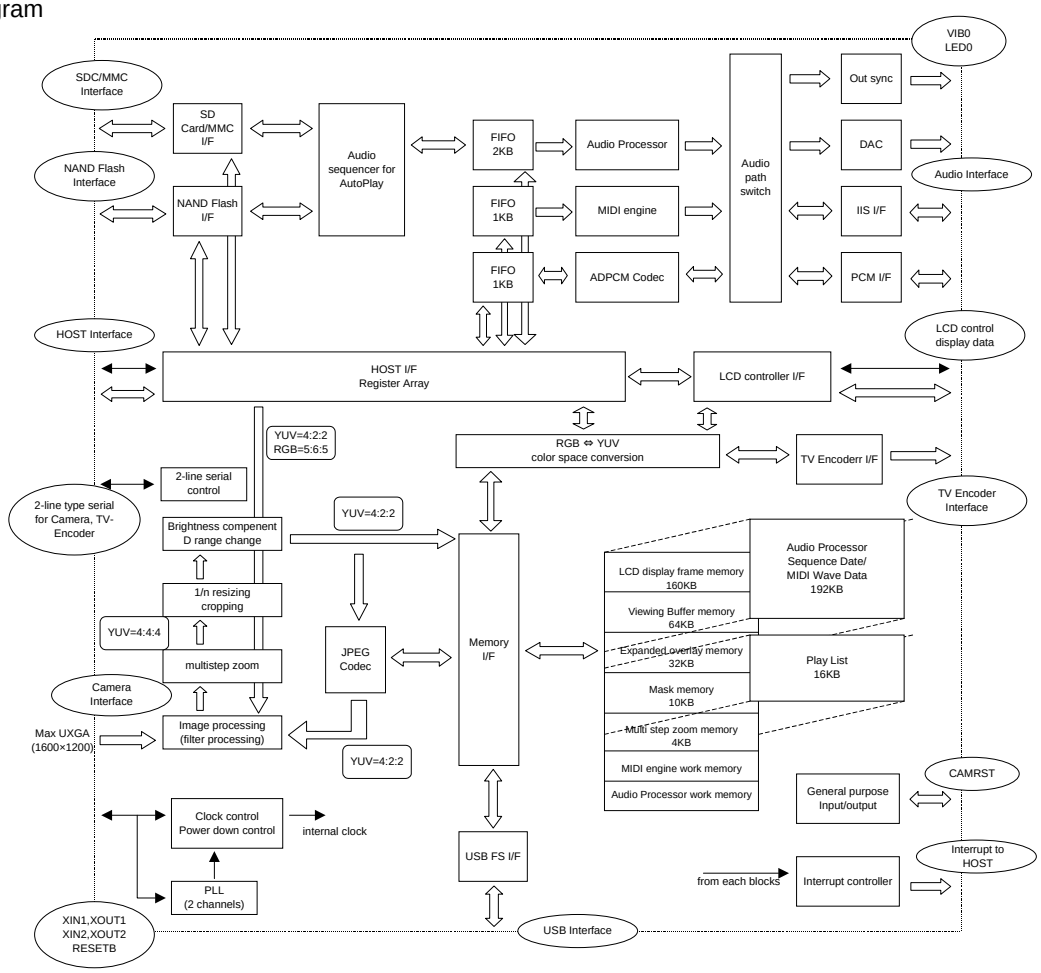
∗ Please supply power source in order of VDD→VDDIO.
（VDDIO1→ VDDIO2→ VDDIO3→ VDDIO4→ ADD）

●Electric characteristics

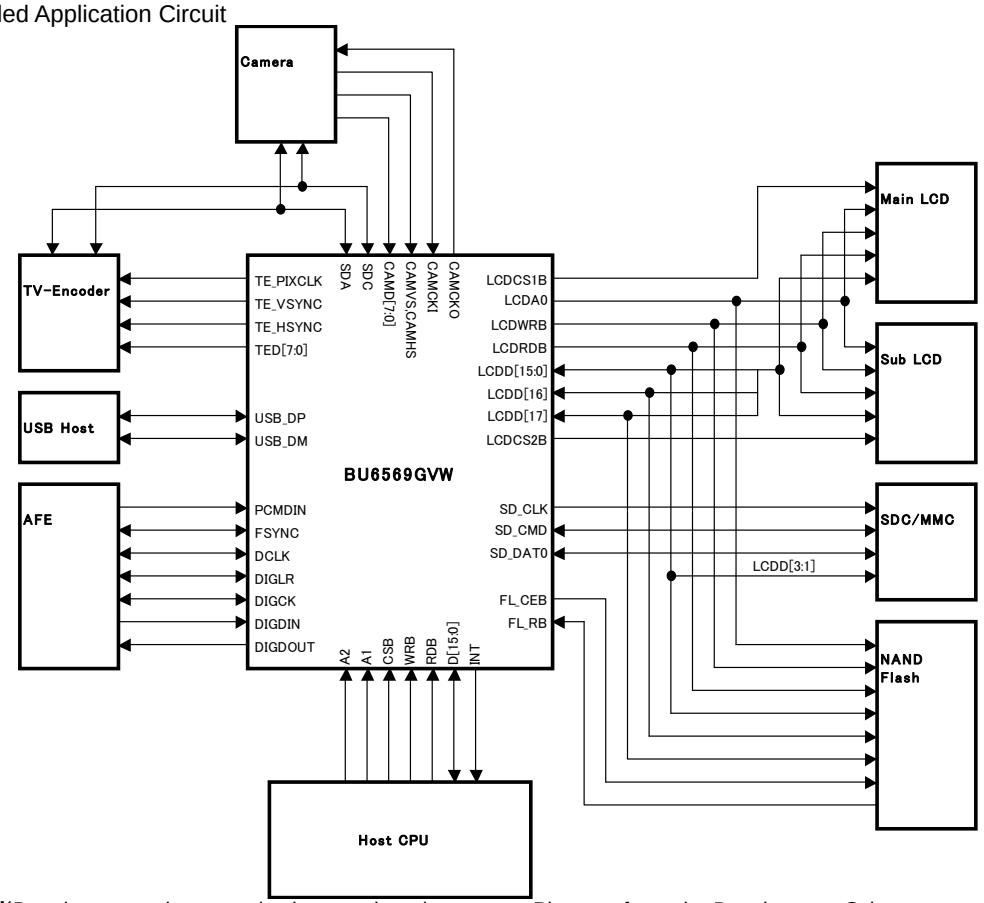
（Unless otherwise specified, VDD=1.50V,VDDIO1,2,3,4,AVDD=3.30V,GND=0V,Ta=25℃,
fXIN1=12.0MHz,fXIN2=12.0MHz,fAUDIO=74.0MHz,fIMAGE=52.0MHz）

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Input frequency 1	fXIN1	2.688	-	26.0	MHz	XIN1 (Duty 50±10%), at PLL ON
Input frequency 2	fXIN2	10.0	-	30.0	MHz	XIN2 (Duty 50±10%), at PLL ON
Internal clock frequency 1	fIMAGE	-	-	52.0	MHz	At PLL ON
Internal clock frequency 2	fAUDIO	-	-	74.0	MHz	At PLL ON
Operating consumption current 1	IDD1	-	12.8	-	mA	At Preview operating
Operating consumption current 2	IDD2	-	17.3	-	mA	At AAC decode operating （at 44kfs, Auto Play from Flash）
Static consumption current	IDDst	-	-	150	μA	At suspend mode setting
Input "H" current 1	IIH1	-10	-	10	μA	VIH=VDDIO1,2,3,4
Input "H" current 2	IIH2	25	50	100	μA	Pull-down terminal, VIH=VDDIO2
Input "H" current 3	IIH3	-10	-	10	μA	Pull-up terminal, VIH=VDDIO2
Input "L" current 1	IIL1	-10	-	10	μA	VIL=GND
Input "L" current 2	IIL2	-10	-	10	μA	Pull-down terminal, VIL=GND
Input "L" current 3	IIL3	-160	-80	-25	μA	Pull-up terminal, VIL=GND
Input "H" voltage1	VIH1	VDDIO*0.8	-	VDDIO+0.3	V	Normal type input
Input "L" voltage 1	VIL1	-0.3	-	VDDIO*0.2	V	Normal type input
Input "H" voltage 2	VIH2	VDDIO*0.85	-	VDDIO+0.3	V	Hysteresis input VDDIO1(CSB,WRB,RDB) VDDIO4(XIN1,XIN2)
Input "L" voltage 2	VIL2	-0.3	-	VDDIO*0.15	V	
Hysteresis voltage width	Vhys	-	0.9	-	V	
Input "H" voltage3	VIH3	2.0	-	-	V	USB_DP,USB_DM Single-ended input voltage level
Input "L" voltage 3	VIL3	-	-	0.8	V	
Differential input sensitivity	VDI	0.2	-	-	V	ABS(VUSB_DP-VUSB_DM)
Differential common mode range	VCM	0.8	-	2.5	V	Include VDI range
Output "H" voltage 1	VOH1	VDDIO-0.4	-	VDDIO	V	IOH1=-1.0mA(DC), Normal type output (Including output mode of I/O terminal)
Output "L" voltage 1	VOL1	0.0	-	0.4	V	IOL1=1.0mA(DC), Normal type output (Including output mode of I/O terminal)
Output "H" voltage 2	VOH2	VDDIO-0.4	-	VDDIO	V	IOH1=-2.0mA(DC), CAMCKO
Output "L" voltage 2	VOL2	0.0	-	0.4	V	IOL1=2.0mA(DC), CAMCKO
Output "H" voltage 3	VOH3	VDDIO-0.4	-	VDDIO	V	IOH1=-4.0mA(DC), SD_CLK
Output "L" voltage 3	VOL3	0.0	-	0.4	V	IOL1=4.0mA(DC), SD_CLK
Output "H" voltage 4	VOH4	2.8	-	VDDIO	V	IOH1=-2.53mA(DC), USB_DP,USB_DM
Output "L" voltage 4	VOL4	0.0	-	0.3	V	IOL1=2.53mA(DC), USB_DP,USB_DM
VREF PIN voltage	VVREF	0.475*AVDD	0.5*AVDD	0.525*AVDD	V	IOUT=0A(no load),VREF
Analog output voltage range	VAOUT	0.47*AVDD	0.5*AVDD	0.53*AVDD	V	IOUT=0A(no load). In Silence
Analog amplitude	VAMP	-	0.6*AVDD	-	VPP	Theoretical Value of Dynamic range
Output load for analog output	RAOUT	10	-	-	KOhm	R_OUT,L_OUT,MONO_OUT

●Block Diagram



●Recommended Application Circuit



※Data is prepared separately about each register setup. Please refer to the Development Scheme on page 14.

●Terminal functions

PIN No.	Land No.	PIN Name	In/Out /Analog	Active Level	Init	Function explanation	Power source system	Function division	I/O type
1	A1	GND	-	GND	-	Digital ground	-	-	-
2	C3	D8	In/Out	DATA	In *1	Host data bus: bit 8	1	HOST	D*2
3	B2	D7	In/Out	DATA	In *1	Host data bus: bit 7	1	HOST	D*2
4	B1	D6	In/Out	DATA	In *1	Host data bus: bit 6	1	HOST	D*2
5	C2	D5	In/Out	DATA	In *1	Host data bus: bit 5	1	HOST	D*2
6	D3	D4	In/Out	DATA	In *1	Host data bus: bit 4	1	HOST	D*2
7	D2	VDD	-	PWR	-	CORE power supply	-	-	-
8	D1	D3	In/Out	DATA	In *1	Host data bus: bit 3	1	HOST	D*2
9	E3	D2	In/Out	DATA	In *1	Host data bus: bit 2	1	HOST	D*2
10	E2	D1	In/Out	DATA	In *1	Host data bus: bit 1	1	HOST	D*2
11	E1	D0	In/Out	DATA	In *1	Host data bus: bit 0	1	HOST	D*2
12	E5	ADVB	In	Low	-	Address latch enable	1	HOST	G
13	E4	CSB	In	Low	-	Chip select signal	1	HOST	G*3
14	F2	WRB	In	Low	-	Write enable signal	1	HOST	G
15	F1	RDB	In	Low	-	Read enable signal	1	HOST	G
16	F5	INT	Out	*	Low	Interrupt signal	1	HOST	C
17	F4	RESETB	In	Low	-	System reset signal	1	SYS	B
18	F3	LED0	Out	-	Low	LED control signal	1	SYS	D*4
19	G1	VIB0	Out	-	Low	Vibrator control signal	1	SYS	D*4
20	G2	DIGLR	In/Out	-	In	Sampling clock for audio data	1	AUD	D*5
21	G3	DIGCK	In/Out	CLK	In	Bit clock for audio data (64Fs/32Fs)	1	AUD	D*5
22	G4	DACMCK	In/Out	CLK	Out/Low	Master clock for audio data(256Fs/384Fs)	1	AUD	D*5
23	H1	DIGDIN	In	DATA	-	Audio data input	1	AUD	D*6
24	H3	DIGDOUT	Out	DATA	-	Audio data output	1	AUD	D*7
25	J1	FSYNC	In/Out	-	In	Sampling clock for PCM data	1	AUD	D*5
26	J2	PCMDIN	In	DATA	-	PCM data input	1	AUD	D*6
27	H4	DCLK	In/Out	CLK	In	Bit clock for PCM data	1	AUD	D*5
28	H2	VDDIO1	-	PWR	-	Digital I/O power supply (System 1)	1	-	-
29	K1	L_OUT	Analog	DATA	-	Stereo L-channel analog output *12, *13	A	AUD	I
30	G5	R_OUT	Analog	DATA	-	Stereo R-channel analog output *12, *13	A	AUD	I
31	L1	AVSS	-	GND	-	Analog ground	A	-	-
32	L2	AVDD	-	PWR	-	Analog power supply	A	-	-
33	K3	AVSS	-	GND	-	Analog ground	A	-	-
34	H5	VREF	Analog	-	-	AC (signal) GND Be sure to connect a 1-µF bypass capacitor between VREF and AVSS.	A	AUD	J
35	K2	MONO_OUT	Analog	DATA	-	Monaural analog output *13, *14	A	AUD	I
36	J3	VDDIO3	-	PWR	-	USB power supply (System 3)	3	-	-
37	K4	USB_DM	Analog	-	In	UBS D- pin	3	USB	H
38	L3	USB_DP	Analog	-	In	USB D+ pin	3	USB	H
39	F6	USB_RDY	In/Out	-	Out/Low	I/O port for USB intialization	3	USB	D*3
40	G6	GND	-	GND	-	Digital ground	-	-	-
41	J4	VDDIO2	-	PWR	-	Digital I/O power supply (System 2)	2	-	-
42	L4	SD_CLK	Out	CLK	-	SD card clock output	2	SD	C
43	K5	SD_CMD	In/Out	DATA	Out/Low	SD card command input/output	2	SD	D*3
44	H6	VDD	-	PWR	-	Core power supply	-	-	-
45	J5	SD_DAT0	In/Out	DATA	Out/Low	SD card data: bit0	2	SD	D*3
46	L5	FL_CEB	Out	Low	-	NAND Flash chip enable	2	FL	D*4
47	K6	FL_RB	In	Low	-	NAND Flash Ready/Busy	2	FL	G*3
48	F7	LCDCS1B	Out	Low	-	LCD controller chip select signal 1	2	LCD	D*7
49	G7	LCDCS2B	Out	Low	High	LCD controller chip select signal 2	2	LCD	D*7
50	L6	LCDWRB / FL_WEB	Out	Low	-	LCD controller write enable signal / NAND Flash write enable signal	2	LCD / FL	D*7
51	H7	LCDRDB / FL_REB	Out	Low	-	LCD controller read enable signal / NAND Flash read enable signal	2	LCD / FL	D*7
52	K7	LCDA0 / FL_ALE	Out	*	-	LCD controller command parameter identification signal/ NAND Flash address latch enable signal	2	LCD / FL	D*7
53	J6	TEST	In	Low	-	Test mode terminal (Connect to GND.)	2	SYS	A
54	L7	LCDD0 / FL_D0	In/Out	DATA	Out/Low	LCD controller data bus: bit 0 / NAND Flash data bus: bit 0	2	LCD / FL	D*3
55	F8	LCDD1 / FL_D1 / SD_DAT1	In/Out	DATA	Out/Low	LCD controller data bus: bit 1 / NAND Flash data bus: bit 1 / SD card IF bus: bit 1	2	LCD / FL / SD	D*3

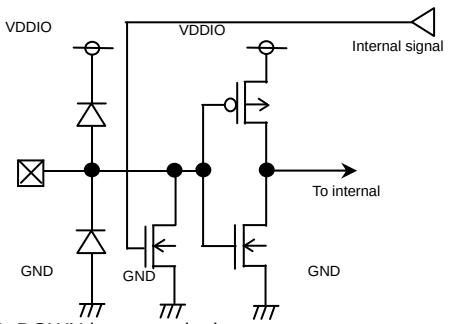
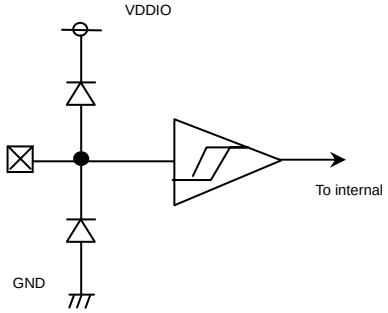
PIN No.	Land No.	PIN Name	In/Out /Analog	Active Level	Init	Function explanation	Power source system	Function division	I/O type
56	G8	LCDD2 / FL_D2 / SD_DAT2	In/Out	DATA	Out/Low	LCD controller data bus: bit 2 / NAND Flash data bus: bit 2 / SD card IF bus: bit 2	2	LCD / FL / SD	D*3
57	L8	LCDD3 / FL_D3 / SD_DAT3	In/Out	DATA	Out/Low	LCD controller data bus: bit 3 / NAND Flash data bus: bit 3 / SD card IF bus: bit 3	2	LCD / FL / SD	D*3
58	K8	LCDD4 / FL_D4	In/Out	DATA	Out/Low	LCD controller data bus: bit 4 / NAND Flash data bus: bit 4	2	LCD / FL	D*3
59	J7	LCDD5 / FL_D5	In/Out	DATA	Out/Low	LCD controller data bus: bit 5 / NAND Flash data bus: bit 5	2	LCD / FL	D*3
60	L9	LCDD6 / FL_D6	In/Out	DATA	Out/Low	LCD controller data bus: bit 6 / NAND Flash data bus: bit 6	2	LCD / FL	D*3
61	L10	LCDD7 / FL_D7	In/Out	DATA	Out/Low	LCD controller data bus: bit 7 / NAND Flash data bus: bit 7	2	LCD / FL	D*3
62	L11	GND	-	GND	-	Digital ground	-	-	-
63	H8	LCDD8 / FL_D8	In/Out	DATA	Out/Low	LCD controller data bus: bit 8 / NAND Flash data bus: bit 8	2	LCD / FL	D*3
64	K9	LCDD9 / FL_D9	In/Out	DATA	Out/Low	LCD controller data bus: bit 9 / NAND Flash data bus: bit 9	2	LCD / FL	D*3
65	K10	LCDD10 / FL_D10	In/Out	DATA	Out/Low	LCD controller data bus: bit 10 / NAND Flash data bus: bit 10	2	LCD / FL	D*3
66	K11	LCDD11 / FL_D11	In/Out	DATA	Out/Low	LCD controller data bus: bit 11 / NAND Flash data bus: bit 11	2	LCD / FL	D*3
67	J8	LCDD12 / FL_D12	In/Out	DATA	Out/Low	LCD controller data bus: bit 12 / NAND Flash data bus: bit 12	2	LCD / FL	D*3
68	J9	LCDD13 / FL_D13	In/Out	DATA	Out/Low	LCD controller data bus: bit 13 / NAND Flash data bus: bit 13	2	LCD / FL	D*3
69	J11	LCDD14 / FL_D14	In/Out	DATA	Out/Low	LCD controller data bus: bit 14 / NAND Flash data bus: bit 14	2	LCD / FL	D*3
70	J10	LCDD15 / FL_D15	In/Out	DATA	Out/Low	LCD controller data bus: bit 15 / NAND Flash data bus: bit 15	2	LCD / FL	D*3
71	H9	LCDD16 / SCL / FL_WPB	In/Out	DATA / DATA / Low	Out/Low	LCD controller data bus: bit 16 / LCD serial transfer clock signal / NAND Flash write protect	2	LCD / FL	D*3
72	H10	LCDD17 / SI / FL_CLE	In/Out	DATA / CLK / High	Out/Low	LCD controller data bus: bit 17 / LCD serial transfer clock signal / NAND Flash command enable	2	LCD / FL	D*3
73	H11	VDDIO2	-	PWR	-	Digital I/O power supply (System 2)	2	-	-
74	G11	CAMRST	In/Out	DATA	Out/Low	Camera reset signal	2	CAM	D*3
75	F11	SDA	In/Out	DATA	Out/Low	two-wire serial data	2	SYS	F
76	G10	SDC	In/Out	CLK	Out/Low	two-wire serial clock	2	SYS	F
77	F10	CAMCKI	In*9	CLK	-	Camera clock input	2	CAM	A
78	E11	CAMCKO	Out	CLK	Low	Camera clock output	2	CAM	C
79	G9	CAMVS	In*9	*	-	Camera vertical timing signal	2	CAM	A
80	F9	CAMHS	In*9	*	-	Camera horizontal timing signal	2	CAM	A
81	D11	VDD	-	PWR	-	Core power supply	-	-	-
82	E10	CAMD0	In*9	DATA	-	Camera data input: bit 0	2	CAM	A
83	C11	CAMD1	In*9	DATA	-	Camera data input: bit 1	2	CAM	A
84	D10	CAMD2	In*9	DATA	-	Camera data input: bit 2	2	CAM	A
85	C10	CAMD3	In*9	DATA	-	Camera data input: bit 3	2	CAM	A
86	B11	CAMD4	In*9	DATA	-	Camera data input: bit 4	2	CAM	A
87	E9	CAMD5	In*9	DATA	-	Camera data input: bit 5	2	CAM	A
88	E8	CAMD6	In*9	DATA	-	Camera data input: bit 6	2	CAM	A
89	B10	CAMD7	In*9	DATA	-	Camera data input: bit 7	2	CAM	A
90	A11	GND	-	GND	-	Digital ground	-	-	-
91	A10	VDDIO2	-	PWR	-	Digital I/O power supply (System 2)	2	-	-
92	D9	TE_VSYNC	Out	Low	High	TV encoder interface Vertical sync	2	TV	D*7
93	C9	TE_HSYNC	Out	Low	High	TV encoder interface Horizontal sync	2	TV	D*7
94	B9	TE_PIXCLK	Out	CLK	Low	TV encoder interface output clock	2	TV	D*7
95	A9	TED0	Out	DATA	High	TV encoder interface data: bit 0	2	TV	D*7
96	D8	TED1	Out	DATA	Low	TV encoder interface data: bit 1	2	TV	D*7
97	C8	TED2	Out	DATA	Low	TV encoder interface data: bit 2	2	TV	D*7
98	A8	TED3	Out	DATA	Low	TV encoder interface data: bit 3	2	TV	D*7
99	B8	TED4	Out	DATA	Low	TV encoder interface data: bit 4	2	TV	D*7
100	A7	TED5	Out	DATA	Low	TV encoder interface data: bit 5	2	TV	D*7
101	E7	TED6	Out	DATA	Low	TV encoder interface data: bit 6	2	TV	D*7
102	D7	TED7	Out	DATA	Low	TV encoder interface data: bit 7	2	TV	D*7
103	C7	GND	-	GND	-	Digital ground	-	-	-

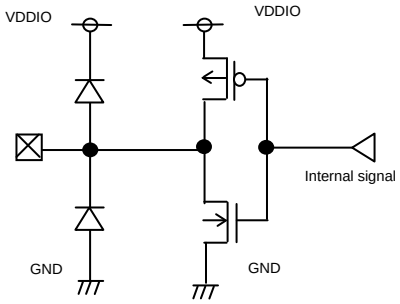
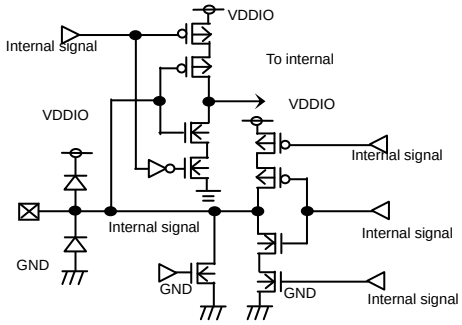
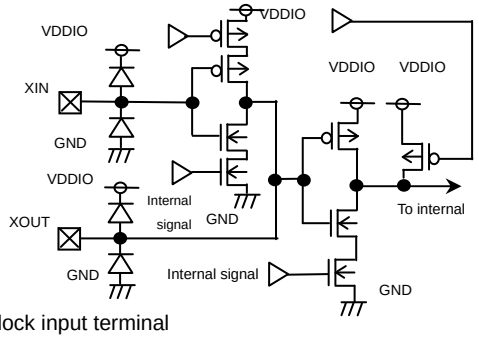
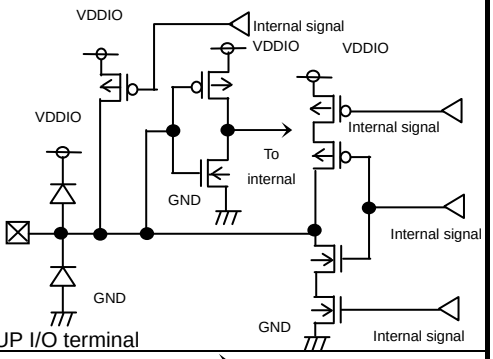
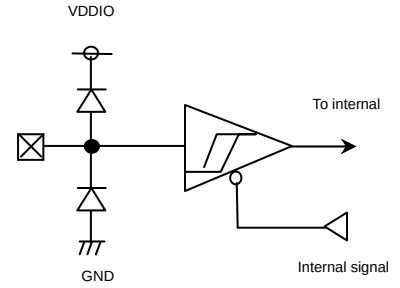
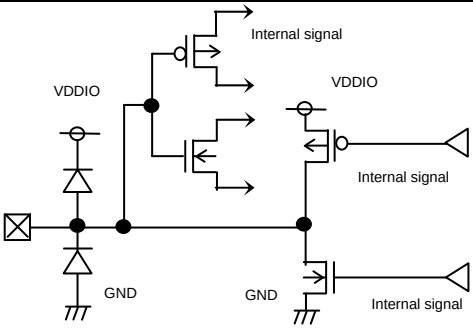
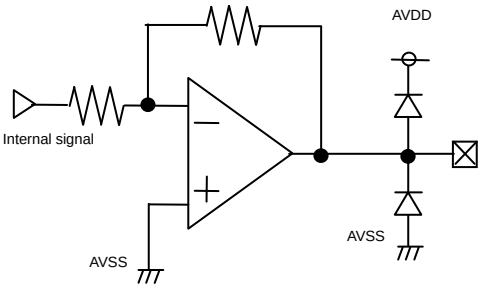
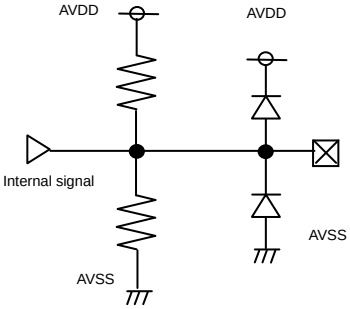
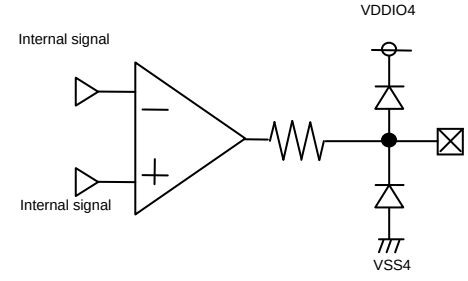
PIN No.	Land No.	PIN Name	In/Out /Analog	Active Level	Init	Function explanation	Power source system	Function division	I/O type
104	A6	VDDIO4	-	PWR	-	PLL power supply (System 4)	4	-	-
105	B7	XIN1	In	CLK	In	Oscilator input1 *10	4	CLK	E,G*11
106	B6	XOUT1	Out	CLK	High	Oscilator output1	4	CLK	E
107	A5	PLL_FILTER	Analog	-	-	Be sure to connect a 2200-μF bypass capacitor between PLL_FILTER and VSS4.	4	CLK	K
108	C6	XIN2	In	CLK	In	Oscilator input2 *10	4	CLK	E,G *11
109	D6	XOUT2	Out	CLK	High	Oscilator output2	4	CLK	E
110	E6	VSS4	-	GND	-	PLL ground	4	-	-
111	A4	VDDIO1	-	PWR	-	Digital I/O power supply (System 1)	1	-	-
112	B5	A2	In	DATA	In	Host address bus: bit 2	1	HOST	D*8
113	B3	A1	In	DATA	In	Host address bus: bit 1	1	HOST	D*8
114	C5	D15	In/Out	DATA	In *1	Host data bus: bit 15	1	HOST	D*2
115	D5	D14	In/Out	DATA	In *1	Host data bus: bit 14	1	HOST	D*2
116	A3	D13	In/Out	DATA	In *1	Host data bus: bit 13	1	HOST	D*2
117	B4	D12	In/Out	DATA	In *1	Host data bus: bit 12	1	HOST	D*2
118	C4	D11	In/Out	DATA	In *1	Host data bus: bit 11	1	HOST	D*2
119	D4	D10	In/Out	DATA	In *1	Host data bus: bit 10	1	HOST	D*2
120	A2	D9	In/Out	DATA	In *1	Host data bus: bit 9	1	HOST	D*2

In the function division column, “HOST” stands for HOST IF, “SYS“→SYSTEM, “CAM“→CAMERA IF, “LCD“→LCD IF, “AUD“→Audio IF, “SD“→SD Card IF, “FL“→NAND Flash IF, “TV“→TV Encoder IF, “USB“→USB IF, and “CLK“→OSC&PLL.
In the power source system column, “1” stands for system 1 (VDDIO1), “2” for system 2 (VDDIO2), “3” for system 3 (VDDIO3), “4” for system 4 (VDDIO4), “A” for system 5 (ADD).
” ∗ ” in Active level column means active level can be changed by setting of register.
Init column is a pin state at the time of reset release.

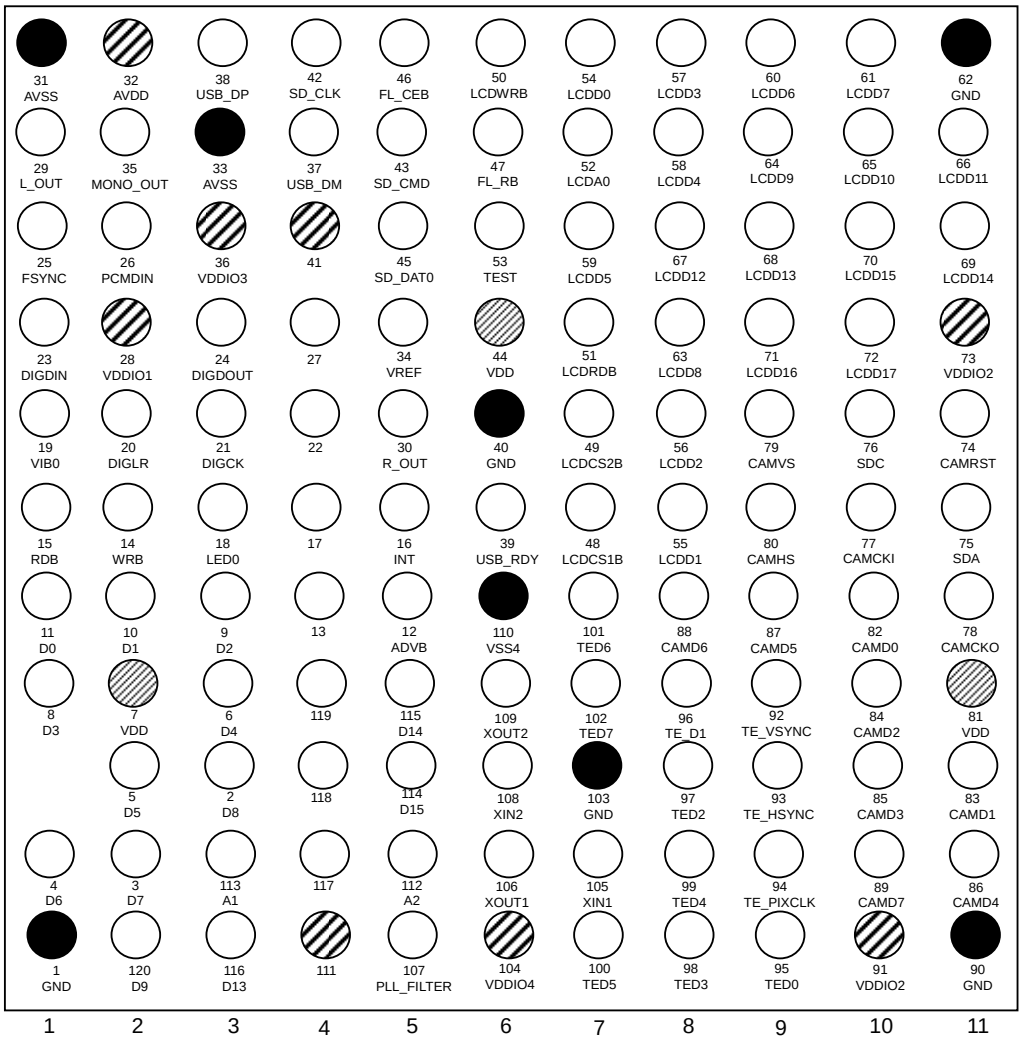
*1 : RESETB=”L”
*2 : Pull-down only a test mode.
*3 : Suspend only a test mode.
*4 : Suspend or input only a test mode.
*5 : Suspend or Pull-down only a test mode.
*6 : Suspend, Pull-down or output function only a test mode.
*7 : Suspend, Pull-down or input function only a test mode.
*8 : Output or pull-down only a test mode.
*9 : Pull-down during CAMOFF mode.
*10 : The crystal oscillation circuit does not include a return resistance, so it is needed to examine an external circuit including return resistance.
*11 : I/O type is E at oscillation mode, it is G at external clock input mode.
*12 : When not during playback, the potential approximates Vref. Hi-Z at reset.
*13 : When disable reset, standby, anout_disable or mono_disable, pop noise occurs.
*14 : This pin outputs inverted signal of (R + L) / 2, If “monaural mode” is not selected. And outputs differential signal with L_OUT, If “monaural mode” is selected.

●Equivalent Circuit Structures of input / output pins

Type	Equivalent circuit structure	Type	Equivalent circuit structure
A	 PULL-DOWN input terminal	**B**	 Hysteresis input terminal

Type	Equivalent circuit structure	Type	Equivalent circuit structure
C	 Output terminal	**D**	 Suspend, PULL-DOWN I/O terminal
E	 Clock input terminal	**F**	 PULL-UP I/O terminal
G	 Suspend, hysteresis input terminal	**H**	 USB
I	 DAC_OUT	**J**	 VREF
K	 PLL_FILTER		

● Terminal Layout



（Bottom View）

●Timing Chart

1. HOST interface timing

1.1 System timing

Table 1.1 BU6569GVW timing conditions (system)

Symbol	Details	MIN.	TYP.	MAX.	Unit	Conditions
tXIN	BU6569GVW Clock input cycle	38.5	-	372.0	ns	
tXIN2	BU6569GVW Clock input cycle 2	33.3	-	100.0	ns	
DutyXIN	BU6569GVW clock duty	45.0	50.0	55.0	%	"H" width / cycle
tSCLK	BU6569GVW SCLK clock cycle	19.2	-	-	ns	
DutySCLK	BU6569GVW SCLK clock duty	33.3	50.0	66.6	%	"H" width / cycle
tCAMCKO	Camera clock output cycle	19.2	-	-	ns	
DutyCAMCKO	Camera clock output duty	33.3	50.0	66.6	%	"H" width / cycle
tCAMCKI	Camera clock input cycle	19.2	-	-	ns	
DutyCAMCKI	Camera clock input duty	45.0	50.0	55.0	%	"H" width / cycle
tRESETB	RESETB "L" pulse width	1.0	-	-	μs	

∗ Regulation all at threshold of VDDIO×1/2

1.2 Register (including RAM via register) write timing.

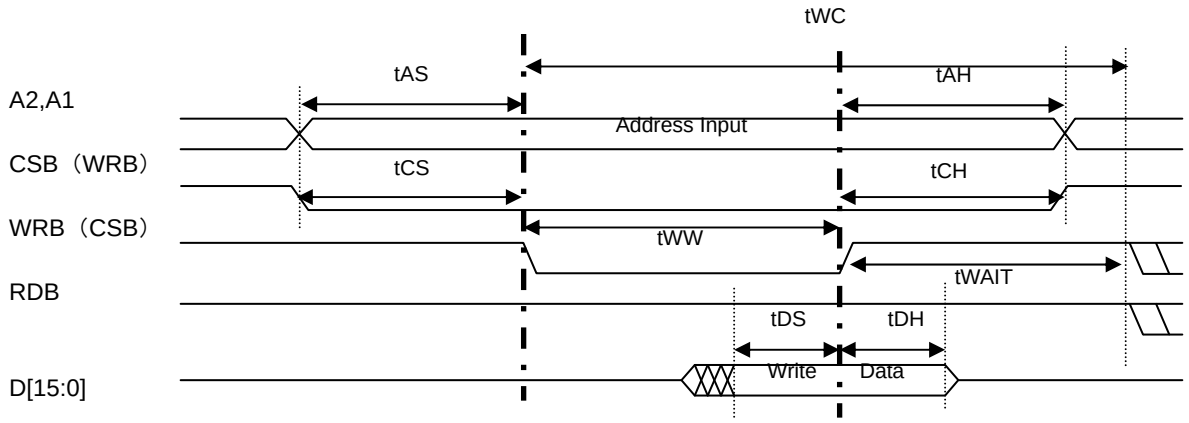


Table 1.2 BU6569GVW timing conditions（RAM, register write cycle）

Symbol	Details	MIN.	TYP.	MAX.	Unit
tWC	Write cycle time	80	-	-	ns
tAS	Address setup time before WRB(CSB) falling	-7	-	-	ns
tAH	Address hold time after WRB(CSB) rising	-1	-	-	ns
tCS	CSB(WRB) input setup time before WRB(CSB) falling	0	-	-	ns
tCH	CSB(WRB) input hold time after WRB(CSB) falling	0	-	-	ns
tWW	WRB(CSB) active time width	45	-	-	ns
tWAIT	Wait time from WRB(CSB) rising to the next WRB(CSB) or to RDB falling	5.5	-	-	ns
tDS	Data setup time before WRB(CSB) rising	40	-	-	ns
tDH	Data hold time after WRB(CSB) rising	-1	-	-	ns

∗ Regulation all at threshold of VDDIO×1/2（VDD=1.50V,VDDIO=3.30V,GND=0V,Ta=25℃）
∗ It is possible to use it with either CSB or WRB active. However, either of them must do LOW pulse operation.

1.3 Register (including RAM via register) read timing.

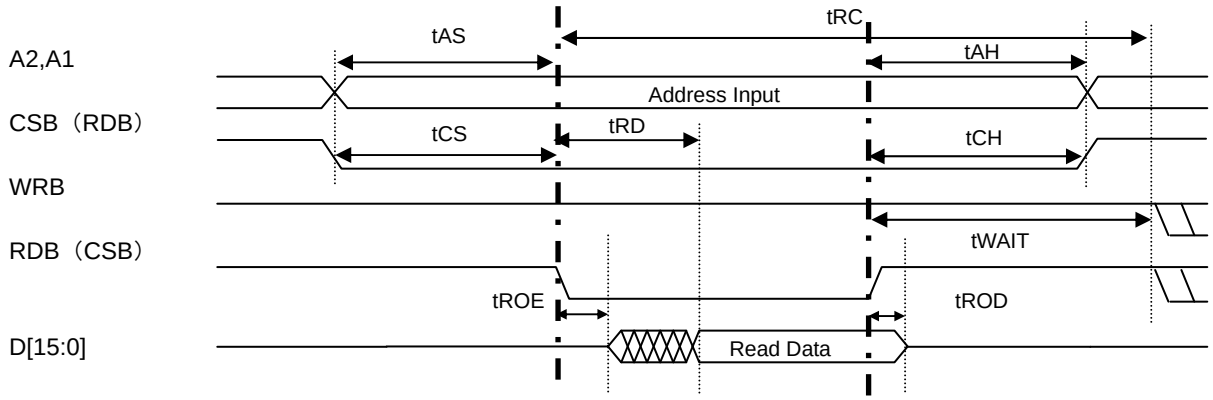


Table 1.3-1 BU6569GVW timing conditions (RAM, register read cycle)

Symbol	Details	MIN.	TYP.	MAX.	Unit
tRC	Read cycle time	110	-	-	ns
tAS	Address setup time before RDB(CSB) falling	-7	-	-	ns
tAH	Address hold time after RDB(CSB) rising	-1	-	-	ns
tCS	CSB(RDB) input setup time before RDB(CSB) falling	0	-	-	ns
tCH	CSB(RDB) input hold time after RDB(CSB) rising	0	-	-	ns
tRD	Access time after RDB(CSB) falling	-	-	70	ns
tWAIT	Wait time from RDB(CSB) falling to the next RDB(CSB) falling or to WRB falling	5.5	-	-	ns
tROE,tROD	Data output enable time after RDB(CSB) rising, Data output disable time after RDB(CSB) falling	-	-	15	ns

∗ Regulation all at threshold of VDDIO×1/2（VDD=1.50V,VDDIO=3.30V,GND=0V,Ta=25℃）
∗ It is possible to use it with either CSB or WRB active. However, either of them must do LOW pulse operation.

2. Camera Module Interface Timing

2.1. System clock and camera clock

BU6569GVW external clock input (XIN) can be divided and supplied as CAMCKO clock to camera module.
The relation between data synchronization CAMCKI clock from camera and system clock SCLK must be set in order to meet the following formula by setting of ACTSW (IDX:00D3h CLKDIV3[5:4]).

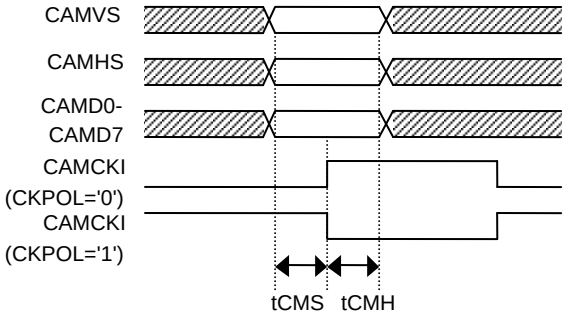
When ACTSW=1h　fSCLK ＝ fCAMCK1　・・・　（Formula:2.1-1）
When ACTSW=2h　fSCLK ≧ 2×fCAMCKI　・・・　（Formula:2.1-2）

Wherein, fSCLK　BU6569GVW system clock frequency
fCAMCKI　CAMCKI terminal input clock frequency

ACTSW=0h,3h is forbidden.
(note) fCAMCKI ＞ fSCLK, 2×fCAMCKI ＞ fSCLK ＞ fCAMCKI is forbidden.

2.2. Camera module interface image data timing

The timing of the camera image signal in camera I/F is shown in Figure 2.2-1.



Symbol	Details	MIN.	TYP.	MAX.	Unit
tCMS	camera data setup time	4	-	-	ns
tCMH	camera data hold time	4	-	-	ns

＊Regulation all at threshold of VDDIO2×1/2

Figure 2.2-1　BU6569GVW timing (camera image data)

3. LCD direct access

・Transparent terminal timing at LCD module direct access

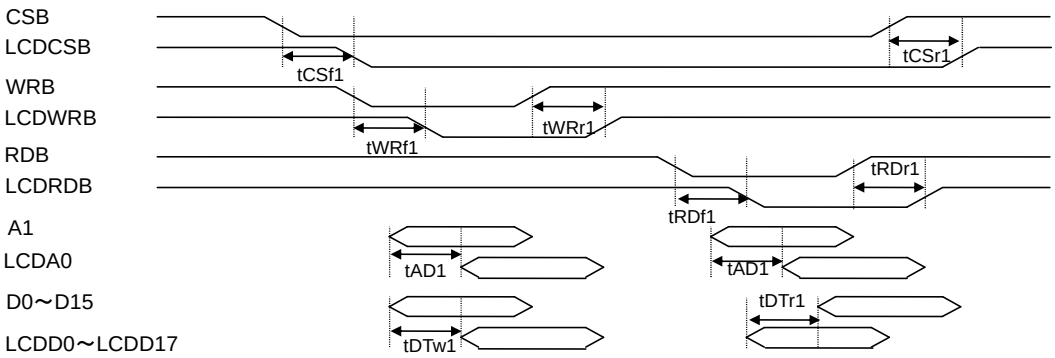


Figure 3-1　BU6569GVW timing conditions (LCD direct access）

Table 3-1　BU6569GVW timing conditions（LCD direct access）

Symbol	Details	MIN.	TYP.	MAX.	Unit
tCSf1	Delay from CSB to LCDCSB falling	4.3	-	16.0	ns
tCSr1	Delay from CSB to LCDCSB rising	2.6	-	10.5	ns
tWRf1	Delay from WRB to LCDWRB falling	4.9	-	17.1	ns
tWRr1	Delay from WRB to LCDWRB rising	2.6	-	11.4	ns
tRDf1	Delay from RDB to LCDRDB falling	5.1	-	17.2	ns
tRDr1	Delay from RDB to LCDRDB rising	2.9	-	11.6	ns
tAD1	Delay from A1 to LCDA0	3.6	-	13.3	ns
tDTw1	Delay from D0～D15 to LCDD0～LCDD17	4.5	-	14.4	ns
tDTr1	Delay from LCDD0～LCDD17 to D0～D15	4.1	-	13.1	ns

＊Regulation all at threshold of VDDIO×1/2

4. LCD transfer timing

Transfer timing to LCD is shown below.

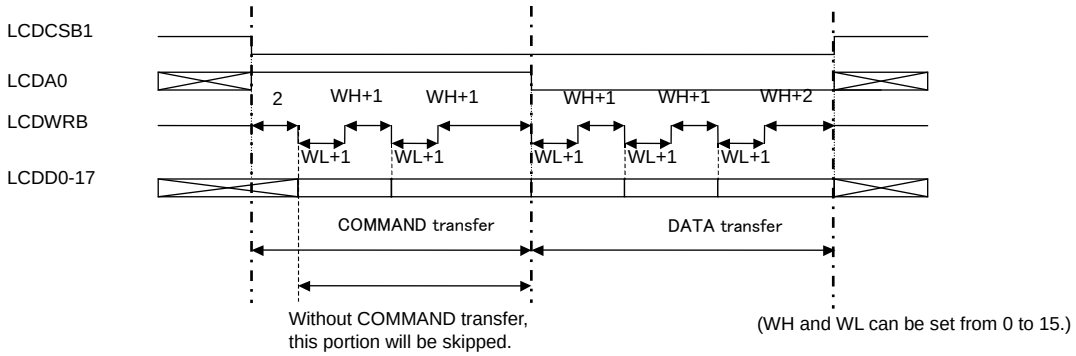
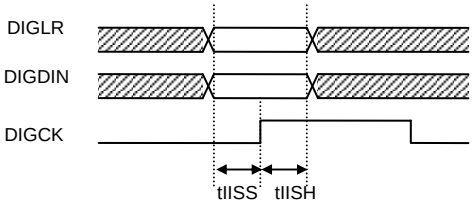


Figure 4-1 MAIN LCD data transfer waveform（Unit：tSCLK）

5. Digital input interface timing

5.1. IIS input timing

The input timing in IIS I/F is shown below.

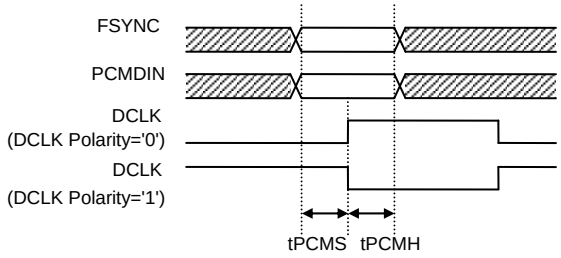


Symbol	Details	MIN.	TYP.	MAX.	Unit
tIISS	IIS input data setup time	5	-	-	ns
tIISH	IIS input data hold time	5	-	-	ns

∗ Regulation all at threshold of VDDIO1×1/2

5.2. PCM input timing

The input timing in PCM I/F is shown below.

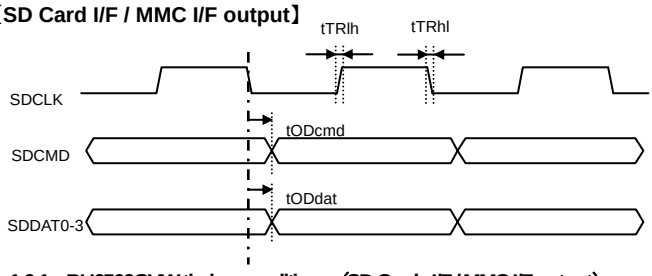


Symbol	Details	MIN.	TYP.	MAX.	Unit
tPCMS	PCM data setup time	5	-	-	ns
tPCMH	PCM data hold time	5	-	-	ns

∗ Regulation all at threshold of VDDIO1×1/2

6. SD Card I/F / MMC I/F input / output timing (Host to/from SD Card)

【SD Card I/F / MMC I/F output】



【SD Card I/F / MMC I/F input】

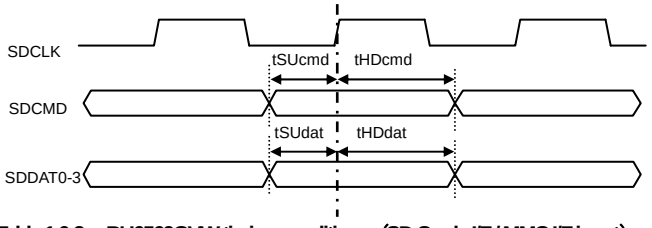


Table 1.6-1 BU6569GVW timing conditions（SD Card I/F / MMC I/F output）

Symbol	Details	MIN.	TYP.	MAX.	Unit
tTRlh	SDCLK clock rise time	-	-	5(∗)	ns
tTRhl	SDCLK clock fall time	-	-	5(∗)	ns
tODcmd	SDCMD output delay against SDCLK falling	-2 (∗)	-	2 (∗)	ns
tODdat	SDDAT0-3 output delay against SDCLK falling	-2 (∗)	-	7 (∗)	ns

(∗)At no load condition

∗ Regulation all at threshold of VDDIO2×1/2

Table 1.6-2 BU6569GVW timing conditions（SD Card I/F / MMC I/F input）

Symbol	Details	MIN.	TYP.	MAX.	Unit
tSUcmd	SDCMD setup time	7	-	-	ns
tHDcmd	SDCMD hold time	1	-	-	ns
tSUdat	SDDAT0-3 setup time	10	-	-	ns
tHDdat	SDDAT0-3 hold time	1	-	-	ns

∗ Regulation all at threshold of VDDIO2×1/2

● Development Scheme

This technical note is aimed at trying the connectivity in the hardware between customer's system and our camera image processor series.

We prepare various data and tools for every development STEP as follows other than this technical note, please contact the sales staff in your duty also including the support system.

(1) Demonstration STEP

(You can try the standard image processing functions by the standard Demonstration kit at once.)

You can confirm the standard functions such as camera image preview, memory data display to LCD, camera image composition JPEG compression/ expansion, frame composition, divided display, and LED lighting, and so forth on the Demonstration board.

・Standard Demonstration board kit

◎Demonstration board

（LCD module provided by ROHM, Camera module provided by ROHM, Check board equipped with the camera image processor, ARM-equipped controller board）

◎Demonstration board operation manual

◎Demonstration software

If the software for the trial board is installed in your Windows PC(Windows 2000/XP/ME/98), more detailed setting is possible.

(Execution tools for the macro command, sample macro command file)

◎USB cable

(2) Confirmation STEP

(We will respond to customer's camera module, LCD module, HOST CPU.)

・Specifications

We will provide specifications for camera image processor according to customer's requirements.

・Function explanation

We will deliver you the function explanation describing detailed functions, register settings, external interfaces, timing, and so forth of camera image processor according to your requests.

・Application note

We will deliver you the detailed explanation data on application development of camera image processor according to your requests.

(3) System check STEP

(You can check the application operation as a system by the kit of system check tools and your module(camera/LCD).)

ROHM creates the system check board using your camera/LCD module.

You can check the interface with your module and the application operation on the system check board using the tools for user's only.

・System check tools kit

・System check software (For Windows PC)

◎Reference C source code summarizing ARM –compatible application program interface(API)

◎The application software (API) as a reference C source code

◎The execution tools for the macro command (BU65XX_USB) for the check by your PC.

◎The macro command file for the check by your PC.

・System check document

◎System check board manual

◎BU65XX Demo_Board Application using API

◎Board circuit diagram

*You can check the detailed functions of the application operation by your PC using the macro command file.

(4) Integrated check STEP with user's system

(You can check the application operation as a system on your system check board using the integrated check software.)

You can check the application operation on the sample LSI-equipped system check board by your camera / LCD module using the integrated check software.

・On line Support ; We will answer your questions about the software development.

How to use the macro command file, API file, and APL file.

Setting flow of the camera function (camera JPEG, preview, etc.)

Interface setting of the camera module, LCD module and the camera image processor.

Header analysis method oh JPEG decode, etc.

・On site Support ; We will help you clarify the questions about the software development on site together on spot.

Check of the operation of each function and the basic operation at each register setting, etc. based on the specification.

Explanation about the specific usage of the macro command file, API file and APL file and relative questions.

How to develop the overlay or special functions, etc.

●Cautions on use

(1)Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2)Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3)Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4)Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5)GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6)Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7)Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8)Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9)Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10)Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

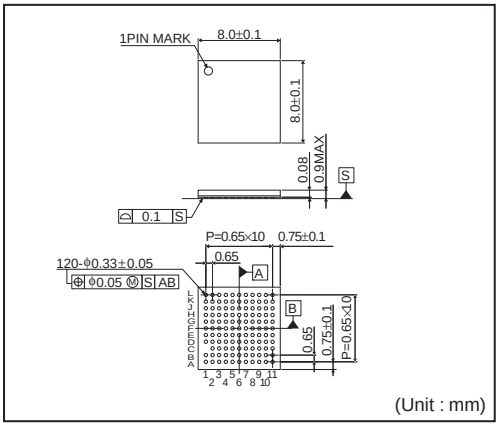
(11)External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

●Order Model Name Selection

B U	6 5 6 9	G V W	—	E 2
ROHM model name	Product number	Package type GVW: SBGA120W080		Taping model name E2: Embossed reel tape

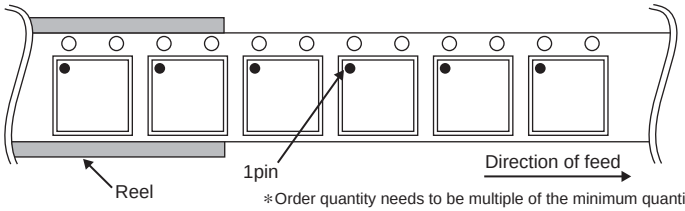
SBGA120W080



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/