512Mb G-die DDR2 SDRAM Specification

60FBGA & 84FBGA with Lead-Free and Halogen-Free

(RoHS compliant)

Table of Contents

1.0 Ordering Information 4
2.0 Key Features 4
3.0 Package Pinout/Mechanical Dimension & Addressing 5
3.1 x4 package pinout (Top View) : 60ball FBGA Package 5
3.2 x8 package pinout (Top View) : 60ball FBGA Package 6
3.3 x16 package pinout (Top View) : 84ball FBGA Package 7
3.4 FBGA Package Dimension(x4/ x8) 8
3.5 FBGA Package Dimension(x16) 9
4.0 Input/Output Functional Description 10
5.0 DDR2 SDRAM Addressing 11
6.0 Absolute Maximum DC Ratings 12
7.0 AC & DC Operating Conditions 12
7.1 Recommended DC Operating Conditions (SSTL - 1.8) 12
7.2 Operating Temperature Condition 13
7.3 Input DC Logic Level 13
7.4 Input AC Logic Level 13
7.5 AC Input Test Conditions 13
7.6 Differential input AC logic Level 14
7.7 Differential AC output parameters 14
8.0 ODT DC electrical characteristics 14
9.0 OCD default characteristics 15
10.0 IDD Specification Parameters and Test Conditions 16
11.0 DDR2 SDRAM IDD Spec 18
12.0 Input/Output capacitance 19
13.0 Electrical Characteristics & AC Timing for DDR2-800/667/533/400 19
13.1 Refresh Parameters by Device Density 19
13.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin 19
13.3 Timing parameters by speed grade (DDR2-800 and DDR2-667) 20
13.4 Timing parameters by speed grade (DDR2-533 and DDR2-400) 22
14.0 General notes, which may apply for all AC parameters 24
15.0 Specific Notes for dedicated AC parameters 26

Revision History

Revision	Month	Year	History
1.0	August	2007	- Initial Release
1.1	October	2007	- Added x16 IDD Specification
1.2	January	2008	- Added x4 Specification
1.21	February	2008	- Typo Correction
1.3	July	2008	- Updated AC timing table with the JEDEC update(JESD79-2E)
1.4	December	2008	- Updated AC/DC operating condition with the JEDEC update(JESD79-2E)

1.0 Ordering Information

Org.	DDR2-800 5-5-5	DDR2-800 6-6-6	DDR2-667 5-5-5	DDR2-533 4-4-4	DDR2-400 3-3-3	Package
128Mx4	K4T51043QG-HC(L)E7	K4T51043QG-HC(L)F7	K4T51043QG-HC(L)E6	K4T51043QG-HC(L)D5	K4T51043QG-HC(L)CC	60 FBGA
64Mx8	K4T51083QG-HC(L)E7	K4T51083QG-HC(L)F7	K4T51083QG-HC(L)E6	K4T51083QG-HC(L)D5	K4T51083QG-HC(L)CC	60 FBGA
32Mx16	K4T51163QG-HC(L)E7	K4T51163QG-HC(L)F7	K4T51163QG-HC(L)E6	K4T51163QG-HC(L)D5	K4T51163QG-HC(L)CC	84 FBGA

Note :
1. Speed bin is in order of CL-tRCD-tRP
2. “H” of Part number(12th digit) stands for Lead-Free, Halogen-Free, and RoHS compliant products.

2.0 Key Features

Speed	DDR2-800 5-5-5	DDR2-800 6-6-6	DDR2-667 5-5-5	DDR2-533 4-4-4	DDR2-400 3-3-3	Units
CAS Latency	5	6	5	4	3	tCK
tRCD(min)	12.5	15	15	15	15	ns
tRP(min)	12.5	15	15	15	15	ns
tRC(min)	57.5	60	60	60	55	ns

- JEDEC standard V_{DD} = 1.8V ± 0.1V Power Supply
- V_{DDQ} = 1.8V ± 0.1V
- 200 MHz f_{CK} for 400Mb/sec/pin, 267MHz f_{CK} for 533Mb/sec/pin, 333MHz f_{CK} for 667Mb/sec/pin, 400MHz f_{CK} for 800Mb/sec/pin
- 4 Banks
- Posted $\overline{CAS}$
- Programmable $\overline{CAS}$ Latency: 3, 4, 5, 6
- Programmable Additive Latency: 0, 1 , 2 , 3, 4 , 5
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4 , 8(Interleave/Nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination
- Special Function Support
  - -50ohm ODT
  - -High Temperature Self-Refresh rate enable
- Average Refresh Period 7.8us at lower than T_{CASE} 85°C, 3.9us at 85°C < $T_{CASE} \leq$ 95 °C
- All of products are Lead-Free, Halogen-Free, and RoHS compliant

The 512Mb DDR2 SDRAM is organized as a 32Mbit x 4 I/Os x 4banks or 16Mbit x 8 I/Os x 4banks or 8Mbit x 16 I/Os x 4 banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 800Mb/sec/pin (DDR2-800) for general applications.
The chip is designed to comply with the following key DDR2 SDRAM features such as posted CAS with additive latency, write latency = read latency -1, Off-Chip Driver(OCD) impedance adjustment and On Die Termination.
All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and $\overline{DQS}$) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a $\overline{RAS}$/$\overline{CAS}$ multiplexing style. For example, 512Mb(x8) device receive 14/10/2 addressing.
The 512Mb DDR2 device operates with a single 1.8V ± 0.1V power supply and 1.8V ± 0.1V V_{DDQ}.
The 512Mb DDR2 device is available in 60ball FBGAs(x8) and in 84ball FBGAs(x16).

Note : The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

Note : This data sheet is an abstract of full DDR2 specification and does not cover the common features which are described in “Samsung’s DDR2 SDRAM Device Operation & Timing Diagram”

3.0 Package Pinout/Mechanical Dimension & Addressing

3.1 x4 package pinout (Top View) : 60ball FBGA Package

1	2	3		7	8	9
V_{DD}	NC	V_{SS}	**A**	V_{SSQ}	$\overline{DQS}$	V_{DDQ}
NC	V_{SSQ}	DM	**B**	DQS	V_{SSQ}	NC
V_{DDQ}	DQ1	V_{DDQ}	**C**	V_{DDQ}	DQ0	V_{DDQ}
NC	V_{SSQ}	DQ3	**D**	DQ2	V_{SSQ}	NC
V_{DDL}	V_{REF}	V_{SS}	**E**	V_{SSDL}	CK	V_{DD}
	CKE	$\overline{WE}$	**F**	$\overline{RAS}$	$\overline{CK}$	ODT
NC	BA0	BA1	**G**	$\overline{CAS}$	$\overline{CS}$	
	A10/AP	A1	**H**	A2	A0	V_{DD}
V_{SS}	A3	A5	**J**	A6	A4	
	A7	A9	**K**	A11	A8	V_{SS}
V_{DD}	A12	NC	**L**	NC	A13	

Note :
1. Pin B3 has identical capacitance as pin B7.
2. V_{DDL} and V_{SSDL} are power and ground for the DLL.

Ball Locations (x4)

● : **Populated Ball**
+ : **Depopulated Ball**

Top View (See the balls through the package)

	1	2	3	4	5	6	7	8	9
A	●	●	●	+	+	+	●	●	●
B	●	●	●	+	+	+	●	●	●
C	●	●	●	+	+	+	●	●	●
D	●	●	●	+	+	+	●	●	●
E	●	●	●	+	+	+	●	●	●
F	+	●	●	+	+	+	●	●	●
G	●	●	●	+	+	+	●	●	+
H	+	●	●	+	+	+	●	●	●
J	●	●	●	+	+	+	●	●	+
K	+	●	●	+	+	+	●	●	●
L	●	●	●	+	+	+	●	●	+

3.2 x8 package pinout (Top View) : 60ball FBGA Package

1	2	3		7	8	9
V_{DD}	NU/ $\overline{RDQS}$	V_{SS}	**A**	V_{SSQ}	$\overline{DQS}$	V_{DDQ}
DQ6	V_{SSQ}	DM/ RDQS	**B**	DQS	V_{SSQ}	DQ7
V_{DDQ}	DQ1	V_{DDQ}	**C**	V_{DDQ}	DQ0	V_{DDQ}
DQ4	V_{SSQ}	DQ3	**D**	DQ2	V_{SSQ}	DQ5
V_{DDL}	V_{REF}	V_{SS}	**E**	V_{SSDL}	CK	V_{DD}
	CKE	$\overline{WE}$	**F**	$\overline{RAS}$	$\overline{CK}$	ODT
NC	BA0	BA1	**G**	$\overline{CAS}$	$\overline{CS}$	
	A10/AP	A1	**H**	A2	A0	V_{DD}
V_{SS}	A3	A5	**J**	A6	A4	
	A7	A9	**K**	A11	A8	V_{SS}
V_{DD}	A12	NC	**L**	NC	A13	

Note :
1. Pins B3 and A2 have identical capacitance as pins B7 and A8.
2. For a read, when enabled, strobe pair RDQS & $\overline{RDQS}$ are identical in function and timing to strobe pair DQS & $\overline{DQS}$ and input masking function is disabled.
3. The function of DM or RDQS/$\overline{RDQS}$ are enabled by EMRS command.
4. V_{DDL} and V_{SSDL} are power and ground for the DLL.

Ball Locations (x8)

● : Populated Ball
+ : Depopulated Ball

Top View (See the balls through the package)

	1	2	3	4	5	6	7	8	9
A	●	●	●	+	+	+	●	●	●
B	●	●	●	+	+	+	●	●	●
C	●	●	●	+	+	+	●	●	●
D	●	●	●	+	+	+	●	●	●
E	●	●	●	+	+	+	●	●	●
F	+	●	●	+	+	+	●	●	●
G	●	●	●	+	+	+	●	●	+
H	+	●	●	+	+	+	●	●	●
J	●	●	●	+	+	+	●	●	+
K	+	●	●	+	+	+	●	●	●
L	●	●	●	+	+	+	●	●	+

3.3 x16 package pinout (Top View) : 84ball FBGA Package

1	2	3		7	8	9
V_{DD}	NC	V_{SS}	A	V_{SSQ}	$\overline{\text{UDQS}}$	V_{DDQ}
DQ14	V_{SSQ}	UDM	B	UDQS	V_{SSQ}	DQ15
V_{DDQ}	DQ9	V_{DDQ}	C	V_{DDQ}	DQ8	V_{DDQ}
DQ12	V_{SSQ}	DQ11	D	DQ10	V_{SSQ}	DQ13
V_{DD}	NC	V_{SS}	E	V_{SSQ}	$\overline{\text{LDQS}}$	V_{DDQ}
DQ6	V_{SSQ}	LDM	F	LDQS	V_{SSQ}	DQ7
V_{DDQ}	DQ1	V_{DDQ}	G	V_{DDQ}	DQ0	V_{DDQ}
DQ4	V_{SSQ}	DQ3	H	DQ2	V_{SSQ}	DQ5
V_{DDL}	V_{REF}	V_{SS}	J	V_{SSDL}	CK	V_{DD}
	CKE	$\overline{\text{WE}}$	K	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
NC	BA0	BA1	L	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10/AP	A1	M	A2	A0	V_{DD}
V_{SS}	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	V_{SS}
V_{DD}	A12	NC	R	NC	NC	

Note :
1. V_{DDL} and V_{SSDL} are power and ground for the DLL.
2. In case of only 8 DQs out of 16 DQs are used, LDQS, LDQSB and DQ0~7 must be used.

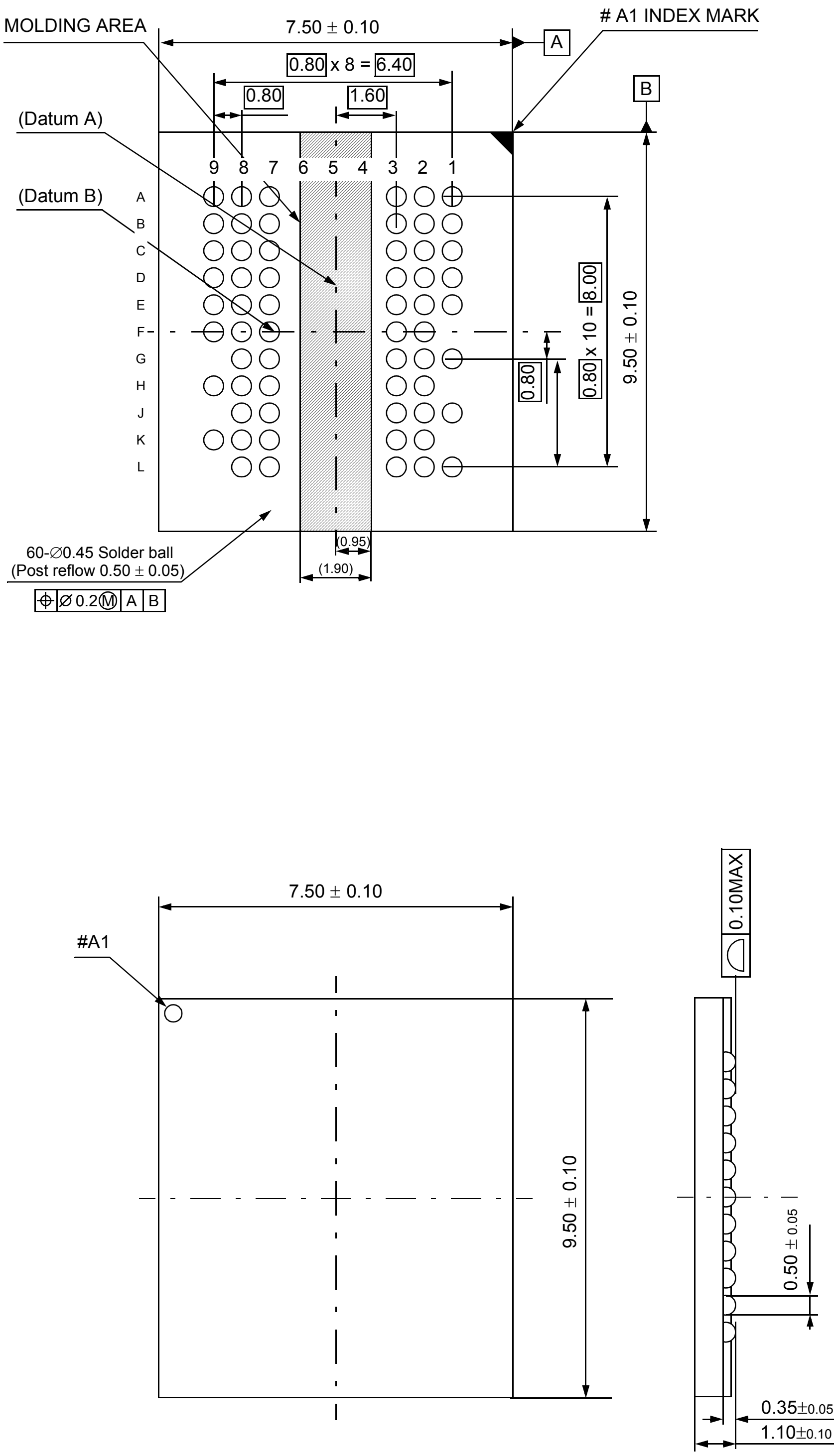
Ball Locations (x16)

● : Populated Ball
\+ : Depopulated Ball

Top View
(See the balls through the package)

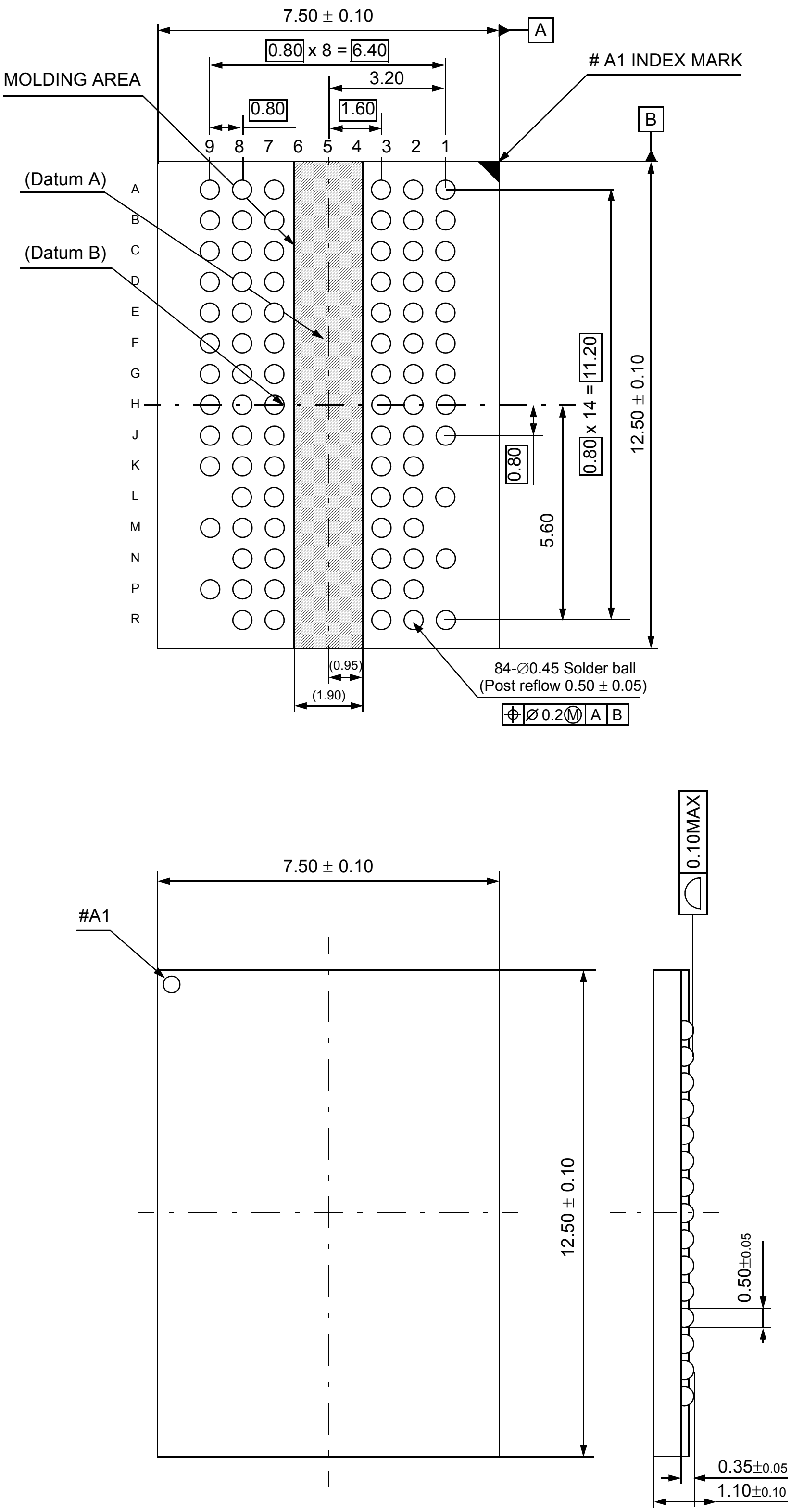
	1	2	3	4	5	6	7	8	9
A	●	●	●	+	+	+	●	●	●
B	●	●	●	+	+	+	●	●	●
C	●	●	●	+	+	+	●	●	●
D	●	●	●	+	+	+	●	●	●
E	●	●	●	+	+	+	●	●	●
F	●	●	●	+	+	+	●	●	●
G	●	●	●	+	+	+	●	●	●
H	●	●	●	+	+	+	●	●	●
J	●	●	●	+	+	+	●	●	●
K	+	●	●	+	+	+	●	●	●
L	●	●	●	+	+	+	●	●	+
M	+	●	●	+	+	+	●	●	●
N	●	●	●	+	+	+	●	●	+
P	+	●	●	+	+	+	●	●	●
R	●	●	●	+	+	+	●	●	+

3.4 FBGA Package Dimension(x4/x8)



SAMSUNG
ELECTRONICS

3.5 FBGA Package Dimension(x16)



4.0 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. After V_{REF} has become stable during the power on and initialization swquence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, V_{REF} must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM signal for x4/x8 configurations. For x16 configuration, ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register Set(EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.
BA0 - BA1	Input	**Bank Address Inputs:** BA0, BA1 and BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A13	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1 and BA2. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$) (LDQS), ($\overline{LDQS}$) (UDQS), ($\overline{UDQS}$) (RDQS), ($\overline{RDQS}$)	Input/Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$, and $\overline{RDQS}$ to provide differential pair signaling to the system during both reads and writes. A control bit at EMRS(1)[A10] enables or disables all complementary data strobe signals. In this data sheet, "differential DQS signals" refers to any of the following with A10 = 0 of EMRS(1) x4 DQS/$\overline{DQS}$ x8 DQS/$\overline{DQS}$ if EMRS(1)[A11] = 0 x8 DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, if EMRS(1)[A11] = 1 x16 LDQS/$\overline{LDQS}$ and UDQS/$\overline{UDQS}$ "single-ended DQS signals" refers to any of the following with A10 = 1 of EMRS(1) x4 DQS x8 DQS if EMRS(1) [A11] = 0 x8 DQS, RDQS, if EMRS(1) [A11] = 1 x16 LDQS and UDQS
NC		**No Connect :** No internal electrical connection is present.
V_{DD}/V_{DDQ}	Supply	**Power Supply :** 1.8V +/- 0.1V, **DQ Power Supply :** 1.8V +/- 0.1V
V_{SS}/V_{SSQ}	Supply	**Ground**, **DQ Ground**
V_{DDL}	Supply	**DLL Power Supply :** 1.8V +/- 0.1V
V_{SSDL}	Supply	DLL Ground
V_{REF}	Supply	Reference voltage

5.0 DDR2 SDRAM Addressing

512Mb

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Banks	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9

* Reference information: The following tables are address mapping information for other densities.

256Mb

Configuration	64Mb x4	32Mb x 8	16Mb x16
# of Banks	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A12	A0 ~ A12	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A8

1Gb

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Banks	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9

2Gb

Configuration	512Mb x4	256Mb x 8	128Mb x16
# of Banks	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A14	A0 ~ A14	A0 ~ A13
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9

4Gb

Configuration	1 Gb x4	512Mb x 8	256Mb x16
# of Banks	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 - A15	A0 - A15	A0 - A14
Column Address/page size	A0 - A9,A11	A0 - A9	A0 - A9

6.0 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	- 1.0 V ~ 2.3 V	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note :
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must be not greater than 0.6 x V_{DDQ}. When V_{DD} and V_{DDQ} and V_{DDL} are less than 500mV, V_{REF} may be equal to or less than 300mV.
4. Voltage on any input or I/O may not exceed voltage on V_{DDQ}.

7.0 AC & DC Operating Conditions

7.1 Recommended DC Operating Conditions (SSTL - 1.8)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	4
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	4
V_{REF}	Input Reference Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV	1,2
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3

Note : There is no specific device V_{DD} supply voltage requirement for SSTL-1.8 compliance. However under all conditions V_{DDQ} must be less than or equal to V_{DD}.
1. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
2. Peak to peak AC noise on V_{REF} may not exceed +/-2% V_{REF}(DC).
3. V_{TT} of transmitting device must track V_{REF} of receiving device.
4. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.

7.2 Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Operating Temperature	0 to 95	°C	1, 2

Note :
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

7.3 Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH}(DC)	DC input logic high	V_{REF} + 0.125	V_{DDQ} + 0.3	V	
V_{IL}(DC)	DC input logic low	- 0.3	V_{REF} - 0.125	V	

7.4 Input AC Logic Level

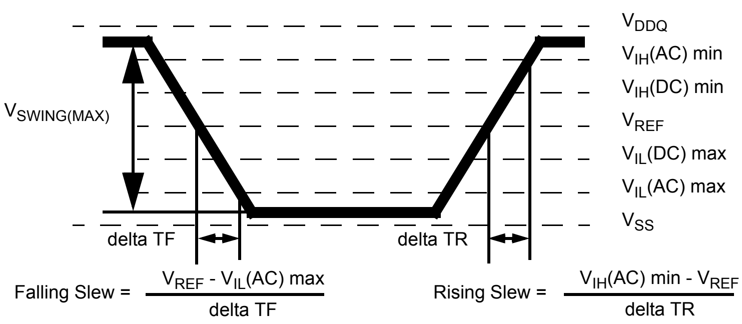
Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units
		Min.	Max.	Min.	Max.	
V_{IH}(AC)	AC input logic high	V_{REF} + 0.250	V_{DDQ} + V_{PEAK}	V_{REF} + 0.200	V_{DDQ} + V_{PEAK}	V
V_{IL}(AC)	AC input logic low	V_{SSQ} - V_{PEAK}	V_{REF} - 0.250	V_{SSQ} - V_{PEAK}	V_{REF} - 0.200	V

Note :
1. For information related to V_{PEAK} value, Refer to overshoot/undershoot specification in device operation and timing datasheet; maximum peak amplitude allowed for overshoot and undershoot.

7.5 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

Note :
1. Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL}$(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH}(AC) min for rising edges and the range from V_{REF} to V_{IL}(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from V_{IL}(AC) to V_{IH}(AC) on the positive transitions and V_{IH}(AC) to V_{IL}(AC) on the negative transitions.



< AC Input Test Signal Waveform >

7.6 Differential input AC logic Level

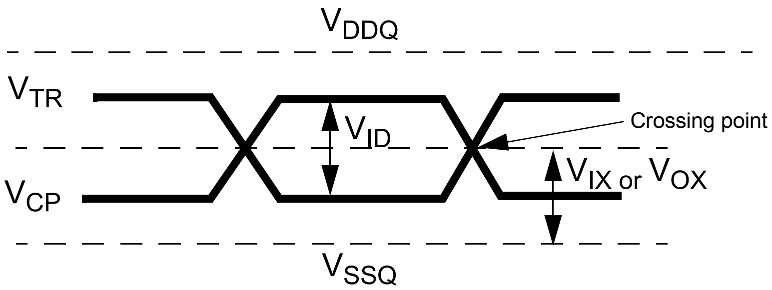
Symbol	Parameter	Min.	Max.	Units	Notes
V_{ID}(AC)	AC differential input voltage	0.5	V_{DDQ}	V	1
V_{IX}(AC)	AC differential cross point voltage	0.5 * V_{DDQ} - 0.175	0.5 * V_{DDQ} + 0.175	V	2

Note :

1. V_{ID}(AC) specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input signal (such as CK, DQS, LDQS or UDQS) and V_{CP} is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to V_{IH} (AC) - V_{IL}(AC).

2. The typical value of V_{IX}(AC) is expected to be about 0.5 * V_{DDQ} of the transmitting device and V_{IX}(AC) is expected to track variations in V_{DDQ} . V_{IX}(AC) indicates the voltage at which differential input signals must cross.

3. For information related to V_{PEAK} value, Refer to overshoot/undershoot specification in device operation and timing datasheet; maximum peak amplitude allowed for overshoot and undershoot.



< Differential signal levels >

7.7 Differential AC output parameters

Symbol	Parameter	Min.	Max.	Units	Note
V_{OX}(AC)	AC differential cross point voltage	0.5 * V_{DDQ} - 0.125	0.5 * V_{DDQ} + 0.125	V	1

Note :

1. The typical value of V_{OX}(AC) is expected to be about 0.5 * V_{DDQ} of the transmitting device and V_{OX}(AC) is expected to track variations in V_{DDQ} . V_{OX}(AC) indicates the voltage at which differential output signals must cross.

8.0 ODT DC electrical characteristics

PARAMETER/CONDITION	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75 ohm	Rtt1(eff)	60	75	90	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150 ohm	Rtt2(eff)	120	150	180	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,1; 50 ohm	Rtt3(eff)	40	50	60	ohm	1
Deviation of VM with respect to V_{DDQ}/2	delta V_M	- 6		+ 6	%	1

Note :

1. Test condition for Rtt measurements

Measurement Definition for Rtt(eff) : Apply V_{IH} (AC) and V_{IL} (AC) to test pin separately, then measure current $I(V_{IH}$ (AC)) and $I(V_{IL}$ (AC)) respectively.

V_{IH} (AC), V_{IL} (AC), and V_{DDQ} values defined in SSTL_18

$$Rtt(eff) = \frac{V_{IH}(AC) - V_{IL}(AC)}{I(V_{IH}(AC)) - I(V_{IL}(AC))}$$

$$\text{delta } V_M = \left(\frac{2 \times V_M}{V_{DDQ}} - 1\right) \times 100\%$$

Measurement Definition for V_M: Measure voltage (V_M) at test pin (midpoint) with no load.

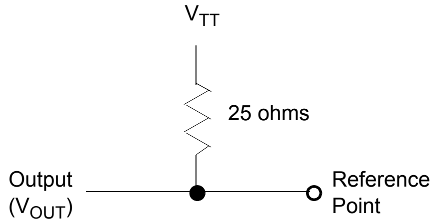
9.0 OCD default characteristics

Description	Parameter	Min	Nom	Max	Unit	Notes
Output impedance		18ohm at norminal condition See full strength default driver characteristics on device operation specification			ohms	1,2
Output impedance step size for OCD calibration		0		1.5	ohms	6
Pull-up and pull-down mismatch		0		4	ohms	1,2,3
Output slew rate	Sout	1.5		5	V/ns	1,4,5,6,7,8

Note :

1. Absolute Specifications (0°C ≤ T_{CASE} ≤ +95°C; V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V)
2. Impedance measurement condition for output source dc current: V_{DDQ} = 1.7V; VOUT = 1420mV; (V_{OUT}-V_{DDQ})/Ioh must be less than 23.4 ohms for values of V_{OUT} between V_{DDQ} and V_{DDQ}- 280mV. Impedance measurement condition for output sink dc current: V_{DDQ} = 1.7V; V_{OUT} = 280mV; V_{OUT}/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
4. Slew rate measured from V_{IL}(AC) to V_{IH}(AC).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18 ohms at nominal conditions across all process and represents only the DRAM uncertainty.

Output slew rate load :



7. DRAM output slew rate specification applies to 400Mb/sec/pin, 533Mb/sec/pin, 667Mb/sec/pin and 800Mb/sec/pin speed bins.
8. Timing skew due to DRAM output slew rate mis-match between DQS / $\overline{DQS}$ and associated DQs is included in tDQSQ and tQHS specification.

10.0 IDD Specification Parameters and Test Conditions

(IDD values are for full operating range of Voltage and Temperature, Notes 1 - 5)

Symbol	Proposed Conditions	Units	Notes
IDD0	**Operating one bank active-precharge current**; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address businputs are SWITCHING; Data pattern is same as IDD4W	mA	
IDD2P	**Precharge power-down current**; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	
IDD2Q	**Precharge quiet standby current**; All banks idle; tCK = tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputsare STABLE; Data bus inputs are FLOATING	mA	
IDD2N	**Precharge standby current**; All banks idle; tCK = tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD3P	**Active power-down current**; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING — Fast PDN Exit MRS(12) = 0	mA	
	Slow PDN Exit MRS(12) = 1	mA	
IDD3N	**Active standby current**; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	
IDD5B	**Burst auto refresh current**; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD6	**Self refresh current**; CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING — Normal	mA	
	Low Power	mA	
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tFAW = tFAW(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions	mA	

Note :
1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is specified by AC Parametric Test Condition
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS, and $\overline{UDQS}$. IDD values must be met with all combinations of EMRS bits 10 and 11.
5. Definitions for IDD

LOW is defined as $V_{IN} \leq V_{IL}AC(max)$

HIGH is defined as $V_{IN} \geq V_{IH}AC(min)$

STABLE is defined as inputs stable at a HIGH or LOW level

FLOATING is defined as inputs at $V_{REF} = V_{DDQ}/2$

SWITCHING is defined as:

inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and

inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

For purposes of IDD testing, the following parameters are utilized

	DDR2-800	DDR2-800	DDR2-667	DDR2-533	DDR2-400	Units
Parameter	5-5-5	6-6-6	5-5-5	4-4-4	3-3-3	
CL(IDD)	5	6	5	4	3	tCK
tRCD(IDD)	12.5	15	15	15	15	ns
tRC(IDD)	57.5	60	60	60	55	ns
tRRD(IDD)-x4/x8	7.5	7.5	7.5	7.5	7.5	ns
tRRD(IDD)-x16	10	10	10	10	10	ns
tCK(IDD)	2.5	2.5	3	3.75	5	ns
tRASmin(IDD)	45	45	45	45	40	ns
tRP(IDD)	12.5	15	15	15	15	ns
tRFC(IDD)	105	105	105	105	105	ns

Detailed IDD7
The detailed timings are shown below for IDD7.
Legend: A = Active; RA = Read with Autoprecharge; D = Deselect

IDD7: Operating Current: All Bank Interleave Read operation
All banks are being interleaved at minimum tRC(IDD) without violating tRRD(IDD) and tFAW(IDD) using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOUT = 0mA

Timing Patterns for 4 bank devices x4/ x8/ x16
-DDR2-400 3/3/3
A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D
-DDR2-533 4/4/4
A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D
-DDR2-667 5/5/5
A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D
-DDR2-667 4/4/4
A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D
-DDR2-800 6/6/6
A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D D
-DDR2-800 5/5/5
A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D

11.0 DDR2 SDRAM IDD Spec

Symbol	128Mx4 (K4T51043QG)										Unit	Notes
	800@CL=5		800@CL=6		667@CL=5		533@CL=4		400@CL=3			
	CE7	LE7	CF7	LF7	CE6	LE6	CD5	LD5	CCC	LCC		
IDD0	80		80		75		75		70		mA	
IDD1	90		90		85		85		85		mA	
IDD2P	8	5	8	5	8	5	8	4.5	8	4.5	mA	
IDD2Q	35		35		35		30		30		mA	
IDD2N	40		40		40		35		35		mA	
IDD3P-F	30		30		30		30		30		mA	
IDD3P-S	12		12		12		12		12		mA	
IDD3N	55		55		55		50		50		mA	
IDD4W	115		115		100		75		75		mA	
IDD4R	125		125		110		85		85		mA	
IDD5	115		115		110		105		105		mA	
IDD6	8	4	8	4	8	4	8	4	8	4	mA	
IDD7	210		210		175		175		175		mA	

Symbol	64Mx8 (K4T51083QG)										Unit	Notes
	800@CL=5		800@CL=6		667@CL=5		533@CL=4		400@CL=3			
	CE7	LE7	CF7	LF7	CE6	LE6	CD5	LD5	CCC	LCC		
IDD0	85		85		75		75		70		mA	
IDD1	95		95		90		85		85		mA	
IDD2P	8	5	8	5	8	5	8	4.5	8	4.5	mA	
IDD2Q	35		35		35		30		30		mA	
IDD2N	40		40		40		35		35		mA	
IDD3P-F	30		30		30		30		30		mA	
IDD3P-S	12		12		12		12		12		mA	
IDD3N	60		60		55		50		50		mA	
IDD4W	110		110		100		85		80		mA	
IDD4R	140		140		130		105		95		mA	
IDD5	110		110		105		105		100		mA	
IDD6	8	4	8	4	8	4	8	4	8	4	mA	
IDD7	210		210		175		175		175		mA	

Symbol	32Mx16 (K4T51163QG)										Unit	Notes
	800@CL=5		800@CL=6		667@CL=5		533@CL=4		400@CL=3			
	CE7	LE7	CF7	LF7	CE6	LE6	CD5	LD5	CCC	LCC		
IDD0	95		95		90		90		90		mA	
IDD1	115		115		110		105		105		mA	
IDD2P	8	5	8	5	8	5	8	4.5	8	4.5	mA	
IDD2Q	35		35		35		30		30		mA	
IDD2N	40		40		40		35		35		mA	
IDD3P-F	30		30		30		30		30		mA	
IDD3P-S	12		12		12		12		12		mA	
IDD3N	60		60		55		50		50		mA	
IDD4W	130		130		115		100		95		mA	
IDD4R	185		185		165		135		130		mA	
IDD5	110		110		105		105		105		mA	
IDD6	8	4	8	4	8	4	8	4	8	4	mA	
IDD7	275		275		235		235		210		mA	

12.0 Input/Output capacitance

Parameter	Symbol	DDR2-400 DDR2-533		DDR2-667		DDR2-800		Units
		Min	Max	Min	Max	Min	Max	
Input capacitance, CK and $\overline{CK}$	CCK	1.0	2.0	1.0	2.0	1.0	2.0	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	x	0.25	x	0.25	x	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	2.0	1.0	2.0	1.0	1.75	pF
Input capacitance delta, all other input-only pins	CDI	x	0.25	x	0.25	x	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	2.5	4.0	2.5	3.5	2.5	3.5	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	x	0.5	x	0.5	x	0.5	pF

13.0 Electrical Characteristics & AC Timing for DDR2-800/667/533/400

(0 °C $\leq T_{OPER} \leq$ 95 °C; V_{DDQ} = 1.8V $\pm$ 0.1V; V_{DD} = 1.8V $\pm$ 0.1V)

13.1 Refresh Parameters by Device Density

Parameter	Symbol		256Mb	512Mb	1Gb	2Gb	4Gb	Units
Refresh to active/Refresh command time	tRFC		75	105	127.5	195	327.5	ns
Average periodic refresh interval	tREFI	0 °C $\leq T_{CASE} \leq$ 85°C	7.8	7.8	7.8	7.8	7.8	µs
		85 °C < $T_{CASE} \leq$ 95°C	3.9	3.9	3.9	3.9	3.9	µs

13.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

Speed	DDR2-800(E7)		DDR2-800(F7)		DDR2-667(E6)		DDR2-533(D5)		DDR2-400(CC)		Units
Bin (CL - tRCD - tRP)	5-5-5		6-6-6		5 - 5 - 5		4 - 4 - 4		3 - 3 - 3		
Parameter	min	max	min	max	min	max	min	max	min	max	
tCK, CL=3	5	8	-	-	5	8	5	8	5	8	ns
tCK, CL=4	3.75	8	3.75	8	3.75	8	3.75	8	5	8	ns
tCK, CL=5	2.5	8	3	8	3	8	3.75	8	-	-	ns
tCK, CL=6	-	-	2.5	8	-	-	-	-	-	-	ns
tRCD	12.5	-	15	-	15	-	15	-	15	-	ns
tRP	12.5	-	15	-	15	-	15	-	15	-	ns
tRC	57.5	-	60	-	60	-	60	-	55	-	ns
tRAS	45	70000	45	70000	45	70000	45	70000	40	70000	ns

13.3 Timing parameters by speed grade (DDR2-800 and DDR2-667)

(For information related to the entries in this table, refer to both the general notes and the specific notes following this table.)

Parameter	Symbol	DDR2-800		DDR2-667		Units	Notes
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-400	400	-450	450	ps	40
DQS output access time from CK/$\overline{CK}$	tDQSCK	-350	350	-400	400	ps	40
Average clock HIGH pulse width	tCH(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36
Average clock LOW pulse width	tCL(avg)	0.48	0.52	0.48	0.52	tCK(avg)	35,36
CK half pulse period	tHP	Min(tCL(abs), tCH(abs))	x	Min(tCL(abs), tCH(abs))	x	ps	37
Average clock period	tCK(avg)	2500	8000	3000	8000	ps	35,36
DQ and DM input hold time	tDH(base)	125	x	175	x	ps	6,7,8,21,28,31
DQ and DM input setup time	tDS(base)	50	x	100	x	ps	6,7,8,20,28,31
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK(avg)	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK(avg)	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC(max)	x	tAC(max)	ps	18,40
DQS/$\overline{DQS}$ low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC(min)	tAC(max)	tAC(min)	tAC(max)	ps	18,40
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2* tAC(min)	tAC(max)	2* tAC(min)	tAC(max)	ps	18,40
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	200	x	240	ps	13
DQ hold skew factor	tQHS	x	300	x	340	ps	38
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	39
DQS latching rising transitions to associated clock edges	tDQSS	- 0.25	0.25	-0.25	0.25	tCK(avg)	30
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK(avg)	
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK(avg)	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK(avg)	30
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK(avg)	30
Mode register set command cycle time	tMRD	2	x	2	x	nCK	
MRS command to ODT update delay	tMOD	0	12	0	12	ns	32
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK(avg)	10
Write preamble	tWPRE	0.35	x	0.35	x	tCK(avg)	
Address and control input hold time	tIH(base)	250	x	275	x	ps	5,7,9,23,29
Address and control input setup time	tIS(base)	175	x	200	x	ps	5,7,9,22,29
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK(avg)	19,41
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK(avg)	19,42
Activate to activate command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4,32
Activate to activate command period for 2KB page size products	tRRD	10	x	10	x	ns	4,32

Parameter	Symbol	DDR2-800		DDR2-667		Units	Notes
		min	max	min	max		
Four Activate Window for 1KB page size products	tFAW	35	x	37.5	x	ns	32
Four Activate Window for 2KB page size products	tFAW	45	x	50	x	ns	32
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay	tCCD	2	x	2	x	nCK	
Write recovery time	tWR	15	x	15	x	ns	32
Auto precharge write recovery + precharge time	tDAL	WR + tnRP	x	WR + tnRP	x	nCK	33
Internal write to read command delay	tWTR	7.5	x	7.5	x	ns	24,32
Internal read to precharge command delay	tRTP	7.5	x	7.5	x	ns	3,32
Exit self refresh to a non-read command	tXSNR	tRFC + 10	x	tRFC + 10	x	ns	32
Exit self refresh to a read command	tXSRD	200	x	200	x	nCK	
Exit precharge power down to any command	tXP	2	x	2	x	nCK	
Exit active power down to read command	tXARD	2	x	2	x	nCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS	8 - AL	x	7 - AL	x	nCK	1,2
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	3	x	3	x	nCK	27
ODT turn-on delay	tAOND	2	2	2	2	nCK	16
ODT turn-on	tAON	tAC(min)	tAC(max)+0.7	tAC(min)	tAC(max)+0.7	ns	6,16,40
ODT turn-on (Power-Down mode)	tAONPD	tAC(min)+2	2*tCK(avg) +tAC(max)+1	tAC(min)+2	2*tCK(avg) +tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	nCK	17,45
ODT turn-off	tAOF	tAC(min)	tAC(max)+0.6	tAC(min)	tAC(max)+0.6	ns	17,43,45
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5*tCK(avg) +tAC(max)+1	tAC(min)+2	2.5*tCK(avg) +tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3	x	3	x	nCK	
ODT power down exit latency	tAXPD	8	x	8	x	nCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK(avg) +tIH	x	tIS+tCK(avg) +tIH	x	ns	15

13.4 Timing parameters by speed grade (DDR2-533 and DDR2-400)

(For information related to the entries in this table, refer to both the general notes and the specific notes following this table.)

Parameter	Symbol	DDR2-533		DDR2-400		Units	Notes
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-500	500	-600	600	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-450	450	-500	500	ps	
CK HIGH pulse width	tCH	0.45	0.55	0.45	0.55	tCK	
CK LOW pulse width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half pulse period	tHP	Min(tCL, tCH)	x	Min(tCL, tCH)	x	ps	11,12
Clock cycle time, CL=x	tCK	3750	8000	5000	8000	ps	15
DQ and DM input hold time (differential strobe)	tDH(base)	225	x	275	x	ps	6,7,8,21,28
DQ and DM input setup time (differential strobe)	tDS(base)	100	x	150	x	ps	6,7,8,20,28
DQ and DM input hold time (single-ended strobe)	tDH1(base)	-25	x	25	x	ps	6,7,8,26
DQ and DM input setup time (single-ended strobe)	tDS1(base)	-25	x	25	x	ps	6,7,8,25
Control & Address input pulse width for each input	tIPW	0.6	x	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	x	0.35	x	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC(max)	x14	tAC(max)	ps	18
DQS(/$\overline{DQS}$) low-impedance time from CK/$\overline{CK}$	tLZ(DQS)	tAC(min)	tAC(max)	tAC(min)	tAC(max)	ps	18
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2* tAC(min)	tAC(max)	2* tAC(min)	tAC(max)	ps	18
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	300	x	350	ps	13
DQ hold skew factor	tQHS	x	400	x	450	ps	12
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	x	tHP - tQHS	x	ps	
DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	-0.25	0.25	tCK	
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK	
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK	
DQS falling edge to CK setup time	tDSS	0.2	x	0.2	x	tCK	
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	
Mode register set command cycle time	tMRD	2	x	2	x	tCK	
MRS command to ODT update delay	tMOD	0	12	0	12	ns	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10
Write preamble	tWPRE	0.35	x	0.35	x	tCK	
Address and control input hold time	tIH(base)	375	x	475	x	ps	5,7,9,23
Address and control input setup time	tIS(base)	250	x	350	x	ps	5,7,9,22
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	19
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	19
Active to active command period for 1KB page size products	tRRD	7.5	x	7.5	x	ns	4
Active to active command period for 2KB page size products	tRRD	10	x	10	x	ns	4

Parameter	Symbol	DDR2-533		DDR2-400		Units	Notes
		min	max	min	max		
Four Activate Window for 1KB page size products	tFAW	37.5	x	37.5	x	ns	
Four Activate Window for 2KB page size products	tFAW	50	x	50	x	ns	
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay	tCCD	2	x	2	x	tCK	
Write recovery time	tWR	15	x	15	x	ns	
Auto precharge write recovery + precharge time	tDAL	WR+tRP	x	WR+tRP	x	tCK	14
Internal write to read command delay	tWTR	7.5	x	10	x	ns	24
Internal read to precharge command delay	tRTP	7.5	x	7.5	x	ns	3
Exit self refresh to a non-read command	tXSNR	tRFC + 10	x	tRFC + 10	x	ns	
Exit self refresh to a read command	tXSRD	200	x	200	x	tCK	
Exit precharge power down to any non-read command	tXP	2	x	2	x	tCK	
Exit active power down to read command	tXARD	2	x	2	x	tCK	1
Exit active power down to read command (slow exit, lower power)	tXARDS	6 - AL	x	6 - AL	x	tCK	1,2
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	3	x	3	x	tCK	27
ODT turn-on delay	tAOND	2	2	2	2	tCK	16
ODT turn-on	tAON	tAC(min)	tAC(max)+1	tAC(min)	tAC(max)+1	ns	16
ODT turn-on (Power-Down mode)	tAONPD	tAC(min)+2	2tCK+ tAC(max)+1	tAC(min)+2	2tCK+ tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK	17,44
ODT turn-off	tAOF	tAC(min)	tAC(max) + 0.6	tAC(min)	tAC(max) + 0.6	ns	17,44
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+ tAC(max)+1	tAC(min)+2	2.5tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3	x	3	x	tCK	
ODT power down exit latency	tAXPD	8	x	8	x	tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	32
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH	x	tIS+tCK+tIH	x	ns	15

14.0 General notes, which may apply for all AC parameters

1. DDR2 SDRAM AC timing reference load

Figure 1 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise repre sentation of the typical system environment or a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

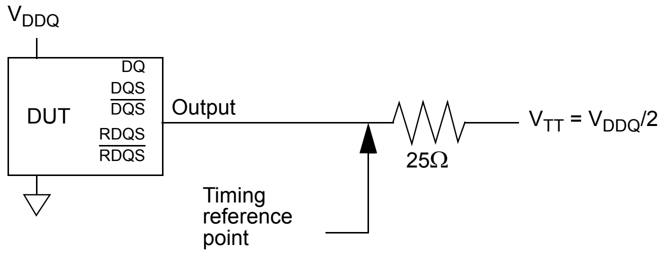


Figure 1 - AC Timing Reference Load

The output timing reference voltage level for single ended signals is the crosspoint with V_{TT}. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. $\overline{DQS}$) signal.

2. Slew Rate Measurement Levels

a) Output slew rate for falling and rising edges is measured between V_{TT} - 250 mV and V_{TT} + 250 mV for single ended signals. For differential signals (e.g. DQS - $\overline{DQS}$) output slew rate is measured between DQS - $\overline{DQS}$ = - 500 mV and DQS - $\overline{DQS}$ = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.
b) Input slew rate for single ended signals is measured from V_{REF}(DC) to $V_{IH(}$AC),min for rising edges and from V_{REF}(DC) to V_{IL}(AC),max for falling edges. For differential signals (e.g. CK - $\overline{CK}$) slew rate for rising edges is measured from CK - $\overline{CK}$ = - 250 mV to CK - $\overline{CK}$ = + 500 mV (+ 250 mV to - 500 mV for falling edges).
c) V_{ID} is the magnitude of the difference between the input voltage on CK and the input voltage on $\overline{CK}$, or between DQS and $\overline{DQS}$ for differential strobe.

3. DDR2 SDRAM output slew rate test load

Output slew rate is characterized under the test conditions as shown in Figure 2.

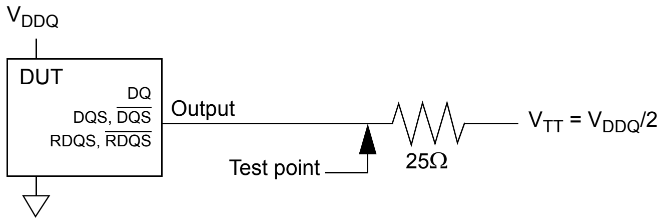


Figure 2 - Slew Rate Test Load

4. Differential data strobe

DDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS "Enable DQS" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, $\overline{DQS}$, must be tied externally to V_{SS} through a 20 Ω to 10 kΩ resistor to insure proper operation.

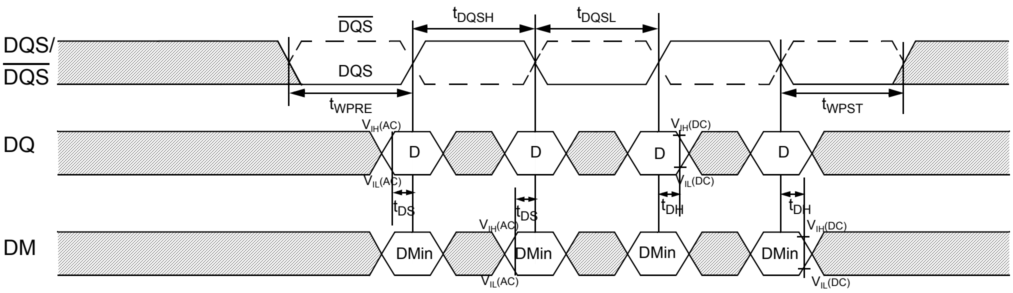


Figure 3 - Data Input (Write) Timing

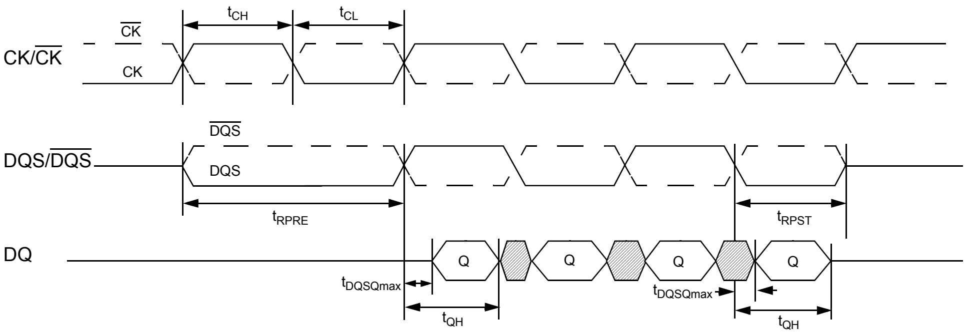


Figure 4 - Data Output (Read) Timing

5. AC timings are for linear signal transitions. See Specific Notes on derating for other signal transitions.

6. All voltages are referenced to V_{SS}.

7. These parameters guarantee device behavior, but they are not necessarily tested on each device.
They may be guaranteed by device design or tester correlation.

8. Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

15.0 Specific Notes for dedicated AC parameters

1. User can choose which active power down exit timing to use via MRS (bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing.

2. AL = Additive Latency.

3. This is a minimum requirement. Minimum read to precharge timing is AL + BL / 2 provided that the tRTP and tRAS(min) have been satisfied.

4. A minimum of two clocks (2 x tCK or 2 x nCK) is required irrespective of operating frequency.

5. Timings are specified with command/address input slew rate of 1.0 V/ns.

6. Timings are specified with DQs, DM, and DQS's (DQS/RDQS in single ended mode) input slew rate of 1.0V/ns.

7. Timings are specified with CK/$\overline{CK}$ differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1.0 V/ns in single ended mode.

8. Data setup and hold time derating.

Table 1 - DDR2-400/533 tDS/tDH derating with differential data strobe

ΔtDS, ΔtDH Derating Values of DDR2-400, DDR2-533 (ALL units in 'ps', the note applies to entire Table)																			
		DQS,$\overline{DQS}$ Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns		0.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	125	45	125	45	125	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	83	21	83	21	83	21	95	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-11	-14	-11	-14	1	-2	13	10	25	22	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-13	-19	-1	-7	11	5	23	17	-	-	-	-
	0.7	-	-	-	-	-	-	-31	-42	-19	-30	-7	-18	5	-6	17	6	-	-
	0.6	-	-	-	-	-	-	-	-	-43	-59	-31	-47	-19	-35	-7	-23	5	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-74	-89	-62	-77	-50	-65	-38	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-127	-140	-115	-128	-103	-116

Table 2 - DDR2-667/800 tDS/tDH derating with differential data strobe

ΔtDS, ΔtDH Derating Values for DDR2-667, DDR2-800 (ALL units in 'ps', the note applies to entire Table)																			
		DQS,$\overline{DQS}$ Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns		0.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
	0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
	0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

Table 3 - DDR2-400/533 tDS1/tDH1 derating with single-ended data strobe

ΔtDS1, ΔtDH1 Derating Values for DDR2-400, DDR2-533(All units in ‘ps’; the note applies to the entire table)																			
		DQS Single-ended Slew Rate																	
		2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns	
		ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1
DQ Slew rate V/ns	2.0	188	188	167	146	125	63	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	146	167	125	125	83	42	81	43	-	-	-	-	-	-	-	-	-	-
	1.0	63	125	42	83	0	0	-2	1	-7	-13	-	-	-	-	-	-	-	-
	0.9	-	-	31	69	-11	-14	-13	-13	-18	-27	-29	-45	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-27	-30	-32	-44	-43	-62	-60	-86	-	-	-	-
	0.7	-	-	-	-	-	-	-45	-53	-50	-67	-61	-85	-78	-109	-108	-152	-	-
	0.6	-	-	-	-	-	-	-	-	-74	-96	-85	-114	-102	-138	-138	-181	-183	-246
	0.5	-	-	-	-	-	-	-	-	-	-	-128	-156	-145	-180	-175	-223	-226	-288
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-210	-243	-240	-286	-291	-351

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the ΔtDS and ΔtDH derating value respectively. Example: tDS (total setup time) =tDS(base) +ΔtDS.

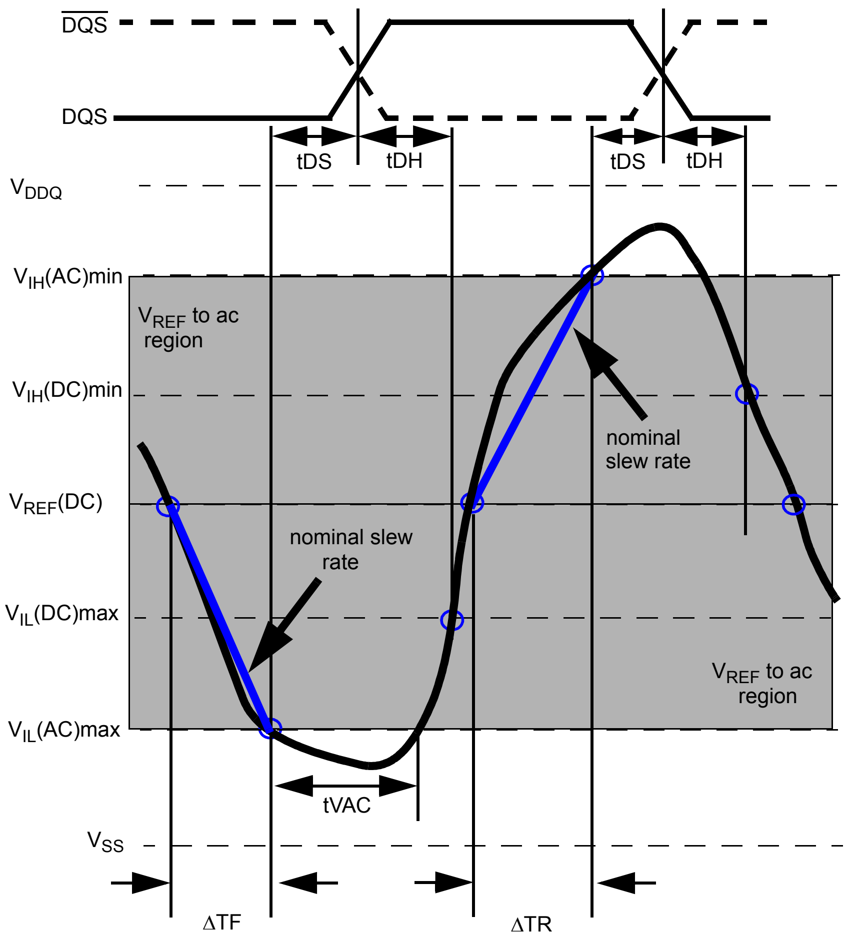
Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF}(DC) and the first crossing of V_{IH}(AC)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF}(DC) and the first crossing of V_{IL}(AC)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'V_{REF}(DC) to ac region', use nominal slew rate for derating value (See Figure 5 for differential data strobe and Figure 6 for single-ended data strobe.) If the actual signal is later than the nominal slew rate line anywhere between shaded 'V_{REF}(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 7 for differential data strobe and Figure 8 for single-ended data strobe)

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{IL}(DC)max and the first crossing of V_{REF}(DC). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{IH}(DC)min and the first crossing of V_{REF}(DC). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to V_{REF}(DC) region', use nominal slew rate for derating value (see Figure 9 for differential data strobe and Figure 10 for single-ended data strobe) If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V_{REF}(DC) region', the slew rate of a tangent line to the actual signal from the dc level to V_{REF}(DC) level is used for derating value (see Figure 11 for differential data strobe and Figure 12 for single-ended data strobe)

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}$(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(AC).

For slew rates in between the values listed in Tables 1, 2 and 3, the derating values may obtained by linear interpolation.

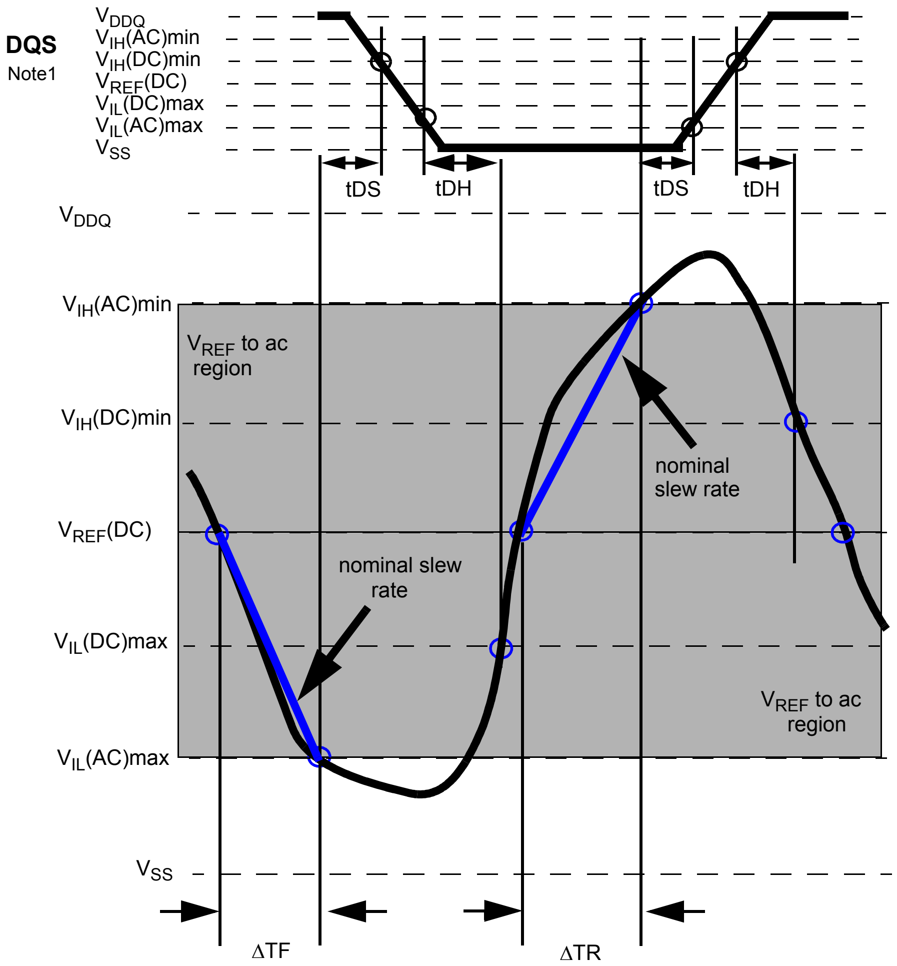
These values are typically not subject to production test. They are verified by design and characterization.



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF}(DC) - V_{IL}(AC)max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH}(AC)min - V_{REF}(DC)}{\Delta TR}$$

Figure 5 - Illustration of nominal slew rate for tDS (differential DQS,$\overline{DQS}$)



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF}(DC) - V_{IL}(AC)max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH}(AC)min - V_{REF}(DC)}{\Delta TR}$$

Note : DQS signal must be monotonic between $V_{IL}(AC)max$ and $V_{IH}(AC)min$.

Figure 6 - Illustration of nominal slew rate for tDS (single-ended DQS)

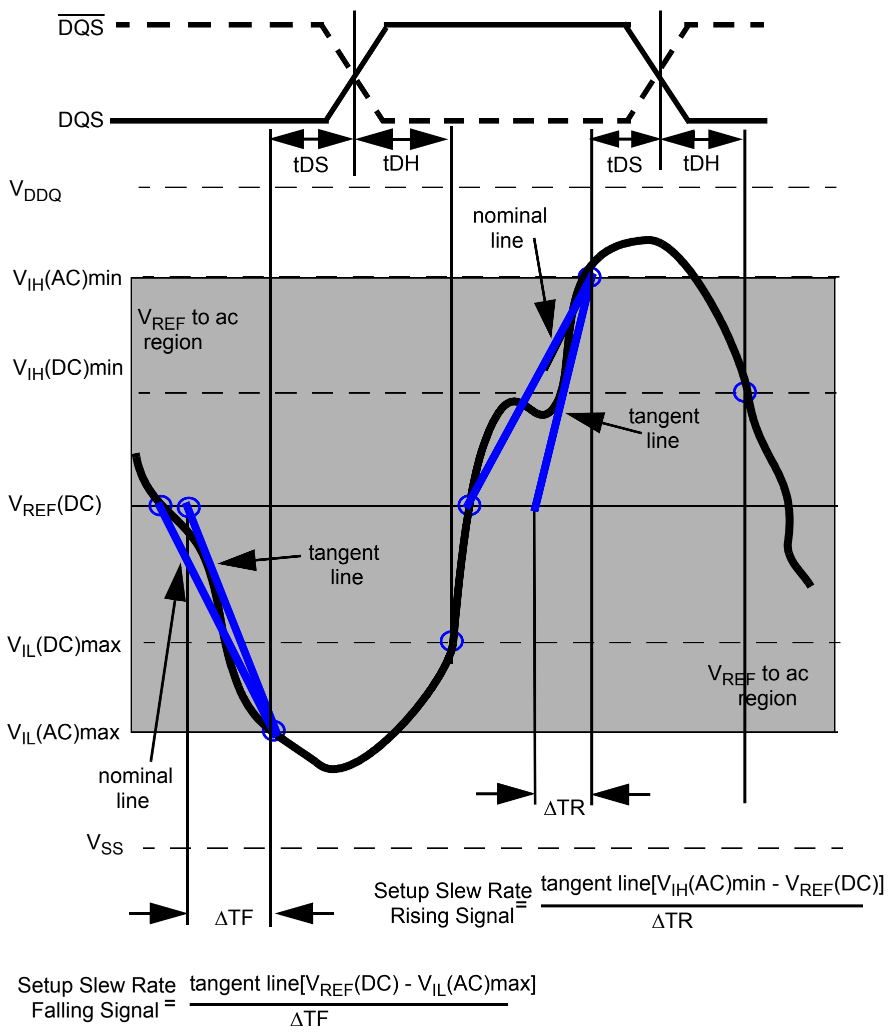
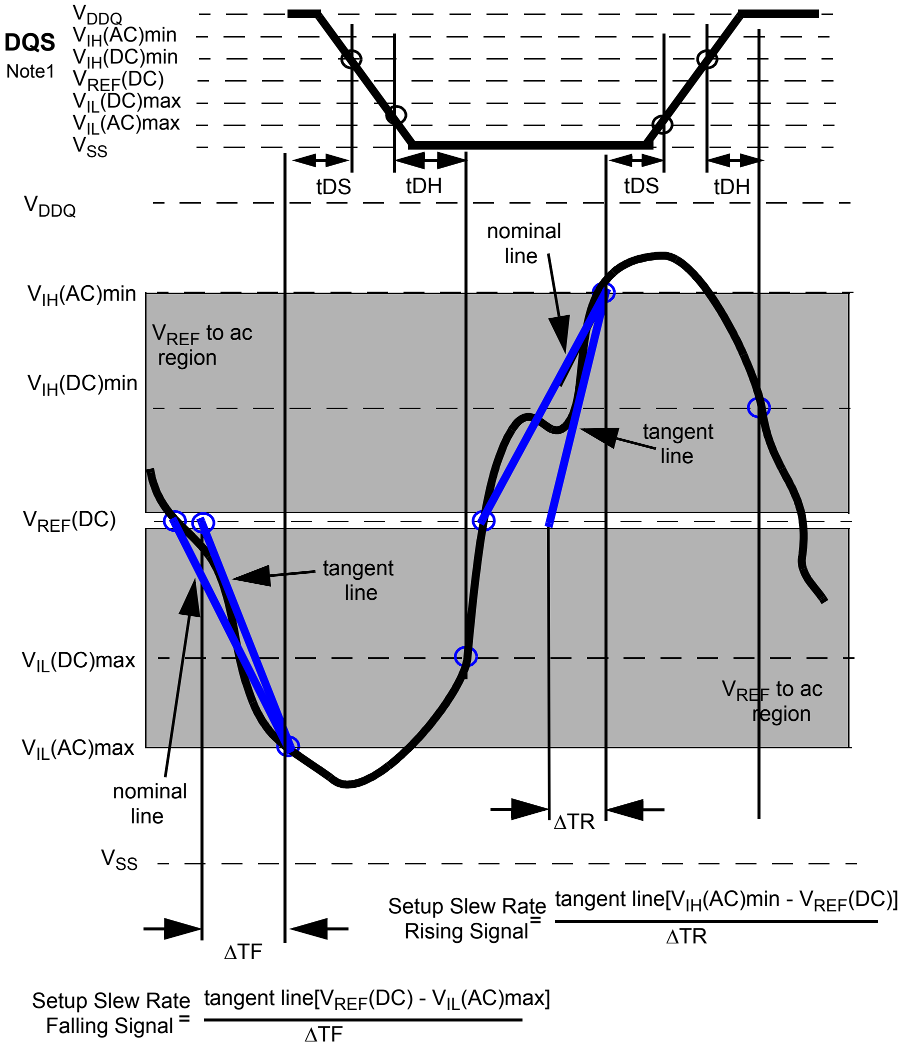
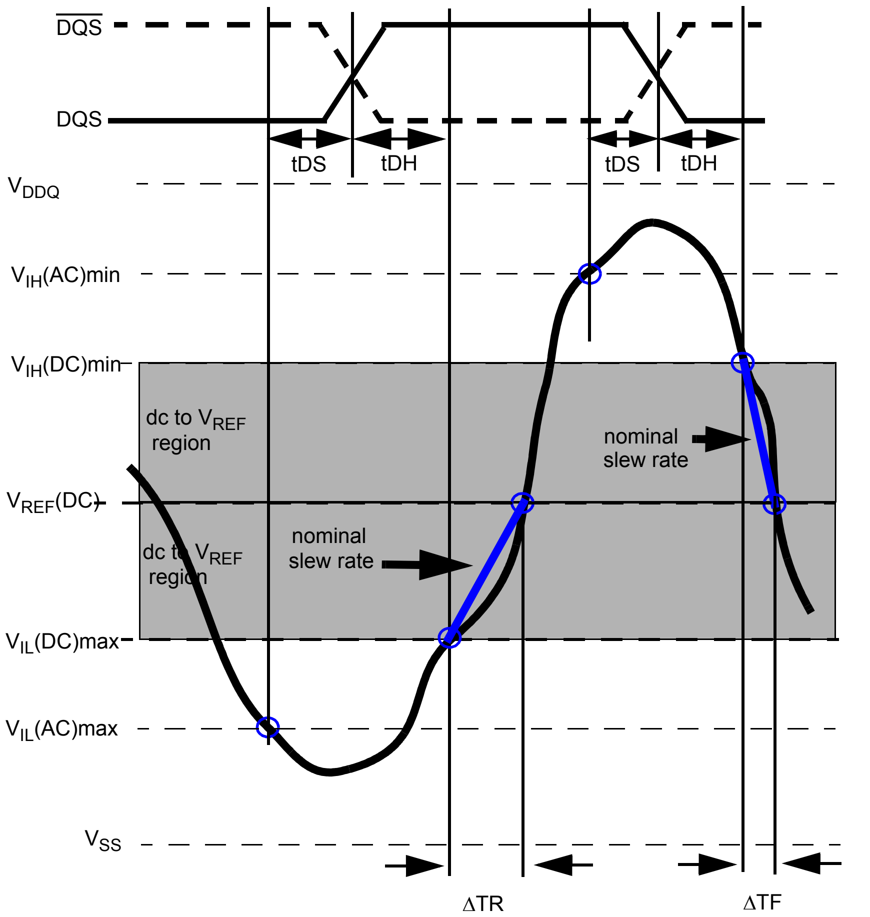


Figure 7 - Illustration of tangent line for tDS (differential DQS, $\overline{DQS}$)



Note : DQS signal must be monotonic between V_{IL}(DC)max and V_{IH}(DC)min.

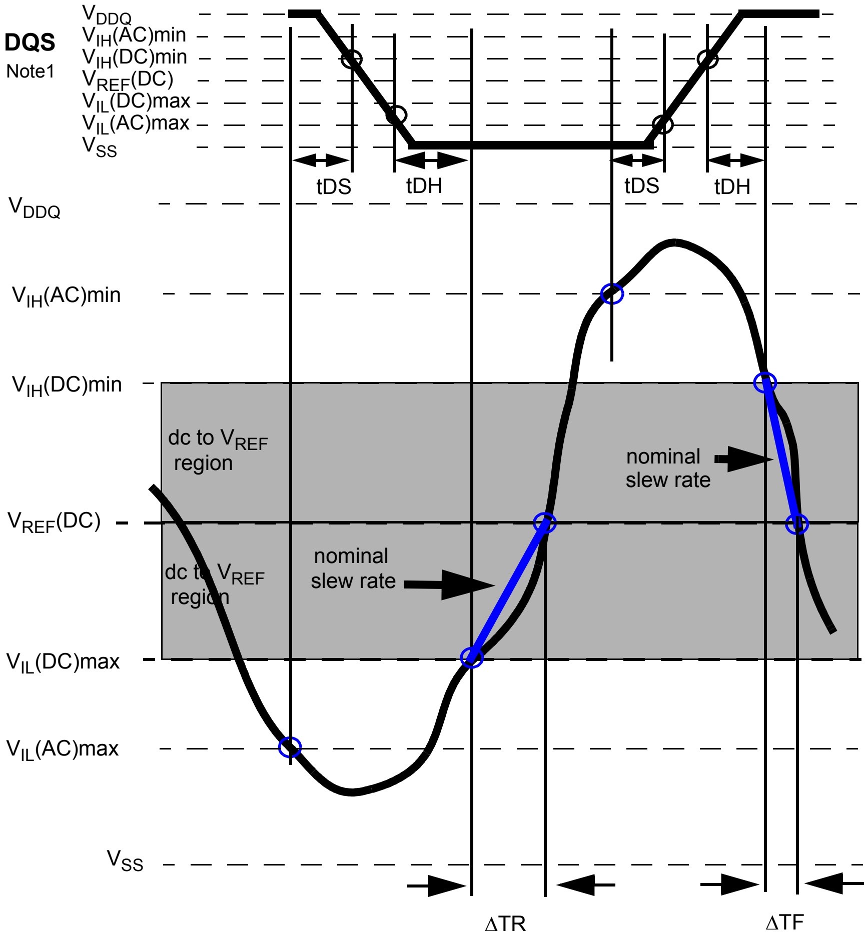
Figure 8 - Illustration of tangent line for tDS (single-ended DQS)



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF}(DC) - V_{IL}(DC)max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH}(DC)min - V_{REF}(DC)}{\Delta TF}$$

Figure 9 - Illustration of nominal slew rate for tDH (differential DQS, $\overline{\text{DQS}}$)

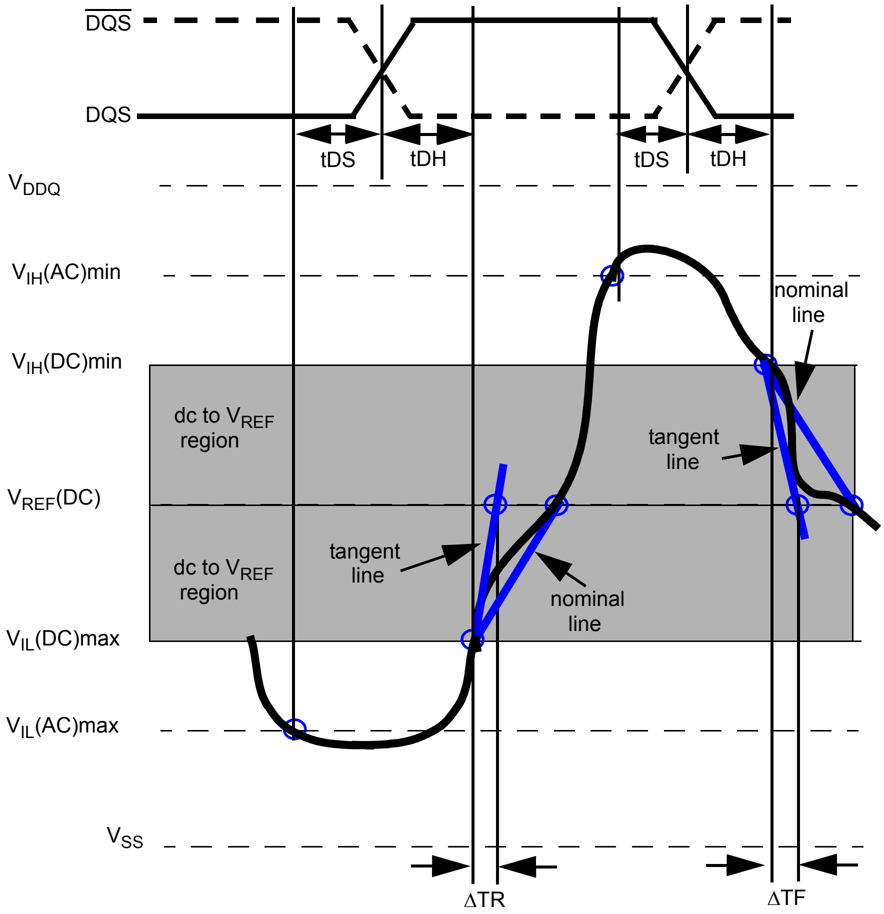


$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF}(DC) - V_{IL}(DC)max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH}(DC)min - V_{REF}(DC)}{\Delta TF}$$

Note : DQS signal must be monotonic between V_{IL}(DC)max and V_{IH}(DC)min.

Figure 10 - Illustration of nominal slew rate for tDH (single-ended DQS)

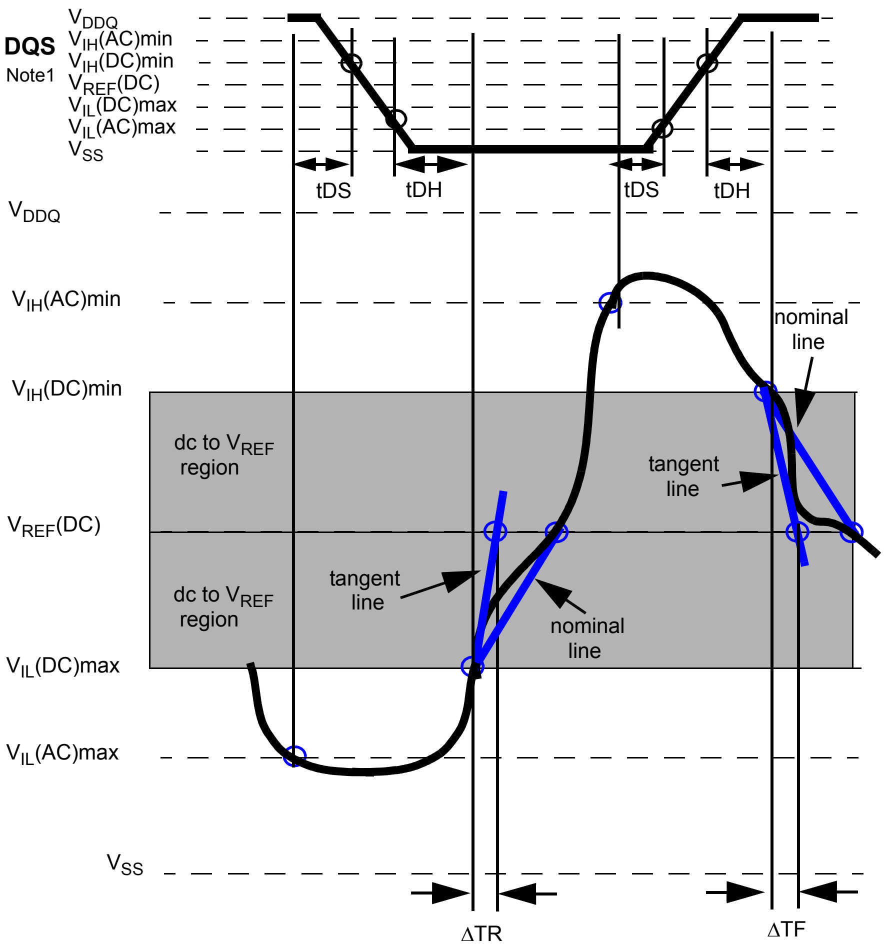


$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF}(DC) - V_{IL}(DC)max]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH}(DC)min - V_{REF}(DC)]}{\Delta TF}$$

Figure 11 - Illustration of tangent line for tDH (differential DQS, $\overline{\text{DQS}}$)

SAMSUNG ELECTRONICS



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF}(DC) - V_{IL}(DC)max]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH}(DC)min - V_{REF}(DC)]}{\Delta TF}$$

Note : DQS signal must be monotonic between $V_{IL}(DC)$max and $V_{IH}(DC)$min.

Figure 12 - Illustration of tangent line for tDH (single-ended DQS)

9. tIS and tIH (input setup and hold) derating

Table 4 - Derating values for DDR2-400, DDR2-533

∆tIS, ∆tIH Derating Values for DDR2-400, DDR2-533									
		CK, $\overline{CK}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns		Units	Notes
		∆tIS	∆tIH	∆tIS	∆tIH	∆tIS	∆tIH		
Command/ Address Slew rate(V/ns)	4.0	+187	+94	+217	+124	+247	+154	ps	1
	3.5	+179	+89	+209	+119	+239	+149	ps	1
	3.0	+167	+83	+197	+113	+227	+143	ps	1
	2.5	+150	+75	+180	+105	+210	+135	ps	1
	2.0	+125	+45	+155	+75	+185	+105	ps	1
	1.5	+83	+21	+113	+51	+143	+81	ps	1
	1.0	0	0	+30	+30	+60	+60	ps	1
	0.9	-11	-14	+19	+16	+49	+46	ps	1
	0.8	-25	-31	+5	-1	+35	+29	ps	1
	0.7	-43	-54	-13	-24	+17	+6	ps	1
	0.6	-67	-83	-37	-53	-7	-23	ps	1
	0.5	-110	-125	-80	-95	-50	-65	ps	1
	0.4	-175	-188	-145	-158	-115	-128	ps	1
	0.3	-285	-292	-255	-262	-225	-232	ps	1
	0.25	-350	-375	-320	-345	-290	-315	ps	1
	0.2	-525	-500	-495	-470	-465	-440	ps	1
	0.15	-800	-708	-770	-678	-740	-648	ps	1
	0.1	-1450	-1125	-1420	-1095	-1390	-1065	ps	1

Table 5 - Derating values for DDR2-667, DDR2-800

∆tIS and ∆tIH Derating Values for DDR2-667, DDR2-800									
		CK, $\overline{CK}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns		Units	Notes
		∆tIS	∆tIH	∆tIS	∆tIH	∆tIS	∆tIH		
Command/ Address Slew rate(V/ns)	4.0	+150	+94	+180	+124	+210	+154	ps	1
	3.5	+143	+89	+173	+119	+203	+149	ps	1
	3.0	+133	+83	+163	+113	+193	+143	ps	1
	2.5	+120	+75	+150	+105	+180	+135	ps	1
	2.0	+100	+45	+130	+75	+160	+105	ps	1
	1.5	+67	+21	+97	+51	+127	+81	ps	1
	1.0	0	0	+30	+30	+60	+60	ps	1
	0.9	-5	-14	+25	+16	+55	+46	ps	1
	0.8	-13	-31	+17	-1	+47	+29	ps	1
	0.7	-22	-54	+8	-24	+38	+6	ps	1
	0.6	-34	-83	-4	-53	+26	-23	ps	1
	0.5	-60	-125	-30	-95	0	-65	ps	1
	0.4	-100	-188	-70	-158	-40	-128	ps	1
	0.3	-168	-292	-138	-262	-108	-232	ps	1
	0.25	-200	-375	-170	-345	-140	-315	ps	1
	0.2	-325	-500	-295	-470	-265	-440	ps	1
	0.15	-517	-708	-487	-678	-457	-648	ps	1
	0.1	-1000	-1125	-970	-1095	-940	-1065	ps	1

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value to the ∆tIS and ∆tIH derating value respectively. Example: tIS (total setup time) = tIS(base) + ∆tIS

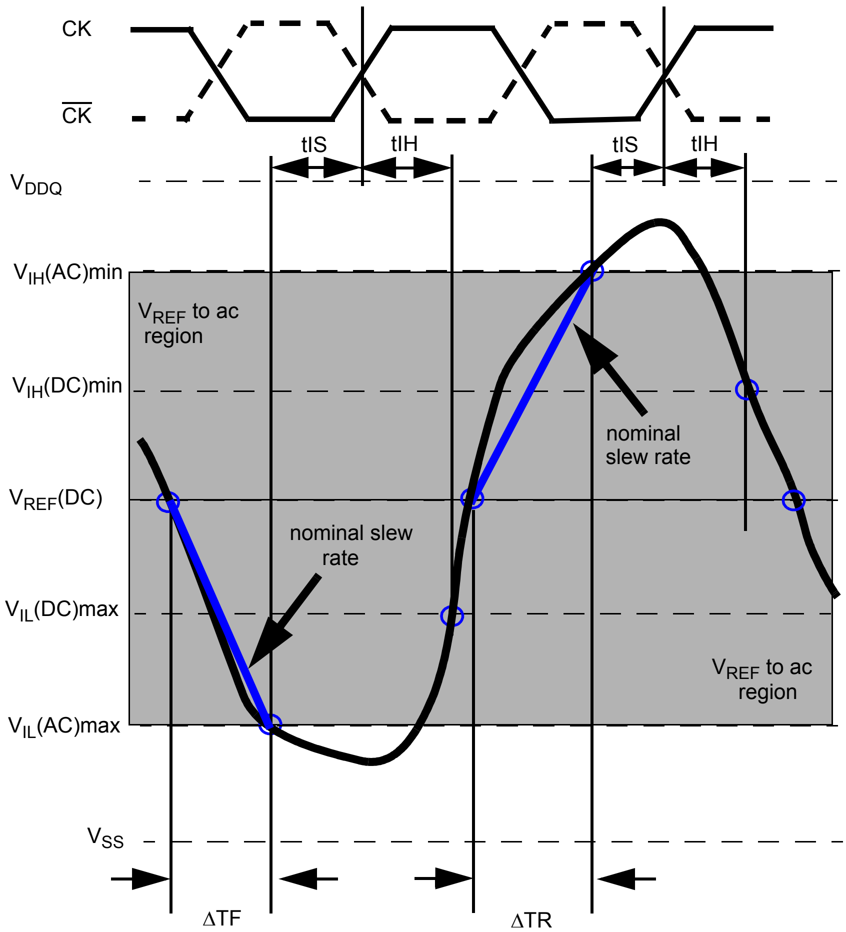
Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF}(DC) and the first crossing of V_{IH}(AC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF}(DC) and the first crossing of V_{IL}(AC)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'V_{REF}(DC) to ac region', use nominal slew rate for derating value (see Figure 13). If the actual signal is later than the nominal slew rate line anywhere between shaded 'V_{REF}(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 14).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{IL}(DC)max and the first crossing of V_{REF}(DC). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{IH}(DC)min and the first crossing of V_{REF}(DC). If the actual signal is always later than the nominal slewrate line between shaded 'dc to V_{REF}(DC) region', use nominal slew rate for derating value (see Figure 15). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V_{REF}(DC) region', the slew rate of a tangent line to the actual signal from the dc level to V_{REF}(DC) level is used for derating value (see Figure 16).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}$(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(AC).

For slew rates in between the values listed in Tables 4 and 5, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF}(DC) - V_{IL}(AC)max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH}(AC)min - V_{REF}(DC)}{\Delta TR}$$

Figure 13 - Illustration of nominal slew rate for tIS

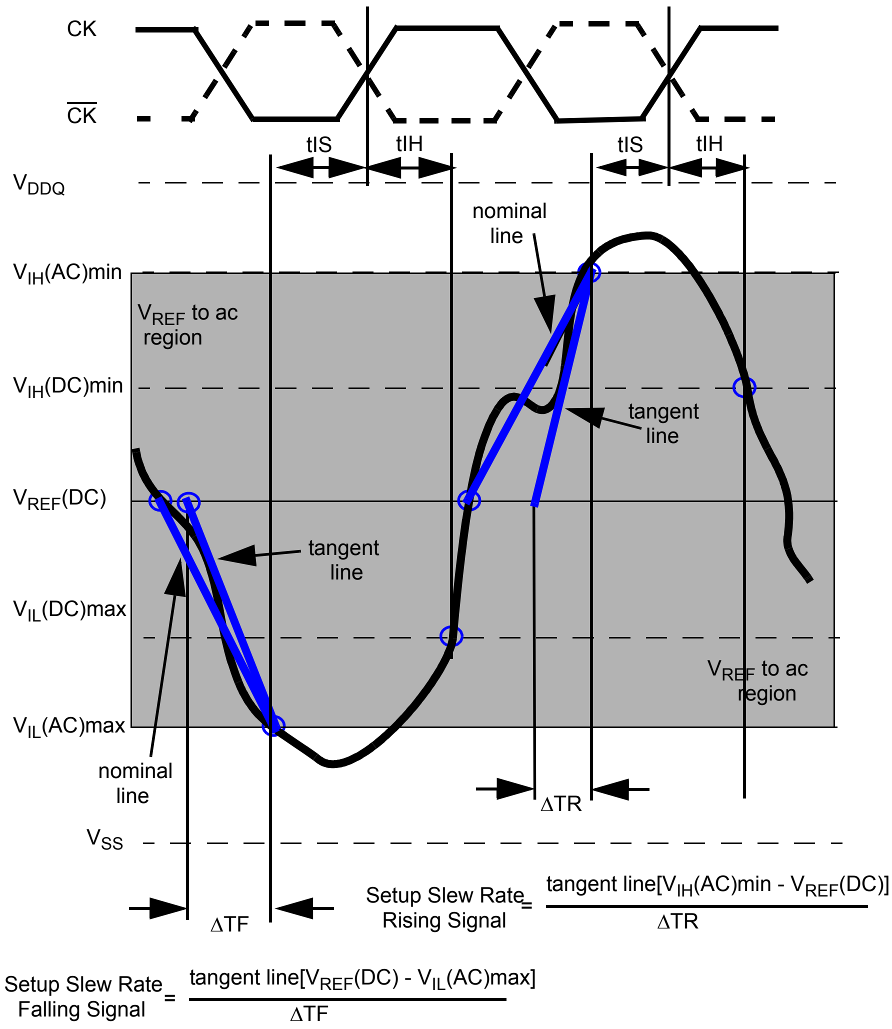
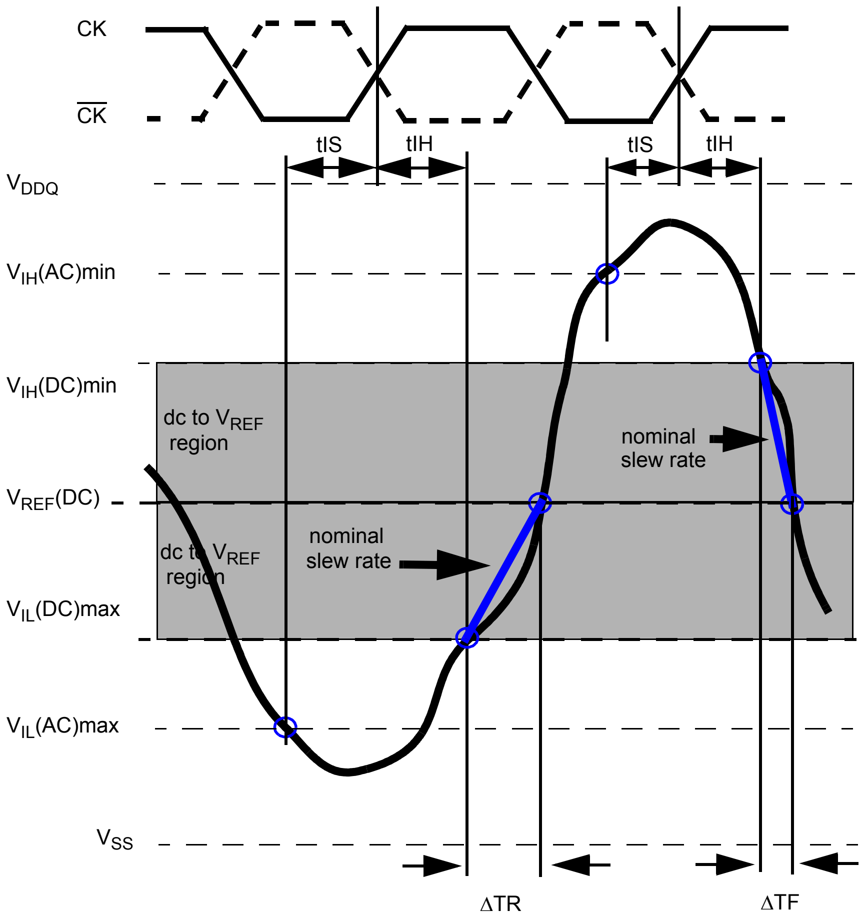


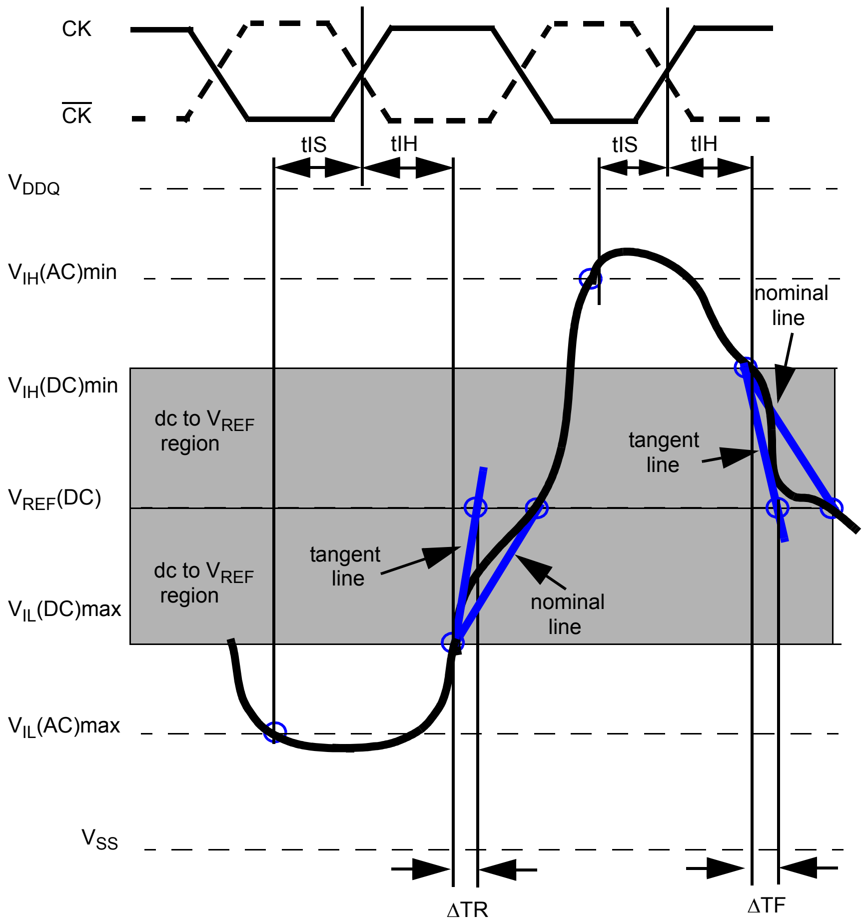
Figure 14 - Illustration of tangent line for tIS



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF}(DC) - V_{IL}(DC)max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH}(DC)min - V_{REF}(DC)}{\Delta TF}$$

Figure 15 - Illustration of nominal slew rate for tIH



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF}(DC) - V_{IL}(DC)max]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH}(DC)min - V_{REF}(DC)]}{\Delta TF}$$

Figure 16 - Illustration of tangent line for tIH

10. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

11. MIN (tCL, tCH) refers to the smaller of the actual clock LOW time and the actual clock HIGH time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH). For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

12. tQH = tHP - tQHS, where :
tHP = minimum half clock period for any given cycle and is defined by clock HIGH or clock LOW (tCH, tCL).
tQHS accounts for:
1) The pulse duration distortion of on-chip clock circuits; and
2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

13. tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS/ $\overline{\text{DQS}}$ and associated DQ in any given cycle.

14. tDAL = WR + RU{ tRP[ns] / tCK[ns] }, where RU stands for round up.
WR refers to the tWR parameter stored in the MRS. For tRP, if the result of the division is not already an integer, round up to the next highest integer. tCK refers to the application clock period.

Example: For DDR533 at tCK = 3.75ns with WR programmed to 4 clocks.

tDAL = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.

15. The clock frequency is allowed to change during self refresh mode or precharge power-down mode.

16. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND, which is interpreted differently per speed bin. For DDR2-400/533, tAOND is 10 ns (= 2 x 5 ns) after the clock edge that registered a first ODT HIGH if tCK = 5 ns. For DDR2-667/800, tAOND is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

17. ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD, which is interpreted differently per speed bin. For DDR2-400/533, tAOFD is 12.5 ns (= 2.5 x 5 ns) after the clock edge that registered a first ODT LOW if tCK = 5 ns. For DDR2-667/800, if tCK(avg) = 3 ns is assumed, tAOFD is 1.5 ns (= 0.5 x 3 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

18. tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begins driving (tLZ) . Figure 17 shows a method to calculate the point when device is no longer driving (tHZ), or beginsdriving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. tLZ(DQ) refers to tLZ of the DQS and tLZ(DQS) refers to tLZ of the (U/L/R)DQS and $\overline{\text{(U/L/R)DQS}}$ each treated as single-ended signal.

19. tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). Figure 17 shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

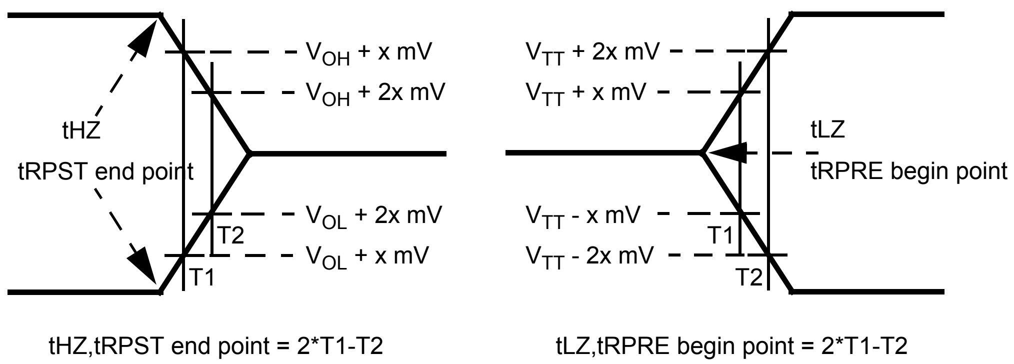


Figure 17 - Method for calculating transitions and endpoints

20. Input waveform timing tDS with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the V_{IH}(AC) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the V_{IL}(AC) level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, $\overline{DQS}$ signals must be monotonic between V_{IL}(DC)max and V_{IH}(DC)min. See Figure 18.

21. Input waveform timing tDH with differential data strobe enabled MR[bit10]=0, is referenced from the differential data strobe crosspoint to the input signal crossing at the V_{IH}(DC) level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the V_{IL}(DC) level for a rising signal applied to the device under test. DQS, $\overline{DQS}$ signals must be monotonic between V_{IL}(DC)max and V_{IH}(DC)min. See Figure 18.

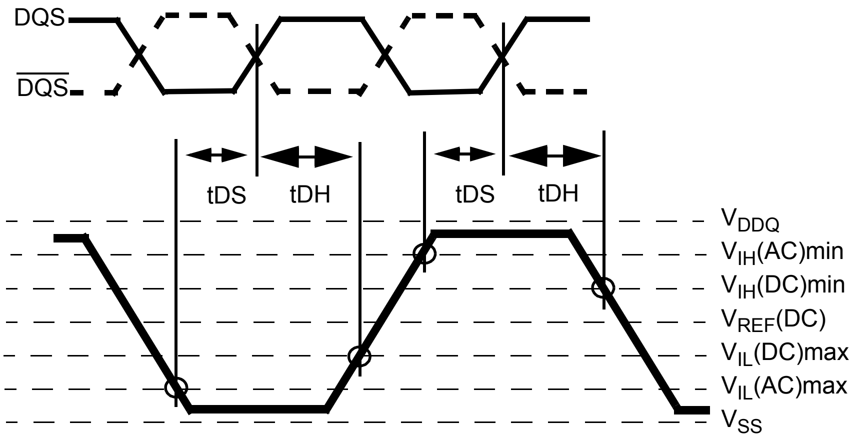


Figure 18 - Differential input waveform timing - tDS and tDH

22. Input waveform timing is referenced from the input signal crossing at the V_{IH}(AC) level for a rising signal and V_{IL}(AC) for a falling signal applied to the device under test. See Figure 19.

23. Input waveform timing is referenced from the input signal crossing at the V_{IL}(DC) level for a rising signal and V_{IH}(DC) for a falling signal applied to the device under test. See Figure 19.

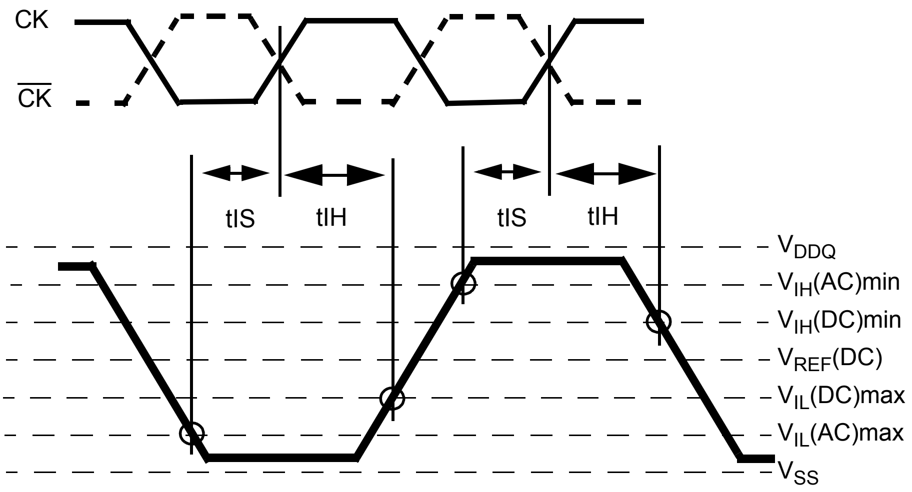


Figure 19 - Differential input waveform timing - tIS and tIH

SAMSUNG ELECTRONICS

24. tWTR is at lease two clocks (2 x tCK or 2 x nCK) independent of operation frequency.

25. Input waveform timing with single-ended data strobe enabled MR[bit10] = 1, is referenced from the input signal crossing at the V_{IH}(AC) level to the single-ended data strobe crossing $V_{IH/L}$(DC) at the start of its transition for a rising signal, and from the input signal crossing at the V_{IL}(AC) level to the single-ended data strobe crossing $V_{IH/L}$(DC) at the start of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between V_{IL}(DC)max and V_{IH}(DC)min.

26. Input waveform timing with single-ended data strobe enabled MR[bit10] = 1, is referenced from the input signal crossing at the V_{IH}(DC) level to the single-ended data strobe crossing $V_{IH/L}$(AC) at the end of its transition for a rising signal, and from the input signal crossing at the V_{IL}(DC) level to the single-ended data strobe crossing $V_{IH/L}$(AC) at the end of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between V_{IL}(DC)max and V_{IH}(DC)min.

27. tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.

28. If tDS or tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

29. These parameters are measured from a command/address signal (CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

30. These parameters are measured from a data strobe signal ((L/U/R)DQS/$\overline{DQS}$) crossing to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

31. These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS/$\overline{DQS}$) crossing.

32. For these parameters, the DDR2 SDRAM device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}, which is in clock cycles, assuming all input clock jitter specifications are satisfied.
For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2-667 5-5-5, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm+5 is valid even if (Tm+5 - Tm) is less than 15ns due to input clock jitter.

33. tDAL [nCK] = WR [nCK] + tnRP [nCK] = WR + RU {tRP [ps] / tCK(avg) [ps] }, where WR is the value programmed in the mode register set.

34. New units, 'tCK(avg)' and 'nCK', are introduced in DDR2-667 and DDR2-800. Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
Note that in DDR2-400 and DDR2-533, 'tCK' is used for both concepts.
ex) tXP = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm+2, even if (Tm+2 - Tm) is 2 x tCK(avg) + tERR(2per),min.

35. Input clock jitter spec parameter. These parameters and the ones in the table below are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2-667 and DDR2-800 only. The jitter specified is a random jitter meeting a Gaussian distribution.

Parameter	Symbol	DDR2-667		DDR2-800		units	Notes
		Min	Max	Min	Max		
Clock period jitter	tJIT(per)	-125	125	-100	100	ps	35
Clock period jitter during DLL locking period	tJIT(per,lck)	-100	100	-80	80	ps	35
Cycle to cycle clock period jitter	tJIT(cc)	-250	250	-200	200	ps	35
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	-200	200	-160	160	ps	35
Cumulative error across 2 cycles	tERR(2per)	-175	175	-150	150	ps	35
Cumulative error across 3 cycles	tERR(3per)	-225	225	-175	175	ps	35
Cumulative error across 4 cycles	tERR(4per)	-250	250	-200	200	ps	35
Cumulative error across 5 cycles	tERR(5per)	-250	250	-200	200	ps	35
Cumulative error across n cycles, n = 6 ... 10, inclusive	tERR(6-10per)	-350	350	-300	300	ps	35
Cumulative error across n cycles, n = 11 ... 50, inclusive	tERR(11-50per)	-450	450	-450	450	ps	35
Duty cycle jitter	tJIT(duty)	-125	125	-100	100	ps	35

Definitions :

- tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$

where $N = 200$

- tCH(avg) and tCL(avg)

tCH(avg) is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$

where $N = 200$

tCL(avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$

where $N = 200$

- tJIT(duty)

tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg).

tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)}
where,
tJIT(CH) = {tCHi- tCH(avg) where i=1 to 200}
tJIT(CL) = {tCLi- tCL(avg) where i=1 to 200}

- tJIT(per), tJIT(per,lck)

tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg).
tJIT(per) = Min/max of {tCKi- tCK(avg) where i=1 to 200}

tJIT(per) defines the single period jitter when the DLL is already locked.
tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
tJIT(per) and tJIT(per,lck) are not guaranteed through final production testing.

- tJIT(cc), tJIT(cc,lck)

tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles : tJIT(cc) = Max of $|tCK_{i+1} - tCK_i|$
tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
tJIT(cc) and tJIT(cc,lck) are not guaranteed through final production testing.

- tERR(2per), tERR (3per), tERR (4per), tERR (5per), tERR (6-10per) and tERR (11-50per)

tERR is defined as the cumulative error across multiple consecutive cycles from tCK(avg).

$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

where
$$\begin{cases} n = 2 & for\ tERR(2per) \\ n = 3 & for\ tERR(3per) \\ n = 4 & for\ tERR(4per) \\ n = 5 & for\ tERR(5per) \\ 6 \le n \le 10 & for\ tERR(6\text{-}10per) \\ 11 \le n \le 50 & for\ tERR(11\text{-}50per) \end{cases}$$

36. These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min and max of SPEC values are to be used for calculations in the table below.)

Parameter	Symbol	Min	Max	Units
Absolute clock Period	tCK(abs)	tCK(avg),min + tJIT(per),min	tCK(avg),max + tJIT(per),max	ps
Absolute clock HIGH pulse width	tCH(abs)	tCH(avg),min x tCK(avg),min + tJIT(duty),min	tCH(avg),max x tCK(avg),max + tJIT(duty),max	ps
Absolute clock LOW pulse width	tCL(abs)	tCL(avg),min x tCK(avg),min + tJIT(duty),min	tCL(avg),max x tCK(avg),max + tJIT(duty),max	ps

Example: For DDR2-667, tCH(abs),min = (0.48 x 3000 ps) - 125 ps = 1315 ps

37. tHP is the minimum of the absolute half period of the actual input clock. tHP is an input parameter but not an input specification parameter. It is used in conjunction with tQHS to derive the DRAM output timing tQH. The value to be used for tQH calculation is determined by the following equation;
tHP = Min (tCH(abs), tCL(abs)),
where,
tCH(abs) is the minimum of the actual instantaneous clock HIGH time;
tCL(abs) is the minimum of the actual instantaneous clock LOW time;

38. tQHS accounts for:
1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual tHP at the input is transferred to the output; and
2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to n-channel variation of the output drivers

39. tQH = tHP - tQHS, where:
tHP is the minimum of the absolute half period of the actual input clock; and tQHS is the specification value under the max column.
{The less half-pulse width distortion present, the larger the tQH value is; and the larger the valid data eye will be.}
Examples:
1) If the system provides tHP of 1315 ps into a DDR2-667 SDRAM, the DRAM provides tQH of 975 ps minimum.
2) If the system provides tHP of 1420 ps into a DDR2-667 SDRAM, the DRAM provides tQH of 1080 ps minimum.

40. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 ps and tERR(6-10per),max = + 293 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(6-10per),max = - 400 ps - 293 ps = - 693 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(6-10per),min = 400 ps + 272 ps = + 672 ps. Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ),min(derated) = - 900 ps - 293 ps = - 1193 ps and tLZ(DQ),max(derated) = 450 ps + 272 ps = + 722 ps.

41. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per) of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tJIT(per),min = - 72 ps and tJIT(per),max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),min = 0.9 x tCK(avg) - 72 ps = + 2178 ps and tRPRE,max(derated) = tRPRE,max + tJIT(per),max = 1.1 x tCK(avg) + 93 ps = + 2843 ps.

42. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(duty) of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tJIT(duty),min = - 72 ps and tJIT(duty),max = + 93 ps, then tRPST,min(derated) = tRPST,min + tJIT(duty),min = 0.4 x tCK(avg) - 72 ps = + 928 ps and tRPST,max(derated) = tRPST,max + tJIT(duty),max = 0.6 x tCK(avg) + 93 ps = + 1592 ps.

43. When the device is operated with input clock jitter, this parameter needs to be derated by { - tJIT(duty),max - tERR(6-10per),max } and { - tJIT(duty),min - tERR(6-10per),min } of the actual input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min = - 272 ps, tERR(6- 10per),max = + 293 ps, tJIT(duty),min = - 106 ps and tJIT(duty),max = + 94 ps, then tAOF,min(derated) = tAOF,min + { - tJIT(duty),max - tERR(6-10per),max } = - 450 ps + { - 94 ps - 293 ps} = - 837 ps and tAOF,max(derated) = tAOF,max + { - tJIT(duty),min - tERR(6-10per),min } = 1050 ps + { 106 ps + 272 ps } = + 1428 ps.

44. For tAOFD of DDR2-400/533, the 1/2 clock of tCK in the 2.5 x tCK assumes a tCH, input clock HIGH pulse width of 0.5 relative to tCK. tAOF,min and tAOF,max should each be derated by the same amount as the actual amount of tCH offset present at the DRAM input with respect to 0.5.

For example, if an input clock has a worst case tCH of 0.45, the tAOF,min should be derated by subtracting 0.05 x tCK from it, whereas if an input clock has a worst case tCH of 0.55, the tAOF,max should be derated by adding 0.05 x tCK to it. Therefore, we have;

tAOF,min(derated) = tAC,min - [0.5 - Min(0.5, tCH,min)] x tCK
tAOF,max(derated) = tAC,max + 0.6 + [Max(0.5, tCH,max) - 0.5] x tCK
or
tAOF,min(derated) = Min(tAC,min, tAC,min - [0.5 - tCH,min] x tCK)
tAOF,max(derated) = 0.6 + Max(tAC,max, tAC,max + [tCH,max - 0.5] x tCK)
where tCH,min and tCH,max are the minimum and maximum of tCH actually measured at the DRAM input balls.

45. For tAOFD of DDR2-667/800, the 1/2 clock of nCK in the 2.5 x nCK assumes a tCH(avg), average input clock HIGH pulse width of 0.5 relative to tCK(avg). tAOF,min and tAOF,max should each be derated by the same amount as the actual amount of tCH(avg) offset present at the DRAM input with respect to 0.5.

For example, if an input clock has a worst case tCH(avg) of 0.48, the tAOF,min should be derated by subtracting 0.02 x tCK(avg) from it, whereas if an input clock has a worst case tCH(avg) of 0.52, the tAOF,max should be derated by adding 0.02 x tCK(avg) to it. Therefore, we have;

tAOF,min(derated) = tAC,min - [0.5 - Min(0.5, tCH(avg),min)] x tCK(avg)
tAOF,max(derated) = tAC,max + 0.6 + [Max(0.5, tCH(avg),max) - 0.5] x tCK(avg)
tAOF,min(derated) = Min(tAC,min, tAC,min - [0.5 - tCH(avg),min] x tCK(avg))
tAOF,max(derated) = 0.6 + Max(tAC,max, tAC,max + [tCH(avg),max - 0.5] x tCK(avg))
where tCH(avg),min and tCH(avg),max are the minimum and maximum of tCH(avg) actually measured at the DRAM input balls.

Note : that these deratings are in addition to the tAOF derating per input clock jitter, i.e. tJIT(duty) and tERR(6-10per). However tAC values used in the equations shown above are from the timing parameter table and are not derated. Thus the final derated values for tAOF are;

tAOF,min(derated_final) = tAOF,min(derated) + { - tJIT(duty),max - tERR(6-10per),max }
tAOF,max(derated_final) = tAOF,max(derated) + { - tJIT(duty),min - tERR(6-10per),min }