iC-NQ

13-bit Sin/D CONVERTER WITH CALIBRATION

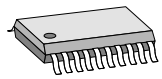
FEATURES

- Resolution of up to 8192 angle steps per sine/cosine period
- Binary and decimal resolution settings, e.g. 500, 512, 1000, 1024; programmable angle hysteresis
- Conversion time of just 250 ns including amplifier settling
- Count-safe vector follower principle, realtime system with 70 MHz sampling rate
- Direct sensor connection; selectable input gain
- Front-end signal conditioning features offset (8 bit), amplitude ratio (5 bit) and phase (6 bit) calibration
- 250 kHz input frequency
- Parameterization and absolute angle output via bidirectional high-speed synchronous-serial BiSS Interface (B protocol)
- A QUAD B incremental outputs with selectable minimum transition distance (e.g. 0.25 µs for 1 MHz at A)
- Index signal processing adjustable in position and width
- Fault monitoring: frequency, amplitude, configuration (CRC)
- Multiturn counting to 8 bit or 24 bit
- Fully re-programmable by BiSS interface with access to serial EEPROM to store setup
- ESD protection and TTL-/CMOS-compatible outputs

APPLICATIONS

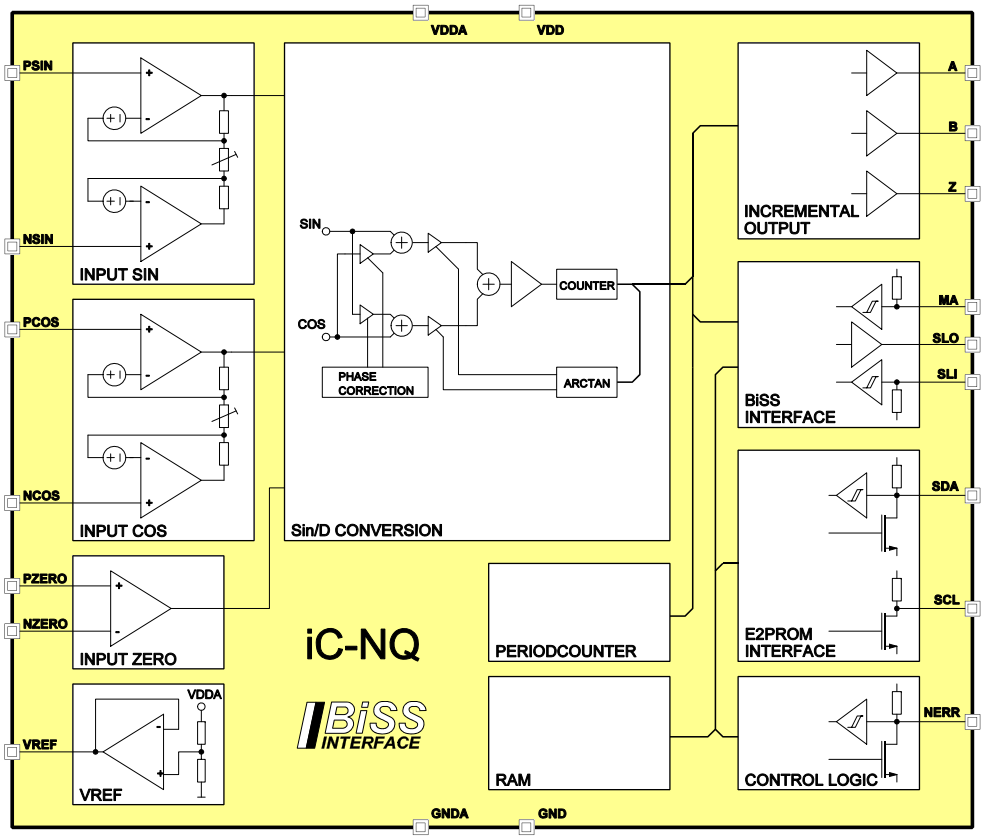
- Interpolator IC for position data acquisition from analog sine/cosine sensors
- Optical linear/rotary encoders
- MR sensor systems

PACKAGES



TSSOP20

BLOCK DIAGRAM



DESCRIPTION

iC-NQ is a monolithic A/D converter which, by applying a count-safe vector follower principle, converts sine/cosine sensor signals with a selectable resolution and hysteresis into angle position data. This absolute value is output via a high-speed synchronous-serial BiSS interface and trails a master clock rate of up to 10 Mbit/s, or, alternatively, can be set so that it is compatible with SSI. A period counter supplements the position data with a multiturn count and can be configured for BiSS single-cycle data output.

At the same time any changes in output data are converted into incremental A QUAD B encoder signals. Here, the minimum transition distance can be adapted to suit the system on hand (cable length, external counter). A synchronised zero index is generated and output to Z if enabled by the PZERO and NZERO inputs.

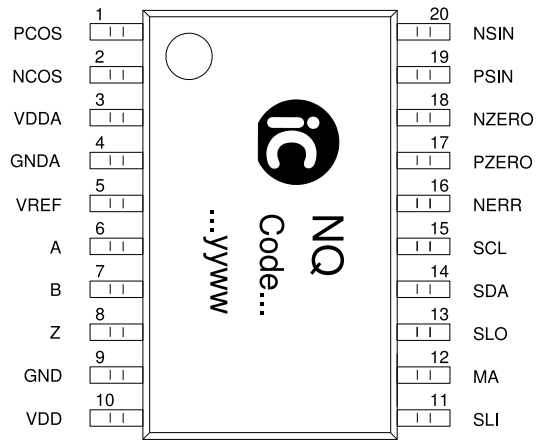
The front-end amplifiers are configured as instrumentation amplifiers, permitting sensor bridges to be directly connected without the need for external resistors. Various programmable D/A converters are available for the conditioning of sine/cosine sensor signals with regard to offset, amplitude ratio and phase errors. Front-end gain can be set in stages graded to suit all common differential sensor signals from approximately 20 mVpp to 1.5 Vpp, and also single-ended sensor signals from 40 mVpp to 3 Vpp respectively.

Two serial interfaces have been included to permit configuration of the device, connection of an EEPROM or synchronous-serial data transfer (BiSS). Both interfaces are bidirectional and enable the complete configuration of the device including the transfer of setup and system data to the EEPROM for permanent storage. If the memory is detected following a power-down reset, the chip setup is read in and automatically repeated if a CRC error occurs.

CONTENTS

PACKAGES TSSOP20 (according to JEDEC Standard)

PIN CONFIGURATION
TSSOP20 4.4 mm, lead pitch 0.65 mm



PIN FUNCTIONS

No.	Name	Function
1	PCOS	Input Cosine +
2	NCOS	Input Cosine -
3	VDDA	+5 V Supply Voltage (analog)
4	GNDA	Ground (analog)
5	VREF	Reference Voltage Output
6	A	Incremental Output A Analog signal COS+ (TMA mode) PWM signal for Offset Sine (Calib.)
7	B	Incremental Output B Analog signal COS- (TMA mode) PWM signal for Offset Cosine (Calib.)
8	Z	Output Index Z PWM signal for Phase/Ratio (Calib.)
9	GND	Ground
10	VDD	+5 V Supply Voltage (digital)
11	SLI	BiSS interface, data input
12	MA	BiSS interface, clock line
13	SLO	BiSS interface, data output
14	SDA	EEPROM interface, data line Analog signal SIN+ (TMA mode)
15	SCL	EEPROM interface, clock line Analog signal SIN- (TMA mode)
16	NERR	Error Input/Output, active low
17	PZERO	Input Zero Signal +
18	NZERO	Input Zero Signal -
19	PSIN	Input Sine +
20	NSIN	Input Sine -

External connections linking VDDA to VDD and GND to GNDA are required.
*) If only a single iC-NQ device and no BiSS chain circuitry is used, pin SLI can remain unwired or can be linked to ground (GND).

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDDA	Analog Supply Voltage		-0.3	6	V
G002	VDD	Digital Supply Voltage		-0.3	6	V
G003	Vpin()	Voltage at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, MA, SLI, SLO, A, B, Z	V() < VDDA + 0.3 V V() < VDD + 0.3 V	-0.3	6	V
G004	Imx(VDDA)	Current in VDDA		-50	50	mA
G005	Imx(GNDA)	Current in GNDA		-50	50	mA
G006	Imx(VDD)	Current in VDD		-50	50	mA
G007	Imx(GND)	Current in GND		-50	50	mA
G008	Imx()	Current in PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, MA, SLI, SLO, A, B, Z		-10	10	mA
G009	Ilu()	Pulse Current in all pins (Latch-up Strength)	according to Jedec Standard No. 78; Ta = 25 °C, pulse duration 10 ms, VDDA = $VDDA_{max}$, VDD = VDD_{max}, Vlu() = (-0.5...+1.5) x $Vpin()_{max}$	-100	100	mA
G010	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G011	Tj	Junction Temperature		-40	150	°C
G012	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating Conditions: VDDA = VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	 TSSOP20 ET -40/125	-25 -40		85 125	°C °C

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -40 ... 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDDA, VDD	Permissible Supply Voltage		4.5		5.5	V
002	I(VDDA)	Supply Current in VDDA	fin() = 200 kHz; A, B, Z open			15	mA
003	I(VDD)	Supply Current in VDD	fin() = 200 kHz; A, B, Z open			20	mA
004	Von	Turn-on Threshold VDDA, VDD		3.2		4.4	V
005	Vhys	Turn-on Threshold Hysteresis		200			mV
006	Vc()hi	Clamp Voltage hi at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF	Vc()hi = V() - VDDA; I() = 1 mA, other pins open	0.3		1.6	V
007	Vc()lo	Clamp Voltage lo at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, MA, SLI, SLO, A, B, Z	I() = -1 mA, other pins open	-1.6		-0.3	V
008	Vc()hi	Clamp Voltage hi at NERR, SCL, SDA, MA, SLI, SLO, A, B, Z	Vc()hi = V() - VDD; I() = 1 mA, other pins open	0.3		1.6	V
Input Amplifiers PSIN, NSIN, PCOS, NCOS							
101	Vos()	Input Offset Voltage	Vin() and G() in accordance with table Gain Select; G ≥ 20 G < 20	 -10 -15		 10 15	 mV mV
102	TCos	Input Offset Voltage Temperature Drift	see 101		±10		µV/K
103	Iin()	Input Current	V() = 0 V ... VDDA	-50		50	nA
104	GA	Gain Accuracy	G() in accordance with table Gain Select	95		102	%
105	GArel	Gain SIN/COS Ratio Accuracy	G() in accordance with table Gain Select	97		103	%
106	fhc	Cut-off Frequency	G = 80 G = 2.667	230 650			kHz kHz
107	SR	Slew Rate	G = 80 G = 2.667	4 9			V/µs V/µs
Sin/D Conversion: Accuracy							
201	AAabs	Absolute Angle Accuracy without calibration	referred to 360° input signal, G = 2.667, Vin = 1.5 Vpp, HYS = 0	-1.0		1.0	DEG
202	AAabs	Absolute Angle Accuracy after calibration	referred to 360° input signal, HYS = 0, internal signal amplitude of 2 ... 4 Vpp	-0.5	±0.35	+0.5	DEG
203	AArel	Relative Angle Accuracy	referred to output signal period of A/B, G = 2.667, Vin = 1.5 Vpp, SELRES = 1024, FCTR = 0x0004 ... 0x00FF, fin < fin_{max} (see table 14)	-10		10	%
Reference Voltage VREF							
801	VREF	Reference Voltage	I(VREF) = -1 mA ... +1 mA	48		52	% VDDA
Oscillator							
A01	fosc()	Oscillator Frequency	presented at SCL with subdivision of 2048; VDDA = VDD = 5 V ±10 % VDDA = VDD = 5 V	 52 60	 72	 90 83	 MHz MHz
A02	TCosc	Oscillator Frequency Temperature Drift	VDDA = VDD = 5 V		-0.1		%/K
A03	VCosc	Oscillator Frequency Power Supply Dependance			+10.6		%/V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -40 ... 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Zero Comparator							
B01	Vos()	Input Offset Voltage	V() = Vcm()	-20		20	mV
B02	Iin()	Input Current	V() = 0 V ... VDDA	-50		50	nA
B03	Vcm()	Common-Mode Input Voltage Range		1.4		VDDA-1.5	V
B04	Vdm()	Differential Input Voltage Range		0		VDDA	V
Incremental Outputs A, B, Z and BiSS Interface Output SLO							
D01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); I() = -4 mA			0.4	V
D02	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	V
D03	tr()	Rise Time	CL() = 50 pF			60	ns
D04	tf()	Fall Time	CL() = 50 pF			60	ns
D05	RL()	Permissible Load at A, B	TMA = 1 (calibration mode)	1			MΩ
BiSS Interface: Inputs MA, SLI							
E01	Vt()hi	Threshold Voltage hi				2	V
E02	Vt()lo	Threshold Voltage lo		0.8			V
E03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	300			mV
E04	Ipu(MA)	Pull-up Current in MA	V() = 0 ... VDD - 1 V	-240	-120	-25	µA
E05	Ipd(SLI)	Pull-down Current in SLI	V() = 1 ... VDD	20	120	300	µA
E06	fclk(MA)	Permissible Clock Frequency at MA	SSI protocol BiSS B protocol: sensor mode BiSS B protocol: register mode			4 10 0.25	MHz MHz MHz
E07	tp(MA-SLO)	Propagation Delay: MA edge vs. SLO output	all modes, RL(SLO) ≥ 1 kΩ	10		50	ns
E08	tbusy()s	Processing Time Sensor Mode	delay of start bit	0	0	0	
E09	tbusy()r	Processing Time Register Mode	delay of start bit with read access to EEPROM			2	ms
E10	tidle()	Interface Blocking Time	powering up with no EEPROM		1	1.5	ms
EEPROM Interface, Control Logic: Inputs SDA, NERR							
F01	Vt()hi	Threshold Voltage hi				2	V
F02	Vt()lo	Threshold Voltage lo		0.8			V
F03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	300			mV
F04	tbusy()cfg	Duration of Startup Configuration	error free EEPROM access		5	7	ms
EEPROM Interface, Control Logic: Outputs SDA, SCL, NERR							
G01	f()	Write/Read Clock at SCL			20	100	kHz
G02	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.45	V
G03	Ipu()	Pull-up Current	V() = 0 ... VDD - 1 V	-600	-300	-75	µA
G04	ft()	Fall Time	CL() = 50 pF			60	ns
G05	tmin()lo	Error Signal Indication Time at NERR (lo signal)	MA = hi, no BiSS access, amplitude or frequeny error	10			ms
G06	Tpwm()	Error Signal PWM Cycle Duration at NERR	fosc() subdivided 2^{22}		60.7		ms
G07	RL()	Permissible Load at SDA, SCL	TMA = 1 (calibration mode)	1			MΩ

CHARACTERISTICS: Diagrams

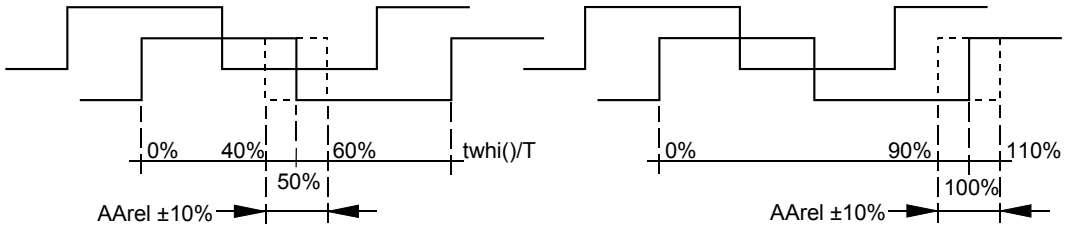


Figure 1: Definition of relative angle error.

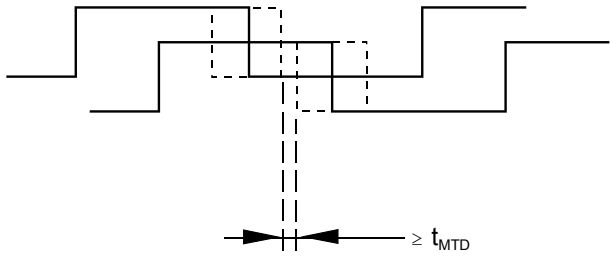


Figure 2: Definition of minimum transition distance.

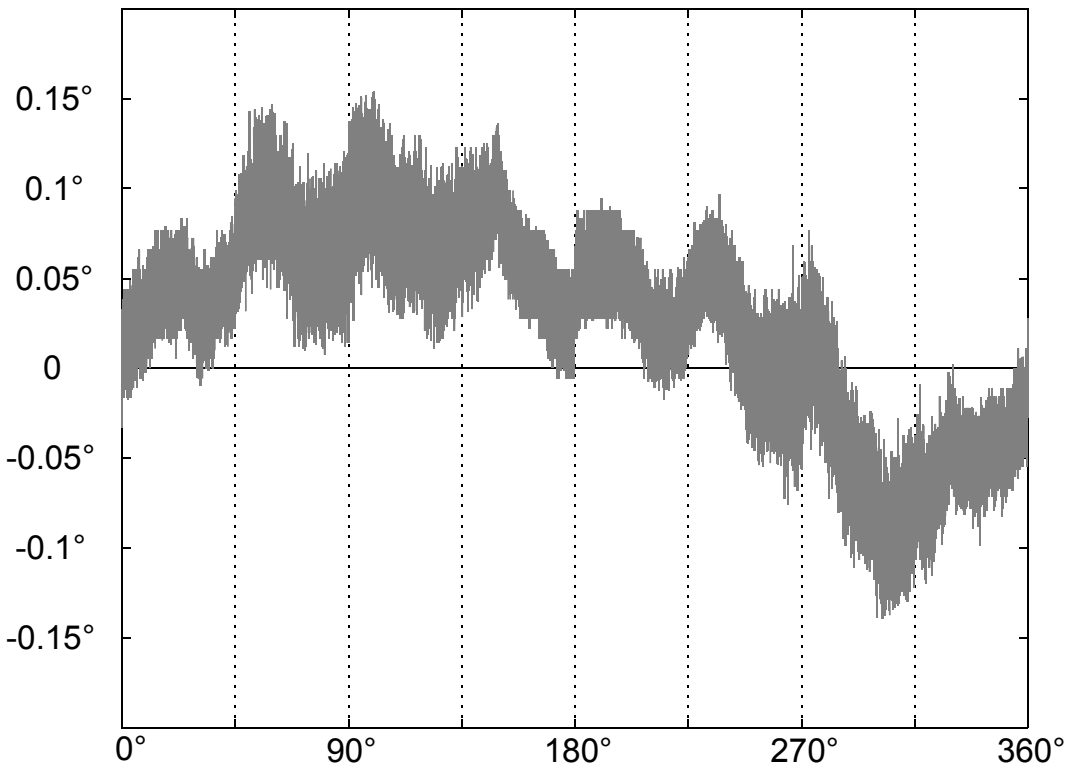


Figure 3: Typical residual absolute angle error after calibration.

OPERATING REQUIREMENTS: BiSS and SSI Interface

Operating Conditions: VDD = 5 V ±10 %, Ta = -25 ... 85 °C; input levels lo = 0 ... 0.45 V, hi = 2.4 V ... VDD

Item No.	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
SSI Output (SELSSI = 1)							
I001	T_{MAS}	Permissible Clock Period	CFGTOS = 0x01	4	250	2x t_{tos}	ns
I002	t_{MASh}	Clock Signal Hi Level Duration		4	25	t_{tos}	ns
I003	t_{MASl}	Clock Signal Lo Level Duration		4	25	t_{tos}	ns
BiSS Sensor Mode							
I004	T_{MAS}	Permissible Clock Period	CFGTOR selected in accordance with table on page 15	5	100		ns
I005	t_{MASh}	Clock Signal Hi Level Duration		5	25	t_{tos}	ns
I006	t_{MASl}	Clock Signal Lo Level Duration		5	25		ns
BiSS Register Mode							
I007	T_{MAR}	Permissible Clock Period	CFGTOR selected in accordance with table on page 15	6	4		µs
I008	t_{idle}	Permissible Clock Halt (idle)		6	0	indefinite	
I009	t_{MARh}	Clock Signal Hi Level Duration		6		t_{tor}	ns
I010	t_{MARh}	Clock Signal Hi Level Duration	read out of register data	6	30	70	% TMAR
I011	t_{MARl}	Clock Signal Lo Level Duration		6		t_{tor}	ns
I012	t_{MA0h}	"Logic 0" Hi Level Duration		6	10	30	% TMAR
I013	t_{MA1h}	"Logic 1" Hi Level Duration		6	70	90	% TMAR

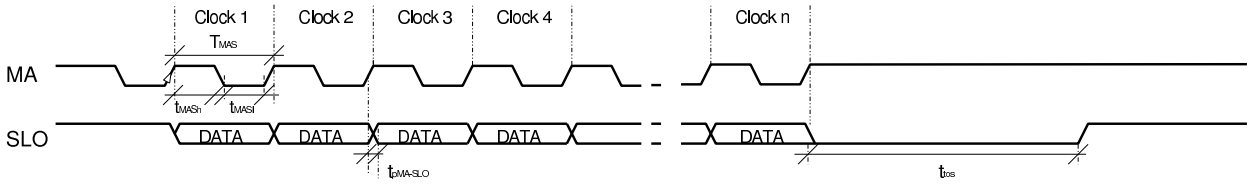


Figure 4: Timing diagram of SSI output.

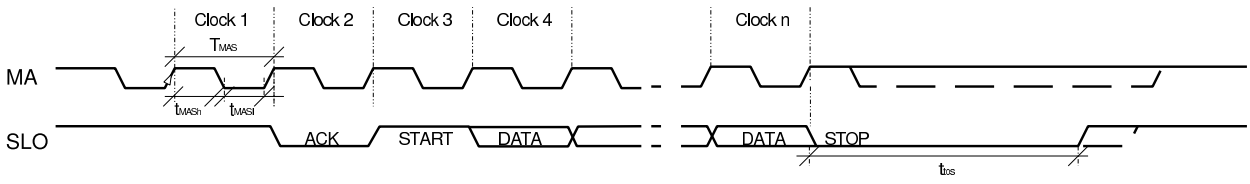


Figure 5: Timing diagram of BiSS sensor mode.

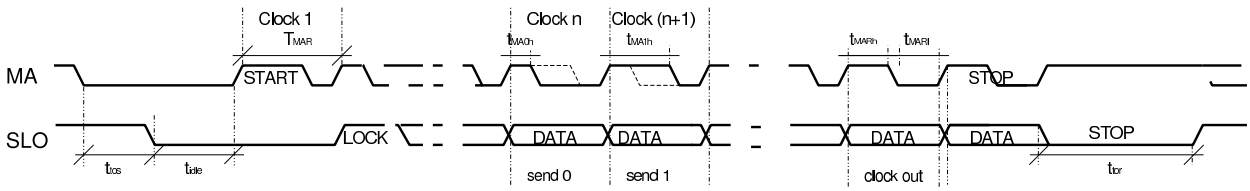


Figure 6: Timing diagram of BiSS register mode.

PARAMETER and REGISTER

OVERVIEW

Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	BiSSMOD	M2S(1:0)		SELRES(4:0)				
0x01	HYS(2:0)			ZPOS(4:0)				
0x02	ENRESDEL	SELSSI	ROT	CBZ	CFGABZ(1:0)		CFGZ(1:0)	
0x03	CFGSSI(1:0)		CFGAB(1:0)		RPL(1:0)		AERR	FERR
0x04	FCTR(7:0)							
0x05		FCTR(14:8)						
0x06	CFGTOR(1:0)		CFGTOS(1:0)		TMODE(2:0)			TMA
0x07*	Reserved address / internal use							
0x08	GAIN(3:0)				RATIO(3:0)			
0x09	SINOFFS(7:0)							
0x0A	COSOFFS(7:0)							
0x0B	PHASE(5:0)						REFOFFS	RATIO(4)
0x0C						SELAMPL	AMPL(1:0)	
0x0D								
0x0E								
0x0F	CRC(7:0) check sum over address 0-14 with CRC polynomial: "100100111" (read out of EEPROM)							
	EEPROM							
0x10 - 0x1F	0x00 - 0xF	Reserved EEPROM register section storing iC-NQ device setup						
0x20 - 0x77	0x10 - 0x67	Free EEPROM registers						
0x78 - 0x7F	0x68 - 0x6F	EEPROM: BiSS Identifier, ROM: Device ID iC-NQ X3: 4E 51 58 33 {ADR0} 00 69 43**						

As no access protections are selected all registers are accessible by read and write operations (see RPL).

*) Programming to value 0x00 is recommended. **) iC-NQ V2: 4E 51 56 32 {Adr 0x00} 00 69 43

Table 5: Register layout

SIGNAL CONDITIONING

Input stages SIN and COS are configured as instrumentation amplifiers. The amplifier gain must be selected in accordance with the sensor signal level and programmed to register GAIN according to the following table. Half of the supply voltage is output to VREF as center voltage to help DC level adaptation.

GAIN	Adr 0x08, Bit 7:4				
		Sine/Cosine Input Signal Levels Vin()			
		Amplitude		Average value (DC)	
Code	Amplification	Differential	Single-ended	Differential	Single-ended
0x0F	80.000	up to 50 mVpp	up to 100 mVpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.2 V
0x0E	66.667	up to 60 mVpp	up to 120 mVpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.2 V
0x0D	53.333	up to 75 mVpp	up to 0.15 Vpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.2 V
0x0C	40.000	up to 0.1 Vpp	up to 0.2 Vpp	1.2 V ... VDDA - 1.2 V	1.3 V ... VDDA - 1.3 V
0x0B	33.333	up to 0.12 Vpp	up to 0.24 Vpp	1.2 V ... VDDA - 1.2 V	1.3 V ... VDDA - 1.3 V
0x0A	28.571	up to 0.14 Vpp	up to 0.28 Vpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.3 V
0x09	26.667	up to 0.15 Vpp	up to 0.3 Vpp	1.2 V ... VDDA - 1.2 V	1.3 V ... VDDA - 1.3 V
0x08	20.000	up to 0.2 Vpp	up to 0.4 Vpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.3 V
0x07	14.287	up to 0.28 Vpp	up to 0.56 Vpp	1.2 V ... VDDA - 1.3 V	1.4 V ... VDDA - 1.4 V
0x06	10.000	up to 0.4 Vpp	up to 0.8 Vpp	1.2 V ... VDDA - 1.3 V	1.4 V ... VDDA - 1.5 V
0x05	8.000	up to 0.5 Vpp	up to 1 Vpp	0.8 V ... VDDA - 1.4 V	1.0 V ... VDDA - 1.6 V
0x04	6.667	up to 0.6 Vpp	up to 1.2 Vpp	0.8 V ... VDDA - 1.4 V	1.1 V ... VDDA - 1.7 V
0x03	5.333	up to 0.75 Vpp	up to 1.5 Vpp	0.9 V ... VDDA - 1.5 V	1.3 V ... VDDA - 1.9 V
0x02	4.000	up to 1 Vpp	up to 2 Vpp	1.2 V ... VDDA - 1.6 V	1.7 V ... VDDA - 2.1 V
0x01	3.333	up to 1.2 Vpp	up to 2.4 Vpp	1.2 V ... VDDA - 1.7 V	1.8 V ... VDDA - 2.3 V
0x00	2.667	up to 1.5 Vpp	up to 3 Vpp	1.3 V ... VDDA - 1.8 V	2.0 V ... VDDA - 2.6 V

Table 6: Gain Select

SINOFFS	Adr 0x09, Bit 7:0	
COSOFFS	Adr 0x0A, Bit 7:0	
Code	Output Offset	Input Offset
0x00	0 V	0 V
0x01	-7.8125 mV	-7.8125* mV / GAIN
...	...	...
0x7F	-0.9922 V	-0.9922 V / GAIN
0x80	0 V	0 V
0x81	+7,8125 mV	+7.8125 mV / GAIN
...	...	...
0xFF	+0.9922 V	+0.9922 V / GAIN
Notes	*) With REFOFFS = 0x00 und VDDA = 5 V.	

Table 7: Offset Calibration Sine/Cosine

REFOFFS	Adr 0x0B, Bit 1
Code	Reference Voltage
0x00	Depending on VDDA (example of application: MR sensors)
0x01	Not depending on VDDA (example of application: Sin/Cos encoders)

Table 8: Offset Calibration Reference

RATIO	Adr 0x0B, Bit 0, Adr 0x08, Bit 3:0		
Code	COS / SIN	Code	COS / SIN
0x00	1.0000	0x10	1.0000
0x01	1.0067	0x11	0.9933
...	...	...	...
0x0F	1.1	0x1F	0.9000

Table 9: Amplitude Calibration

PHASE	Adr 0x0B, Bit 7:2		
Code	Phase Shift	Code	Phase Shift
0x00	90°	0x20	90°
0x01	90.703125°	0x21	89.296875°
...	...	...	...
0x12	102.65625°	0x32	77.34375°
...	102.65625°	...	77.34375°
0x1F	102.65625°	0x3F	77.34375°

Table 10: Phase Calibration

CONVERTER FUNCTIONS

SELRES	Adr 0x00, Bit 4:0	
Code	Binary Resolutions	Examples of Permissible Input Frequencies fin_{max} (FCTR 0x0004, 0x4304)
0x00	-	
0x01	-	
0x02	-	
0x03	8192	158 Hz, 635 Hz
0x04	4096	317 Hz, 1.27 kHz
0x05	2048	634 Hz, 2.54 kHz
0x06	1024	1.27 kHz, 5.1 kHz
0x07	512	2.54 kHz, 10.2 kHz
0x08	256	5.1 kHz, 20.3 kHz
0x09	128	10.2 kHz, 40.6 kHz
0x0A	64	20.3 kHz, 81.3 kHz
0x0B	32	40.6 kHz, 162.5 kHz
0x0C	16	81.3 kHz (max. 250 kHz @ 0x4202)
0x0D	8	162 kHz (max. 250 kHz @ 0x4102)
0x0E	-	
0x0F	-	

Table 11: Binary Resolutions

SELRES	Adr 0x00, Bit 4:0	
Code	Decimal Resolutions	Examples of Permissible Input Frequencies fin_{max} (FCTR 0x0004, 0x4304)
0x10	2000	650 Hz, 2.6 kHz
0x11	1600	812 Hz, 3.3 kHz
0x12	1000	1.3 kHz, 5.2 kHz
0x13	800	1.6 kHz, 6.5 kHz
0x14	500	2.6 kHz, 10.4 kHz
0x15	400	3.2 kHz, 13 kHz
0x16	250 *1	5.2 kHz, 20.8 kHz
0x17	125 *1,2	5.2 kHz, 20.8 kHz
0x18	320	4.1 kHz, 16.3 kHz
0x19	160 *2	4.1 kHz, 16.3 kHz
0x1A	80 *4	4.1 kHz, 16.3 kHz
0x1B	40 *8	4.1 kHz, 16.3 kHz
0x1C	200	6.5 kHz, 26 kHz
0x1D	100 *2	6.5 kHz, 26 kHz
0x1E	50 *1,4	6.5 kHz, 26 kHz
0x1F	25 *1,8	6.5 kHz, 26 kHz
Notes	*1 Not useful with increment A quad B output. *2,4,8 The internal converter resolution is higher by factor 2, 4 or 8.	

Table 12: Decimal Resolutions

HYS	Adr 0x01, Bit 7:5		
Code	Hysteresis in degree	Hysteresis in LSB	Absolute error*
0x00	0°		
0x01	0.0879°	1 LSB @ 12 bit	0.044°
0x02	0.1758°	1/2 LSB @ 10 bit	0.088°
0x03	0.3516°	1 LSB @ 10 bit	0.176°
0x04	0.7031°	1/2 LSB @ 8 bit	0.352°
0x05	1.4063°	1 LSB @ 8 bit	0.703°
0x06	5.625°		2.813°
0x07	45°	only recommended for calibration	22.5°
Notes	*) The absolute error is equivalent to one half the angle hysteresis		

Table 13: Hysteresis

MAXIMUM POSSIBLE CONVERTER FREQUENCY

The converter frequency automatically adjusts to the value necessary for the input frequency and resolution. This value ranges from zero to a maximum dependent on the oscillator frequency which can be set using register FCTR.

Serial data output

For BiSS or SSI output the maximum possible converter frequency can be adjusted to suit the maximum input frequency; an automatic converter resolution step-down feature can be enabled via the FCTR register. Should the input frequency exceed the frequency limit of the selected converter resolution, the LSB is kept stable and not resolved any further; the interpolation resolution halves.

If the next frequency limit is overshot, the LSB and the LSB+1 are kept stable and so on. When the input frequency again sinks below this frequency limit, the fine resolution automatically returns.

Max. Possible Converter Frequency For Serial Data Output

	Resolution Requirements			Protocol		Max. Input Frequency	Restrictions at high input frequencies	Examples* fin_{max} [kHz] at resol.		
FCTR	**Min. Res.**	**bin**	**dec**	**BiSS**	**SSI**	**fin_{max}**		**8192**	**1024**	**200**
0x0004		X	X	X	X	f(OSC)min / 40 / Resolution	–	0.16	1.27	6.5
0x4102	≥ 8	X	X	X	X	f(OSC)min / 24 / Resolution	Rel. angle error 2x increased	0.26	2.1	10.8
0x4202	≥ 16	X	X	X	X	2 x f(OSC)min / 24 / Res.	Rel. angle error 4x increased	0.53	4.2	21.6
0x4304	≥ 32	X	X	X	X	4 x f(OSC)min / 40 / Res.	Rel. angle error 8x increased	0.64	5.1	26.0
0x4602	≥ 64	X	-	X	X	4 x f(OSC)min / 24 / Res.	Resolution lowered by factor of 2	1.1	8.5	-
0x4A02	≥ 128	X	-	X	X	8 x f(OSC)min / 24 / Res.	Res. lowered by factor of 2-4	2.1	16.9	-
0x4E02	≥ 256	X	-	X	X	16 x f(OSC)min / 24 / Res.	Res. lowered by factor of 2-8	4.2	33.8	-
0x5202	≥ 512	X	-	X	X	32 x f(OSC)min / 24 / Res.	Res. lowered by factor of 2-16	8.5	67.7	-
0x5602	≥ 1024	X	-	X	X	64 x f(OSC)min / 24 / Res.	Res. lowered by factor of 2-32	16.9	135	-
0x5A02	≥ 2048	X	-	X	X	128 x f(OSC)min / 24 / Res.	Res. lowered by factor of 2-64	33.8	250	-
0x5E02	≥ 4096	X	-	X	X	256 x f(OSC)min / 24 / Res.	Res. lowered by factor of 2-128	67.7	-	-
0x6202	8192	X	-	X	X	512 x f(OSC)min / 24 / Res.	Res. lowered by factor of 2-256	135	-	-
Notes	*) Calculated with fosc()min taken from Electrical Characteristics item A01.									

Table 14: Maximum converter frequency for serial data output.

Incremental output to A, B and Z

There are two criteria which must be considered when setting the maximum possible converter frequency via the FCTR register:

1. The maximum input frequency
2. System limitations, e.g. due to slow counters or cable transmission

When facing system limitations it is useful to preselect a minimum transition distance for the output signals. A digital zero-delay glitch filter then takes care of a temporal edge-to-edge separation, guaranteeing spike-free output signals after an ESD impact to the sensor, for instance.

A serial data output is simultaneously possible at any time, using the BiSS or SSI protocol. However, for the transfer of angle data to the output register the incremental output is halted for one period of the clock signal applied to pin MA.

1. Max. Possible Converter Frequency Defined By The Maximum Input Frequency								
	Output Frequency fout @ fin_{max}	Resolution Requirem.		Maximum Input Frequency	Restrictions at high input frequencies	Examples* fin_{max} [kHz] at resol.		
FCTR	**A, B**	**bin**	**dec**	**fin_{max}**		**8192**	**1024**	**200**
0x0004	325 kHz	X	X	f(OCS)min / 40 / Resolution	None	0.16	1.27	6.5
0x4102	542 kHz	X	X	f(OSC)min / 24 / Resolution	Relative angle error 2x increased	0.26	2.1	10.8
0x4202	1.08 MHz	X	X	2 x f(OSC)min / 24 Res.	Relative angle error 4x increased	0.53	4.2	21.6
0x4304	1.3 MHz	X	X	4 x f(OSC)min / 40 / Res.	Relative angle error 8x increased	0.64	5.1	26.0
Notes	*) Calculated with fosc()min taken from Electrical Characteristics item A01.							

Table 15: Max. converter frequency for incremental A/B/Z output, defined by the max. input frequency

2. Max. Possible Converter Frequency Defined By The Minimum Transition Distance						
	Output Frequency fout @ t_{MTD}	Resolution Requirem.		Minimum Transition Distance at A, B	Restrictions at high input frequencies	Example* t_{MTD} [µsec]
FCTR	**A, B**	**bin**	**dec**	**t_{MTD}**		
0x00FF	10 kHz	X	X	2048 / f(OSC)max	None	22.8
0x00FE	10.05 kHz	X	X	2040 / f(OSC)max	None	22.7
0x00FD	10.09 kHz	X	X	2032 / f(OSC)max	None	22.6
...	...	...	...	...	...	...
0x0006	366 kHz	X	X	56 / f(OSC)max	None	0.62
0x0005	427 kHz	X	X	48 / f(OSC)max	None	0.53
0x0004	512 kHz	X	X	40 / f(OSC)max	None	0.44
0x4102	854 kHz	X	X	24 / f(OSC)max	Relative angle error 2x increased	0.27
0x4202	1.7 MHz	X	X	12 / f(OSC)max	Relative angle error 4x increased	0.13
0x4304	2.1 MHz	X	X	10 / f(OSC)max	Relative angle error 8x increased	0.11
Notes	*) Calculated with fosc()max taken from El.Char. item A01; the min. transition distance refers to output A vs. output B without reversing the sense of rotation.					

Table 16: Max. converter frequency for incremental A/B/Z output, defined by the min. transition distance

INCREMENTAL SIGNALS

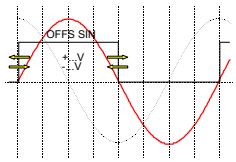
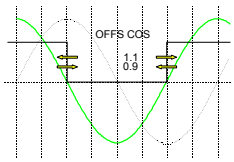
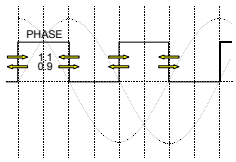
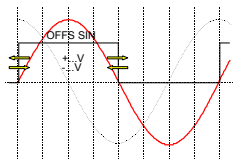
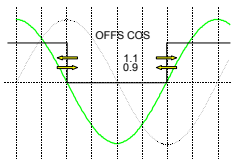
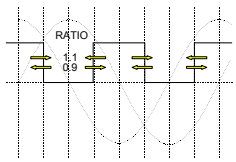
CFGABZ	Adr 0x02, Bit 3:2			
Code	Mode	A	B	Z
0x00	Normal	A	B	Z
0x01	Control signals for external period counters	CA	CB	CZ
0x02	Calibration mode The following settings are required additionally: SELRES = 0x0D ZPOS = 0x00 HYS = 0x07 ROT = 0x00 AERR = 0x00	 Figure 7: Offset SIN*	 Figure 8: Offset COS*	 Figure 9: Phase*
0x03	Calibration mode The following settings are required additionally: SELRES = 0x0D ZPOS = 0x00 HYS = 0x07 ROT = 0x00 AERR = 0x00	 Figure 10: Offset SIN*	 Figure 11: Offset COS*	 Figure 12: Amplitude*
Notes	*) Trimmed accurately when duty cycle is 50 %; Recommended trimming order (after selecting GAIN): Offset, Phase, Amplitude Ratio, Offset;			

Table 17: Outputs A, B, Z

ROT	Adr 0x02, Bit 5
Code	Direction
0x00	Not inverted
0x01	Inverted

Table 18: Direction of Rotation

CBZ	Adr 0x02, Bit 4
Code	Clear by zero
0x00	Disabled
0x01	Enabled

Table 19: Reset Enable for Period Counter

ENRESDEL	Adr 0x02, Bit 7	
Code	Output*	Function
0x00	immediately	An external counter displays the absolute angle following power on.
0x01	after 5 ms	An external counter only displays changes vs. the initial power-on condition (moving halted to reapply power is precondition.)
Notes	*) Output delay after device configuration and internal reset.	

Table 20: Output Turn-On Delay A, B, Z

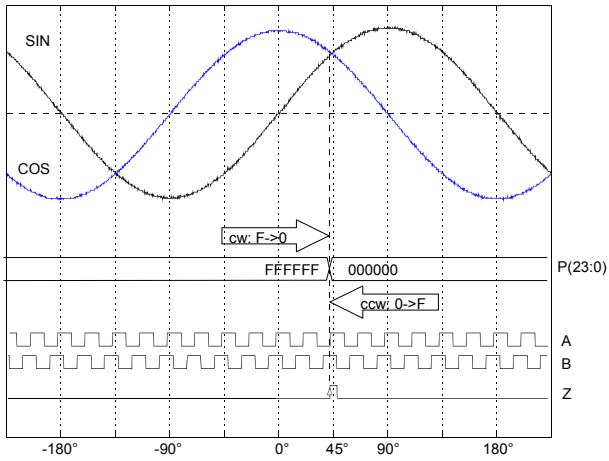


Figure 13: Clear by zero function of the period counter when enabled by CBZ = 1.
Example for chip release iC-NQ V2 at resolution 64 (SELRES = 0x0A), zero signal at 45° (ZPOS = 0x04, CFGAB = 0x00) and the direction of rotation not inverted (ROT = 0x00, COS leads SIN).

ZPOS	Adr 0x01, Bit 4:0
	Chip versions iC-NQ X2, iC-NQ X3:
Code	Position
0x00	0°
0x08	90°
0x10	180°
0x18	270°
	Chip version iC-NQ V2:
Code	Position
0x01	11.25° (1 x 11.25°)
...	...
0x1F	348.75° (31 x 11.25°)
Notes	The zero signal is only output if released by the input pins (for instance with PZERO = 5 V, NZERO = VREF).

Table 21: Zero Signal Position

CFGZ	Adr 0x02, Bit 1:0
Code	Length
0x00	90°
0x01	180°
0x02.. 03	Synchronization

Table 22: Zero Signal Length

CFGAB	Adr 0x03, Bit 5:4
Code	Z = 1 for
0x00	B = 1, A = 1
0x01	B = 0, A = 1
0x02	B = 1, A = 0
0x03	B = 0, A = 0

Table 23: Zero Signal Logic

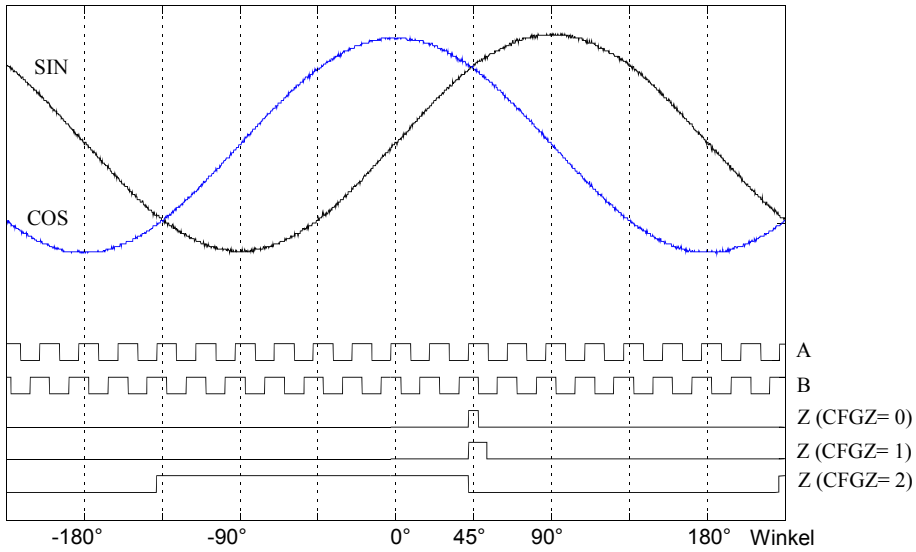


Figure 14: Incremental output signals for various length of the zero signal.
Example for chip release iC-NQ V2 with resolution 64 (SELRES = 0x0A), a zero signal position of 45° (ZPOS = 0x04, CFGAB = 0x00) and no reversal of the rotational sense (ROT = 0x00, COS leads SIN).

SIGNAL MONITORING and ERROR MESSAGES

SELAMPL **AMPL**	Adr 0x0C, Bit 2 Adr 0x0C, Bit 1:0	
	Max (|Sin| , |Cos|)	
Code	Voltage threshold V_{th}	Output amplitude*
0x00	0.60 x VDDA	1.4 V_{pp} (0.28 x VDDA)
0x01	0.64 x VDDA	2.0 V_{pp} (0.40 x VDDA)
0x02	0.68 x VDDA	2.6 V_{pp} (0.51 x VDDA)
0x03	0.72 x VDDA	3.1 V_{pp} (0.62 x VDDA)
	Sin^2 + Cos^2	
Code	$V_{thmin} \leftrightarrow V_{thmax}$	Output amplitude*
0x04	0.48 ↔ 0.68 x VDDA	2.4 V_{pp} ↔ 3.4 V_{pp}
0x05	0.56 ↔ 0.76 x VDDA	2.8 V_{pp} ↔ 3.8 V_{pp}
0x06	0.64 ↔ 0.84 x VDDA	3.2 V_{pp} ↔ 4.2 V_{pp}
0x07	0.72 ↔ 0.92 x VDDA	3.6 V_{pp} ↔ 4.6 V_{pp}
Notes	*) Entries are calculated with VDDA = 5 V.	

Table 24: Signal Amplitude Monitoring

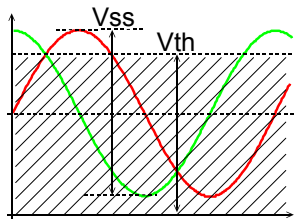


Figure 15: Signal monitoring of minimum amplitude.

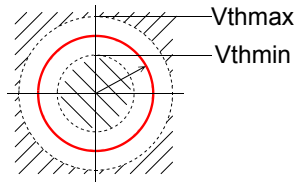


Figure 16: Sin^2 + Cos^2 signal monitoring.

AERR	Adr 0x03, Bit 1
Code	Amplitude error message
0x00	disabled
0x01	enabled

Table 25: Amplitude Error

FERR	Adr 0x03, Bit 0
Code	Excessive frequency error message
0x00	disabled
0x01	enabled
Note	Input frequency monitoring is operational for resolutions $\geq$ 16

Table 26: Frequency Error

Configuration Error	
-	Messaging always released

Table 27: Configuration Error

Error Keys		
Failure Mode	Pin NERR	Error bits E1, E0 with BiSS and SSI
No error	HI	11
Amplitude error	LO/HI = 75 % (AERR = 0: HI)	01 (11)
Frequency error	LO/HI = 50 % (FERR = 0: HI)	10 (11)
Configuration	LO	00
Undervoltage	LO	00
System error	NERR = low caused by an external error signal	00

Table 28: Error Keys

Each phase in the configuration process is signaled by NERR = low; the signal is only reset following a successful CRC (cyclic redundancy check).

If the data transfer from the EEPROM is faulty and the CRC unsuccessful, then the configuration phase is automatically repeated.

The process aborts following a third unsuccessful attempt and the error message output remains set to low until a write access occurs at address 0 via the BiSS Interface (internal reset).

To enable the successful diagnosis of faults other types of error are signaled at NERR using a PWM code as given in the key on the left.

Two error bits are provided to enable communication via the BiSS Interface; these bits can decode four different types of error. If NERR is held at low by an external source, such as an error message from the system, for example, this can also be verified via the BiSS Interface.

Error events are stored for the BiSS sensor data output and deleted afterwards. Errors at NERR are displayed for a minimum of ca. 10 ms, as far as no BiSS readout causes a deletion.

If an error in amplitude occurs the conversion process is terminated and the incremental output signals halted. An error in amplitude rules out the possibility of an error in frequency.

TEST FUNCTIONS

TMODE	Adr 0x06, Bit 3:1	
Code	Signal at Z	Description
0x00	Z	no test mode
0x01	A xor B	Output A EXOR B
0x02	ENCLK	iC-Haus device test
0x03	NLOCK	iC-Haus device test
0x04	CLK	iC-Haus device test
0x05	DIVC	iC-Haus device test
0x06	PZERO - NZERO	iC-Haus device test
0x07	TP	iC-Haus device test
Condition	CFGABZ = 0x00	

Table 29: Test Mode

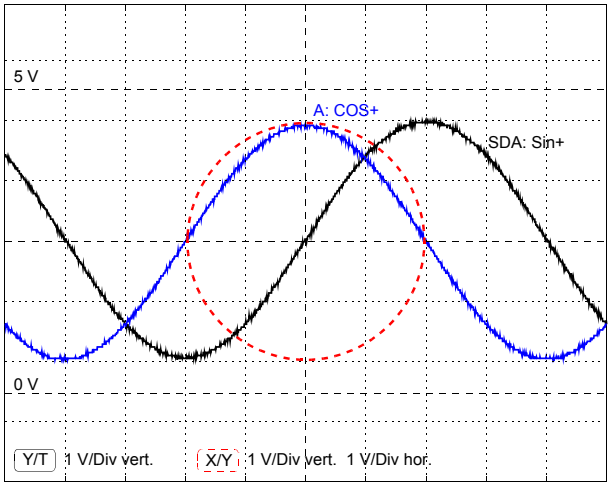


Figure 17: Calibrated signals with TMA mode.

TMA	Adr 0x06, Bit 0			
Code	**Pin A**	**Pin B**	**Pin SDA**	**Pin SCL**
0x00	A	B	SDA	SCL
0x01	COS+	COS-	SIN+	SIN-
Notes	To permit the verification of GAIN and OFFSET settings, the input amplifier outputs are available at the pins. To operate the converter a signal of 4 Vpp is the ideal here and should not be exceeded. Pin loads above 1 MΩ are adviceable for accurate measurements.			

Table 30: Analog Test Mode

Parameter GAIN ideally adjusts the signal levels to ca. 4 Vpp and should not be touched afterwards.

Both scope display modes are feasible for OFFS (positive values) or RATIO adjustments; regarding the adjustment of PHASE the X/Y mode may be preferred.

For OFFS adjustment towards negative values the test signals COS- (pin B) and SIN- (pin SCL) are relevant.

BiSS INTERFACE

Serial BiSS communication differentiates between the fast cyclic transmission of sensor data for the output of angle position and period counter data and the transmission of register data which can include bidirectional read and write access.
The required mode of communication is initiated by the interface master; as a slave iC-NQ determines up to which maximum clock interval the selected mode is retained. Sensor mode timeout t_{tos} and register mode timeout t_{tor} thus give the master a minimum clock frequency of fclk(MA)min.

CFGTOS	Adr 0x06, Bit 5:4		
Code	Timeout t_{tos} Sensor mode	Ref. clock counts	fclk(MA) min*
0x00	typ. 128 µs	256-259	11 kHz
0x01	typ. 16 µs	32-35	88 kHz
0x02	typ. 4 µs	8-11	352 kHz
0x03	typ. 1 µs	2-5	1.41 MHz
CFGTOR	Adr 0x06, Bit 7:6		
Code	Timeout t_{tor} Regist. mode	Ref. clock counts	fclk(MA) min*
0x00	typ. 1 ms	2049-2060	1.4 kHz
0x01	typ. 256 µs	513-514	5.5 kHz
0x02	typ. 32 µs	67-68	42 kHz
0x03	not permitted	–	–
Notes	A ref. clock count is equal to $\frac{32}{fosc}$ (see El. Char. A01). The permissible max. clock frequency is specified by item E06.		

Table 31: Interface Timeouts

M2S	Adr 0x00, Bit 6:5		
		SCD	MCD
Code	SCD*	CRC Poly.	not in use
	Chip releases iC-NQ X2, iC-NQ X3:		
0x00	-	0x25	1 zero bit
0x01	P(7:0)	0x25	1 zero bit
	Chip release iC-NQ V2:		
0x00	-	0x25	1 zero bit
0x01	P(7:0)	0x25	1 zero bit
0x02	P(11:0)	0x43	1 zero bit
0x03	P(23:0)	0x43	n/a
Notes	*) Period counter output via SCD		

Table 32: Period Counter Output

BiSSMOD	Adr 0x00, Bit 7	
Code	Version	Description
0x00	B	BiSS B without multicycle data
0x01	C	Transparency for BiSS C

Table 33: Protocol Version

Protocol and Data Format

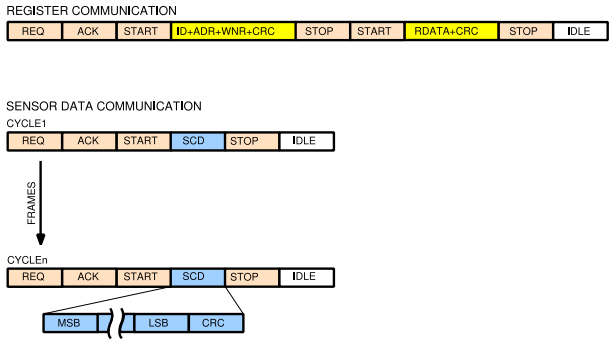


Figure 18: BiSS B Protocol

Single-Cycle Data Channel: SCD		
Bits	Type	Label
0, 8 0,8, 12, 24*	DATA	Period Counter P(7:0) Period Counter P(23:0)* (multiturn position)
3...13	DATA	Angle Data S(12:0): 3 to 13 bits (singleturn position)
1	ERROR	Error bit E1 (amplitude error)
1	ERROR	Error bit E0 (frequency error)
5 6*	CRC CRC	Polynomial 0x25 $x^5 + x^2 + x^0$ (inverted bit output) Polynomial 0x43* $x^6 + x^1 + x^0$ (inverted bit output)
Multicycle Data Channel: MCD - not in use		
Bits	Type	Label
1	zero bit	
Register Data Channel: CD		
Bits	Type	Label
3	ID	Slave ID
7	ADR	Register Address
1	WNR	Write-Not-Read Command
4	CRC	Polynomial 0x13 $x^4 + x^1 + x^0$ (inverted bit output)
	Adr	Content
8	0x10.. 1F	Device Configuration Data
	0x20.. 77	OEM Daten
	0x78.. 7F	BiSS Identifier
4	CRC	Polynomial 0x13 $x^4 + x^1 + x^0$ (inverted bit Output)

Table 34: BiSS Data Channels
*) For chip release iC-NQ V2

Sensor Data Communication

The sensor data produced by iC-NQ contains 3 to 13 bits of angle value (S), the period counter (P) with up to 24 bits (optional), 2 bits of error messages (E1, E0), and 5 CRC bits (C). Here, M2S sets the output enable for the position counter; the counter bits, with the MSB leading, are transmitted in front of the angle value.

The 5 bit CRC output is based on the polynomial 0x25 (100101b), the 6 bit CRC output on the polynomial 0x43 (1000011b) and comes active with longer SCD data. Generally, CRC bits are output inverted.

As soon as the storage of sensor data is initiated *Latch* conversion is paused for one MA clock cycle. This time must be taken into consideration when calculating the maximum input frequency. The synchronization output at Z (CFGZ = 0x02) is stored until the start bit of the previous slave arrives.

SCD: Angle data		
Bits	Type	Label
13	DATA	Angle Data S(12:0)
2	ERROR	Error bits E1, E0
5	CRC	Polynomial 0x25
1	Zero bit	
Config.	SELRES = 0x03, M2S = 0x00	

Table 35: Format example 1

SCD: Angle data with 8-bit period counter		
Bits	Typ	Label
8	DATA	Period Counter S(7:0)
13	DATA	Angle Data S(12:0)
2	ERROR	Error Bits E1, E0
5	CRC	Polynomial 0x25
1	Zero bit	
Config.	SELRES = 0x03, M2S = 0x01	

Table 36: Format example 2

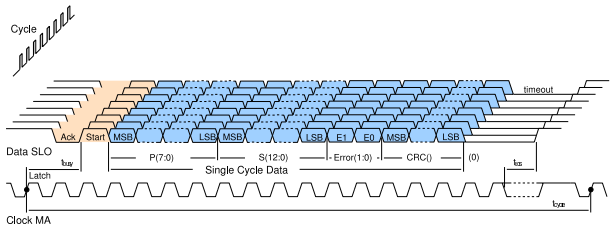


Figure 19: BiSS B protocol

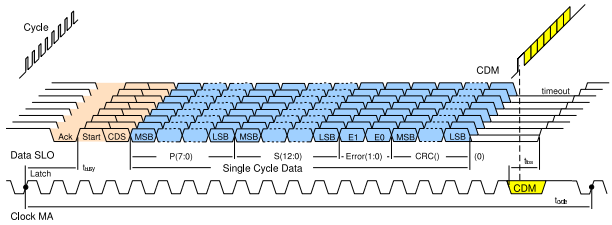


Figure 20: BiSS C protocol transparency, no interpretation of CDM

Register Data Communication

For as long as the configuration error is active the longest timeout is used for the register mode independent of CFGTOR. Thus when configuring via BiSS CFGTOR and RPL should be written before address 0.

A write access at Address 0 triggers an internal reset. This allows the period counter to be set to zero and configuration errors to be reset; the EEPROM is not read out a second time.

Register access via BiSS can be limited using the programming bits RPL according to the following table.

RPL	Adr 0x03, Bit 3:2		
RPL	Configuration Address 0-31	User Address 32-119	BiSS Identifier Address 120-127
0x00	Read / Write	Read / Write	Read / Write
0x01	Read	Read / Write	Read
0x02	-	Read / Write	Read
0x03	-	Read	Read

Table 37: Register Access Safety Level

Sensor Data Output in SSI Format

With **SELSSI** = 1 the communication timing is switched to SSI compatibility. Data output is in binary format starting with the MSB. It can be configured if the error bits are to be send afterwards.

CFGSSI	Adr 0x03, Bit 7:6	
Code	Additional bits	Ring register operation
0x00	E1, E0, zero bit	no
0x01	none	no
0x02	E1, E0, zero bit	yes
0x03	none	yes

Table 38: SSI Output

Examples of SSI formats

SSI Output Formats																						
13-bit SSI																						
Res	**Mode**	**Error**	**CRC**	**T1**	**T2**	**T3**	**T4... T10**	**T11**	**T12**	**T13**	**T14**	**T15**	**T16**	**T17**	**T18**	**T19**	**T20**	**T21**	**T22**	**T23**	**T24**	**T25**
10 bit	SSI	X	-	S9	S8	S7	S6 ... S0	E1	E0	0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
			Example							0	0	0	0	0	0	0	0	0	0	0	0	0
13 bit	SSI *1	-	-	S12	S11	S10	S9 ... S3	S2	S1	S0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
			Example								0	0	0	0	0	0	0	0	0	0	0	0
	SSI-R *2	-	-	S12	S11	S10	S9 ... S3	S2	S1	S0	Stop	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2
			Example								0											
25-bit SSI																						
13 bit	SSI	X	-	S12	S11	S10	S9 ... S3	S2	S1	S0	E1	E0	0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
			Example										0	0	0	0	0	0	0	0	0	0
8 + 13 bit *3	SSI	X	-	P7	P6	P5	P4 ... P0, S12, S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	E1	E0	0	Stop
			Example																		0	0
Configuration				Input SLI = 0, SELSSI = 1 CFGMCD = 0x00, CFGSSI = 0x00, unless otherwise noted. *1 CFGSSI = 0x01; *2 CFGSSI = 0x03; *3 CFGMCD = 0x01																		
Caption				SSI protocol SSI ring operation																		

Table 39: SSI Output Formats

EEPROM INTERFACE

Serial EEPROM components permitting operation from 3.3 V to 5 V can be connected (such as 24C02, for example). When the device is switched on the memory area of bytes 0 to 15 is mapped onto iC-NQ's registers. The higher memory areas, bytes 16-111, are readily available to the system via BiSS. The EEPROM addresses 0-111 are mapped onto the BiSS addresses 16-127. If no EEPROM is connected the device must be configured via BiSS and address 0 written last. In this case iC-NQ does not respond to addresses 16-119; reading addresses 120-127 sends the device ID plus the contents of register 0 to address 124.

APPLICATION HINTS

Principle Input Circuits

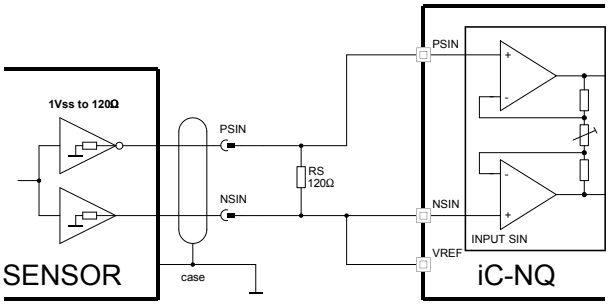


Figure 21: Input circuit for voltage signals of 1 Vpp with no ground reference. When grounds are not separated the connection NSIN to VREF must be omitted.

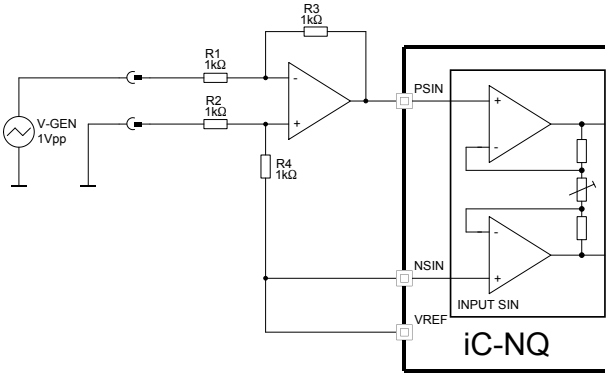


Figure 23: Input circuit for single-side voltage or current source signals with ground reference (adaptation via resistors R3, R4).

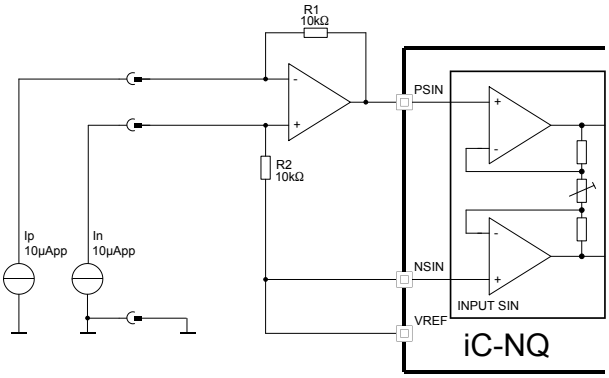


Figure 25: Input circuit for differential current sink sensor outputs, eg. using Opto Encoder iC-WG.

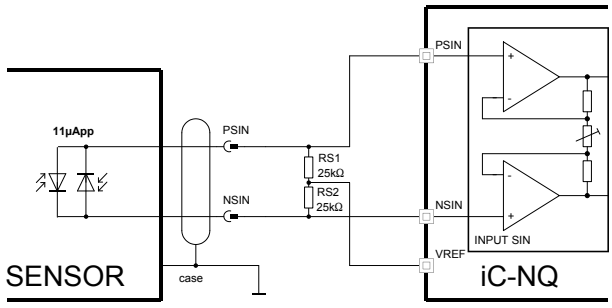


Figure 22: Input circuit for current signals of 11 µA.

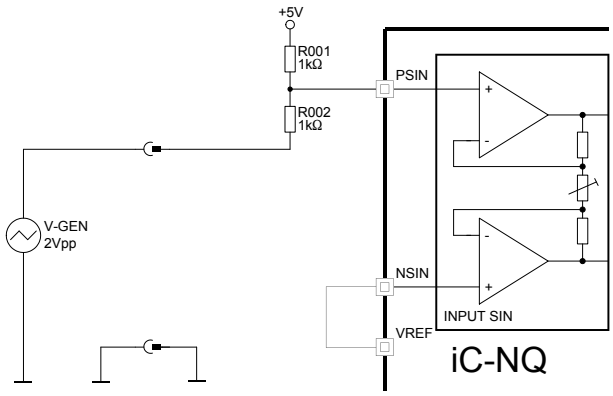


Figure 24: Simplified input wiring for single-side voltage signals with ground reference.

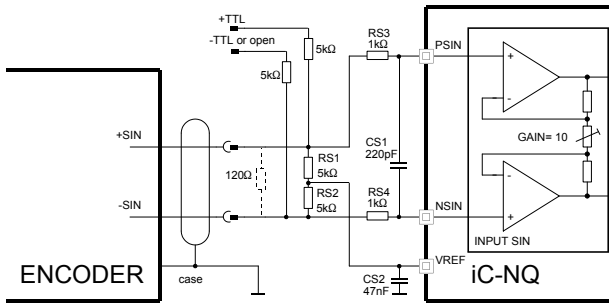


Figure 26: Combined input circuit for 11 µA, 1 Vpp (with 120 Ω termination) or TTL encoder signals. RS3/4 and CS1 serve as protection against ESD and transients.

Basic circuit

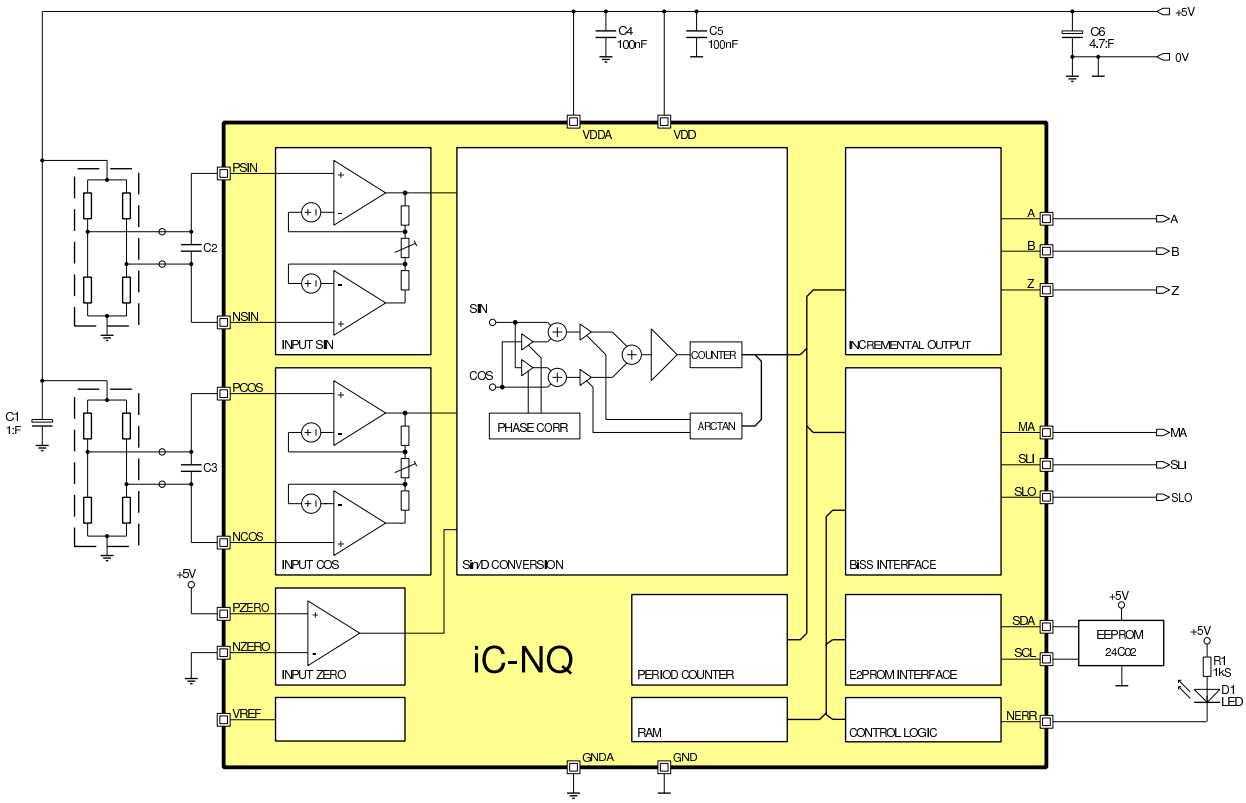


Figure 27: Basic circuit for evaluation of magneto-resistor bridge sensors.

EVALUATION BOARD

The iC-NQ device is equipped with an evaluation board for test purposes; descriptions are available separately.

DESIGN REVIEW: Notes On Chip Functions

iC-NQ X2 **iC-NQ X3**		
No.	Function, Parameter/Code	Description and Application Hints
1	**SELRES** Illegal setting: 0x0E for resolution 4	A minimal resolution of 8 is required for the frequency monitoring function and period counting as well. Thus, a binary resolution of 4 is not permitted when using the period counter and the serial interface for data output with the BiSS or SSI protocol. A resolution of 4 may be used for solely incremental applications with A/B/Z output, what then requires the deactivation of the frequency monitoring function (by FERR set to 0x00).
2	**ZPOS** Illegal settings: 0x01...0x07, 0x09...0x0F, 0x11...0x17, 0x19...0x1F	Illegal settings of ZPOS delay accurate converter operation following power on. Depending on the sin/cos input signals (phase angle) the A/B outputs can provide pulses causing an external counter to alternately count up and down. This may disturb the startup of a drive if the motion controller tolerates only single A/B edges during standstill checking. The converter operation is again accurate when the sin/cos input signals have changed, by a maximum of 45 angular degrees.
3	**M2S** Illegal settings: 0x02, 0x03	Illegal settings, enabling a period counter output of 12 or 24 bits, may cause position data jumping with fast changes in the direction of count (e.g. applications with length gauges). It is thus advisable to use 8-bit period counting (M2S 0x01) and to capture the overflow in the external microcontroller.

Table 40: Notes on chip functions regarding iC-NQ chip releases X2, X3

iC-NQ V2		
No.	Function, Parameter/Code	Description and Application Hints
1	**SELRES**	See description given for iC-NQ X2, X3
2		No further exclusions known at time of printing.

Table 41: Notes on chip functions regarding iC-NQ chip release V2

ORDERING INFORMATION

Type	Package	Order Designation
iC-NQ	TSSOP20 4.4 mm	iC-NQ TSSOP20 iC-NQ TSSOP20 ET -40/125
Evalutaion Board		iC-NQ EVAL NQ1D

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