OptiMOS®-T Power-Transistor

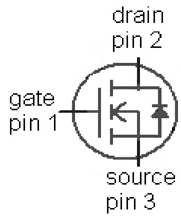
Product Summary

V_{DS}	55	V
$R_{DS(on),max}$	20	mΩ
I_D	30	A

Features

- N-channel - Logic Level - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS compliant)
- 100% Avalanche tested

PG-TO252-3-11



Type	Package	Marking
IPD30N06S3L-20	PG-TO252-3-11	3N06L20

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current[1)]	I_D	T_C=25 °C, V_{GS}=10 V	30	A
		T_C=100 °C, V_{GS}=10 V[2)]	25	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25 °C	120	
Avalanche energy, single pulse[2)]	E_{AS}	I_D=15 A	100	mJ
Avalanche current, single pulse	I_{AS}		30	A
Gate source voltage[3)]	V_{GS}		±16	V
Power dissipation	P_{tot}	T_C=25 °C	45	W
Operating and storage temperature	T_j, T_{stg}		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2]						
Thermal resistance, junction - case	R_{thJC}		-	-	3.3	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[4]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D= 1 mA	55	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=20 µA	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=55 V, V_{GS}=0 V, T_j=25 °C	-	0.01	1	µA
		V_{DS}=55 V, V_{GS}=0 V, T_j=125 °C[2]	-	1	100	
Gate-source leakage current	I_{GSS}	V_{GS}=16 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=5 V, I_D=11 A	-	32	38	mΩ
		V_{GS}=10 V, I_D=17 A	-	17	20	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2)]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	2260	2600	pF
Output capacitance	C_{oss}		-	283	425	
Reverse transfer capacitance	C_{rss}		-	270	405	
Turn-on delay time	$t_{d(on)}$	V_{DD}=27.5 V, V_{GS}=10 V, I_D=30 A, R_G=25 Ω	-	9	-	ns
Rise time	t_r		-	34	-	
Turn-off delay time	$t_{d(off)}$		-	43	-	
Fall time	t_f		-	74	-	
Gate Charge Characteristics[2)]						
Gate to source charge	Q_{gs}	V_{DD}=11 V, I_D=30 A, V_{GS}=0 to 10 V	-	12	16	nC
Gate to drain charge	Q_{gd}		-	6	9	
Gate charge total	Q_g		-	32	37	
Gate plateau voltage	$V_{plateau}$		-	4.9	-	V
Reverse Diode						
Diode continous forward current[2)]	I_S	T_C=25 °C	-	-	30	A
Diode pulse current[2)]	$I_{S,pulse}$		-	-	120	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=30 A, T_j=25 °C	0.6	0.9	1.3	V
Reverse recovery time[2)]	t_{rr}	V_R=27.5 V, I_F=I_S, di_F/dt=100 A/µs	-	32	-	ns
Reverse recovery charge[2)]	Q_{rr}		-	28	-	nC

1) Current is limited by bondwire; with an R_{thJC} = 3.3 K/W the chip is able to carry 35 A at 25°C. For detailed information see Application Note ANPS071E.

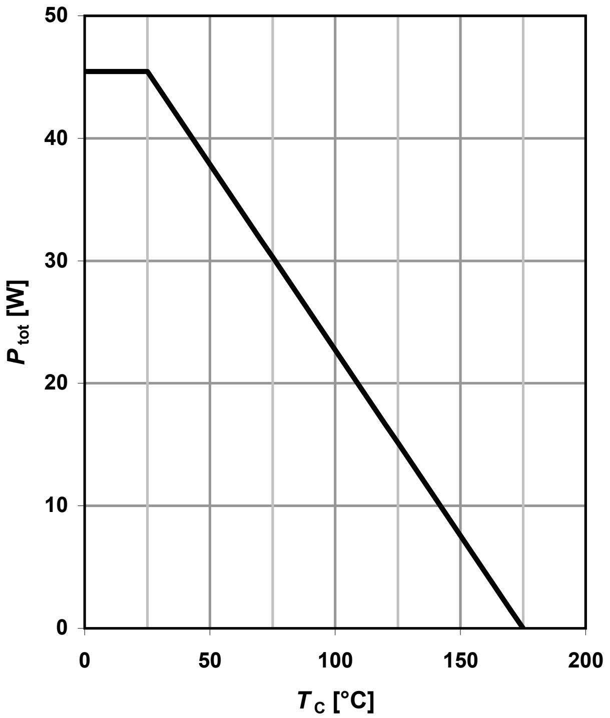
2) Defined by design. Not subject to production test.

3) Qualified at -5V and +20V.

4) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

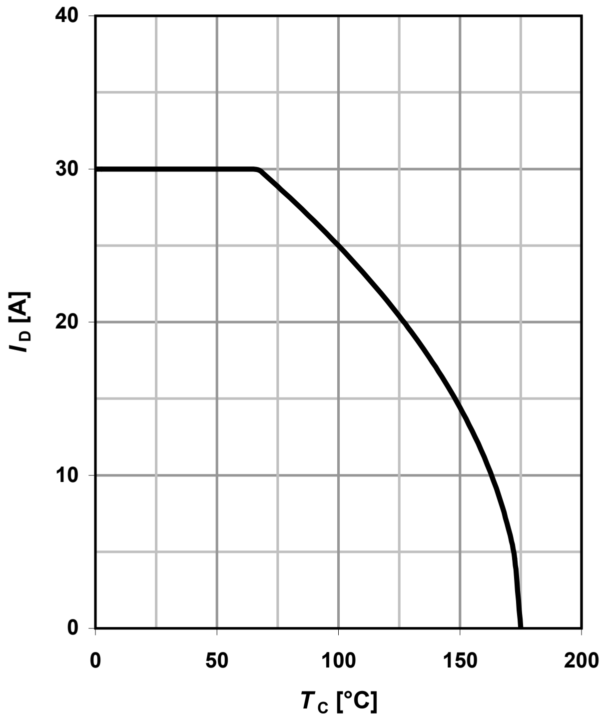
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 4$ V



2 Drain current

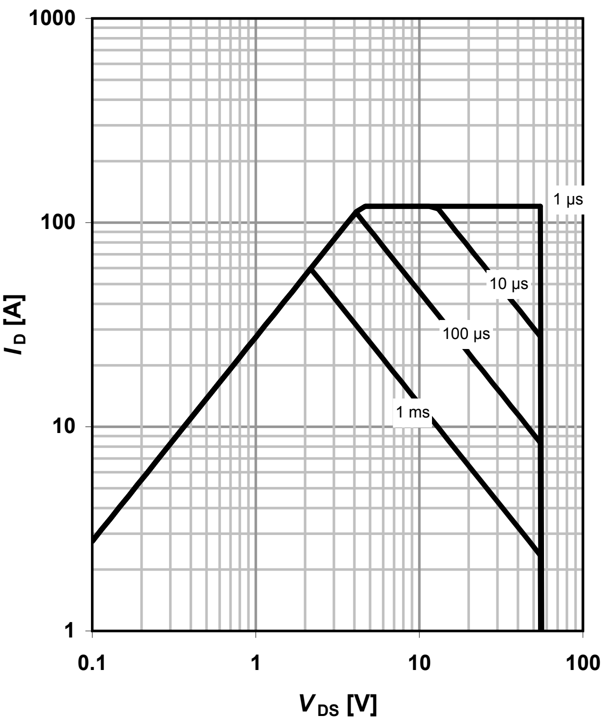
$I_D = f(T_C)$; $V_{GS} \geq 4$ V



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

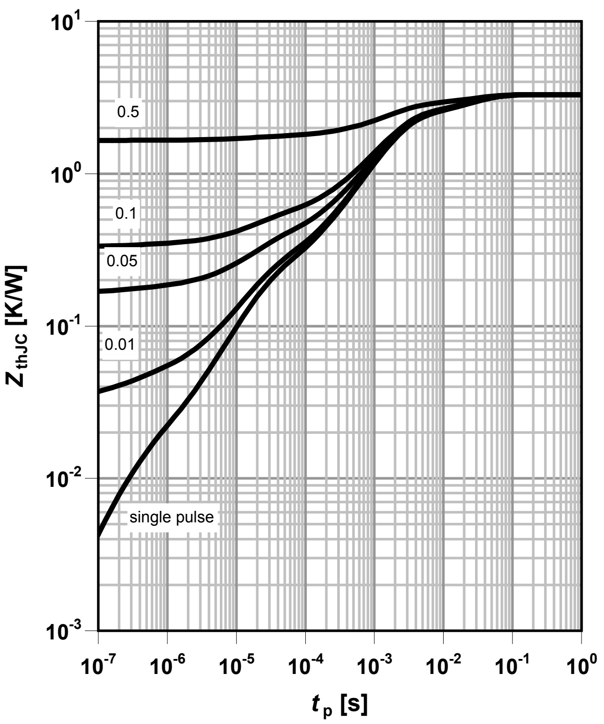
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

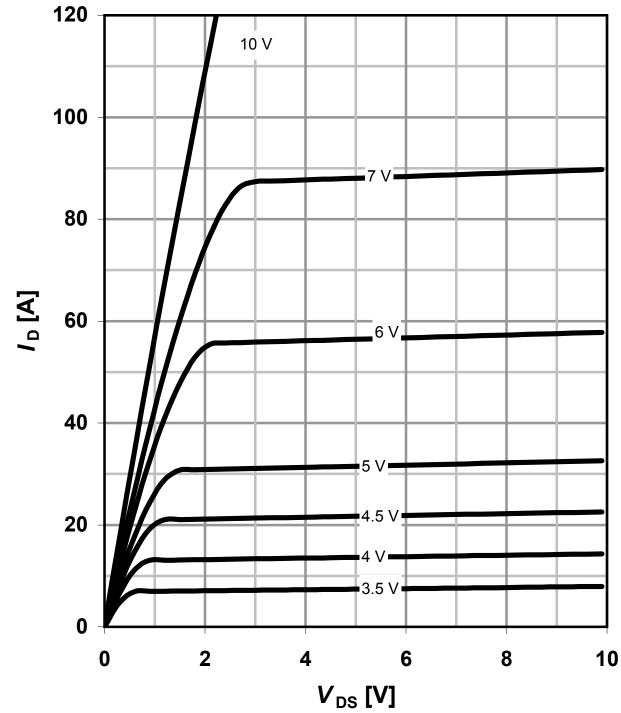
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C

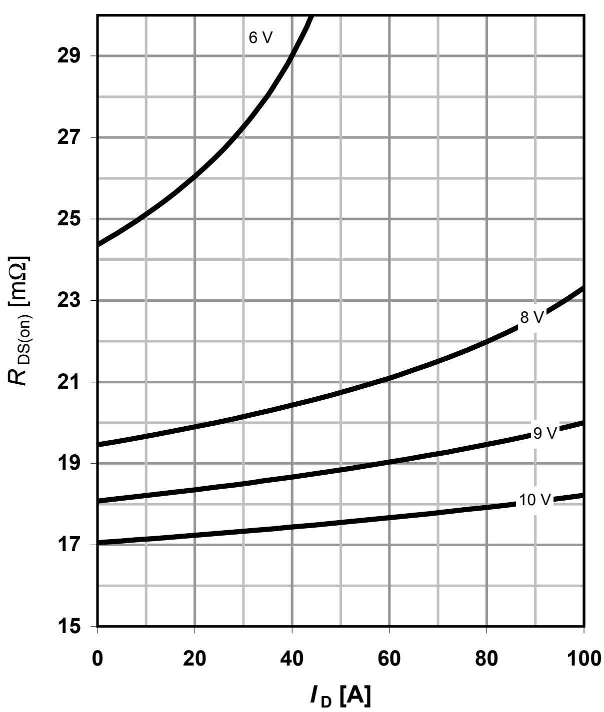
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C

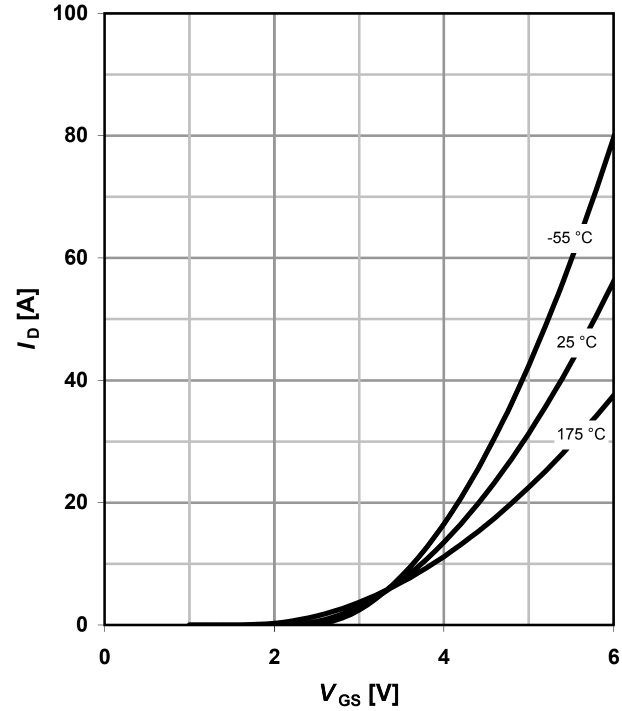
parameter: V_{GS}



7 Typ. transfer characteristics

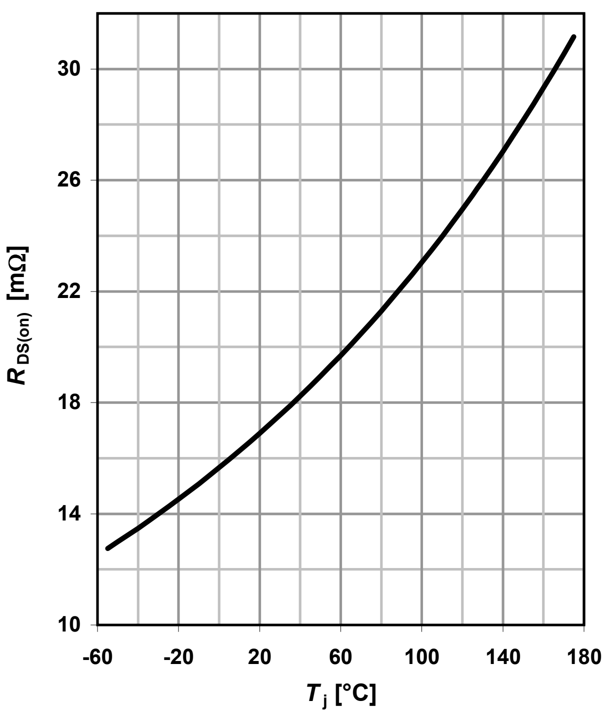
$I_D = f(V_{GS})$; $V_{DS} = 4$ V

parameter: T_j



8 Typ. drain-source on-state resistance

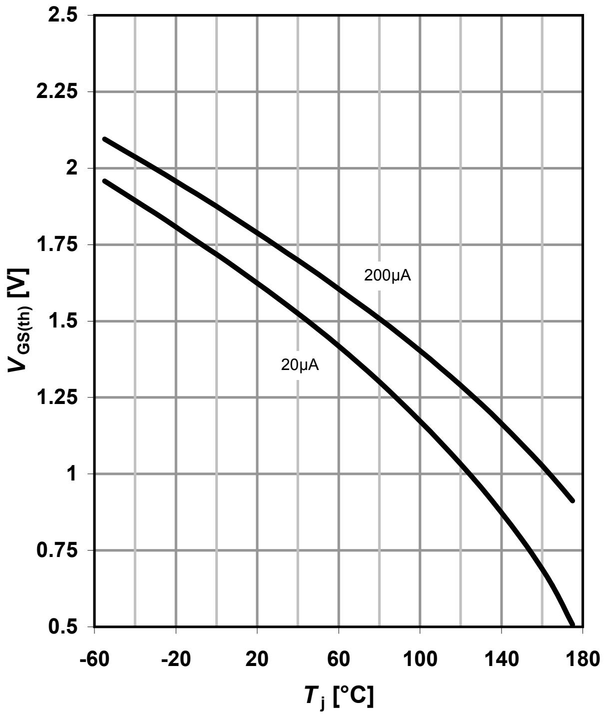
$R_{DS(on)} = f(T_j)$; $I_D = 18$ A; $V_{GS} = 10$ V



9 Typ. gate threshold voltage

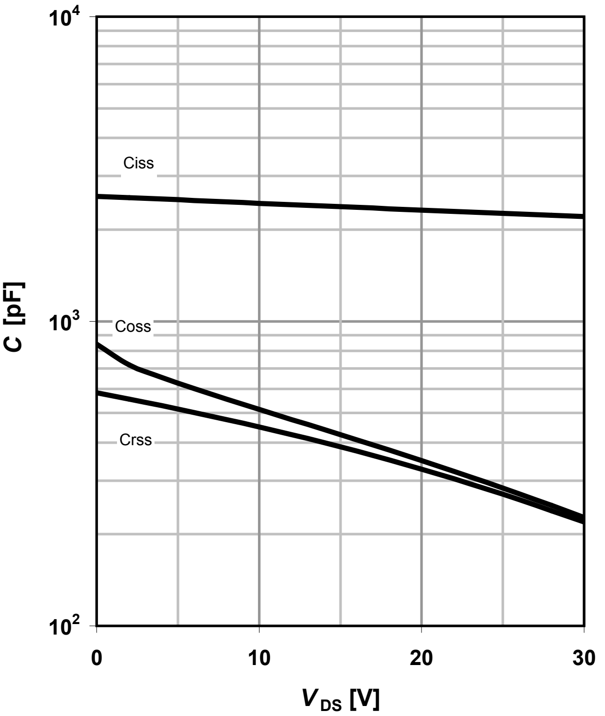
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

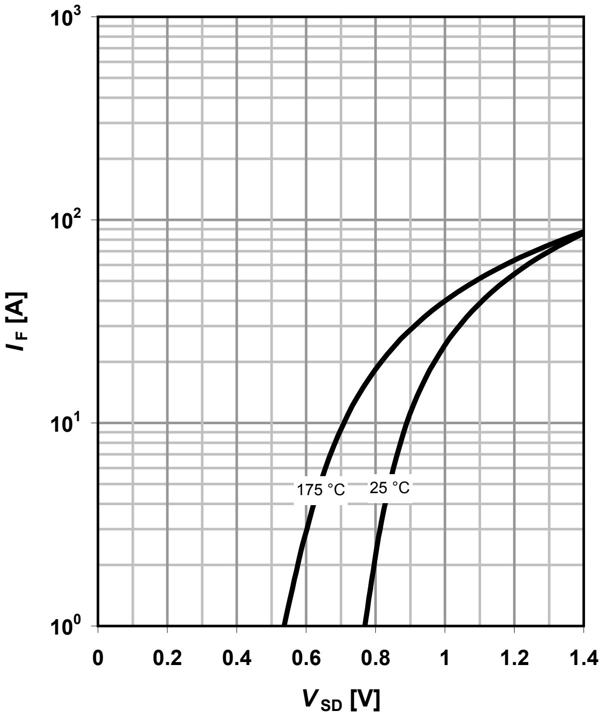
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis

IF = $f(V_{SD})$

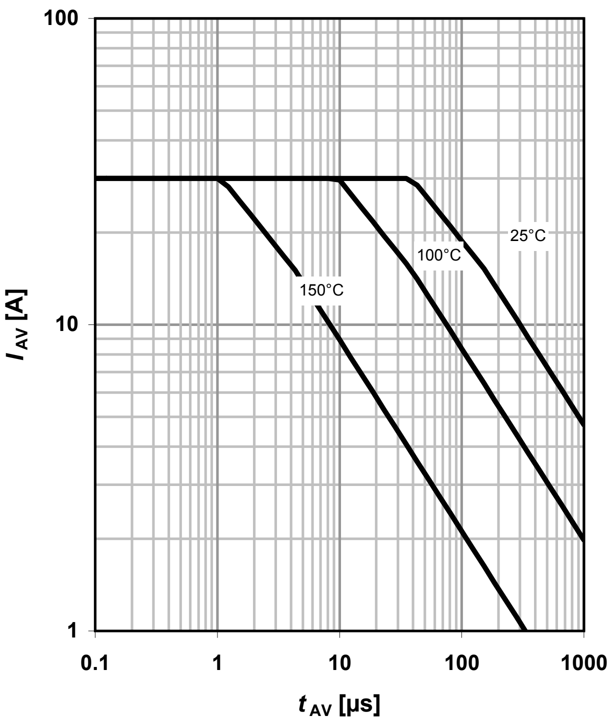
parameter: T_j



12 Typ. avalanche characteristics

$I_{AV} = f(t_{AV})$

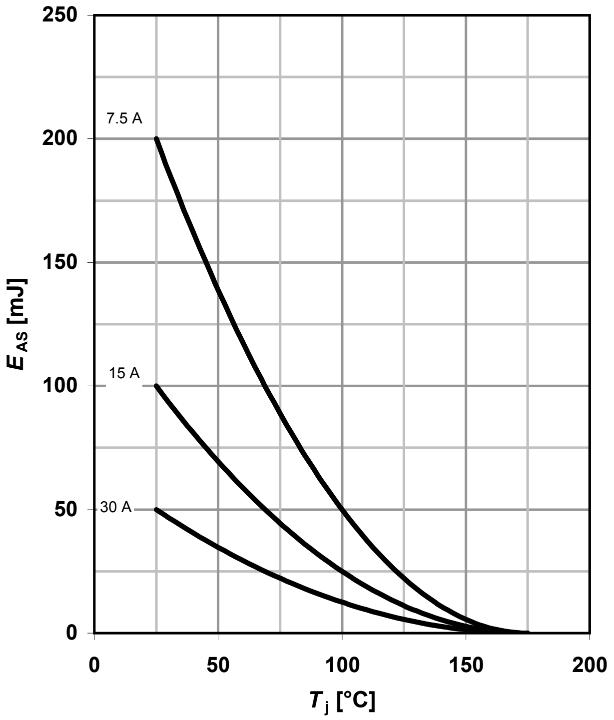
parameter: $T_{j(start)}$



13 Typical avalanche Energy

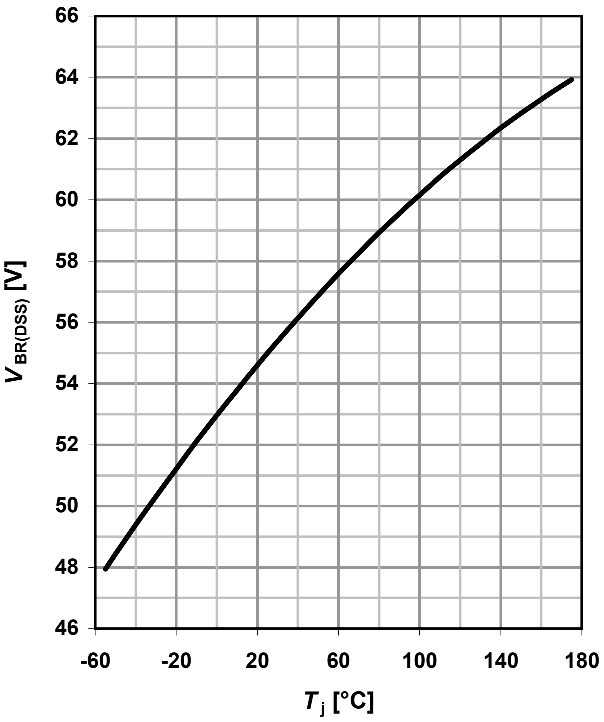
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

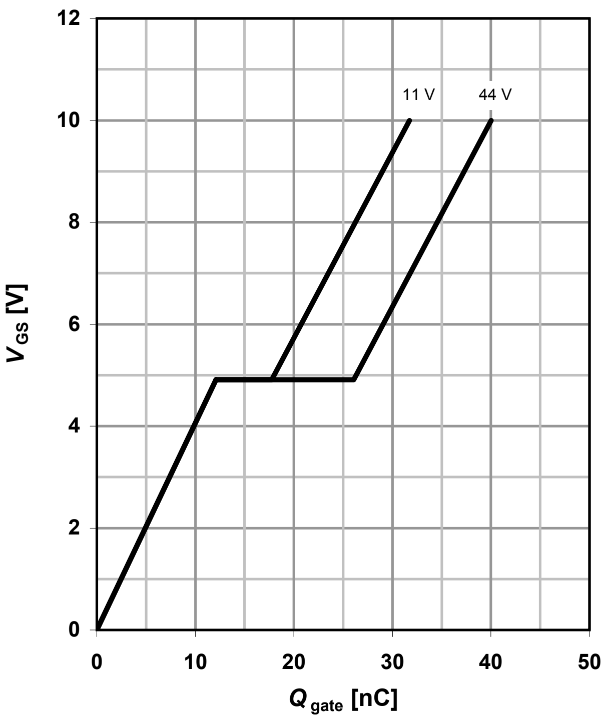
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



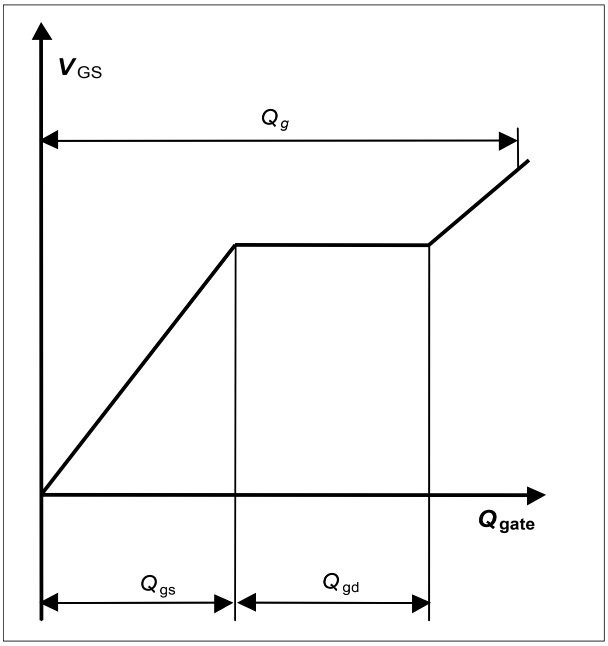
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 30$ A pulsed

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Data Sheet version 1.1	07.11.2007	Removal of feature: ultra low Rdson
Data Sheet version 1.1	07.11.2007	Implementation of avalanche current single pulse
Data Sheet version 1.1	07.11.2007	Update of package drawing
Data Sheet version 1.1	07.11.2007	Update of avalanche diagram 12 and 13
Data Sheet version 1.1	07.11.2007	implementation of footnote 2 for Eas specification