FAIRCHILD SEMICONDUCTOR®

February 2007

FAN7383
Half-Bridge Gate-Drive IC

Features

- Floating Channel Designed for Bootstrap Operation to +600V.
- Typically 350mA/650mA Sourcing/Sinking Current Driving Capability for Both Channels
- Extended Allowable Negative V_S Swing to -9.8V for Signal Propagation at V_{DD}=V_{BS}=15V
- High-Side Output in Phase of IN Signal
- Built-in UVLO Functions for Both Channels
- Built-in Common-Mode dv/dt Noise Canceling Circuit
- Typically Internal 330ns Minimum Dead-Time
- Programmable Turn-On Delay Time Control (Dead-Time)

Applications

- SMPS
- Motor Drive Inverter
- Fluorescent Lamp Ballast
- HID Ballast

Description

The FAN7383 is a half-bridge gate-drive IC with shutdown and programmable dead-time control functions for driving MOSFETs and IGBTs that operate up to +600V.

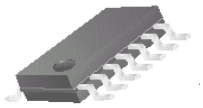
Fairchild's high voltage process and common-mode noise canceling technique give stable operation of high-side drivers under high-dv/dt noise circumstances.

An advanced level-shift circuit allows high-side gate driver operation up to V_S= -9.8V (typical) for V_{BS}=15V.

The UVLO circuits for both channels prevent malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

Output drivers typically source/sink 350mA/650mA, respectively, which is suitable for all kinds of half and full bridge inverter.

14-SOP



Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packing Method
FAN7383M(1)	14-SOP	Yes	-40°C ~ 125°C	Tube
FAN7383MX(1)				Tape & Reel

Note:

1. These devices passed wave soldering test by JESD22A-111.

Typical Application Circuit

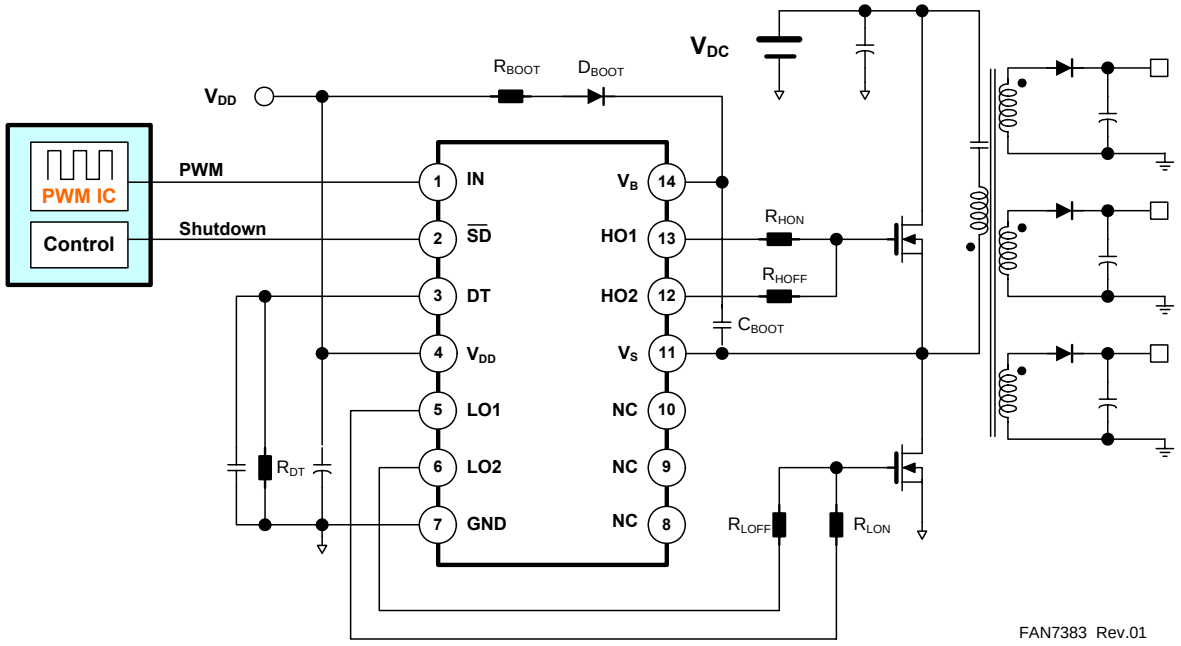


Figure 1. Application Circuit for Half-Bridge Switching Power Supply

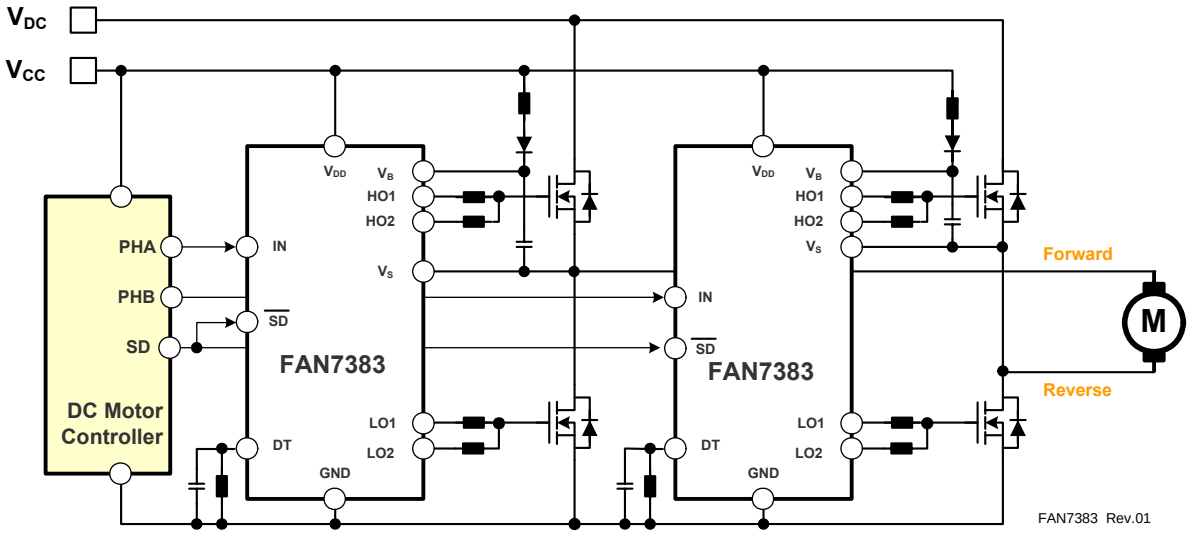


Figure 2. Application Circuit for Full-Bridge DC Motor Driver

Internal Block Diagram

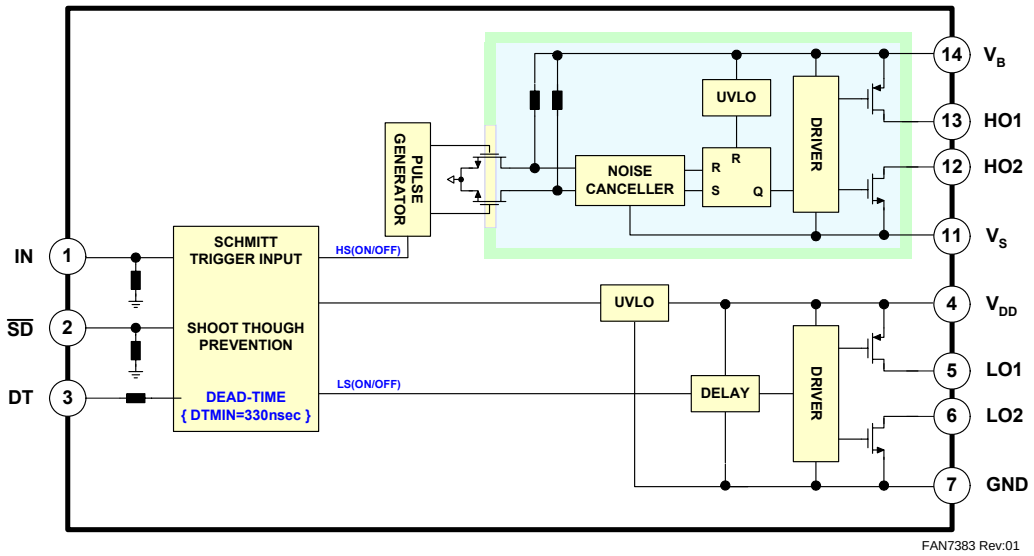


Figure 3. Functional Block Diagram of FAN7383

Pin Configuration

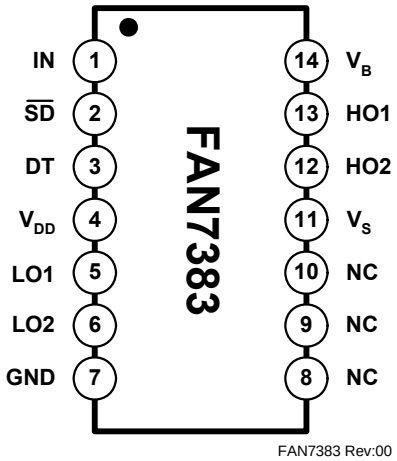


Figure 4. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	IN	Logic Input for Gate Driver
2	$\overline{SD}$	Logic Input for Shutdown (Active Low)
3	DT	Programmable Dead-Time Control with External Resistor
4	V_{DD}	Low-Side Supply Voltage
5	LO1	Low-Side Driver Source Output
6	LO2	Low-Side Driver Sink Output
7	GND	Ground
8	N.C.	Not connected
9	N.C.	Not connected
10	N.C.	Not connected
11	V_S	High-Side Floating Supply Return
12	HO2	High-Side Driver Sink Output
13	HO1	High-Side Driver Source Output
14	V_B	High-Side Floating Supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_S	High-side offset voltage	V_B-25	V_B+0.3	V
V_B	High-side floating supply voltage	-0.3	625	V
V_{HO}	High-side floating output voltage HO1, HO2	V_S-0.3	V_B+0.3	V
V_{DD}	Low-side and logic fixed supply voltage	-0.3	25	V
V_{LO}	Low-side output voltage LO1, LO2	-0.3	V_{DD}+0.3	V
V_{IN}	Logic input voltage (IN)	-0.3	V_{DD}+0.3	V
$V_{\overline{SD}}$	Shutdown logic input voltage	-0.3	V_{DD}+0.3	V
V_{DT}	Dead-time control voltage	-0.3	5.0	V
GND	Logic ground	V_{DD}-25	V_{DD}+0.3	V
dV_S/dt	Allowable offset voltage slew rate		50	V/ns
P_D[(2)(3)(4)]	Power dissipation		1.0	W
θ_{JA}	Thermal resistance, junction-to-ambient		110	°C/W
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature		150	°C

Notes:

2. When mounted on 76.2 x 114.3 x 1.6mm PCB. (FR-4 glass epoxy material).

3. Please refer to:

   JESD51-2: Integral circuits thermal test method environmental conditions - Natural convection

   JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages

4. Do not exceed P_D under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min.	Max.	Unit
V_B	High-side floating supply voltage		V_S+15	V_S+20	V
V_S	High-side floating supply offset voltage		6-V_{DD}	600	V
V_{DD}	Low-side supply voltage		15	20	V
V_{HO}	High-side (HO) output voltage		V_S	V_B	V
V_{LO}	Low-side (LO) output voltage		GND	V_{DD}	V
V_{IN}	Logic input voltage (IN)		GND	V_{DD}	V
T_A	Ambient temperature		-40	125	°C

Electrical Characteristics

V_{BIAS} (V_{DD}, V_{BS}) = 15.0V, R_{DT} = GND, T_A = 25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are referenced to V_S and GND and are applicable to the respective outputs HO and LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SUPPLY CURRENT SECTION						
I_{QBS}	Quiescent V_{BS} supply current	V_{IN}=0V or 5V		35	90	μA
I_{QDD}	Quiescent V_{DD} supply current	V_{IN}=0V or 5V, R_{DT}=0Ω		650	900	
I_{SD}(5)	V_{DD} supply current at shutdown mode	$\overline{SD}$=GND		650	900	
I_{PBS}	Operating V_{BS} supply current	f_{IN}=20kHz,rms value		400	700	
I_{PDD}	Operating V_{DD} supply current	f_{IN}=20kHz,rms value, R_{DT}=0Ω		950	1200	
I_{LK}	Offset supply leakage current	V_B=V_S=600V			10	
POWER SUPPLY SECTION						
V_{DDUV+} V_{BSUV+}	V_{DD} and V_{BS} supply under-voltage positive going threshold		10.7	11.6	12.5	V
V_{DDUV-} V_{BSUV-}	V_{DD} and V_{BS} supply under-voltage negative going threshold		10.0	10.8	11.6	
V_{DDUVH} V_{BSUVH}	V_{DD} and V_{BS} supply under-voltage lockout hysteresis			0.8		
GATE DRIVER OUTPUT SECTION						
V_{OH}	High-level output voltage, V_{BIAS}-V_O	I_O=20mA			1.0	V
V_{OL}	Low-level output voltage, V_O				0.6	V
I_{O+}	Output high short-circuit pulse current	V_O=0V, V_{IN}=5V with PW<10μs	250	350		mA
I_{O-}	Output low short-circuit pulsed current	V_O=15V, V_{IN}=0V with PW<10μs	500	650		mA
V_S	Allowable negative V_S pin voltage for IN signal propagation to HO			-9.8	-7.0	V
LOGIC INPUT SECTION (INPUT AND SHUTDOWN)						
V_{IH}	Logic "1" input voltage		2.9			V
V_{IL}	Logic "0" input voltage				1.2	V
I_{IN+}	Logic "1" input bias current	V_{IN}=5V		50	100	μA
I_{IN-}	Logic "0" input bias current	V_{IN}=0V			2.0	μA
$\overline{SD}$+	Shutdown "1" input voltage				1.2	V
$\overline{SD}$-	Shutdown "0" input voltage		2.9			V
R_{PD}	Input pull-down resistance			100		KΩ

Note:

5.This parameter guaranteed by design.

Dynamic Electrical Characteristics

V_{BIAS} (V_{DD}, V_{BS}) = 15.0V, V_S = GND, C_L=1000pF, R_{DT} = GND, and T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Turn-on propagation delay	V_S=0V		500	670	ns
t_{OFF}	Turn-off propagation delay	V_S=0V or 600V(5)		170	250	
t_R	Turn-on rise time			50	100	
t_F	Turn-off fall time			30	80	
t_{SD}(5)	Shutdown propagation delay			100	180	
DT1, DT2	Dead-time LO OFF to HO ON and HO OFF to LO ON	R_{DT}=0Ω	250	330	420	ns
		R_{DT}=200KΩ	1.20	1.68	2.30	µs
DMT	Dead-time matching	R_{DT}=0Ω		0	60	ns
		R_{DT}=200KΩ		0	150	

Note:

5.These parameters guaranteed by design.

Typical Characteristics

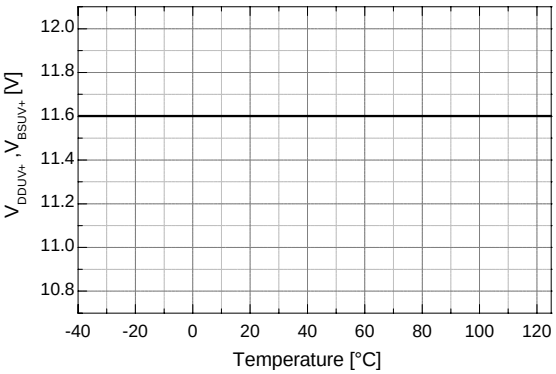


Figure 5. V_{DD}/V_{BS} UVLO (+) vs. Temperature

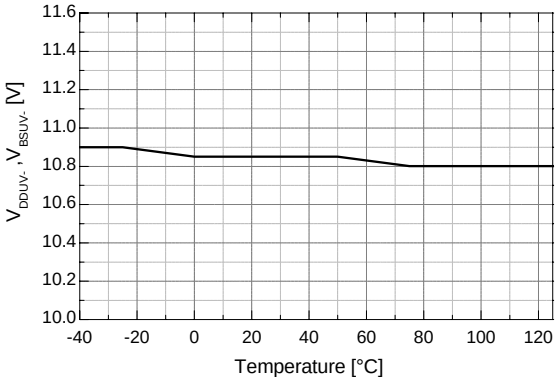


Figure 6. V_{DD}/V_{BS} UVLO (-) vs. Temperature

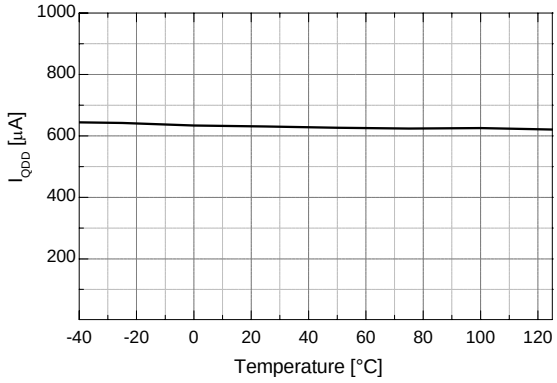


Figure 7. V_{DD} Quiescent Current vs. Temperature

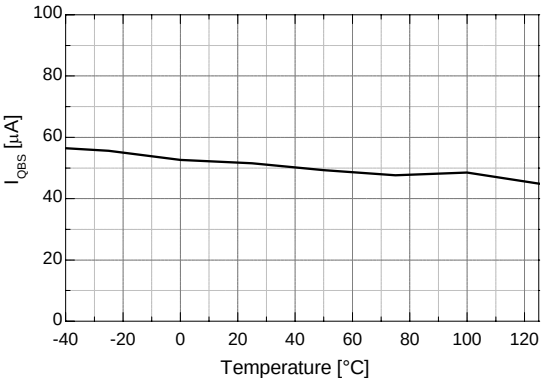


Figure 8. V_{BS} Quiescent Current vs. Temperature

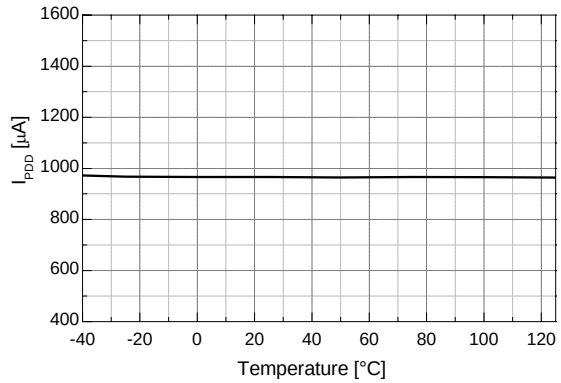


Figure 9. V_{DD} Operating Current vs. Temperature

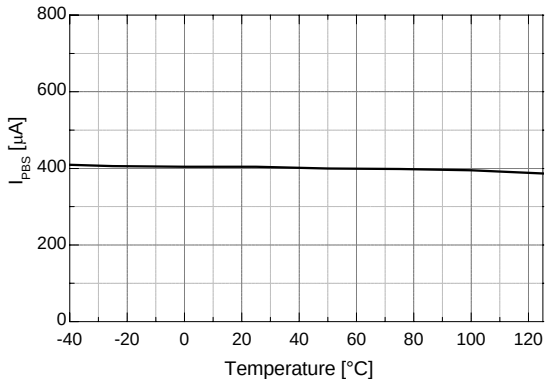


Figure 10. V_{BS} Operating Current vs. Temperature

Typical Characteristics (Continued)

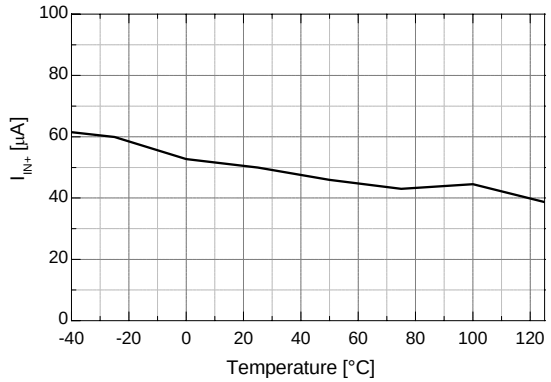


Figure 11. Logic Input Current vs. Temperature

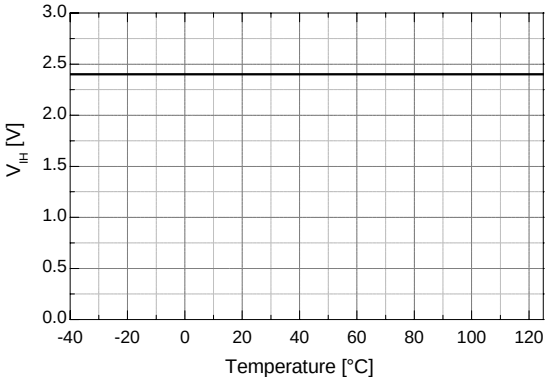


Figure 12. Logic Input High Voltage vs. Temperature

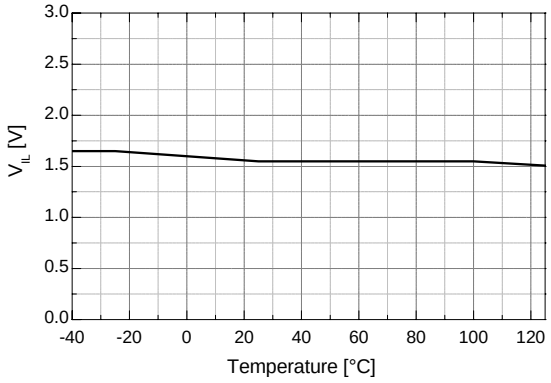


Figure 13. Logic Input Low Voltage vs. Temperature

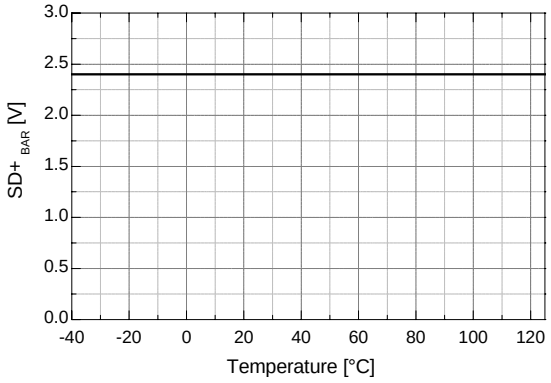


Figure 14. $\overline{SD}$ Positive Threshold vs. Temperature

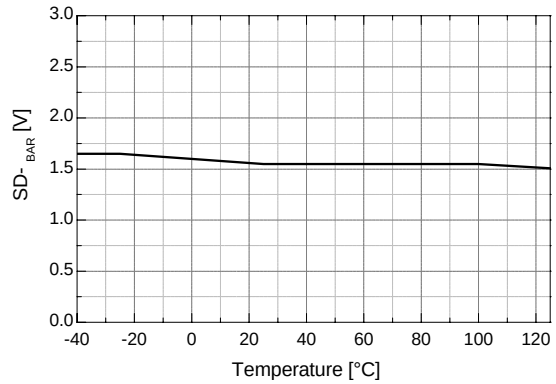


Figure 15. $\overline{SD}$ Negative Threshold vs. Temperature

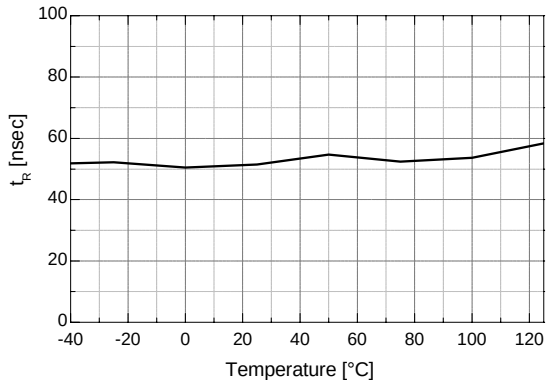


Figure 16. Rising Time vs. Temperature

Typical Characteristics (Continued)

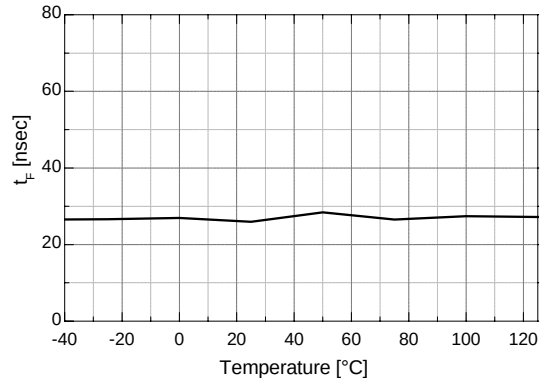


Figure 17. Falling Time vs. Temperature

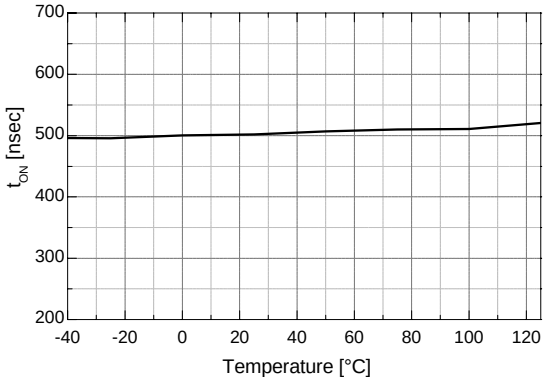


Figure 18. Turn-on Delay Time vs. Temperature

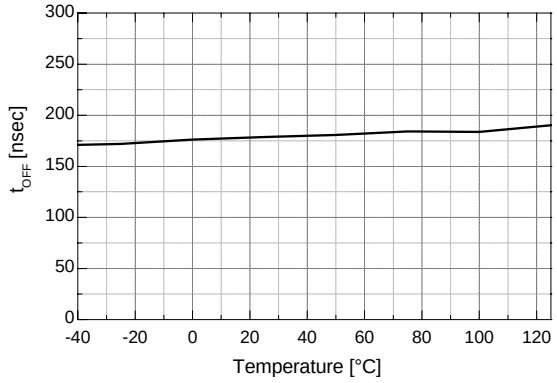


Figure 19. Turn-off Falling Time vs. Temperature

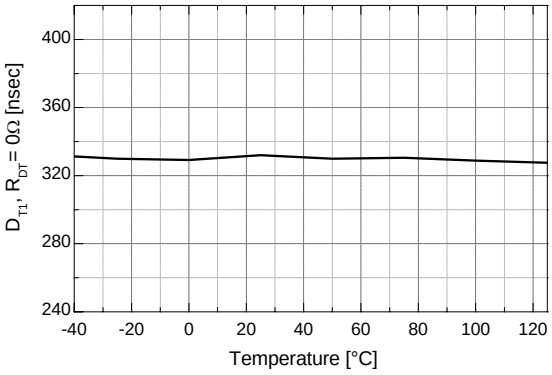


Figure 20. Dead-Time (R_{DT}=0kΩ) vs. Temperature

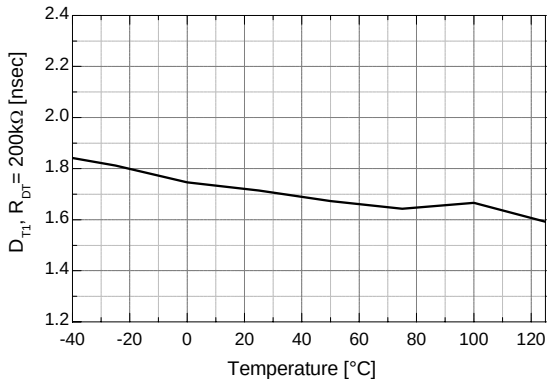


Figure 21. Dead Time (R_{DT}=200kΩ) vs. Temperature

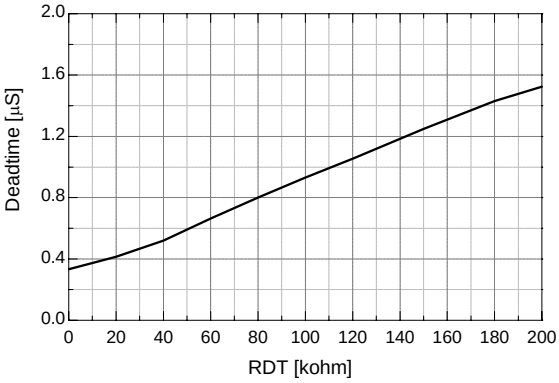


Figure 22. R_{DT} vs. Dead Time

Typical Characteristics (Continued)

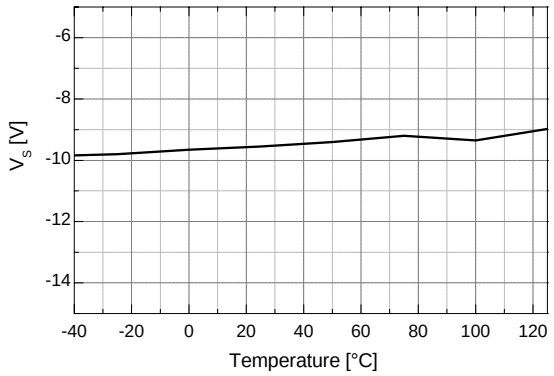


Figure 23. Allowable Negative V_S Voltage for Signal Propagation to High Side vs. Temperature

Switching Time Definitions

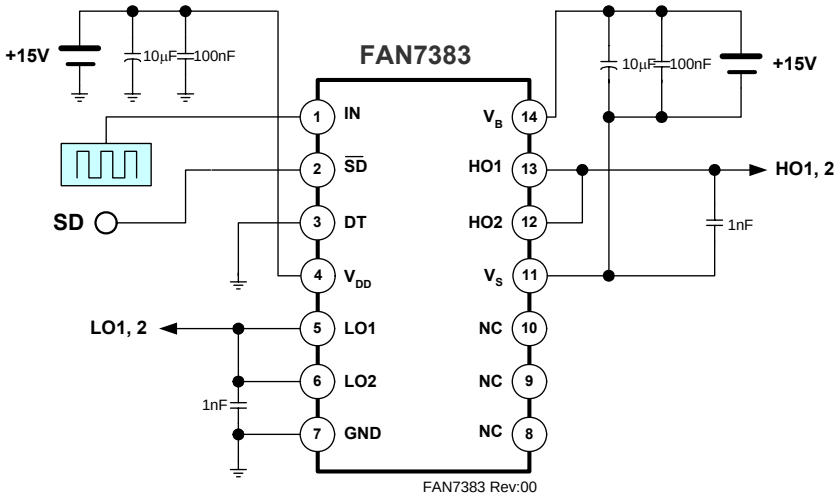


Figure 24. Switching Time Test Circuit

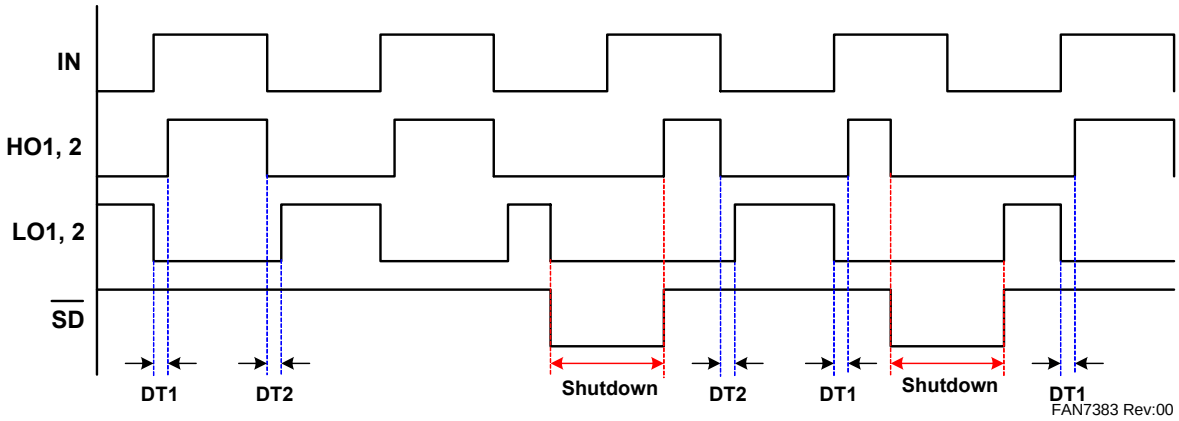


Figure 25. Input / Output Waveforms

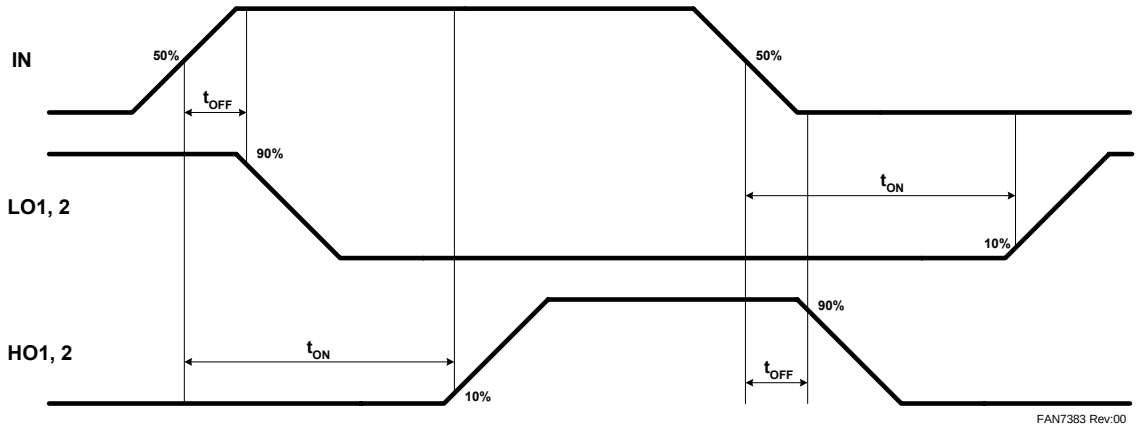


Figure 26. Switching Time Waveform Definitions

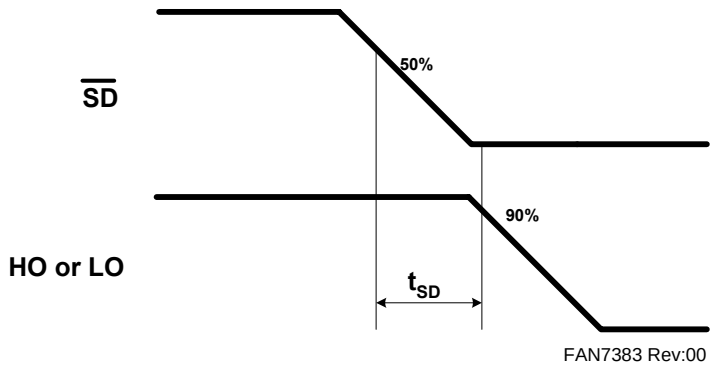


Figure 27. Shutdown Waveform Definition

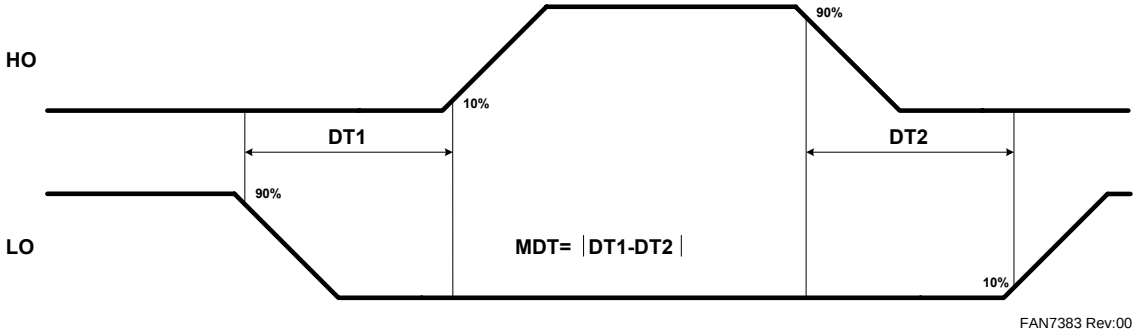


Figure 28. Dead-Time Waveform Definition

Typical Application Information

1. Normal Operating Consideration

The FAN7383 is a single PWM input half-bridge gate-drive IC with programmable dead-time and shutdown function.

The dead-time is set with a resistor (R_{DT}) at the DT pin. The wide dead-time programming range provides the flexibility to optimize drive signal timing for a selection of switching devices (MOSFET or IGBT) and applications.

The turn-on time delay circuitry (Dead-Time) accommodates resistor values from 0Ω to 200kΩ with a dead-time proportional to the R_{DT} resistance.

Grounding the DT pin programs the FAN7383 to drive both outputs with minimum dead time.

If the $\overline{SD}$ pin voltage decrease below 1.2V in normal operation, the IC enters the shutdown mode.

2. Under-Voltage Lockout (UVLO)

The FAN7383 has an under-voltage lockout (UVLO) protection circuitry for high and low side channels to prevent malfunction when V_{DD} or V_{BS} is lower than the specified threshold voltage. The UVLO circuitry monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (V_{BS}) independently.

3. Layout Consideration

For optimum performance of high- and low-side gate drivers, cannot be achieved without taking due considerations must be taken during printed circuit board (PCB) layout.

3.1 Supply Capacitors

If the output stages are able to quickly turn on the switching device with high value of current, the supply capacitors must be placed as close as possible to the device pins (V_{DD} and GND for the ground-tied supply, V_B and V_S for the floating supply) to minimize parasitic inductance and resistance.

3.2 Gate Drive Loop

Current loops behave like an antenna, able to receive and transmit noise. To reduce the noise coupling/ emission and improve the power switch turn-on and off performances, gate drive loops must be reduced as much as possible.

3.3 Ground Plane

Ground plane must not be placed under or nearby the high-voltage floating side to minimize noise coupling.

Package Dimensions

14-SOP

Dimensions are in millimeters unless otherwise noted.

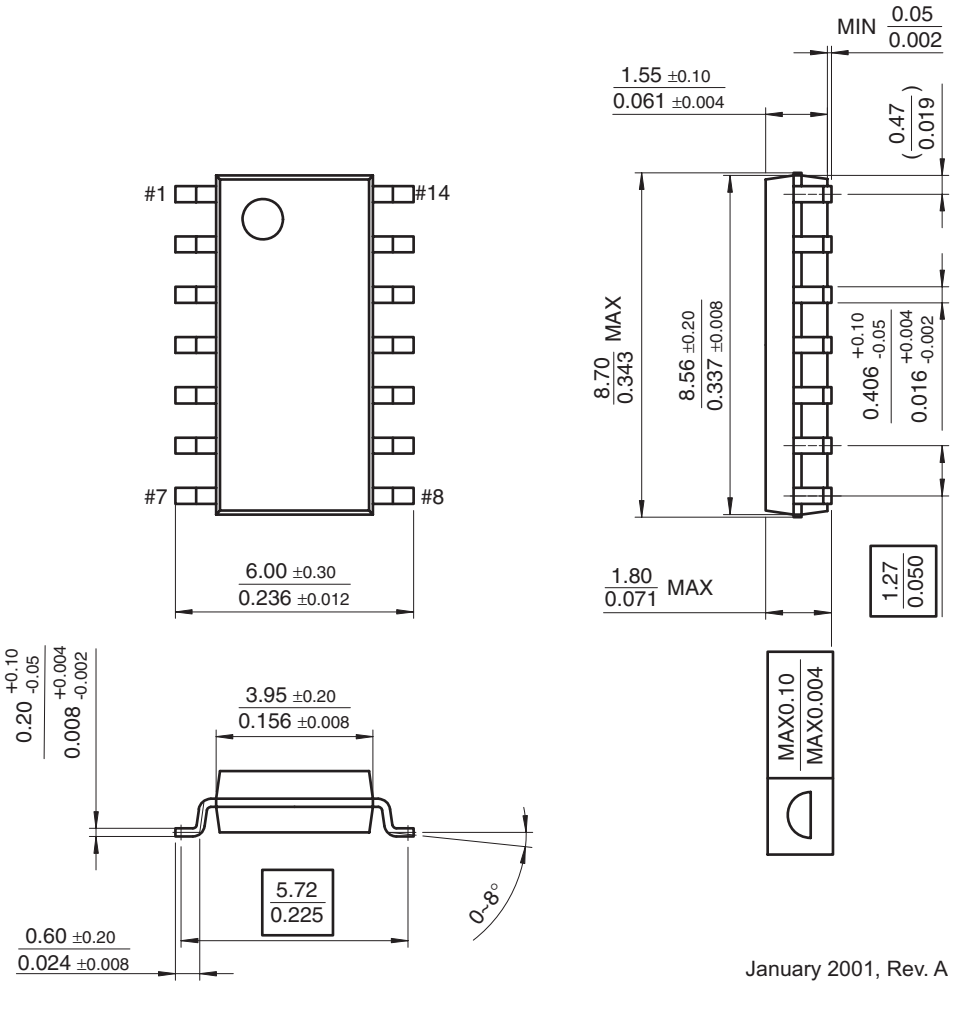


Figure 29. 14-Lead Small Outline Package (SOP)

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Across the board. Around the world.™
ActiveArray™
Bottomless™
Build it Now™
CoolFET™
CROSSVOLT™
CTL™
Current Transfer Logic™
DOME™
E^2CMOS™
EcoSPARK®
EnSigna™
FACT Quiet Series™
FACT®
FAST®
FASTr™
FPS™
FRFET®
GlobalOptoisolator™
GTO™
HiSeC™
i-Lo™
ImpliedDisconnect™
IntelliMAX™
ISOPLANAR™
MICROCOUPLER™
MicroPak™
MICROWIRE™
MSX™
MSXPro™
OCX™
OCXPro™
OPTOLOGIC®
OPTOPLANAR®
PACMAN™
POP™
Power220®
Power247®
PowerEdge™
PowerSaver™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
ScalarPump™
SMART START™
SPM®
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
TCM™
The Power Franchise®
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyWire™
TruTranslation™
μSerDes™
UHC®
UniFET™
VCX™
Wire™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I23