PROCESS CP230

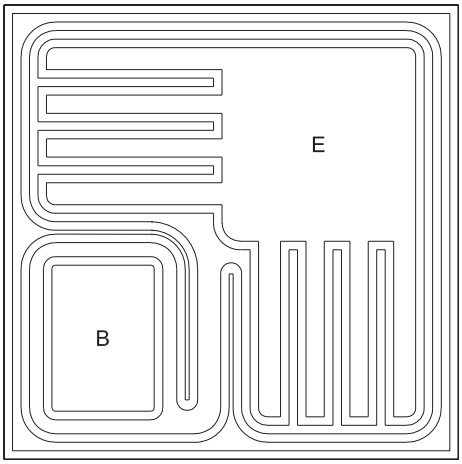
Power Transistor

NPN - Silicon Darlington Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL BASE
Die Size	80 x 80 MILS
Die Thickness	8.0 MILS
Base Bonding Pad Area	18 x 27 MILS
Emitter Bonding Pad Area	34 x 34 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Ti/Pd/Ag - 20,000Å

GEOMETRY



BACKSIDE COLLECTOR R1

GROSS DIE PER 4 INCH WAFER

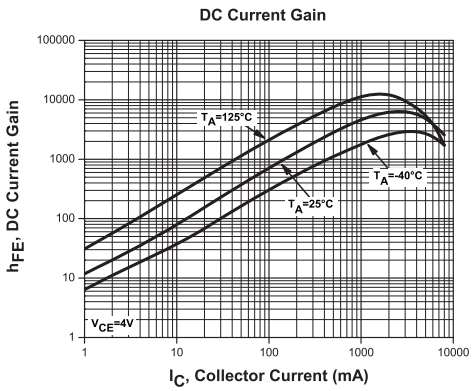
1,445

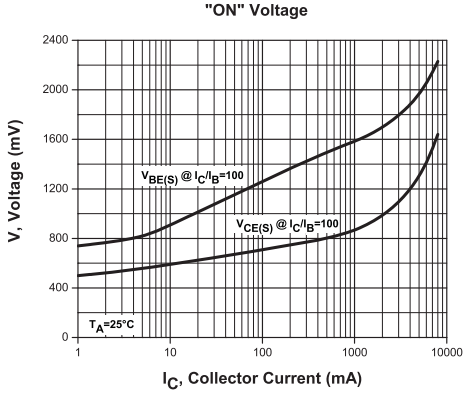
PRINCIPAL DEVICE TYPES

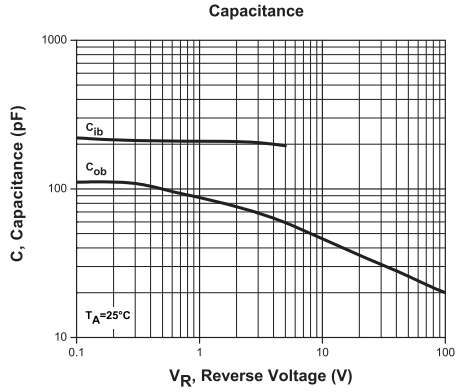
CZT122
CJD122

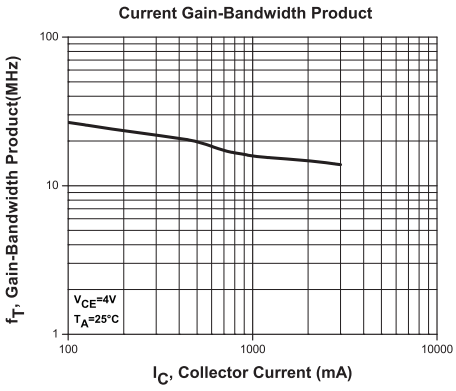
PROCESS CP230

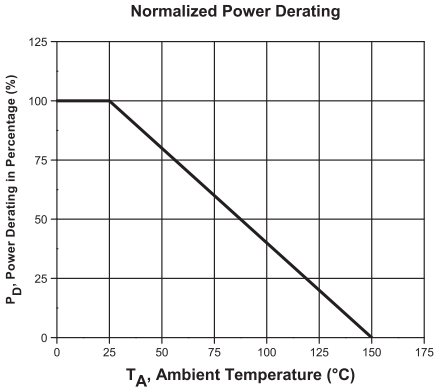
Typical Electrical Characteristics











R2 (22-March 2010)