Three-Phase IGBT BRIDGE, With Gate Driver and Magnetic Isolation

DESCRIPTION: A 600 VOLT, 140 AMP, THREE PHASE IGBT BRIDGE

ELECTRICAL CHARACTERISTICS PER IGBT DEVICE ($T_j=25^0C$ UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
IGBT SPECIFICATIONS					
Collector to Emitter Breakdown Voltage I_C = 500uA, V_{GE} = 0V	BV_{CES}	600	-	-	V
Continuous Collector Current T_C = 25 ^OC T_C = 80 ^OC	I_C	-	-	140 140	A
Zero Gate Voltage Collector Current (For the module) V_{CE} = 600 V, V_{GE}=0V T_i=25^{o}C V_{CE} = 480 V, V_{GE}=0V T_i=125^{o}C	I_{CES}	-	-	 2 15	 mA mA
Collector to Emitter Saturation Voltage, T_j = 25 ^OC I_C = 90A, V_{GE} = 15V, T_j = 125 ^OC	$V_{CE(SAT)}$	-	1.5 1.8	1.8	V
IGBT Internal Turn On Gate Resistance		-	8.2	-	Ohm
IGBT Internal Turn Off Gate Resistance		-	6.2	-	Ohm
IGBT Internal Soft Shutdown Turn Off Gate Resistance		-	100	-	Ohm
IGBT turn-on switching loss V_{CE} = 300 V, I_C = 50A Tj=25^{o}C		-	1.5	-	mJ
IGBT turn-off switching loss V_{CE} = 300 V, I_C = 50A Tj=25^{o}C		-	2.1	-	mJ
Short Circuit Withstand Time, Conditions 300V DC link, VGE=15V, T_{jstart} < 150 ^OC		-	5	-	usec
DC Bus Voltage Rate of Rise With 15V Supply Removed, dv/dt		-	-	20	V/usec
Junction To Case Thermal Resistance	$R_{\theta JC}$	-	-	0.22	^{o}C/W

MODULE TOTAL WEIGHT					
Total Weight		-	-	13	OZ

Brake IGBT SPECIFICATIONS					
Continuous Collector Current (T_C = 25 °C) (Limited by Terminals) (T_C = 90 °C)	I_C	-	-	80 80	A
Pulsed Collector Current, 0.5mS	I_{CM}	-	-	200	A
IGBT Internal Gate Resistance		-	10	-	Ohm
IGBT Internal Gate Shunt Resistance		-	10	-	K Ohm
Junction To Case Thermal Resistance	$R_{\theta JC}$	-	-	0.28	°C/W

ULTRAFAST DIODES RATING AND CHARACTERISTICS					
Diode Peak Inverse Voltage	PIV	600	-	-	V
Continuous Forward Current, T_C = 90 °C	I_F	-	-	140	A
Diode Forward Voltage, I_F = 90A	V_F	-	1.4	1.6	V
Diode Reverse Recovery Time (I_F=80A, V_{RR}=300V , di/dt = 1500 A/μs)	t_{rr}	-	200	300	nsec
Diode switching loss V_{CE} = 300 V, I_F = 50A Tj=25°C		-	0.3	-	mJ
Junction To Case Thermal Resistance	$R_{\theta JC}$	-	-	0.35	°C/W

MODULE STORAGE AND OPERATING CONDITIONS					
Operating Junction Temperature	T_j	-40	-	150	°C
Storage Ambient Temperature	$T_{Storage}$	-55	-	150	°C
Operating Case Temperature	T_c	-40	-	85	°C
Operating Ambient Temperature	T_A	-40	-	105	°C
Operating Altitude		-	50000	-	Ft
Vibration and shock requirements (1)					

Gate Driver					
Supply Voltage, limits apply to Vcc	Vcc	14	15	16	V
Magnetic -Isolator Logic Low Input Threshold	V_{iL}	-	0.3VDD	-	V
Magnetic -Isolator Logic High Input Threshold	V_{iH}	-	0.7VDD	-	V
Under Voltage Lockout, positive going threshold Vcc,	VCCUV	11.8	12.2	12.7	V
Under Voltage Lockout, negative going threshold Vcc	VCCUV	11.3	11.8	12.2	V
Internal Bootstrap Capacitor Value		-	12	-	uF
Desaturation Detection, High Input Threshold Voltage		-	8.0	-	V
Desaturation Detection, Low Input Threshold Voltage		-	7.0	-	V
Logic Input to Phase Output Turn On Delay Output Turn On Rise Time **Logic Input to Phase Output Turn Off Delay** Output Turn Off Fall Time at VCC=600V, IC=50A, T_C = 25	t_{ond} t_r t_{offd} t_f	- - - - 	650 100 800 150	800 200 1200 200	nsec
Dead Time Requirement, for Shoot Through Prevention		750	1000	-	nsec
Magnetic -Isolator Operating Input Common Mode Voltage		-	-	1000	V
Magnetic -Isolator Operating Input Common Mode Transient		-	-	15	KV/usec

Module Isolation					
Gnd2 Isolation To Phase Lines, and to Gnd1 (Device will be tested at 3000V for 10 seconds), leakage less than 10uA	-	2500	-	-	VDC
Pin-To-Case Isolation Voltage, DC Voltage (Device will be tested at 3000V for 10 seconds), leakage less than 10uA		2500	-	-	VDC

+5V output, power supply Referenced to Gnd1		4.75	5	5.25	V
Maximum load current		-	-	30	mA

+5V Input, Isolated power supply (2) Referenced to Gnd2	VDD	4.75	5	5.25	V

Base Plate Temperature (2)					
Base Plate Temperature Sensor Output Gain Referenced to Gnd2	Tco	-	6.25	-	mV/^{o}C
Temperature Sensor Output DC Offset, at T_C=25^{o}C Referenced to Gnd2		-	424	-	mV
Accuracy, at temperature range from - 40 ^{o}C to 125 ^{o}C		-	+/-4.0	-	^{o}C

DC Bus Current Sensor (Bi-directional Output)					
Shunt Resistor Value	-	-	0.50	-	mOhm
Current Amplifier Gain, measured at Pin 22 and Referenced to Gnd1 (Non-isolated output)		0.0023	0.0026	0.0030	V/A
Current Amplifier DC Offset (Zero DC Bus Current), measured at Pin 22		-10	0	10	mV
Over-Current Set Point		75	85	120	A
Isolated PWM fixed frequency output at Pin 17		100	130	180	KHz
Isolated PWM output Duty cycle at Pin 17 , AT + 82 A , AT - 82 A		- -	91% 9%	- -	

Phase A, Phase B, and Phase C Current Sensors (Bi-directional Output) (2)					
Current Amplifier Gain Referenced to Gnd2		+/- 0.0160	+/-0.0175	+/- 0.0195	V/A
Output DC Reference at Pins 1, 3, 5		VDD/2 - 0.04	VDD/2	VDD/2 +0.04	V
Current Amplifier DC Offset (Zero Phase Current) Measured between Pins (1,2), (3,4), (5,6)		- 0.02	0	+0.02	V
Offset temperature Drift mV/ ^{o}C, Ta = -40 ^{o}C to 125 ^{o}C		-0.3	0	+0.3	mV/ ^{o}C
Maximum Current Measurement Range		-	+/-110	-	A

*(1) Unit is designed to meet **Vibration and Shock requirements, Mil-STD-810F shall be used. (514.5 and 516.5 methods respectively).***

(2) Phase current sensors and base plate temperature sensor are floating sensors referenced to Gnd2. An isolated 5V power supply shall be used to power these sensors.

Pinout

Pin #	Function	Pin #	Function
1	ICd DC offset of VDD/2 +/- 0.040V for Differential Output Reading of Output at Pin 2	18	VDD +5V Input
2	ICo, Phase C Current Sensor output	19	Return for all Input/outputs at Pins 1 to 18 (Signal Ground, **Gnd2**)
3	IBd DC offset of VDD/2 +/- 0.040V for Differential Output Reading of Output at Pin 4	20	Isolated SD Input
4	IBo, Phase B Current Sensor output		
5	IAd DC offset of VDD/2 +/- 0.040V for Differential Output Reading of Output at Pin 6	21	Itrip-Ref 1 Adjustable Reference for over-Current Shutdown
6	IAo, Phase A Current Sensor output	22	Itrip-Ref 2 Adjustable Reference for over-Current Shutdown
7	TCo Case Temperature Output with a gain of 6.25 mV/^{o}C	23	+5V Output
8	Isolated Input for Low-side IGBT of Phase A	24	+15V Rtn (Signal Ground, **Gnd1**)
9	Isolated Input for High-side IGBT of Phase A	25	+15V Input
10	Isolated Input for Low -side IGBT of Phase B	26,27	Brake Terminal. Brake Resistor Shall be Connected Between These Terminals and +VDC
11	Isolated Input for High-side IGBT of Phase B	28	Brake IGBT Gate Input Brake IGBT Emitter input is internally connected to DC Bus return
12	Isolated Input for Low-side IGBT of Phase C	29 to 32	DC Bus return
13	Isolated Input for High-side IGBT of Phase C	33 to 36	DC Bus “+VDC” input
14	Isolated Flt Clear Input	37 to 39	Phase C output
15	Isolated SD output	40 to 42	Phase B output
16	Isolated Flt output	43 to 45	Phase A output
17	Isolated Idco output		
		Case	Isolated

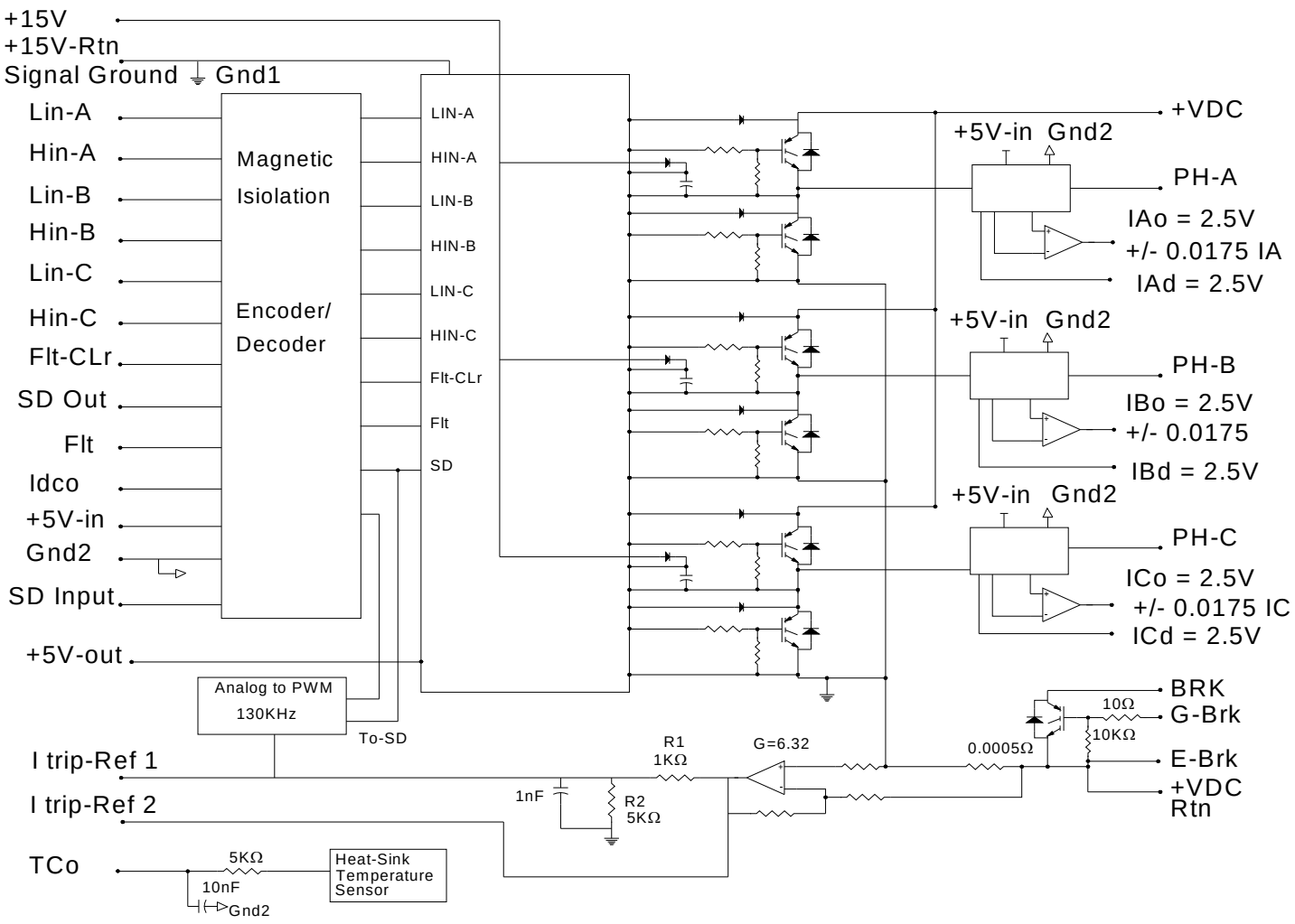
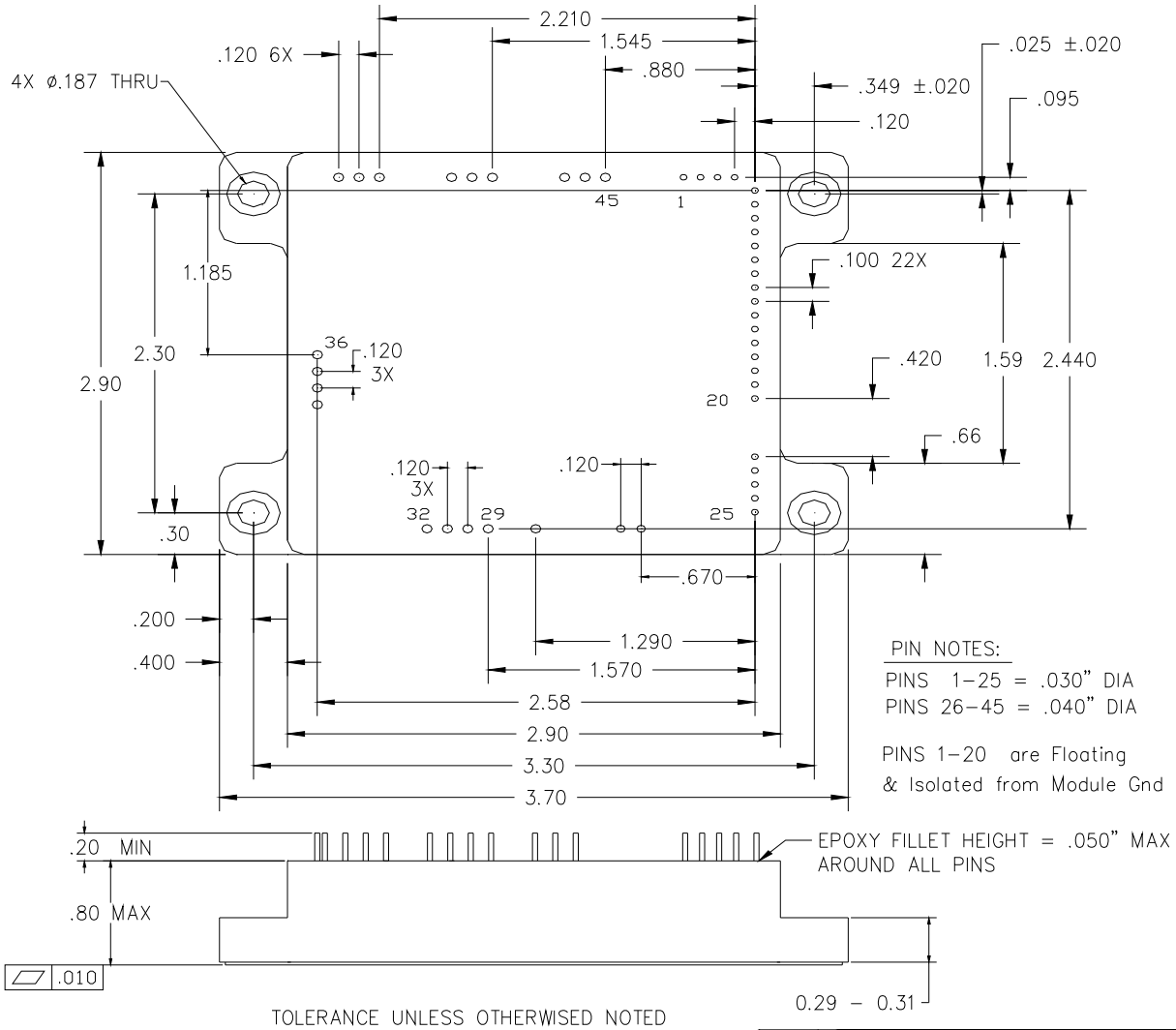


Fig. 1. Block Diagram

Figure 2. Mechanical Outline



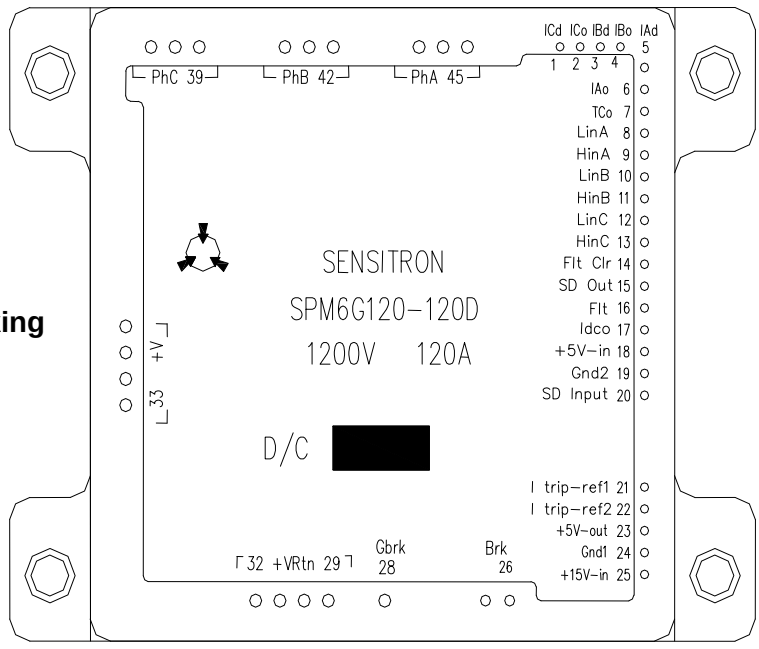


Figure 3. Device Pinout and Marking

Normalized Thermal Impedance Curves for Both IGBTs and Diodes

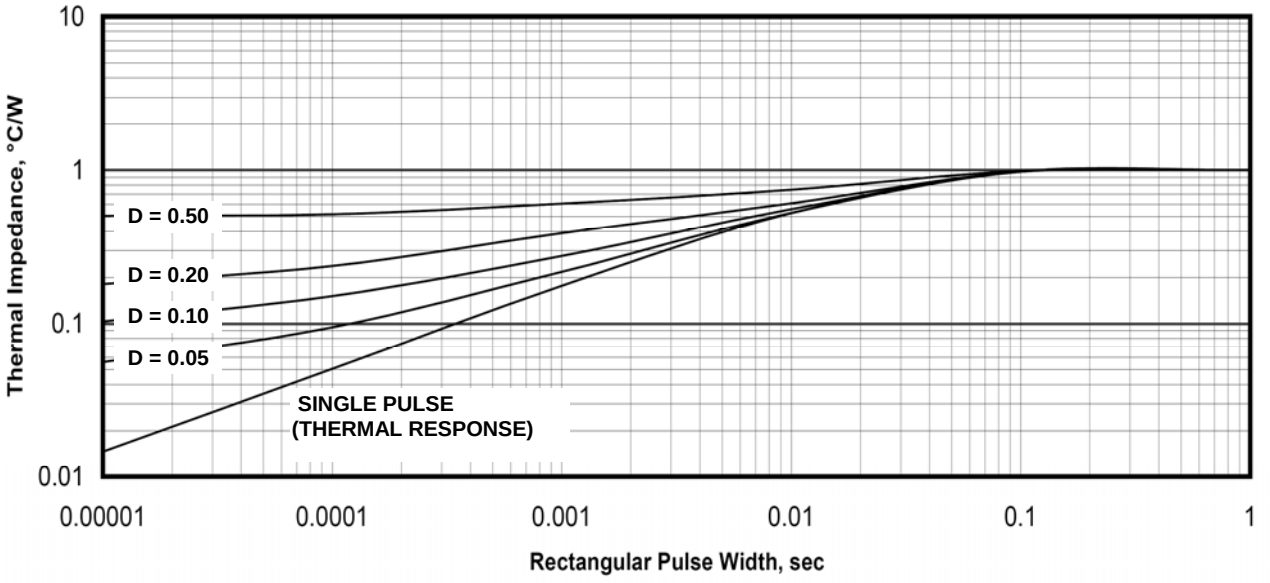


Figure 4. Normalized Transient Thermal Impedance, Junction-to-Case (IGBT)

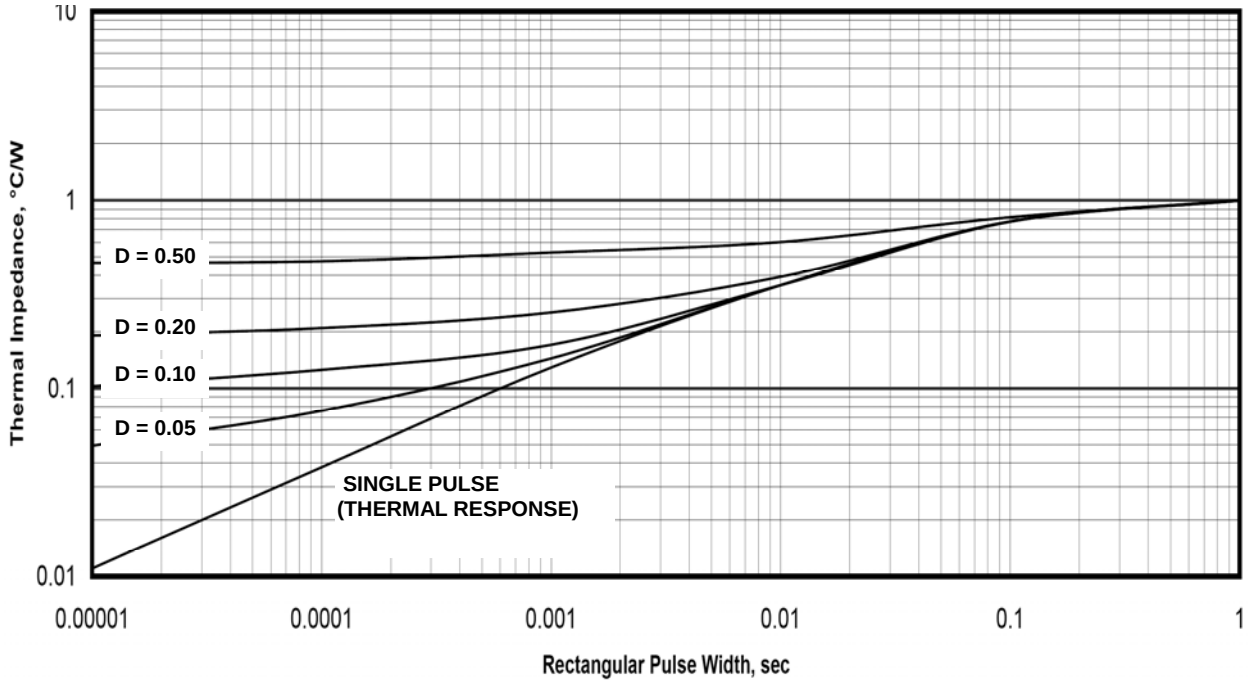


Figure 5. Normalized Transient Thermal Impedance, Junction-to-Case (Diode)

Pin Descriptions

ICd (Pin 1) : A +2.5V DC offset used for differential output reading of **ICo.**

ICo (Pin 2): Hall current sensor output for phase C. The output can be measured between Pin2 and Pin 1 differentially. Zero current corresponds to zero output, current entering Phase C pins will produce positive output voltage at Pin2, and current out of Phase C pins will produce negative output voltage at Pin2. Also, the output can be measured as single ended between Pin2 and Pin19. In this case zero current will correspond to 2.5V output, current entering Phase C pins will produce positive output voltage above 2.5V, and current out of Phase C pins will produce positive output voltage below 2.5V.The sensitivity of this sensor is 0.018V/A.

IBd (Pin 3): A +2.5V DC offset used for differential output reading of **IBo.**

IBo (Pin 4): Hall current sensor output for phase B. The output can be measured between Pin4 and Pin 3 differentially. Zero current corresponds to zero output, current entering Phase B pins will produce positive output voltage at Pin4, and current out of Phase B pins will produce negative output voltage at Pin4. Also, the output can be measured as single ended between Pin4 and Pin19. In this case zero current will correspond to 2.5V output, current entering Phase B pins will produce positive output voltage above 2.5V, and current out of Phase B pins will produce positive output voltage below 2.5V. The sensitivity of this sensor is 0.018V/A.

IAd (Pin 5): A +2.5V DC offset used for differential output reading of **IAo.**

IAo (Pin 6): Phase A hall current sensor output. The output can be measured between Pin6 and Pin 5 differentially. Zero current corresponds to zero output, current entering Phase A pins will produce positive output voltage at Pin6, and current out of Phase A pins will produce negative output voltage at Pin6. Also, the output can be measured as single ended between Pin6 and Pin19. In this case zero current will correspond to 2.5V output, current entering Phase A pins will produce positive output voltage above 2.5V, and current out of Phase A pins will produce positive output voltage below 2.5V. The sensitivity of this sensor is 0.018V/A.

TCo (Pin 7): An analog output of case temperature sensor. The sensor output gain is 6.25mV/^{o}C, with 424 mV DC offset. This sensor can measure both positive and negative ^{o}C. The internal impedance of this output is 4.99KΩ. The internal block diagram of the temperature sensor is shown in Fig. 6.

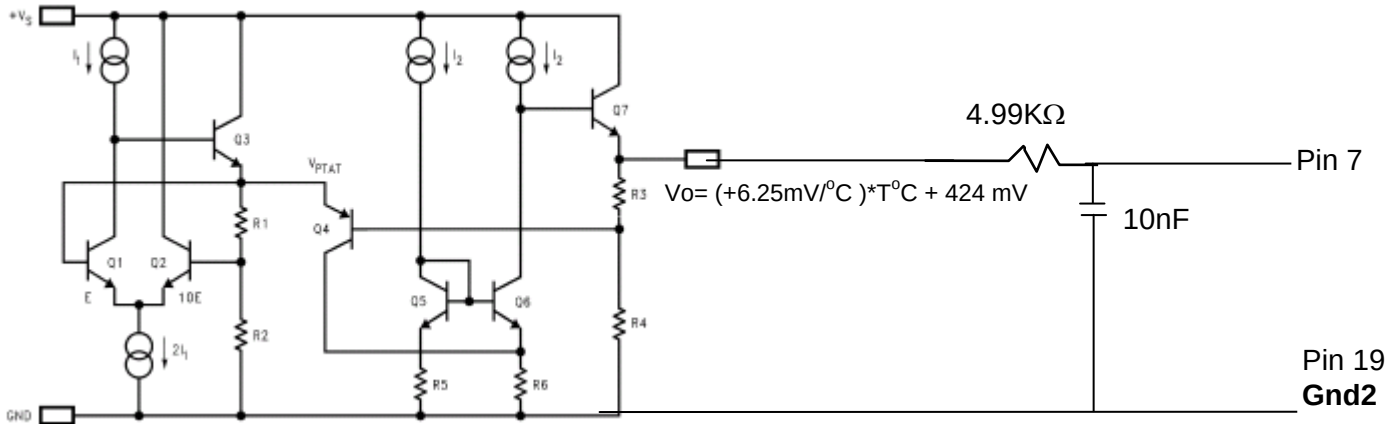


Fig. 6 Temperature Sensor Internal Block Diagram

The output voltage reading vs temperature will be:
TCo = + 0.58V at Tc= +25^{o}C
TCo = + 1.205V at Tc= +125^{o}C
TCo = + 0.174V at Tc= -40^{o}C

LinA (Pin 8) : An isolated drive input for Low-side IGBT of Phase A.

HinA (Pin 9): An isolated drive input for High-side IGBT of Phase A.

LinB- (Pin 10): An isolated drive input for Low-side IGBT of Phase B.

HinB (Pin 11): An isolated drive input for High-side IGBT of Phase B.

LinC (Pin 12): An isolated drive input for Low-side IGBT of Phase C.

HinC (Pin 13): An isolated drive input for High-side IGBT of Phase C.

Flt-Clr(Pin 14): A fault clear input. It can be used to reset a latching fault condition, due to desaturation protection. Pin 14 an active high input. It is internally pulled down by 20.0KΩ. A latching fault due to desaturation can be cleared by pulling this input high to +5V. **It is recommended to activate fault clear input for more than 500 μsec at startup.** ***To charge boot-strap circuit at startup, it is recommended to turn on all low-side switches for 500 μsec while Flt-Clr is active.***

SD Out (Pin 15): Is internally activated due to desaturation protection, over-current shutdown, or under voltage lockout. Desaturation shutdown is a latching feature. **SD Out** can be used as a fault condition output. A continuous low output at SD out indicates a latching fault situation.

Flt (Pin 16): Is internally pulled down by 20.0KΩ. Pin 16, reports desaturation protection activation. When desaturation protection is activated a low output for about 9 μsec is reported. If any other protection feature is activated, it will not be reported by Pin 16.

Idco (Pin 17): Is DC bus bi-directional current sense output. The sensor output is isolated. It is a PWM signal with fixed frequency and variable duty cycle. **The PWM frequency is 130 KHz.** The maximum duty cycle is 91%, corresponding to 82 A. Minimum duty cycle is 9%, corresponding to –82A.

VDD, +5V-in (Pin 18): The +5V input biasing supply connection for the phase current sensors, magnetic isolators, and temperature sensor. Pin 18 should be connected to an isolated 5V power supply, recommended limits are 4.75V to 5.25V. The return of this input is pin 19. **Recommended power supply capability for VDD is about 50mA.**

Gnd2 (Pin 19): The signal ground for **+5V-in**,. This pin is internally floating for flexibility. The phase current sensors and temperature sensor are referenced to Gnd2. **Gnd2 isolation from Gnd1 is over 2500V.**

SD Input (Pin 20): The SD input. A high input will disable all gate drive signals. This input is internally pulled high to +5V by 20 K ohms.

Itrip-Ref1 (Pin 21): An adjustable voltage divider reference for over-current shutdown.

Itrip-Ref2 (Pin 22): An adjustable voltage divider reference for over-current shutdown. The internal set point over-current shutdown is 82A. The re-start delay time is about 0.50 msec. **+5V Output (Pin 23),** is a +5V output. Maximum output current is 30mA.

Gnd1 (Pin 24) : The signal ground for **+15V-in**,. This pin is internally connected to DC Bus return. **No external connection shall be established between Signal Gnd1 and +VDC Rtn. Gnd1 is isolated from Gnd2. Note that Pins 21 to 23 are referenced to Gnd1.**

+15V-in (Vcc) (Pin 25): The +15V input biasing supply connection for the controller. Under-voltage lockout keeps all outputs off for Vcc below 11.5V. Vcc pin should be connected to an isolated 15V power supply. Vcc recommended limits are 14V to 16V , and shall not exceed 18V. The return of Vcc is pin 24. **Recommended power supply capability is about 70mA.**

Brk (Pins 26,27), is Brake Terminal. Brake Resistor shall be connected between these terminals and +VDC. If the brake resistor is inductive, a freewheeling diode shall be connected across this resistor.

Gbrk (Pin 28), is Brake IGBT Gate Input. Brake IGBT Emitter is internally connected to DC Bus return.

+VDC Rtn (Pins 29 to 32), is DC Bus return.

+VDC (Pins 33 to 36), is +DC Bus input.

PhC (Pins 37 to 39), is Phase C output.

PhB (Pins 40 to 42), is Phase B output.

PhA (Pins 43 to 45), is Phase A output.

A- DC Bus Charging from 15V

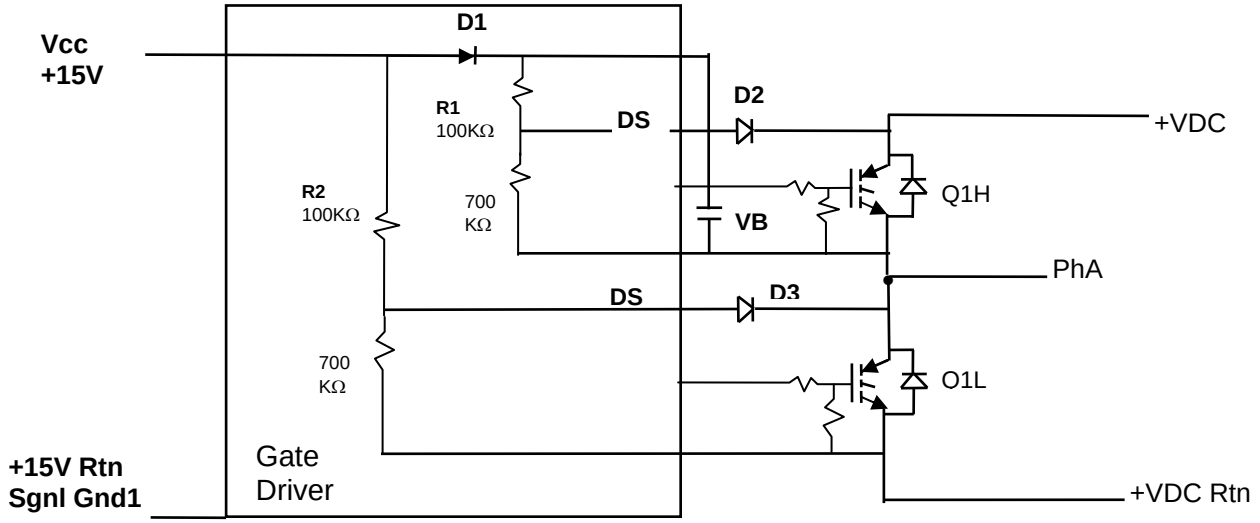


Figure 7. Charging Path from 15V Supply to DC Bus when DC Bus is off

- Each IGBT is protected against desaturation.
- D2 is the desaturation sense diode for the high-side IGBT
- D3 is the desaturation sense diode for the low-side IGBT
- When the DC bus voltage is not applied or below 15V, there is a charging path from the 15V supply to the DC bus through D2 and D3 and the corresponding pull up 100K Ohm resistor. The charging current is 0.15mA per IGBT. Total charging current is about 1.5mA.
- **Do not apply PWM signal if the DC bus voltage is below 20V.**

B- Bias For Desaturation Detection Circuit:

The desaturation detection is done by diode D2 for the high side IGBT Q1H, and by diode D3 for the low side IGBT Q1L. The internal detection circuit, input DSH for the high-side and input DSL for the low-side, is biased by the local supply voltage VCC for the low side and VBS for the high side. When the IGBT is on the corresponding detection diode is on. The current flowing through the diode is determined by the internal pull resistor, R1 for the high side and R2 for the low side. To minimize the current drain from VCC and VBS, R1 and R2 are set to be 100KΩ. Lower value of R1 will overload the bootstrap circuit and reduce the bootstrap capacitor holding time.

TECHNICAL DATA
DATASHEET 4977, Rev. B

Cleaning Process:
Suggested precaution following cleaning procedure:
If the parts are to be cleaned in an aqueous based cleaning solution, it is recommended that the parts be baked immediately after cleaning. This is to remove any moisture that may have permeated into the device during the cleaning process. For aqueous based solutions, the recommended process is to bake for at least 2 hours at 125^{o}C. Do not use solvents based cleaners.

Recommended Soldering Procedure:
Signal pins 1-25: 210C for 10 seconds max
Power pins 26-45: 260C for 10 seconds max. Pre-warm module to 125C to aid in power pins soldering.

Ordering Information:
SPM6G140-060D is a standard product with all the features listed in the data sheet.

A, is a standard product with all the features listed in the data sheet except Pins 26, 27,28 are removed. The associated circuits with these Pins are removed.

B, is a standard product with all the features listed in the data sheet except Pins 17,21,22,26, 27,28 are removed or not connected. The associated circuits with these Pins are removed.