

PSRAM

8-Mbit (512K x 16)

Pseudo Static RAM

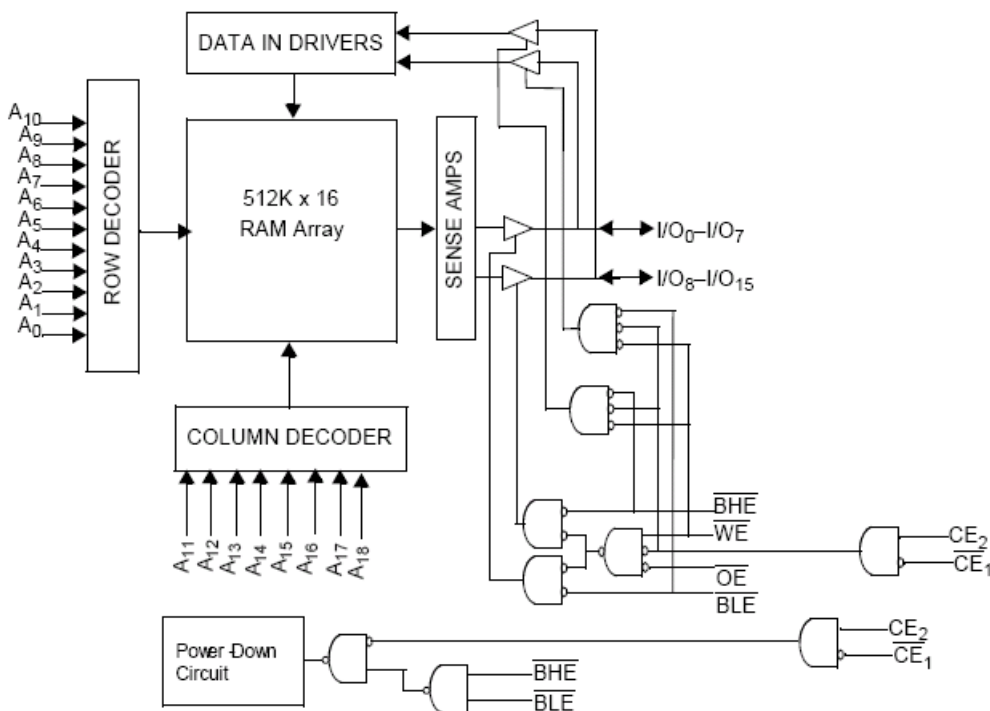
Features

- Advanced low-power architecture
- High speed: 55 ns, 70 ns
- Wide voltage range: 2.7V to 3.6 V
- Typical active current: 2 mA @ f = 1 MHz
- Typical active current: 11 mA @ f = f<sub>MAX</sub>
- Low standby power
- Automatic power-down when deselected

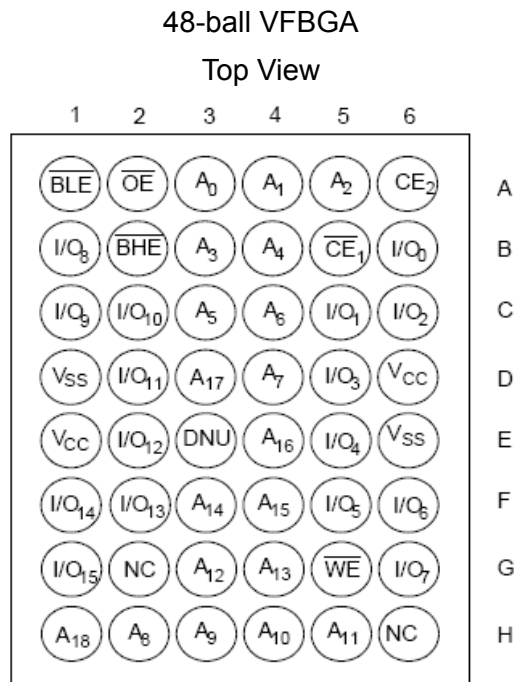
Functional Description

The M24L816512DA is a high-performance CMOS pseudo static RAM (PSRAM) organized as 512K words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for portable applications such as cellular telephones. The device can be put into standby mode reducing power consumption dramatically when deselected ( $\overline{CE1}$  LOW,  $CE2$  HIGH or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE1}$  HIGH,  $CE2$  LOW),  $\overline{OE}$  is deasserted HIGH, or during a write operation (Chip Enabled and Write Enable  $\overline{WE}$  LOW). Reading from the device is accomplished by asserting the Chip Enables ( $\overline{CE1}$  LOW and  $CE2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the Truth Table for a complete description of read and write modes.

Logic Block Diagram



## Pin Configuration[2, 3, 4]



## Product Portfolio Product

Product	V <sub>CC</sub> Range (V)			Speed(ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby, I <sub>SB2</sub> (μA)	
	f = 1MHz		f = f <sub>MAX</sub>		Typ. [5]	Max.				
	Min.	Typ.	Max.				Typ.[5]	Max.	Typ. [5]	Max.
M24L816512DA	2.7	3.0	3.6	55	2	5	11	22	55	100
				70				17		110(for V <sub>CC</sub> >3.3V )

### Notes:

- 2.DNU pins are to be left floating or tied to VSS.
- 3.Ball G2, H6 are the address expansion pins for the 16-Mbit and 32-Mbit densities respectively.
- 4.NC "no connect"—not connected internally to the die.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC (typ)</sub> and T<sub>A</sub> = 25°C.

## Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)  
 Storage Temperature .....-65°C to +150°C  
 Ambient Temperature with Power Applied .....-40°C to +85°C  
 Supply Voltage to Ground Potential .....-0.4V to 4.6V  
 DC Voltage Applied to Outputs in High-Z State[6, 7, 8] .....-0.4V to 3.7V  
 DC Input Voltage[6, 7, 8] .....-0.4V to 3.7V  
 Output Current into Outputs (LOW) .....20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)  
 Latch-up Current .....> 200 mA

## Operating Range

Range	Ambient Temperature (T <sub>A</sub> )	V <sub>CC</sub>
Extended	-25°C to +85°C	2.7V to 3.6V
Industrial	-40°C to +85°C	2.7V to 3.6V

## DC Electrical Characteristics (Over the Operating Range) [5, 6, 7, 8]

Parameter	Description	Test Conditions	-55			-70			Unit
			Min.	Typ. [5]	Max.	Min.	Typ. [5]	Max.	
V <sub>CC</sub>	Supply Voltage		2.7	3.0	3.6	2.7		3.6	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> -0.4			V <sub>CC</sub> -0.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		0.8* V <sub>CC</sub>		V <sub>CC</sub> +0.4V	0.8* V <sub>CC</sub>		V <sub>CC</sub> +0.4V	V
V <sub>IL</sub>	Input LOW Voltage	f = 0	-0.4		0.4	-0.4		0.4	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>IN</sub> < V <sub>CC</sub>	-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		11	22		11	17	mA
		f = 1 MHz		2	5		2	5	
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>MAX</sub> (Address and Data Only), f = 0 ( $\overline{OE}$ , $\overline{WE}$ , $\overline{BHE}$ and $\overline{BLE}$ )		100	400		100	400	μA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0	V <sub>CC</sub> = 3.3V	55	100	55	100	110	μA
			V <sub>CC</sub> = 3.6V		110				

## Capacitance[9]

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = V <sub>CC(typ)</sub>	8	pF

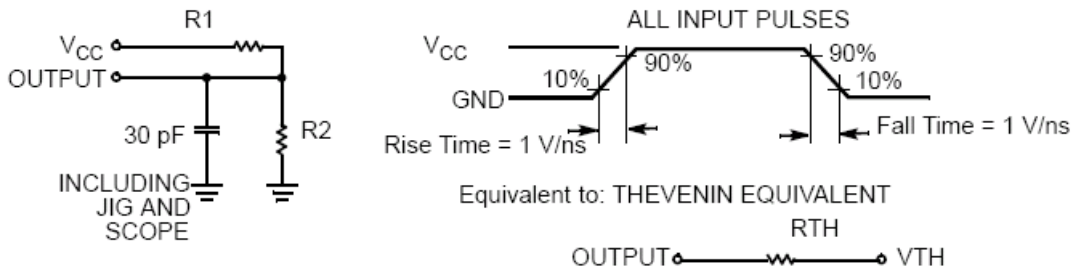
## Thermal Resistance[9]

Parameter	Description	Test Conditions	BGA	Unit
ΘJA	Thermal Resistance(Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/ JESD51.	55	°C/W
ΘJC	Thermal Resistance (Junction to Case)		17	°C/W

### Notes:

- V<sub>IH(MAX)</sub> = V<sub>CC</sub> + 0.5V for pulse durations less than 20 ns.
- V<sub>IL(MIN)</sub> = -0.5V for pulse durations less than 20 ns.
- Overshoot and undershoot specifications are characterized and are not 100% tested.
- Tested initially and after design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Parameters	3.0V V <sub>CC</sub>	Unit
R1	22000	Ω
R2	22000	Ω
R <sub>TH</sub>	11000	Ω
V <sub>TH</sub>	1.50	V

## Switching Characteristics Over the Operating Range[10, 11, 12, 13, 14]

Parameter	Description	-55		-70		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t <sub>RC</sub>	Read Cycle Time	55[14]		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		5		ns
t <sub>ACE</sub>	$\overline{CE1}$ LOW and CE2 HIGH to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to LOW Z[11, 12]	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z[11, 12]		25		25	ns
t <sub>LZCE</sub>	$\overline{CE1}$ LOW and CE2 HIGH to Low Z[11, 12]	5		5		ns
t <sub>HZCE</sub>	$\overline{CE1}$ HIGH and CE2 LOW to High Z[11, 12]		25		25	ns
t <sub>DBE</sub>	$\overline{BLE/BHE}$ LOW to Data Valid		55		70	ns
t <sub>LZBE</sub>	$\overline{BLE/BHE}$ LOW to Low Z[11, 12]	5		5		ns
t <sub>HZBE</sub>	$\overline{BLE/BHE}$ HIGH to High Z[11, 12]		10		25	ns
t <sub>SK</sub> [14]	Address Skew		0		10	ns

### Notes:

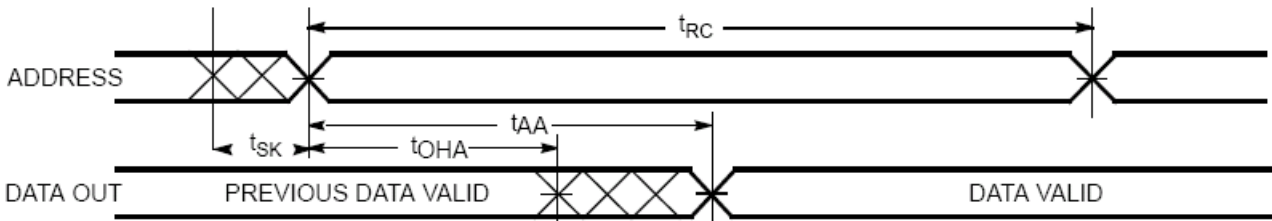
- Test conditions assume signal transition time of 1V/ns or higher, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0V to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high-impedance state.
- High-Z and Low-Z parameters are characterized and are not 100% tested.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE1} = V_{IL}$ ,  $CE2 = V_{IH}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates write.
- To achieve 55-ns performance, the read access should be  $\overline{CE}$  controlled. In this case t<sub>ACE</sub> is the critical parameter and t<sub>SK</sub> is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

Switching Characteristics (Over the Operating Range) (continued)[10, 11, 12, 13, 14]

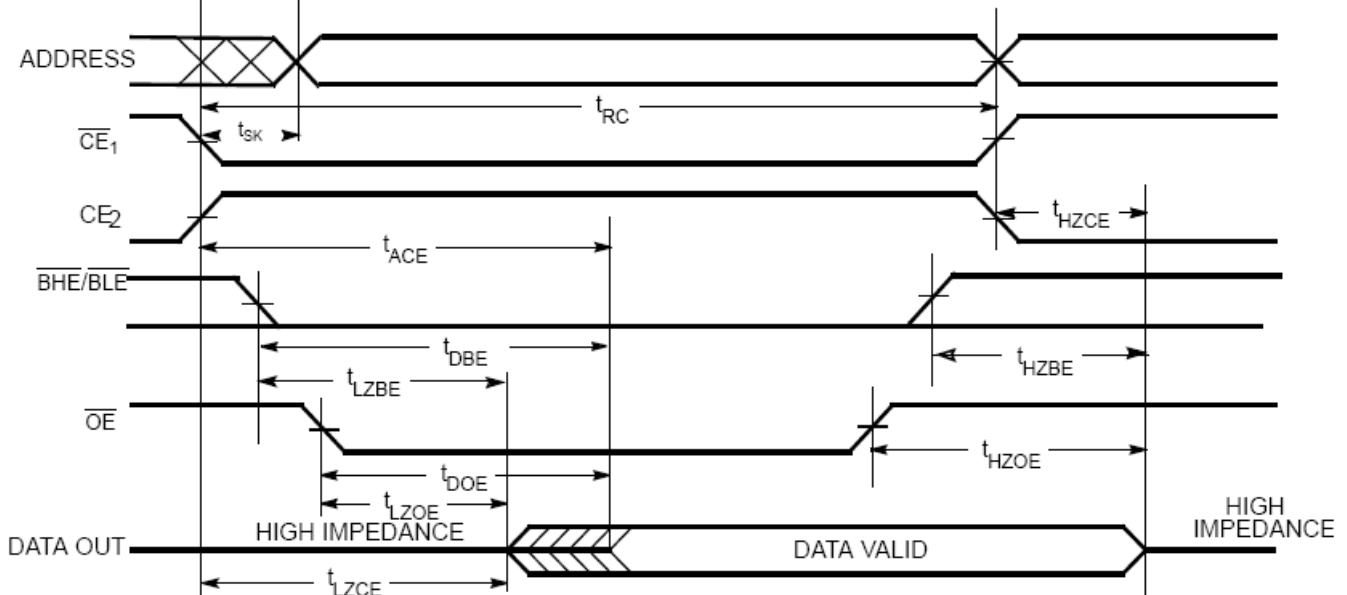
Parameter	Description	-55		-70		Unit
		Min.	Max.	Min.	Max.	
Write Cycle[13]						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	$\overline{CE1}$ LOW and $CE2$ HIGH to Write End	45		55		ns
$t_{AW}$	Address Set-up to Write End	45		55		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	40		55		ns
$t_{BW}$	$\overline{BLE}/\overline{BHE}$ LOW to Write End	50		55		ns
$t_{SD}$	Data Set-up to Write End	42		42		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z[11, 12]		25		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z[11, 12]	5		5		ns

### Switching Waveforms

#### Read Cycle 1 (Address Transition Controlled)[14, 15, 16]



#### Read Cycle 2 ( $\overline{OE}$ Controlled)[14, 15]

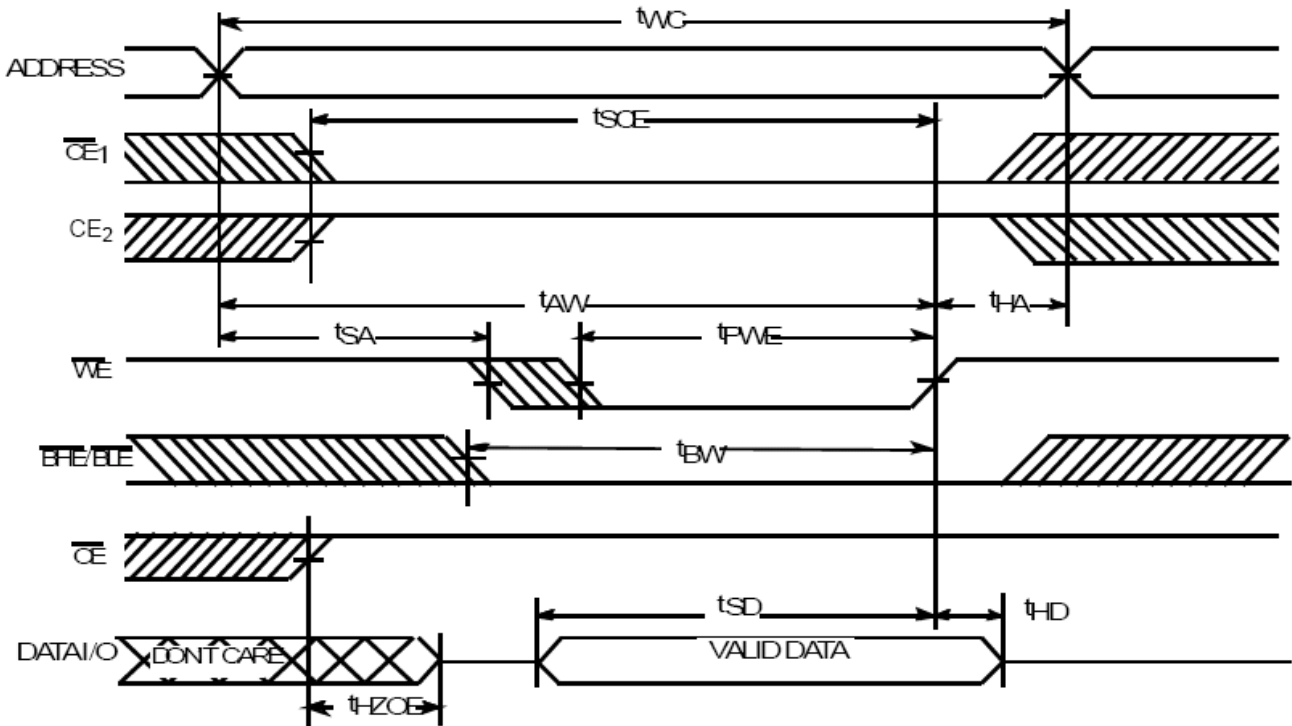


Notes:

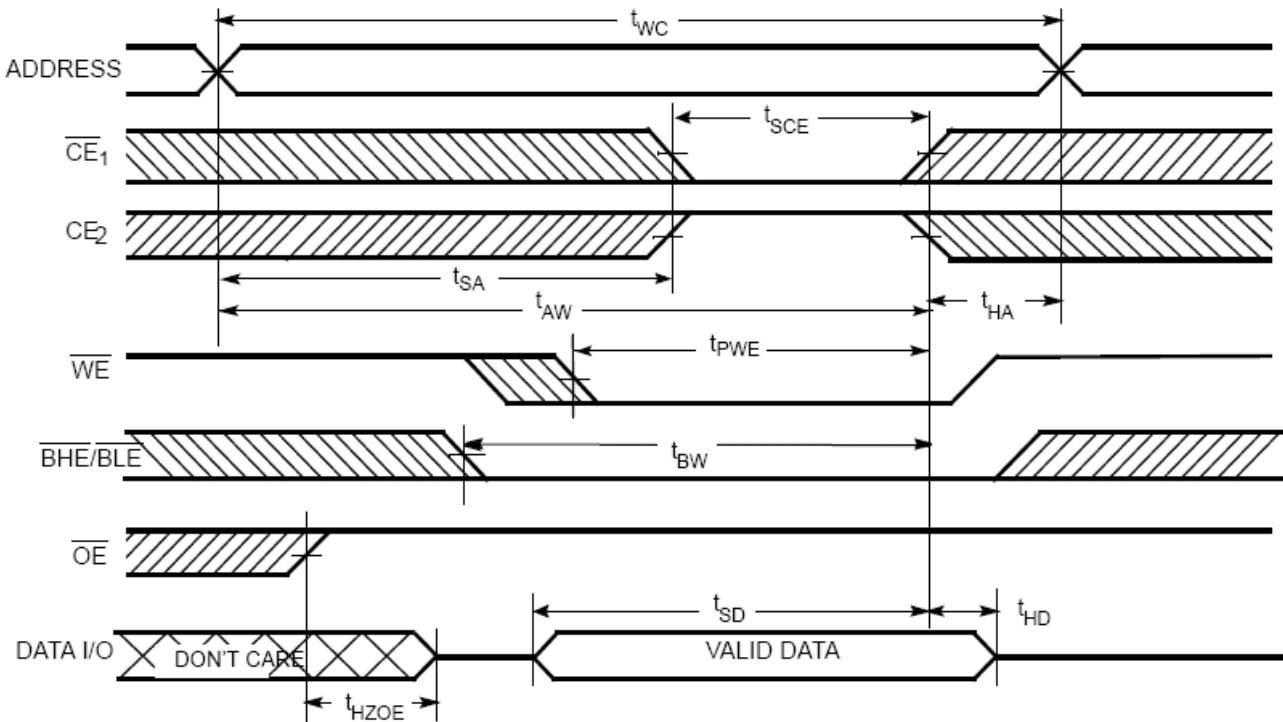
- 15.  $\overline{WE}$  is HIGH for Read Cycle.
- 16. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$

## Switching Waveforms (continued)

### Write Cycle 1 (WE Controlled) [12, 13, 17, 18, 19]



### Write Cycle 2 (CE1 or CE2 Controlled) [12, 13, 17, 18, 19]



#### Notes:

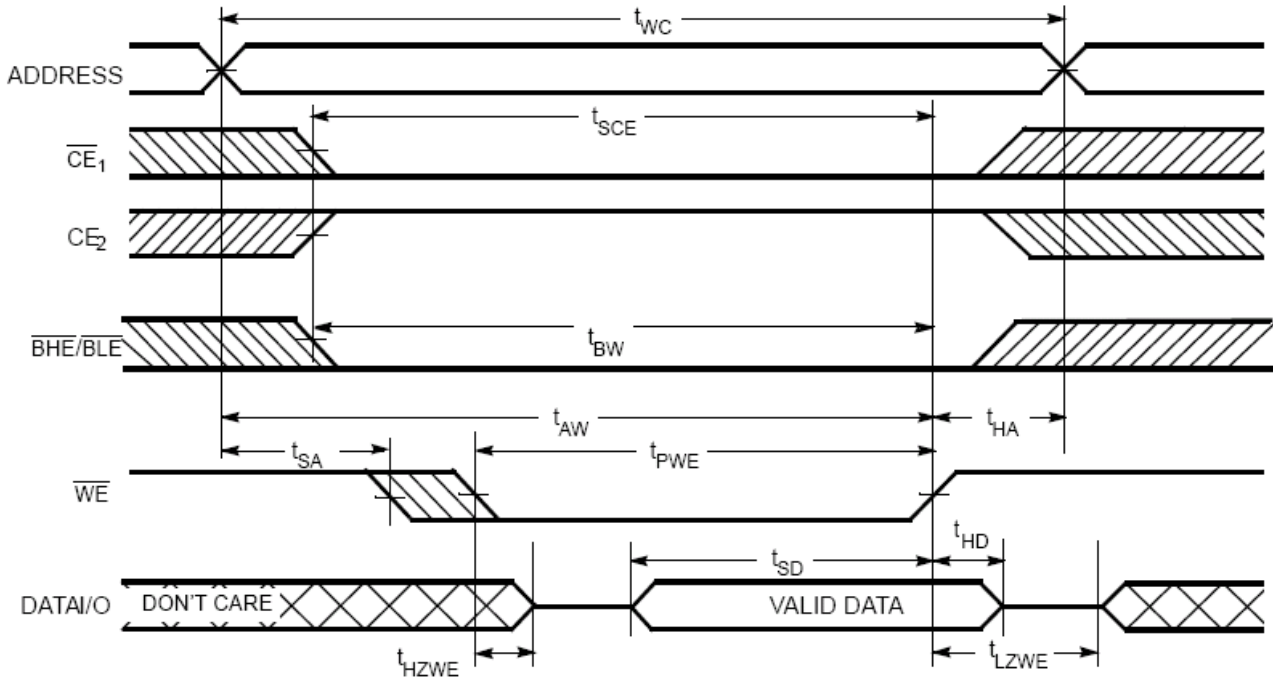
17. Data I/O is high impedance if  $\overline{OE} \geq V_{IH}$ .

18. If Chip Enable goes INACTIVE simultaneously with  $\overline{WE} = \text{HIGH}$ , the output remains in a high-impedance state.

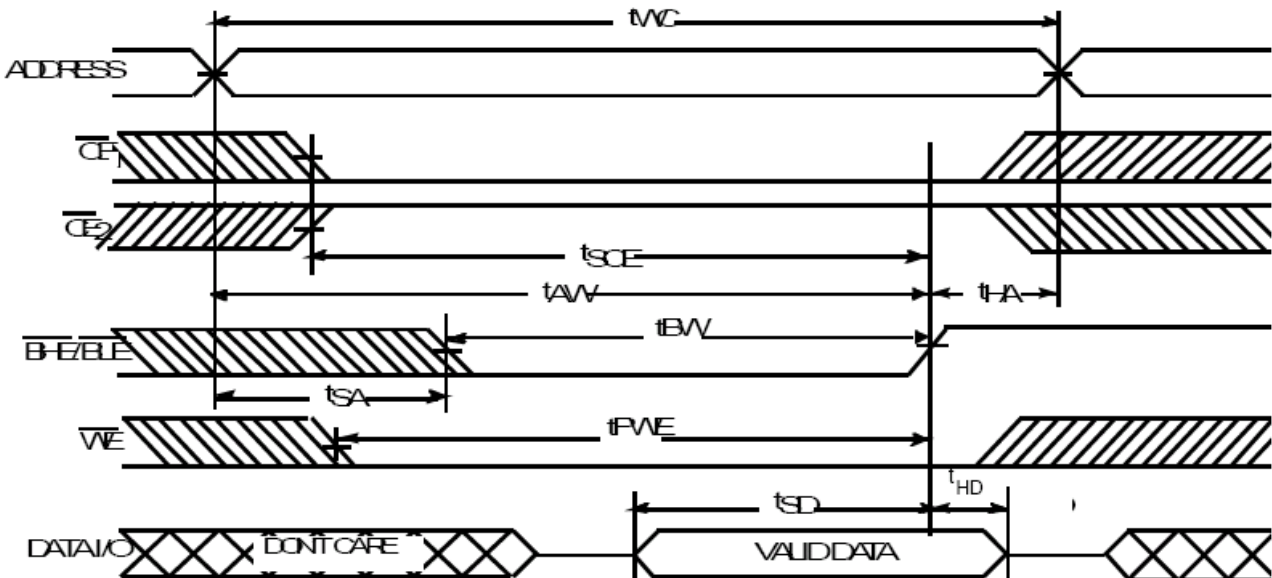
19. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)[18, 19]



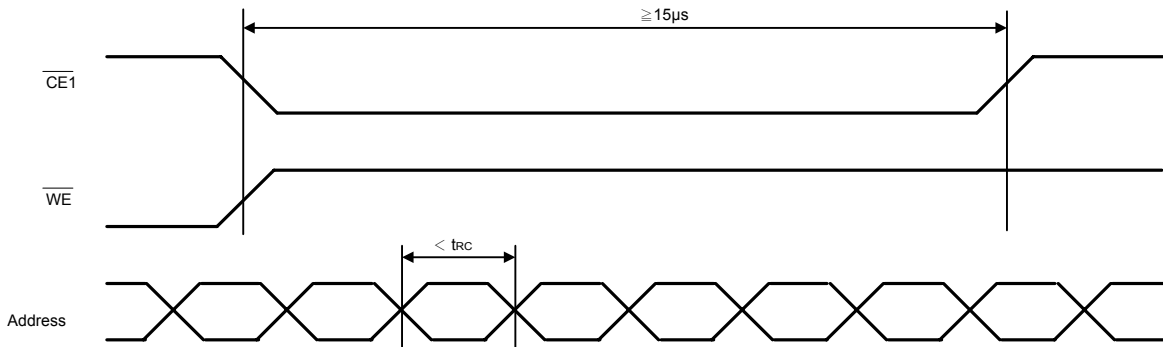
Write Cycle 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW)[18, 19]



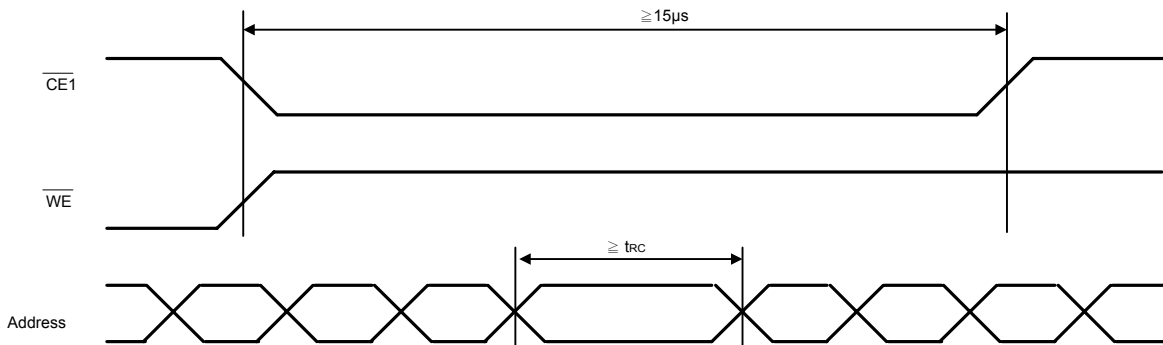
**Avoid Timing**

ESMT Pseudo SRAM has a timing which is not supported at read operation, If your system has multiple invalid address signal shorter than  $t_{RC}$  during over  $15\mu s$  at read operation shown as in Abnormal Timing, it requires a normal read timing at least during  $15\mu s$  shown as in Avoidable timing 1 or toggle  $\overline{CE1}$  to high ( $\geq t_{RC}$ ) one time at least shown as in Avoidable Timing 2.

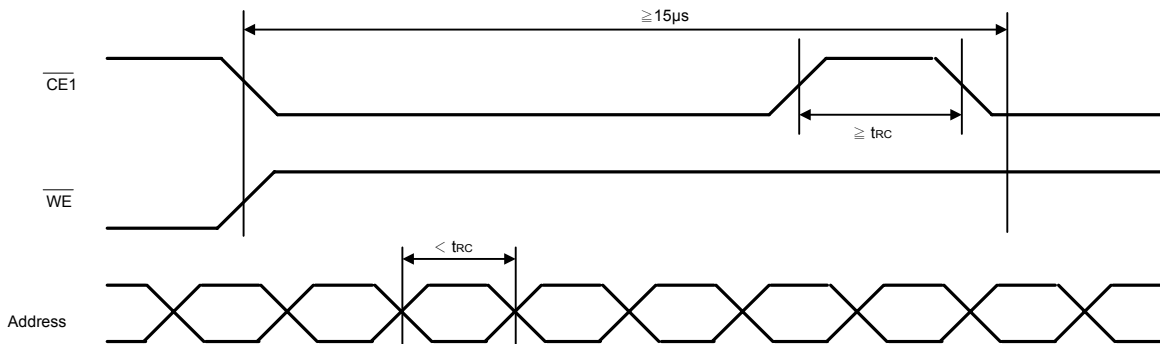
**Abnormal Timing**



**Avoidable Timing 1**



**Avoidable Timing 2**





**Truth Table[20]**

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $I/O_0-I/O_{15}$ )	Read (Upper Byte and Lower Byte)	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out ( $I/O_0-I/O_7$ ); ( $I/O_8-I/O_{15}$ ) in High Z	Read (Lower Byte only)	Active ( $I_{CC}$ )
L	H	H	L	L	H	Data Out ( $I/O_8-I/O_{15}$ ); ( $I/O_0-I/O_7$ ) in High Z	Read (Upper Byte only)	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $I/O_0-I/O_{15}$ )	Write (Upper Byte and Lower Byte)	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In ( $I/O_0-I/O_7$ ); ( $I/O_8-I/O_{15}$ ) in High Z	Write (Lower Byte Only)	Active ( $I_{CC}$ )
L	H	L	X	L	H	Data Out ( $I/O_8-I/O_{15}$ ); ( $I/O_0-I/O_7$ ) in High Z	Write (Upper Byte Only)	Active ( $I_{CC}$ )

## Ordering Information

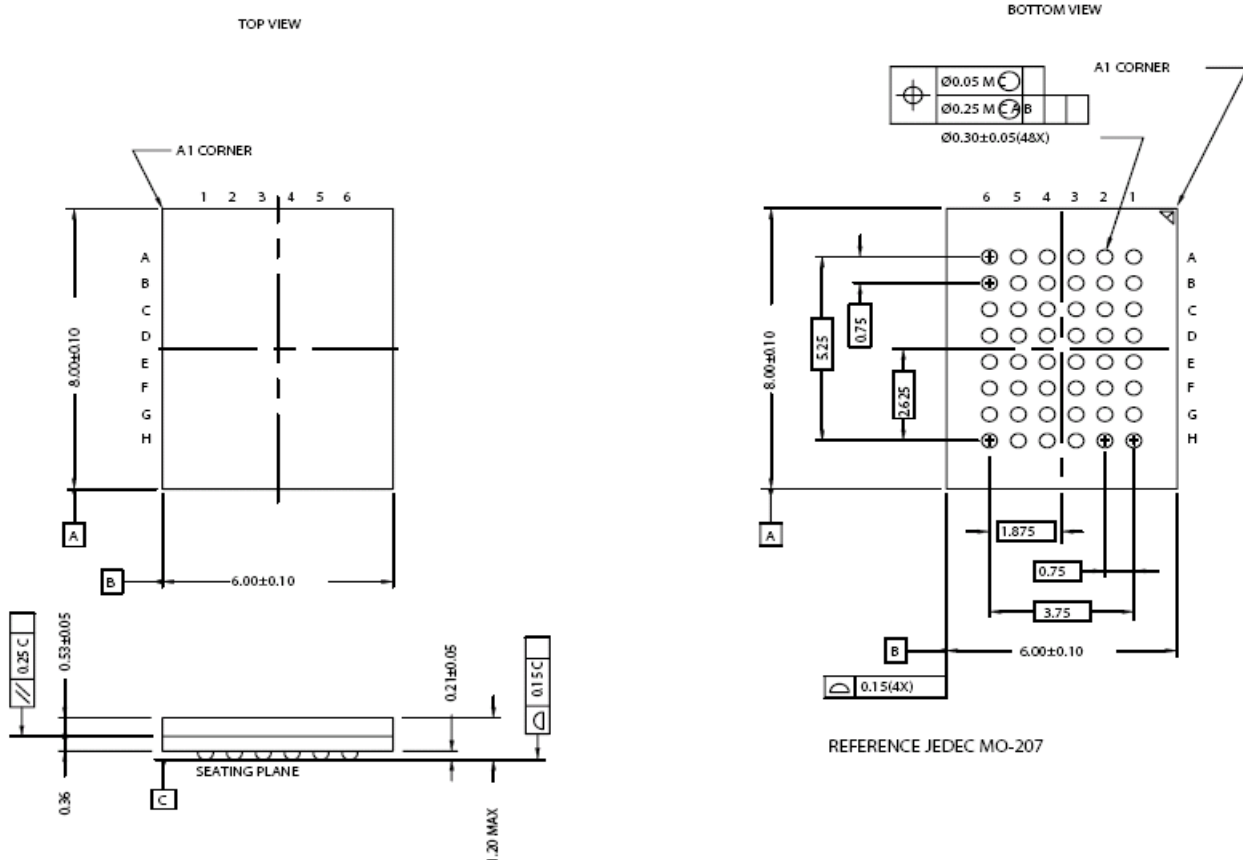
Speed (ns)	Ordering Code	Package Type	Operating Range
55	M24L816512DA-55BEG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.2 mm) (Pb-Free)	Extended
70	M24L816512DA-70BEG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.2 mm) (Pb-Free)	Extended
55	M24L816512DA-55BIG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.2 mm) (Pb-Free)	Industrial
70	M24L816512DA-70BIG	48-ball Very Fine Pitch BGA (6.0 x 8.0 x 1.2 mm) (Pb-Free)	Industrial

Note:

20.H = Logic HIGH, L = Logic LOW, X = Don't Care.

## Package Diagrams

### 48-Ball (6 mm x 8mm x 1.2 mm) FBGA



**Revision History**

<b>Revision</b>	<b>Date</b>	<b>Description</b>
1.0	2007.07.04	Original
1.1	2008.07.04	1. Move Revision History to the last 2. Modify voltage range 2.7V~3.3V to 2.7V~3.6V 3. Add Industrial grade 4. Add Avoid timing

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