iC-MQ PROGRAMMABLE 9-BIT
Sin/Cos INTERPOLATION IC WITH RS422 DRIVER

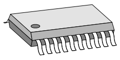
FEATURES

- Latency-free sine-to-digital conversion to 400 angle steps
- 500 kHz input frequency for interpolation factors of x1 and x2 (10 kHz for x100)
- Flexible pin assignment due to signal path multiplexers
- PGA inputs for differential and single-ended signals
- Variable input resistance for current/voltage conversion
- Signal conditioning for offset, amplitude and phase
- Controlled 50 mA current source for LED or MR sensor supply
- Fault-tolerant RS422 outputs with 50 mA sink/source drive current
- Preselectable minimum phase distance for spike-proof counter stimulus
- Zero signal conditioning and electronic index pulse generation
- Signal and operation monitoring with configurable alarm output, output shutdown and error storage
- I^{2}C multimaster interface for in-circuit calibration and parameters (EEPROM)
- Adjustable overtemperature alarm and shutdown
- Supply from 4.3 to 5.5 V, operation from -25(-40) to +100 °C
- Reverse polarity proof including the sub-system

APPLICATIONS

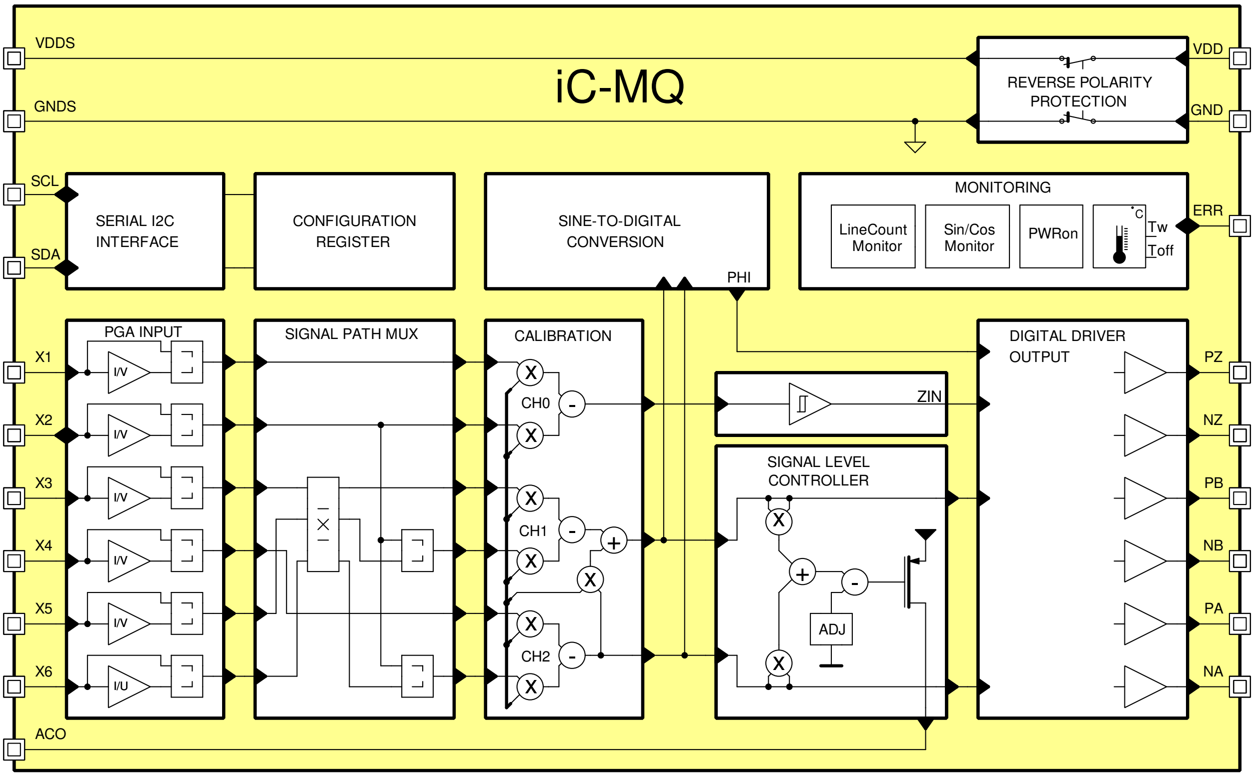
- Optical and magnetic position sensors
- Angle encoders
- Linear scales

PACKAGES



TSSOP20

BLOCK DIAGRAM



DESCRIPTION

Interpolator iC-MQ is a non-linear A/D converter which digitizes sine/cosine sensor signals using a count-safe tracking conversion principle with selectable resolution and hysteresis. The angle resolution per sine period can be set using SELRES; up to 400 angle steps are possible (see page 26).

The angle position is output incrementally by differential RS422 drivers as an encoder quadrature signal with a zero pulse or, if selected, as a counter signal for devices compatible with 74HC191 or 74HC193.

The zero pulse is generated electronically when an enable has been set by the X1/X2 inputs. This pulse can be configured extensively: both in its relative position to the input signal with regard to the logic gating with A and/or B and in its width from 90° to 360° (1/4 to 1 T).

A preselectable minimum transition distance permits glitch-free output signals and prevents counting errors which in turn boosts the noise immunity of the position encoder.

Programmable instrumentation amplifiers with selectable gain levels allow differential or single-ended, referenced input signals; via input X2 the external reference can be used as reference voltage for the offset correction.

The modes of operation differentiate between high impedance (V modes) and low impedance (I modes). This adaptation of the iC to voltage or current signals enables MR sensor bridges or photosensors to be directly connected up to the device. The optical scanning of low resolution code discs is also supported by the reference function of input X2; these discs do not evaluate tracks differentially but in comparison with a reference photodiode.

The integrated signal conditioning unit allows signal amplitudes and offset voltages to be calibrated accurately and also any phase error between the sine and cosine signals to be corrected. The channel for the zero signal can be configured separately.

A control signal is generated from the conditioned signals which can track the transmitting LED of optical encoders via the integrated 50 mA driver stage (output ACO). If MR sensors are connected this driver stage can also track the power supply of the measuring bridges. By tracking the sensor energy supply any temperature and aging effects are compensated for, the input signals stabilized and the exact calibration of the input signals is maintained. This enables a constant accuracy of the interpolation circuit across the entire operating temperature range.

When control limits are reached, these can be indicated at the maskable error pin ERR. Faults such as overdrive, wire breakage, short circuiting, dirt or aging, for example, are logged.

iC-MQ includes extensive self-test and system diagnosis functions which check whether the sensor is working properly or not. For all error events the user can select whether the fault be displayed at error pin ERR or the outputs shutdown. At the same time errors can be stored in the EEPROM to enable failures to be diagnosed at a later stage. For encoder applications the line count of the code disc, the sensor signal regarding signal level and frequency and the operating temperature can be monitored, for example, the latter using an adjustable on-chip sensor.

Display error pin ERR is bidirectional; a system fault recognized externally can be recorded and also registered in the error memory.

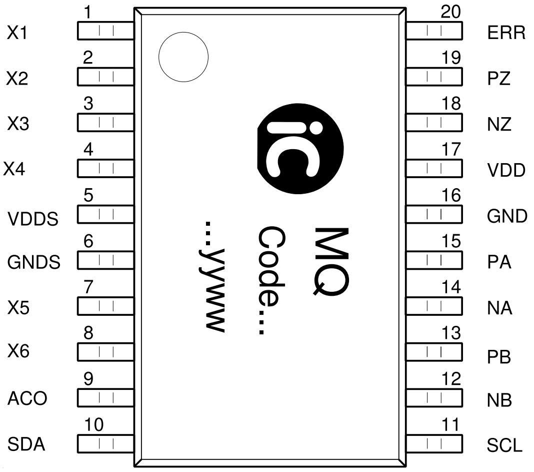
iC-MQ is protected against reverse polarity and offers its monitored supply voltage to the external circuit, thus extending the protection to the system (for load currents to 20 mA). Reverse polarity protection also covers the short-circuit-proof line drivers so that an unintentional faulty wiring during initial operation is tolerated.

On being activated the device configuration is loaded via the serial configuration interface from an external EEPROM and verified by a CRC. A microcontroller can also configure iC-MQ; the implemented interface is multimaster-competent and enables direct RAM access.

CONTENTS

PACKAGES

PIN CONFIGURATION TSSOP20



PIN FUNCTIONS

No.	Name	Function
1	X1	Signal Input 1 (Index +)
2	X2	Signal Input 2 (Index -)
3	X3	Signal Input 3
4	X4	Signal Input 4
5	VDDS	Switched Supply Output (reverse polarity proof, load to 20 mA max.)
6	GNDS	Switched Ground (reverse polarity proof)
7	X5	Signal Input 5
8	X6	Signal Input 6
9	ACO	Signal Level Controller, high-side current source output
10	SDA	Serial Configuration Interface, data line
11	SCL	Serial Configuration Interface, clock line
12	NB	Incremental Output B-
13	PB	Incremental Output B+
14	NA	Incremental Output A-
15	PA	Incremental Output A+
16	GND	Ground
17	VDD	+4.3...5.5 V Supply Voltage
18	NZ	Incremental Output Z-
19	PZ	Incremental Output Z+
20	ERR	Error Signal (In/Out) / Test Mode Trigger Input

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD, PA, NA, PB, NB, PZ, NZ, SCL, SDA, ACO		-6	6	V
G002	V()	Voltage at ERR		-6	8	V
G003	V()	Pin-Pin Voltage			6	V
G004	V()	Voltage at X1...X6, SCL, SDA		-0.3	VDDS + 0.3	V
G005	I(VDD)	Current in VDD		-20	400	mA
G006	I()	Current in VDDS, GNDS		-50	50	mA
G007	I()	Current in X1...X6, SCL, SDA, ERR		-20	20	mA
G008	I()	Current in PA, NA, PB, NB, PZ, NZ		-100	100	mA
G009	I(ACO)	Current in ACO		-100	20	mA
G010	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G011	Ptot	Permissible Power Dissipation			300	mW
G012	Tj	Junction Temperature		-40	150	°C
G013	Ts	Storage Temperature		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended range to -40 °C on request)		-25		100	°C
T02	Rthja	Thermal Resistance Chip to Ambient			80		K/W

All voltages are referenced to pin GNDS unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3...5.5 V, Tj = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	V(VDD)	Permissible Supply Voltage	Load current I(VDDS) to 10 mA Load current I(VDDS) to 20 mA	4.3 4.5		5.5 5.5	V V
002	I(VDD)	Supply Current	Tj = -40...125 °C, no load Tj = 27 °C, no load		 12	25	mA mA
003	I(VDDS)	Permissible Load Current VDDS		-20		0	mA
004	Vcz()hi	Clamp-Voltage hi at all pins				11	V
005	Vc()hi	Clamp-Voltage hi at Inputs SCL, SDA	Vc()hi = V() - V(VDD), I() = 1 mA	0.4		1.5	V
006	Vc()hi	Clamp-Voltage hi at Inputs X1...X6	Vc()hi = V() - V(VDD), I() = 4 mA	0.3		1.2	V
007	Vc()lo	Clamp-Voltage lo at all pins	I() = -4 mA	-1.2		-0.3	V
Signal Conditioning, Inputs X1...X6 (CH1, CH2: i = 12, CH0: I = 0)							
101	Vin()sig	Permissible Input Voltage Range	RINi() = 0x01 RINi() = 0x09	0.75 0		VDDS − 1.5 VDDS	V V
102	Iin()sig	Permissible Input Current Range	RINi(0) = 0; BIASi = 0 RINi(0) = 0; BIASi = 1	-300 10		-10 300	µA µA
103	Iin()	Input Current	RINi() = 0x01	-10		10	µA
104	Rin()	Input Resistance vs. VREFin	Tj = 27 °C; RINi(3:0) = 0x09 RINi(3:0) = 0x00 RINi(3:0) = 0x02 RINi(3:0) = 0x04 RINi(3:0) = 0x06	 16 1.1 1.6 2.2 3.2	 20 1.6 2.3 3.2 4.6	 24 2.1 3.0 4.2 6.0	 kΩ kΩ kΩ kΩ kΩ
105	TC(Rin)	Temperature Coefficient of Rin			0.15		%/K
106	VREFin()	Reference Voltages VREFin0, VREFin12	RINi(0) = 0, BIASi = 1 RINi(0) = 0, BIASi = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
107	G0, G12	Selectable Gain Factors	RINi(3) = 0, GRi and GFi = 0x0 RINi(3) = 0, GRi and GFi = max. RINi(3) = 1, GRi and GFi = 0x0 RINi(3) = 1, GRi and GFi = max.		2 100 0.5 25		
108	Gdiff	Relative Gain Ratio CH1 vs. CH2	GF2 = 0x10, GF1 = 0x0 GF2 = 0x10, GF1 = 0x7F		39 255		% %
109	ΔG	Step Width Of Fine Gain Adjustment	for CH0 for CH1 for CH2		1.06 1.015 1.06		
110	INL(Gi)	Integral Linearity Error of Gain Adjustment		-1.06		1.06	
111	Vin()diff	Recommended Differential Input Voltage	Vin()diff = V(PCHx) - V(NCHx); RINi(3) = 0 RINi(3) = 1	 10 40		 500 2000	 mVpp mVpp
112	Vin()os	Input Offset Voltage	referred to side of input		25		µV
113	VOScal	Offset Calibration Range	referenced to the selected source (VOS0 resp. VOS12), mode *Calibration 2*; ORi = 00 ORi = 01 ORi = 10 ORi = 11		 ±100 ±200 ±600 ±1200		 %V() %V() %V() %V()
114	ΔOF0	CH0 Offset Calibration Step Width	referenced to the selected source VOS0; OR0 = 0x0		3.2		%
115	ΔOF12	CH1/2 Offset Calibration Step Width	referenced to the selected source VOS12; OR12 = 0x0		0.79		%
116	INL(OFi)	Integral Linearity Error of Offset Calibration	limited test coverage (guaranteed by design)	-5		5	LSB
117	PHI12	Phase Error Calibration Range	CH1 vs. CH2		±20.2		°

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3...5.5 V, Tj = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
118	∆PHI12	Phase Error Calibration Step Width			0.63		°
119	INL(PHI12)	Integral Linearity Error of Phase Calibration	limited test coverage (guaranteed by design)	-0.8		0.8	°
120	fin()	Permissible Maximum Input Freq.	analog signal path	200			kHz
121	Vout(X2)	Output Voltage at X2	BIASEX = 10, I(X2) = 0, referenced to VREFin12	95	100	105	%
122	Vin(X2)	Permissible Input Voltage Range at X2	BIASEX = 11	0.5		VDDS – 2	V
123	Rin(X2)	Input Resistance at X2	BIASEX = 11, RIN0(3:0) = 0x01, RIN12(3:0) = 0x01	20	27	30	kΩ
Sine-To-Digital Conversion							
201	AAabs	Absolute Angle Accuracy	referenced to 360° input signal, ideal waveform, quasi static signals, adjusted signal conditioning, SELHYS = 0		0.9	1.8	°
202	AArel	Relative Angle Accuracy	referenced to output period T (see Fig. 1), ideal waveform, quasi static signals;				
			at 4 edges per period			10	%
			at 100 edges per period		<0.5	10	%
			at 384 edges per period			10	%
			at 400 edges per period		<2	10	%
203	AAR	Repeatability	see 201; VDD = const., T_j = const.		0.1		°
Line Driver Outputs PA, NA, PB, NB, PZ, NZ							
501	Vs()hi	Saturation Voltage hi	Vs() = VDD - V();				
			SIK(1:0) = 00, I() = -1.2 mA			200	mV
			SIK(1:0) = 01, I() = -4 mA			200	mV
			SIK(1:0) = 10, I() = -20 mA			400	mV
			SIK(1:0) = 11, I() = -50 mA			700	mV
502	Vs()lo	Saturation Voltage lo	SIK(1:0) = 00, I() = 1.2 mA			200	mV
			SIK(1:0) = 01, I() = 4 mA			200	mV
			SIK(1:0) = 10, I() = 20 mA			400	mV
			SIK(1:0) = 11, I() = 50 mA			700	mV
503	Isc()hi	Short-Circuit Current hi	V() = 0 V;				
			SIK(1:0) = 00	-4		-1.2	mA
			SIK(1:0) = 01	-12		-4	mA
			SIK(1:0) = 10	-60		-20	mA
			SIK(1:0) = 11	-150		-50	mA
504	Isc()lo	Short-Circuit Current lo	V() = VDD;				
			SIK(1:0) = 00	1.2		4	mA
			SIK(1:0) = 01	4		12	mA
			SIK(1:0) = 10	20		60	mA
			SIK(1:0) = 11	50		150	mA
505	tr()	Rise Time	RL = 100 Ω to GND;				
			SSR(1:0) = 00	5		20	ns
			SSR(1:0) = 01	5		40	ns
			SSR(1:0) = 10	20		140	ns
			SSR(1:0) = 11	50		350	ns
506	tf()	Fall Time	RL = 100 Ω to VDD;				
			SSR(1:0) = 00	5		20	ns
			SSR(1:0) = 01	5		40	ns
			SSR(1:0) = 10	30		140	ns
			SSR(1:0) = 11	50		350	ns
507	Ilk()tri	Leakage Current	TRIHL(1:0) = 11 (tristate)		20	100	µA
508	Ilk()rev	Leakage Current	reversed supply voltage		100		µA
509	Rin()cal	Test Signal Source Impedance	Op. modes *Calibration 1, 2, 3*		2.5	4	kΩ
510	I()cal	Permissible Test Signal Load	Op. modes *Calibration 1, 2, 3*	-3		3	µA
511	tclk()lo	Clock Signal Low-Pulse Duration for CP, CPD, CPU	Op. mode *Mode 191/193*;				
			MTD = 0x0		110		ns
			MTD = 0x7		800		ns
512	tw()hi	Duty Cycle	referenced to output period T, see Fig. 1		50		%

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3...5.5 V, Tj = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
513	t_{AB}	Phase Shift A vs. B	see Fig. 1		25		%
514	t_{MTD}	Minimum Phase Distance	edge to edge, see Fig. 1;				
			MTD = 0x0, IBN calibrated to 200 µA		220		ns
			MTD = 0x0, IBN calibrated to 220 µA		200		ns
515	$\Delta t()$MTD	Minimum Phase Distance Tolerance	nominal values in Table 52	-18		13.5	%
516	$\Delta t()$MTD	Minimum Phase Distance Variation	variation versus VDD = 5 V, Tj = 27 °C due to VDD = 4.3...5.5 V or Tj = -40...125 °C		+/- 2		%
Signal Level Controller ACO							
601	Vs()hi	Saturation Voltage hi	Vs() = VDD - V();				
			ADJ(8:0) = 0x11F, I(ACO) = -5 mA			1	V
			ADJ(8:0) = 0x13F, I(ACO) = -10 mA			1	V
			ADJ(8:0) = 0x15F, I(ACO) = -25 mA			1	V
			ADJ(8:0) = 0x17F, I(ACO) = -50 mA			1.2	V
602	Isc()hi	Short-Circuit Current hi	V() = 0 ... VDD - 1 V;				
			ADJ(8:0) = 0x11F	-10		-5	mA
			ADJ(8:0) = 0x13F	-20		-10	mA
			ADJ(8:0) = 0x15F	-50		-25	mA
			V() = 0 ... VDD - 1.2 V;				
			ADJ(8:0) = 0x17F	-100		-50	mA
603	It()min	Control Range Monitoring 1: lower limit	referenced to range ADJ(6:5)		3		%Isc
604	It()max	Control Range Monitoring 2: upper limit	referenced to range ADJ(6:5)		90		%Isc
605	Vt()min	Signal Level Monitoring 1: lower limit	referenced to Vscq()		40		%Vpp
606	Vt()max	Signal Level Monitoring 2: upper limit	referenced to Vscq()		130		%Vpp
Bias Current Source and Reference Voltages							
801	IBN	Bias Current Source	*Calibration 1*, I(NB) vs. VDDS;				
			CFGIBN = 0x0	110			µA
			CFGIBN = 0xF			370	µA
			IBN calibrated at T = 25 °C	180	200	220	µA
802	VBG	Internal Bandgap Reference		1.2	1.25	1.3	V
803	VPAH	Reference Voltage		45	50	55	%VDDS
804	V05	Reference Voltage V05		450	500	550	mV
805	V025	Reference Voltage V025			50		%V05
Power-Down-Reset							
901	VDDon	Turn-on Threshold VDD, Power-Up-Enable	increasing voltage at VDD	3.6	4.0	4.3	V
902	VDDoff	Turn-off Threshold VDD, Power-Down-Reset	decreasing voltage at VDD	3.0	3.5	3.8	V
903	VDDhys	Hysteresis		0.4			V
Error Signal Input/Output, Pin ERR							
B01	Vs()lo	Saturation Voltage lo	versus GND, I() = 4 mA			0.4	V
B02	Isc()lo	Short-Circuit Current lo	versus GND, V(ERR) ≤ VDD	4	5	8	mA
B03	Isc()	Low-Side Current Source For Data Output	versus GND, V(ERR) > VTMon				
			L state		2		mA
			Z state		0		mA
B04	Vt()hi	Input Threshold Voltage hi	versus GND			2	V
B05	Vt()lo	Input Threshold Voltage lo	versus GND	0.8			V
B06	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi − Vt()lo	300	500		mV
B07	Ipu()	Input-Pull-Up-Current	V() = 0...VDD − 1 V, EPU = 1	-400	-300	-200	µA
B08	Vpu()	Pull-Up-Voltage	Vpu() = VDD − V(), I() = -5 µA, EPU = 1			0.4	V
B09	VTMon	Test Mode Turn-on Threshold	increasing voltage at ERR			VDD + 2	V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3...5.5 V, Tj = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B10	VTMoff	Test Mode Turn-off Threshold	decreasing voltage at ERR	VDD + 0.5			V
B11	VTMhys	Test Mode Threshold Hysteresis	VTMhys = VTMon − VTMoff	0.15	0.3		V
B12	fclk()	Data Output Signal Frequency	ENFAST = 0	120	160	200	kHz
			ENFAST = 1	480	640	800	kHz
B13	tp(ERR)in	Process Delay for System Error Message at ERR	upon power up (VDD > VDDon)		10		ms
Reverse Polarity Protection and Supply Switches VDDS, GNDS							
C01	Vs()	Saturation Voltage vs. VDD	Vs(VDDS) = VDD − V(VDDS);				
			I(VDDS) = -10...0 mA			150	mV
			I(VDDS) = -20...-10 mA			250	mV
C02	Vs()	Saturation Voltage vs. GND	Vs(GNDS) = V(GNDS) − GND;				
			I(GNDS) = 0...10 mA			150	mV
			I(GNDS) = 10...20 mA			200	mV
C03	Irev(VDD)	Reversed Polarity Current	V(VDD) = −5.5V...−4.3 V	-1		0	mA
Serial Configuration Interface SCL, SDA							
D01	Vs()lo	Saturation Voltage lo	I = 4 mA			400	mV
D02	Isc()lo	Short-Circuit Current lo		4		75	mA
D03	Vt()hi	Input Threshold Voltage hi				2	V
D04	Vt()lo	Input Threshold Voltage lo		0.8			V
D05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi − Vt()lo	300	500		mV
D06	Ipu()	Input Pull-Up Current	V() = 0...VDDS − 1 V	-600	-300	-60	µA
D07	Vpu()	Pull-Up Voltage	Vpu() = VDDS − V(), I() = -5 µA			0.4	V
D08	fclk()	Clock Frequency at SCL	ENFAST = 0	60	80	100	kHz
			ENFAST = 1	240	320	400	kHz
D09	tbusy()cfg	Duration of Startup Configuration	IBN not calibated, EEPROM access without read failure, time to outputs operational;				
			ENFAST = 0		36	48	ms
			ENFAST = 1		24	34	ms
D10	tbusy()err	End Of I2C Communication; Time Until I2C Slave Is Enabled	IBN not calibrated;				
			V(SDA) = 0 V		4	12	ms
			V(SCL) = 0 V or arbitration lost		indef.		ms
			no EEPROM		45	135	ms
			CRC ERROR		95	285	ms
D11	tp()	Start Of Master Activity On I2C Protocol Error	SCL without clock signal: V(SCL) = constant;				
			IBN not calibrated	25	80	240	µs
			IBN calibrated to 200 µA	64	80	120	µs
Temperature Monitoring							
E01	VTs	Temperature Sensor Voltage	VTs() = VDDS − V(PA), *Calibration 3*, without Load;				
			Tj = -40 °C	740	770	790	mV
			Tj = 27 °C	620	650	670	mV
			Tj = 100 °C	460	520	540	mV
E02	TCs	Temp. Co. Temperature Sensor Voltage			-1.8		mV/K
E03	VTth	Temperature Warning Activation Threshold	VTth() = VDDS - V(NA), Tj = 27 °C, *Calibration 3*, without Load;				
			CFGTA(3:0) = 0x0	260	310	360	mV
			CFGTA(3:0) = 0xF	470	550	630	mV
E04	TCth	Temp. Co. Temperature Warning Activation Threshold			0.06		%/K
E05	Tw	Warning Temperature	CFGTA(3:0) = 0x0	125	140		°C
			CFGTA(3:0) = 0xF		65	80	°C
E06	Thys	Warning Temperature Hysteresis	80 °C < T_j < 125 °C	10	15	25	°C
E07	ΔT	Relative Shutdown Temperature	ΔT = Toff − Tw	5	15	25	°C

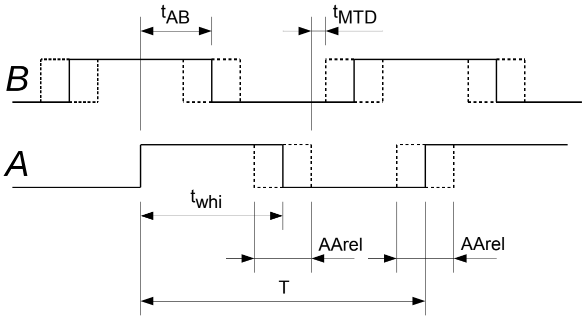


Figure 1: Definition of relative angle error and minimum phase distance

PROGRAMMING

Register Map, Overview .... Page 12

Serial Configuration Interface .... Page 14

ENFAST:	I^{2}C Fast Mode Enable
ENSL:	I^{2}C Slave Mode Enable
DEVID:	Device ID of EEPROM providing the chip configuration data (e.g. 0x50)
CHKSUM:	CRC of chip configuration data (address range 0x00 to 0x2F)
CHPREL:	Chip Release
END:	Configuration Enable

Calibration .... Page 16

CFGIBN:	Bias Current
CFGTA:	Temperature Monitoring

Operating Modes .... Page 17

MODE:	Operating Mode

Input Configuration and Signal Path Multiplexer .... Page 19

INMODE:	Diff./Single-Ended Input Mode
RIN12:	I/V Mode and Input Resistance CH1, CH2
BIAS12:	Reference Voltage CH1, CH2
RIN0:	I/V Mode and Input Resistance CH0
BIAS0:	Reference Voltage CH0
BIASEX:	Input Reference Selection
INVZ:	Index Signal Inversion
MUXIN:	Input-To-Channel Assignment: X3...X6 to CH1, CH2

Signal Conditioning CH1, CH2 (X3...X6) ... Page 21

GR12:	Gain Range CH1, CH2 (coarse)
GF1:	Gain Factor CH1 (fine)
GF2:	Gain Factor CH2 (fine)
VOS12:	Offset Reference Source CH1, CH2
VDC1:	Intermediate Voltage CH1
VDC2:	Intermediate Voltage CH2
OR1:	Offset Range CH1 (coarse)
OF1:	Offset Factor CH1 (fine)
OR2:	Offset Range CH2 (coarse)
OF2:	Offset Factor CH2 (fine)
PH12:	Phase Correction CH1 vs. CH2

Signal Conditioning CH0 (X1, X2) .... Page 24

GR0:	Gain Range CH0 (coarse)
GF0:	Gain Factor CH0 (fine)
VOS0:	Offset Reference Source CH0
OR0:	Offset Range CH0 (coarse)
OF0:	Offset Factor CH0 (fine)

Signal Level Controller .... Page 25

ADJ:	Setup of ACO Output Function

Sine-To-Digital Conversion .... Page 26

SELRES:	Resolution
SELHYS:	Hysteresis

Quadrature Output Logic .... Page 27

CFGABZ:	Output Logic
CFGZPOS:	Zero Signal Positioning
ENZFF:	Zero Signal Synchronisation

Quadrature Output Settings .... Page 29

MTD:	Minimum Phase Distance
SIK:	Driver Short-Circuit Current
SSR:	Driver Slew Rate
TRIHL:	Driver Mode

Error Monitoring and Alarm Output .... Page 30

EMTD:	Minimal Alarm Indication Time
EPH:	Alarm Input/Output Logic
EPU:	Alarm Output Pull-Up Enable
EMASKA:	Error Mask For Alarm Indication (pin ERR)
EMASKE:	Error Mask For Protocol (EEPROM)
EMASKO:	Error Mask For Driver Shutdown
PDMODE:	Driver Activation After Cycling Power
LINECNT:	Line Count (Pulses) Between 2 Zero Pulses
ERR1:	Error Protocol: First Error
ERR2:	Error Protocol: Last Error
ERR3:	Error Protocol: History

Test Mode .... Page 33

EMODE:	Test Mode
EMODE2:	Register And Address Selection For Test Mode

REGISTER MAP

Register Map

Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Serial Configuration Interface								
0x00	ENFAST	DEVID(6:0)						
Calibration								
0x01	CFGIBN(3:0)				CFGTA(3:0)			
Operating Mode								
0x02	END	1	0	ENZFF	MODE(3:0)			
Input Configuration								
0x03	0	0	0	0	INVZ	INMODE	MUXIN(1:0)	
Signalkonditionierung CH1, CH2								
0x04	GF2(4:0)					GR12(2:0)		
0x05	GF1(3:0)				0	0	0	0
0x06	VDC1(0)	0	0	0	0	GF1(6:4)		
0x07	0	0	0	VDC1(5:1)				
0x08	OR1(0)	VDC2(5:0)						0
0x09	OF1(3:0)				0	0	0	OR1(1)
0x0A	0	0	OR2(1:0)		OF1(7:4)			
0x0B	OF2(6:0)							0
0x0C	PH12(2:0)			0	0	0	0	OF2(7)
0x0D	BIASEX(1:0)		0	1	1	PH12(5:3)		
0x0E	1	BIAS12	VOS12(1:0)		RIN12(3:0)			
Signal Level Controller								
0x0F	ADJ(0)	—	0	1	0	0	0	0
0x10	ADJ(8:1)							
Signal Conditioning CH0								
0x11	GF0(4:0)					GR0(2:0)		
0x12	OF0(5:0)						OR0(1:0)	
0x13	0	BIAS0	VOS0(1:0)		RIN0(3:0)			
Error Monitoring and Alarm Output								
0x14	EMASKA(7:0)							
0x15	EMODE(1:0)		EMTD(2:0)			EPH	EMASKA(9:8)	
0x16	EMASKO(7:0)							
0x17	EMASKE(3:0)				ENSL	EPU	EMASKO(9:8)	
0x18	EMODE2	PDMODE	EMASKE(9:4)					
Zero Signal Output								
0x19	CFGABZ(7:0)							
0x1A	CFGZPOS(7:0)							
Sine-To-Digital Conversion, Minimum Phase Distance								
0x1B	SELRES(7:0)							
0x1C	—	SELRES(14:8)						
0x1D	MTD(3:0)				SELHYS(3:0)			
Output Driver Settings								
0x1E	—	—	SIK(1:0)		SSR(1:0)		TRIHL(1:0)	

Register Map								
Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Line Counter								
0x1F	LINECNT(7:0)							
0x20	0	0	LINECNT(13:8)					
Reserved								
0x21	0	0	0	0	1	0	0	0
0x22	0x00 (recommended programming)							
0x23	0x00 (recommended programming)							
0x24	free for OEM data							
0x25	free for OEM data							
0x26	free for OEM data							
0x27	free for OEM data							
0x28	free for OEM data							
0x29	free for OEM data							
0x2A	free for OEM data							
0x2B	free for OEM data							
0x2C	free for OEM data							
0x2D	free for OEM data							
0x2E	free for OEM data							
Check Sum								
0x2F	CHKSUM(7:0) of EEPROM data [CHPREL(7:0), refer to Table 7]							
Error Register								
0x30	ERR1(7:0)							
0x31	ERR2(5:0)						ERR1(9:8)	
0x32	ERR3(3:0)				ERR2(9:6)			
0x33	—	—	ERR3(9:4)					
Notes	The device RAM initially contains random data following power-on.							

Table 4: Register layout (EEPROM)

SERIAL CONFIGURATION INTERFACE

The serial configuration interface consists of the two pins SCL and SDA and enables read and write access to an EEPROM with an I^{2}C interface. The readout clock rate can be selected using ENFAST.

ENFAST	Adr 0x00, bit 7
Code	Function
0	Regular clock rate, f(SCL) approx. 80 kHz
1	High clock rate, f(SCL) approx. 320 kHz
Notes	For in-circuit programming bus lines SCL and SDA require pull-up resistors. For line capacitances to 170 pF, adequate values are: 4.7 kΩ with clock frequency 80 kHz 2 kΩ with clock frequency 320 kHz The pull-up resistors may not be less than 1.5 kΩ. To separate the signals a ground line between SCL and SDA is recommended. iC-MQ requires a supply voltage during EEPROM programming (5 V to VDD).

Table 5: Clock Frequency Configuration Interface

Once the supply has been switched on the iC-MQ outputs are high impedance (tristate*) until a valid configuration is read out from the EEPROM using device ID 0x50.

Bit errors in the 0x00 to 0x2F memory section are pinpointed by the CRC deposited in register CHKSUM(7:0) (address 0x2F in the EEPROM; the CRC polynomial used is "'1 0001 1101"' with a start value of "1").

Should the read configuration data not be confirmed by the CRC, the readin process is repeated. If no valid configuration data is available after a fourth readin, iC-MQ terminates EEPROM access and switches to I^{2}C slave mode. This switch takes place after 150 ms at the latest (see Electrical Characteristics, D11), for example when no EEPROM is connected.

For devices loading a valid configuration from the EEPROM register bit ENSL decides whether the I^{2}C slave function is enabled or not.

ENSL	Adr 0x17, bit 3
Code	Function
0	Normal operation
1	I^{2}C Slave Mode Enable (Device ID 0x55)

Table 6: Config. Interface Mode

The device ID for the EEPROM can be entered in register DEVID(6:0) (address 0x00), from which iC-MQ will take its configuration after exiting test mode (see page 33). The DEVID stored therein is then accepted.

Example of CRC Calculation Routine

```
unsigned char ucDataStream = 0;
int iCRCPoly = 0x11D;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 1; // start value !!!
for (iReg = 0; iReg<47; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1) ^ iCRCPoly;
    else
      ucCRC = (ucCRC << 1);
    ucDataStream = ucDataStream << 1;
  }
}
```

EEPROM Selection

The following minimal requirements must be fulfilled:

- Operation from 3.3 to 5 V, I^{2}C interface
- At least 512 bits, 64x8 (address range used is 0x00 to 0x3F)
- Support of *Page Write* with *Pages* of at least 4 bytes. Errors can otherwise not be saved to the EEPROM (EMASKE = 0x0).
- Device ID 0x50 "1010 000", no occupation of 0x55 (A2...A0 = 0). iC-MQ can otherwise not be accessed via 0x55 in I^{2}C slave mode.

Recommended device: Atmel AT24C01B, ST M24C01W

I^{2}C Slave Mode (ENSL = 1)

In this mode iC-MQ behaves like an I^{2}C slave with the device ID 0x55 and the configuration interface permits write and read accesses to iC-MQ's internal registers.

For chip release verification purposes an identification value is stored under ROM address 0x2F; a write access to this address is not permitted.

CHPREL	Adr 0x2F, bit 7:0 (ROM)
Code	Chip Release
0x00	Not available
0x04	iC-MQ 3
0x08	iC-MQ X
0x09	iC-MQ X1

Table 7: Chip Release

END	Adr 0x02, bit 7
Code	Function
0	Sin/D converter and line driver disabled (RAM configuration data invalid)
1	Restart of Sin/D conversion, line driver active (RAM configuration data valid)

Table 8: Configuration Enable

Register	Read access via I^{2}C slave mode (ENSL = 1)
RAM Addr	Content
0x00-0x21	Configuration data (see EEPROM addresses 0x00-0x21)
0x22-0x2A	Not available
0x2B-0x2E	Configuration data (see EEPROM addresses 0x2B-0x2E)
0x2F	Chip release CHPREL(7:0)
0x30-0x33	Configuration data (see EEPROM addresses 0x30-0x33)
0x34-0x3A	Not available
0x3B-0x3E	Configuration data (see EEPROM addresses 0x2B-0x2E)
0x3F	Chip release CHPREL(7:0)
0x40-0x43	Current error memory (only active when enabled by EMASKE; messages will be transferred to EEPROM Addresses 0x30-0x33)
0x44-0x7F	Not available

Table 9: RAM Read Access

Register	Write access via I^{2}C slave mode (ENSL = 1)
RAM Addr	Access and conditions
0x00	Changes possible, no restrictions
0x01	Changes possible (wrong entries for CFGIBN can limit functions)
0x02	Changes to bits 6:0 are permitted only when Sin/D conversion is halted (END = 0, ie. bit 7); Restarting Sin/D conversion by changing END (bit 7) is permitted only with no changes of operating mode (bits 6:0 remain as set)
0x03-0x16	Changes possible, no restrictions
0x17	Changes to bits 7:4 and 2:0 are permitted (ENSL, bit 3 must be kept 1)
0x18	Changes possible, no restrictions
0x19-0x21	Changes possible when Sin/D conversion is halted (END = 0)
0x2B-0x2E	Changes possible, no restrictions
0x2F-0x3F	No write access permitted
0x40-0x43	No write access permitted
0x44-0x7F	Not available

Table 10: RAM Write Access

Notes: The converter function should be halted by END = 0 for the deletion of errors saved in the EEPROM (Dev-ID 0x50, Addresses 0x30-0x33). Otherwise active errors could be transferred to the EEPROM again (from addresses 0x40-0x43 if enabled by EMASKE).

BIAS CURRENT SOURCE AND TEMPERATURE SENSOR CALIBRATION

Bias Current

The calibration of the bias current source in operation mode *Calibration 1* (see Table 13) is prerequisite for adherence to the given electrical characteristics and also instrumental in the determination of the chip timing (e.g. clock frequency at SCL). For setup purposes the IBN bias current is measured using a 10 kΩ resistor by pin VDDS connected to pin NC. The setpoint is 200 µA which is equivalent to a voltage drop of 2 V.

CFGIBN	Adr 0x01, bit 7:4		
Code k	$IBN \sim \frac{31}{39-k}$	Code k	$IBN \sim \frac{31}{39-k}$
0x0	79 %	0x8	100 %
0x1	81 %	0x9	103 %
0x2	84 %	0xA	107 %
0x3	86 %	0xB	111 %
0x4	88 %	0xC	115 %
0x5	91 %	0xD	119 %
0x6	94 %	0xE	124 %
0x7	97 %	0xF	129 %

Table 11: Calibration of Bias Current

Temperature Sensor

The temperature monitoring is calibrated in operating mode *Calibration 3*.

To set the required warning temperature T_2 the temperature sensor voltage VTs at which the warning message is generated is first determined. To this end a voltage ramp from VDDS towards GNDS is applied to pin PA until pin ERR displays the warning message. The following settings are required here: EMASKA = 0x20, EMTD = 0x00 and EPH = 0x00.

The signal at ERR first switches from tristate to low (on reaching the warning threshold VTs) and then from low to tristate (on overshooting the internal hysteresis which is not relevant to calibration). To avoid confusion a clear change of state (from low to high) must be generated with the help of an external pull-up resistor at pin ERR.

Example: $VTs(T_1)$ is ca. 650 mV, measured from VDDS versus PA, with T_1 = 25 °C;

The necessary reference voltage $VTth(T_1)$ is then calculated. The required warning temperature T_2, temperature coefficients TCs and TCth (see Electrical Characteristics, Section E) and measurement value $VTs(T_1)$ are entered into this calculation:

$$VTth(T_1) = \frac{VTs(T_1) + TCs \cdot (T_2 - T_1)}{1 + TCth \cdot (T_2 - T_1)}$$

Example: For $T_2 = T_1 + 100\,K$ $VTth(T_1)$ must be programmed to 443 mV.

Reference voltage $VTth(T_1)$ is provided for a high impedance measurement (10 MΩ) at output pin NA (measurement versus VDDS) and must be set by programming CFGTA(3:0) to the calculated value.

Example: Altering $VTth(T_1)$ from 310 mV (measured with CFGTA(3:0)= 0x0) to 443 mV is equivalent to 143 %, the closest value for CFGTA is 0x9;

CFGTA	Adr 0x01, bit 3:0		
Code k	$VTth \sim \frac{65+3k}{65}$	Code k	$VTth \sim \frac{65+3k}{65}$
0x0	100 %	0x8	140 %
0x1	105 %	0x9	145 %
0x2	110 %	0xA	150 %
0x3	115 %	0xB	155 %
0x4	120 %	0xC	160 %
0x5	125 %	0xD	165 %
0x6	130 %	0xE	170 %
0x7	135 %	0xF	175 %
Notes	With CFGTA = 0xF Toff is 80 °C typ., with CFGTA = 0x0 Toff is 155 °C typ.		

Table 12: Calibration of Temperature Monitoring

OPERATING MODES

iC-MQ has various modes of operation, for which the functions of outputs PA, NA, PB, NB, PZ, NZ and ERR are altered.

Two operating modes can be selected for the output of the angle position in normal operation. *Mode 191/193* provides control signals for devices compatible with 74HC191 or 74HC193, whereas in *Mode ABZ* the angle position is output incrementally as an encoder quadrature signal with a zero pulse. Only in these modes are the line drivers and the reverse polarity protection feature active.

In order to condition the input signals and to calibrate and test iC-MQ *Calibration* and *Test* modes are available. Digital and analog test signals are provided; the latter must always be measured at high load impedance.

MODE(3:0)		Addr. 0x02; bit 3:0						
Code	Operating Mode	PA	NA	PB	NB	PZ	NZ	ERR
0x00	Mode ABZ	A	not(A)	B	not(B)	Z	not(Z)	ERR
0x0F	Mode 191/193	CPD	CPU	CP	nU/D	MR	nPL	ERR
0x01	Calibration 1	TANAZ(2)	VREFIZ	VREFISC	IBN	PCH0	NCH0	IERR
0x02	Calibration 2	PCH1	NCH1	PCH2	NCH2	VDC1	VDC2	
0x03	Test 3*	VPAH	VPD	—	CGUCK	IPF	V05	IERR
0x04	Test 4*	PS_out	NS_out	PC_out	NC_out	PZO	NZO	IERR
0x05	Test 5*	PSIN	NSIN	PCOS	NCOS	PZO	NZO	IERR
0x06	Test 6*	PCH1I	NCH1I	PCH2I	NCH2I	VDC1	VDC2	res.
0x07	Calibration 3	VTs	VTth	—	—	VTTFE	VTTSE	ERR
0x08	Lo-Signal	All outputs and SCL, SDA, ERR to low level						
0x09	Hi-Signal	All outputs to high level						
0x0A	Test 10*	TP	CLK6	CLK1	CLK3/8	Z_{In}	CLK4	
0x0B	System Test*	A_4	A_8	B_4	B_8	Z_{In}	TP1	ERR
0x0C	Test 12*	A	not(A)	B	not(B)	Z	not(Z)	ERR
0x0D	—	—	—	—	—	—	—	—
0x0E	IDDQ Test*	All PU/PD resistors, oscillator and analog supply voltage deactivated.						
	Hints	*) Test function for iC-Haus device test only.						

Table 13: Operating Modes

Mode ABZ

In *Mode ABZ* A/B signals are generated and output via PA, NA, PB and NB. A freely configurable zero signal is simultaneously provided at pins PZ and NZ. The differential RS422 line drivers are active; an Nx pin constantly supplies a complementary signal which is the inversion of pin Px.

Mode 191/193

In *Mode 191/193* the output pins provide control signals for counter devices compatible with 74HC191 or 74HC193 according to the following table. The driving capability (SIK) and the slew rate (SSR) of the output drivers must be selected so that the clock pulses can be output with a low pulse of typically 50 ns (see Electrical Characteristics, 511).

Mode 191/193		
Pin	Signal	Description
PA	CPD	Clock Down Pulse
NA	CPU	Clock Up Pulse
PB	CP	Clock Pulse
NB	nU/D	Count Direction (0: up, 1: down)
PZ	MR	Asynch. Master Reset (active high) Signal is ’1’ if index position is reached, otherwise ’0’.
NZ	nPL	Asynch. Parallel Load Input (active low) / Reset (active low) Signal is ’0’ if index position is reached, otherwise ’1’.

Table 14: Operating mode for counter devices compatible with 74HC191 or 74HC193.

Calibration 1, 2, 3

These modes are used to condition the input signals and calibrate iC-MQ. In mode *Calibration 1* the user can measure the IBN bias current and the zero channel analog signals are available following signal conditioning (PCH0 and NCH0).

In mode *Calibration 2* the conditioned sine and cosine signals are output (PCH1, NCH1, PCH2 and NCH2). In addition intermediate potential VDC1 is provided for compensating circuit CH1, as is intermediate potential VDC2 for CH2 (for a description of the calibration process, see page 21).

In mode *Calibration 3* the internal temperature monitoring signals are provided. Calibration of the bias current source and temperature monitoring is described on page 16 and calibration of the zero channel on page 24.

TEST 6

The input voltages at pins X3 to X6 can be checked in mode *Test 6*. The following settings are required here:

- GF1 = 0x0
- GF2 = 0x0
- Byte 0x05, bit 3:0 = ’0000’
- Byte 0x0F, bit 3 = ’1’
- Byte 0x0F, bit 4 = ’0’

System Test

This mode enables the signal conditioning to be adjusted using comparated sine and cosine signals. To this end at a resolution of 8 the interpolator generates a switchpoint every 45 degrees. The objective of the calibration procedure is a pulse duty cycle of exactly 50% respectively for A_4, B_4 und A_8, B_8. The following settings are required for mode *System Test*:

- MODE = 0x0B
- SELRES = 0x1B0
- SELHYS = 0xF
- CFGABZ(7:4) = ’0000’

System Test		
Pin	Signal	Description
PA	A_4	Offset CH1
NA	A_8	Phase deviation from 90° between CH1 and CH2
PB	B_4	Offset CH2
NB	B_8	Amplitude deviation between CH1 and CH2
PZ	Z_{In}	Digital zero signal, unmasked
NZ	TP1	Verification of line count (pulses) between two zero pulses Low signal: verification running (state after power on reset) High signal: verification finished An error messaging at ERR is valid after the second zero signal (enable required).

Table 15: Digital Calibration Signals

INPUT CONFIGURATION

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Referenced input signals can be processed; input X2 can be configured as a reference input. Both current and voltage signals can be processed, selected using RIN12 and RIN0.

INMODE	Adr 0x03, bit 2
Code	Function
0	Differential input signals
1	Single-ended input signals *
Note	* Input X2 is reference for all inputs.

Table 16: Input Signal Mode

Current Signals

In I Mode an input resistor Rin() becomes active at each input pin, converting the current signal into a voltage signal. Input resistance Rin() consists of a pad wiring resistor and resistor Rui() which is linked to the adjustable bias voltage source VREFin(). BIASEX must be set to '00'. The table besides shows the possible selections, with Rin() giving the typical resulting input resistance (see Electrical Characteristics for tolerances). The input resistor should be set in such a way that intermediate potentials VDC1 and VDC2 lie between 125 mV and 250 mV (verifiable in mode *Calibration 2*).

Voltage Signals

In V mode an optional voltage divider can be selected which reduces unacceptably large input amplitudes to ca. 25 %. The circuitry is equivalent to the resistor chain in I mode; the pad wiring resistor is considerably larger here, however. For sensors whose offset calibration is to be proportional to an external DC voltage source the reference source can be selected using BIASEX; for all other sensors BIASEX should be set to '00'.

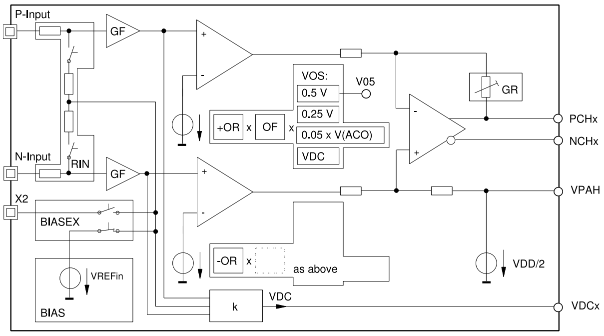


Figure 2: Signal Conditioning

RIN12 **RIN0**	Adr 0x0E, bit 3:0 Adr 0x13, bit 3:0		
Code	Nominal Rin()	Internal Rui()	I/V Mode
–000	1.7 kΩ	1.6 kΩ	current input
–010	2.5 kΩ	2.3 kΩ	current input
–100	3.5 kΩ	3.2 kΩ	current input
–110	4.9 kΩ	4.6 kΩ	current input
1—1	20 kΩ	5 kΩ	voltage input
0—1	high impedance	1 MΩ	voltage input

Table 17: I/V Mode and Input Resistance

BIAS12 **BIAS0**	Adr 0x0E, bit 6 Adr 0x13, bit 6	
Code	VREFin()	Type of sensor
0	2.5 V	Lowside sink current (I Mode)
1	1.5 V	Highside current source (I Mode)
Note	Not valid with BIASEX=11.	

Table 18: Reference Voltage

BIASEX	Adr 0x0D, bit 7:6	
Code	VREFin()	Signal at X2
00*	1.5 / 2.5 V (internal)	Neg. Zero Signal (Index -), input
10	1.5 / 2.5 V (internal)	Ref. Voltage VREFin12, output
11	external	Voltage at X2 supplies VREFin

Table 19: Input Reference Selection

SIGNAL PATH MULTIPLEXING

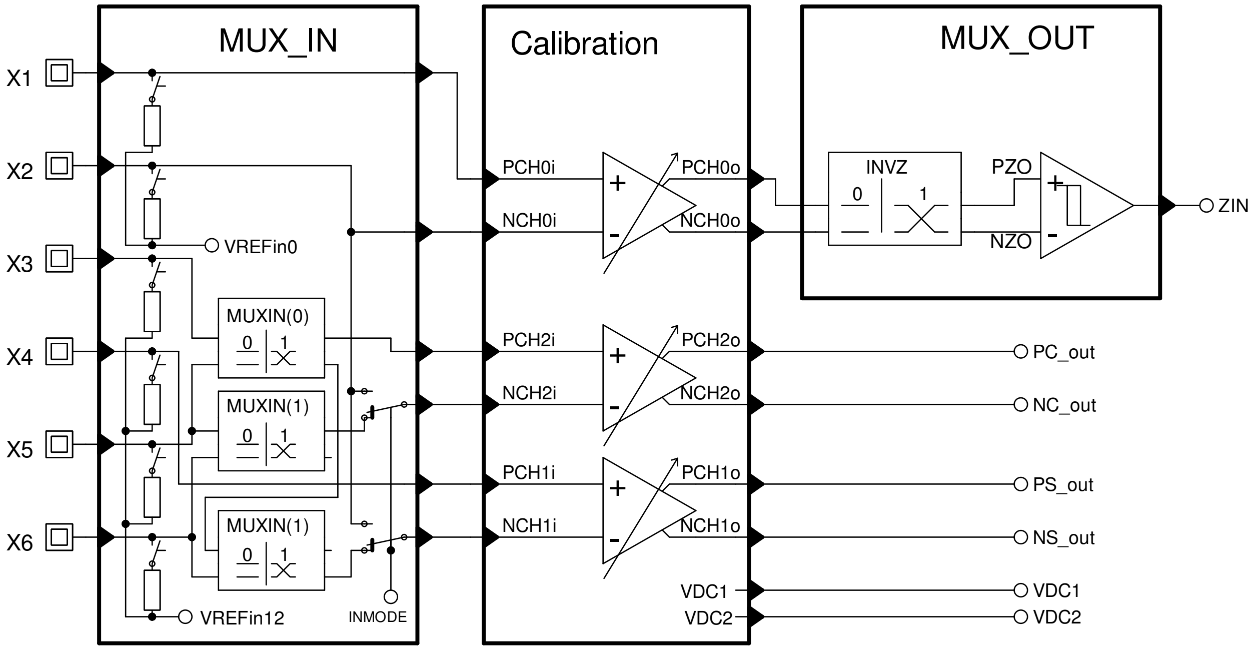


Figure 3: Principle Of Multiplexer Function

The signals for index channel CH0 are connected up to pins X1 and X2. Pins X3 to X6 are allocated to internal channels CH1 and CH2 via MUXIN. INMODE can be activated for referenced input signals; this then selects X2 as the reference signal input. For output purposes INVZ allows the index signal phase to be inverted for channel CH0.

MUXIN	Adr 0x03, bit 1:0			
Code	PCH1i	NCH1i	PCH2i	NCH2i
00	X4	X6	X3	X5
01	not permitted			
10	X4	X5	X3	X6
11	X4	X3	X5	X6

Table 20: Input Multiplexer for INMODE = 0

MUXIN	Adr 0x03, bit 1:0			
Code	PCH1i	NCH1i	PCH2i	NCH2i
00	X4	X2	X3	X2
01	not permitted			
10	not permitted			
11	X4	X2	X5	X2

Table 21: Input Multiplexer for INMODE = 1

INVZ	Adr 0x03, bit 3	
Code	PZO	NZO
0	PCH0o	NCH0o
1	NCH0o	PCH0o

Table 22: Index Signal Inversion

SIGNAL CONDITIONING CH1, CH2

The analog voltage signals necessary for the calibration of the sine signals can be measured in operation mode *Calibration 2*. Alternatively, characteristic digital test signals are also available for offset, amplitude and phase errors in operating mode *System Test*.

Gain Settings

The gain is set in four steps:

1. The sensor supply controller is shut down and the constant current source for the ACO output set to a suitable output current (register ADJ; current value close to the later operating point).

2. The coarse gain is selected so that differential signal amplitudes of ca. 1 Vpp are produced internally (signal Px versus Nx, see Figure).

3. Using fine gain factor GF2 the CH2 signal amplitude is then adjusted to 1 Vpp.

4. The CH1 signal amplitude can then be adjusted to the CH2 signal amplitude via fine gain factor GF1. This results in a total gain of GR12 * GFi for differential input signals.

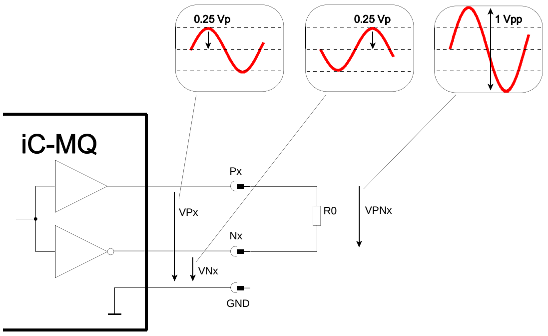


Figure 4: Definition of 1 Vpp signal. Termination R0 must be high-ohmic during all *Test* and *Calibration* modes.

GR12	Adr 0x04, bit 2:0	
Code	Range RIN12=0x9	Range RIN12≠0x9
0x0	0.5	2.0
0x1	1.0	4.1
0x2	1.3	5.3
0x3	1.7	6.7
0x4	2.2	8.7
0x5	2.6	10.5
0x6	3.3	13.2
0x7	4.0	16.0

Table 23: Gain Range CH1, CH2

GF2	Adr 0x04, bit 7:3
Code	Factor
0x00	1.00
0x01	1.06
...	$6.25^{\frac{GF2}{31}}$
0x1F	6.25

Table 24: Fine Gain Factor CH2

GF1	Adr 0x06, bit 2:0, Adr 0x05, bit 7:4
Code	Factor
0x00	1.0
0x01	1.015
...	$6.25^{\frac{GF1}{124}}$
0x7F	6.53

Table 25: Fine Gain Factor CH1

Offset Calibration CH1, CH2

In order to calibrate the offset the reference source must first be selected using VOS12. Two fixed voltages and two dependent sources are available for this purpose. The fixed voltage sources should be selected for external sensors which provide stable, self-regulating signals.

So that photosensors can be operated in optical encoders iC-MQ tracks changes in offset voltages via the signal-dependent source VDC when used in conjunction with the controlled sensor current source for LED supply (pin ACO). The VDC potential automatically tracks higher DC photocurrents. To this end intermediate potentials VDC1 and VDC2 must be adjusted to a minimal AC ripple using the selectable k factor (this calibration must be repeated when the gain setting is altered). The ideal DC voltage level of 0.125 V to 0.25 V is selected via input resistor Rui().

The feedback of pin voltage V(ACO) fulfills the same task as source VDC when MR bridge sensors are supplied by the controlled sensor current source. In this instance the VDC sources do not need adjusting.

VOS12	Adr 0x0E, bit 5:4
Code	Source
0x0	$0.05 \cdot$ V(ACO)
0x1	0.5 V
0x2	0.25 V
0x3	VDC (VDC1 for CH1, VDC2 for CH2)

Table 26: Offset Reference Source CH1, CH2

VDC1	Adr 0x07, bit 4:0; Adr 0x06, bit 7
VDC2	Adr 0x08, bit 6:1
Code	$VDC = k \cdot VPi + (1 - k) \cdot VNi$
0x00	$k = 0.33$
0x01	$k = 0.335$
...	$k = 0.33 + VDCi \cdot 0.0052$
0x3F	$k = 0.66$

Table 27: Intermediate Voltages CH1, CH2

The offset calibration range for CH1 and CH2 is dependent on the selected VOS12 source and is set using OR1 and OR2. Both sine and cosine signals are then calibrated using factors OF1 and OF2. The calibration target is reached when the DC fraction of the differential signals PCHi versus NCHi is zero.

OR1	Adr 0x09, bit 0; Adr 0x08, bit 7
OR2	Adr 0x0A, bit 5:4
Code	Range
0x0	x1
0x1	x2
0x2	x6
0x3	x12

Table 28: Offset Range CH1, CH2

OF1	Adr 0xA, bit 3:0; Adr 0x9, bit 7:4		
OF2	Adr 0xC, bit 0; Adr 0xB, bit 7:1		
Code	Factor	Code	Factor
0x00	0	0x80	0
0x01	0.0079	0x81	-0.0079
...	$0.0079 \cdot OFi$	...	$-0.0079 \cdot OFi$
0x7F	1	0xFF	-1

Table 29: Offset Factors CH1, CH2

Phase Correction CH1 vs. CH2

The phase shift between CH1 and CH2 can be adjusted using parameter PH12. Following phase calibration other calibration parameters may have to be adjusted again (those as amplitude compensation, intermediate potentials and offset voltages).

PH12	Adr 0xD, bit 2:0; Adr 0xC, bit 7:5		
Code	Correction angle	Code	Correction angle
0x00	+0	0x20	-0
0x01	+0.65	0x21	-0.65
...	$+0.65 \cdot PH12$	...	$-0.65 \cdot PH12$
0x1F	+20.2	0x3F	-20.2

Table 30: Phase Correction CH1 vs. CH2

Signal Conditioning Examples

1. Photodiode array connected to current inputs, LED supply with constant current source

Step	Operating Mode	Calibration and Signal
1.		Presets VOS12= 0x3, GF1= 0x40, VDC1= 0x20, OF1= 0x0, GF2= 0x10, VDC2= 0x20, OF2= 0x0 Example: LED current approx. 6.25 mA ADJ(8)= 1 (constant current source), ADJ(6:5)= 11 (range 50 mA), ADJ(4:0)= 0x04 (value 12.5)
2.	*Calibration 2*	Calibration of Channel 1: Parameter GR12: Adjust diff. signal at PA vs. NA to approx. 1 Vpp amplitude Parameter GF1: Adjust diff. signal at PA vs. NA to exactly 1 Vpp amplitude Parameter VDC1: Minimization of VDC1 AC fraction at output PZ (ripple < 10 mVpeak) Parameter OR1, OF1: Calibration of DC fraction to zero for diff. signal PA vs. NA (< 5 mVdc)
3.	*Calibration 2*	Calibration of Channel 2: Parameter GF2: Adjust diff. signal at PB vs. NB to exactly 1 Vpp amplitude Parameter VDC2: Minimization of VDC2 AC fraction at ouput NZ (ripple < 10 mVpeak) Parameter OR2, OF2: Calibration of DC fraction to zero for diff. signal PB vs. NB (< 5 mVdc)
4.	*System Test*	1. Iteration, Calibration of Channel 1 vs. Channel 2: Parameter OF1: Adjust duty ratio of A_4 at PA to 50 % Parameter OF2: Adjust duty ratio of B_4 at PB to 50 % Parameter PH12: Adjust duty ratio of A_8 at NA to 50 % Parameter GF1: Adjust duty ratio of B_8 at NB to 50 %
5.	*Calibration 2*	Repeated Adjustment of Intermediate Voltages, VDC1 and VDC2: Parameter VDC1: Minimization of VDC1 AC fraction at ouput PZ Parameter VDC2: Minimization of VDC2 AC fraction at ouput NZ
6.	*System Test*	2. Iteration, Calibration of Channel 1 vs. Channel 2: Parameter OF1: Adjust duty ratio of A_4 at PA to 50 % Parameter OF2: Adjust duty ratio of B_4 at PB to 50 % Parameter PH12: Adjust duty ratio of A_8 at NA to 50 % Parameter GF1: Adjust duty ratio of B_8 at NB to 50 %

Table 31: Conditioning example 1

2. Encoder supplying 100 mVpp to voltage inputs

Step	Operating Mode	Calibration and Signal
1.		Presets VOS12= 0x1, GF1= 0x40, OF1= 0x0, GF2= 0x10, OF2= 0x0
2.	*Calibration 2*	Calibration of Channel 1: Parameter GR12: Adjust diff. signal at PA vs. NA to approx. 1 Vpp amplitude Parameter GF1: Adjust diff. signal at PA vs. NA to exactly 1 Vpp amplitude Parameter OR1, OF1: Calibration of DC fraction to zero for diff. signal PA vs. NA (< 5 mVdc)
3.	*Calibration 2*	Calibration of Channel 2: Parameter GF2: Adjust diff. signal at PB vs. NB to exactly 1 Vpp amplitude Parameter OR2, OF2: Calibration of DC fraction to zero for diff. signal PB vs. NB (< 5 mVdc)
4.	*System Test*	Calibration of Channel 1 vs. Channel 2: Parameter OF1: Adjust duty ratio of A_4 at PA to 50 % Parameter OF2: Adjust duty ratio of B_4 at PB to 50 % Parameter PH12: Adjust duty ratio of A_8 at NA to 50 % Parameter GF1: Adjust duty ratio of B_8 at NB to 50 %

Table 32: Conditioning example 2

SIGNAL CONDITIONING CH0

The voltage signals needed to calibrate the zero channel are available in mode *Calibration 1*. The relative phase position of the ungated zero signal Zin compared to A and B can be determined in mode *System Test*.

Gain Settings CH0

Parallel to the conditioning process for the CH1 and CH2 signals the CH0 gain is also set in the following steps:

1. The sensor supply controller is shut down and the constant current source for the ACO output set to the same output current as in the calibration of CH1 and CH2 (register ADJ; current value close to the later operating point).

2. The coarse gain is selected so that a differential signal amplitude of ca. 1 Vpp is produced internally (signal PCHi versus NCHi).

3. GF0 then permits fine gain adjustment to 1 Vpp. The total gain is accrued from GR0 x GF0.

GR0	Adr 0x11, bit 2:0	
Code	Range RIN0 = 0x9	Range RIN0 ≠ 0x9
0x0	0.5	2.0
0x1	1.0	4.1
0x2	1.3	5.3
0x3	1.7	6.7
0x4	2.2	8.7
0x5	2.6	10.5
0x6	3.3	13.2
0x7	4.0	16.0

Table 33: Gain Range CH0

GF0	Adr 0x11, bit 7:3
Code	Factor
0x00	1.00
0x01	1.06
...	$6.25^{\frac{GF0}{31}}$
0x1F	6.25

Table 34: Fine Gain Factor CH0

Offset Calibration CH0

To calibrate the offset the reference source must first be selected using VOS0 (see Offset Calibration CH1 and CH2 for further information). For the CH0 path the dependent source VDC is identical to source VDC1.

VOS0	Adr 0x13, bit 5:4
Code	Source
0x0	0.05 · V(ACO)
0x1	0.5 V
0x2	0.25 V
0x3	VDC (i.e. VDC1)

Table 35: Offset Reference Source CH0

OR0	Adr 0x12, bit 1:0
Code	Range
0x0	x1
0x1	x2
0x2	x6
0x3	x12

Table 36: Offset Range CH0

OF0	Adr 0x12, bit 7:2		
Code	Factor	Code	Factor
0x00	0	0x20	0
0x01	0.0322	0x21	-0.0322
...	0.0322 · OF0	...	-0.0322 · OF0
0x1F	1	0x3F	-1

Table 37: Offset Factor CH0

SIGNAL LEVEL CONTROL and SIGNAL MONITORING

Via the controlled sensor current source (pin ACO) iC-MQ can keep the input signals for the internal sine-to-digital converter constant regardless of temperature and aging effects by tracking the sensor supply.

Both the controller operating range and input signal amplitude for the controller are monitored and can be enabled for error messaging. A constant current source can be selected for the ACO output when setting the signal conditioning; the current range for the highside current source is adjusted using ADJ(6:5).

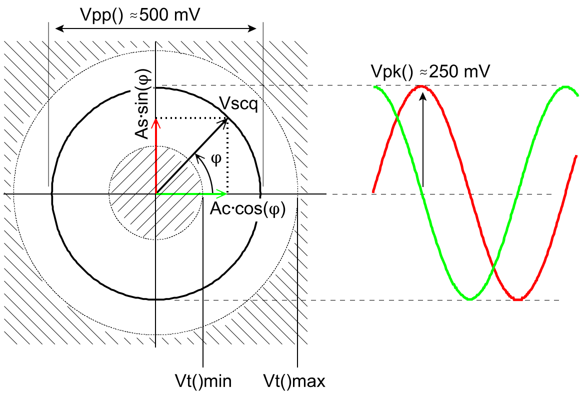


Figure 5: Internal signal level monitoring and test signals in *Calibration 2* mode (example for ADJ(8:0) = 0x19; see Elec. Char. Nos. 605 and 606 regarding Vt()min and Vt()max).

ADJ (8:7)	Adr 0x10, bit 7:6
Code	Function
00	Sine/cosine square control
01	Sum control
10	Constant current source
11	Not permitted (device test only)

Table 38: Controller Operating Modes

ADJ (6:5)	Adr 0x10, bit 5:4
Code	Function
00	5 mA - Range
01	10 mA - Range
10	25 mA - Range
11	50 mA - Range

Table 39: ACO Output Current Range (applies for control modes and constant current source)

ADJ (4:0)	Adr 0x10, bit 3:0; Adr 0x0F, bit 7
Code	**Square control** ADJ(8:7) = 00
0x00	Vpp() ca. 300 mV (60 %)
0x01	Vpp() ca. 305 mV (61 %)
...	Vpp() $\approx 300\,mV\,\frac{77}{77-(1.25*Code)}$
0x19	Vpp() ca. 500 mV (98 %)
...	...
0x1F	Vpp() ca. 600 mV (120 %)

Table 40: Internal Sin/Cos Signal Amplitude For Square Control

In operation with the active square control mode ADJ(4:0) sets the internal signal amplitudes according to the relation (PCH1-NCH1)² + (PCH2-NCH2)²; these should be set to 0.25 Vpk.

ADJ (4:0)	Adr 0x10, bit 3:0; Adr 0x0F, bit 7
Code	**Sum control** ADJ(8:7) = 01
0x00	VDC1 + VDC2 ca. 245 mV
0x01	VDC1 + VDC2 ca. 249 mV
...	VDC1 + VDC2 $\approx 245mV\,\frac{77}{77-(1.25*Code)}$
0x1F	VDC1 + VDC2 ca. 490 mV

Table 41: DC Setpoint For Sum Control

ADJ (4:0)	Adr 0x10, bit 3:0; Adr 0x0F, bit 7
Code	**Constant current source** ADJ(8:7) = 10
0x00	I(ACO) ca. 3.125% Isc(ACO)
0x01	I(ACO) ca. 6.25% Isc(ACO)
...	I(ACO) $\approx 3.125\% * (Code + 1) * \; Isc(ACO)$
0x1F	I(ACO) ca. 100% Isc(ACO)
Notes	See Elec. Char. No. 602 for Isc(ACO)

Table 42: I(ACO) With Constant Current Source

SINE-TO-DIGITAL CONVERSION

iC-MQ's converter resolution can be set using SELRES. For a resolution of 4, four angle steps per input signal period are generated so that the switching frequency at the A and B output matches the sine frequency at the input.

The programmable converter hysteresis is determined by SELHYS. It is set in multiples of the increment size and may have a maximum of 45° of the input signal period.

SELRES	Adr 0x1C, bit 6:0; Adr 0x1B, bit 7:0		
Value	STEP Angle Steps Per Period	IPF Interpolation Factor	fin()max Permissible Input Frequency (MTD=0x8)
0x00E0	4	1	500 kHz
0x01B0	8	2	500 kHz
0x02A0	12	3	200 kHz
0x0398	16	4	200 kHz
0x0414	20	5	200 kHz
0x0590	24	6	166 kHz
0x078C	32	8	125 kHz
0x090A	40	10	100 kHz
0x0B88	48	12	83 kHz
0x0F86	64	16	62.5 kHz
0x1305	80	20	50 kHz
0x1784	96	24	40 kHz
0x1804	100	25	40 kHz
0x1F83	128	32	30 kHz
0x2F82	192	48	20 kHz
0x3102	200	50	20 kHz
0x5F81	384	96	10 kHz
0x6301	400	100	10 kHz

Table 43: Converter Resolution

SELHYS	Adr 0x1D, bit 3:0
Code	Function
0x0	Nearly no hysteresis
0x1	1 increment (≈ 0.9°)
0x2	2 increments (≈ 1.8°)
0x3-0xD	3-13 increments (≈ 2.7°-11.7°)
0xE	SELRES(6:1) increments (0.5 LSB)
0xF*	SELRES(6:0) increments
Notes	*) Not permissible with SELRES = 0x00E0

Table 44: Converter Hysteresis

OUTPUT SETTINGS AND ZERO SIGNAL

The set interpolation factor IPF determines the number of A/B signal cycles generated internally which are counted via register POS to enable the positioning of the zero pulse. At a sine/cosine phase angle of zero degree the A/B cycle count starts at POS = 0, and the highest cycle count is reached when POS_{max} = IPF-1. The internal A/B signal cycle adheres to the following pattern:

A	1	1	0	0
B	1	0	0	1

Table 45: Internal A/B Signal Cycle

Inversions and reversals can be selected for the output of the A/B/Z signals and any logic combination for the output of the zero signal. The output logic pairs parameters CFGABZ in accordance with the table below:

CFGABZ	Adr 0x19, bit 7:0
Bit	Function and Description
7	Output inversion for channel A: PA<>NA PA = P1i xor CFGABZ(7)
6	Output inversion for channel B: PB<>NB PB = P2i xor CFGABZ(6)
5	Output inversion for index channel: PZ<>NZ PZ = P0i xor CFGABZ(5)
4	Exchange of A/B signal assignation 0: P1i = A, P2i = B 1: P1i = B, P2i = A
	Zero Signal Logic CFGABZ(3:0)
3	Enable for A = 1, B = 1
2	Enable for A = 1, B = 0
1	Enable for A = 0, B = 0
0	Enable for A = 0, B = 1

Table 46: Output Logic

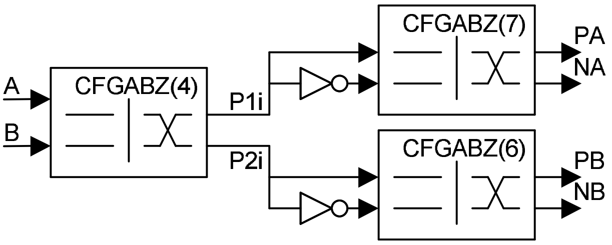


Figure 6: Signal Path from A and B to PA/NA and PB/NB

Zero Signal Generation
The generation of the zero signal is dependant on the internal enable signal Z_{In} which is produced by comparing the processed X1 and X2 input signals. The offset calibration of CH0 influences the width of the enable signal so that the correct position of Z_{In} should be checked before the zero signal logic is configured. In *Mode ABZ* this is possible at the error signal output (pin ERR; required settings are EMASKA = 0x010 and EMTD = 0x0).

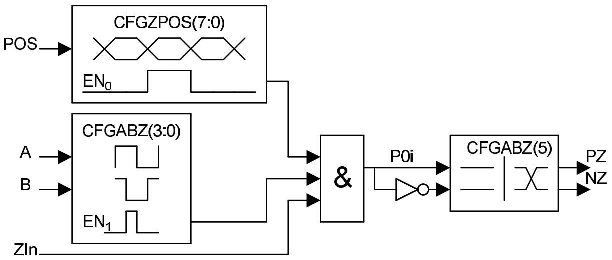


Figure 7: Signal path from Z_{In} to PZ/NZ

The positioning of the zero signal by CFGZPOS is relative to the internal A/B cycle count POS. A cycle must be selected across which enable signal Z_{In} is centered as far as is possible. For cycle counts which cannot be achieved due to a smaller interpolation factor no zero signal is generated.

CFGZPOS	Adr 0x1A, bit 7:0
Bit	Description
7	Mask Enable (zero signal position determined by POS)
(6:0)	POS = A/B cycle count nl (releases zero signal output)

Table 47: Zero Signal Positioning

ENZFF	Adr 0x02, bit 4
Bit	Description
0	Zero signal output with state change of P0i
1	Zero signal output synchronized with A/B signal

Table 48: Zero Signal Synchronization

Description Of CFGABZ Setup

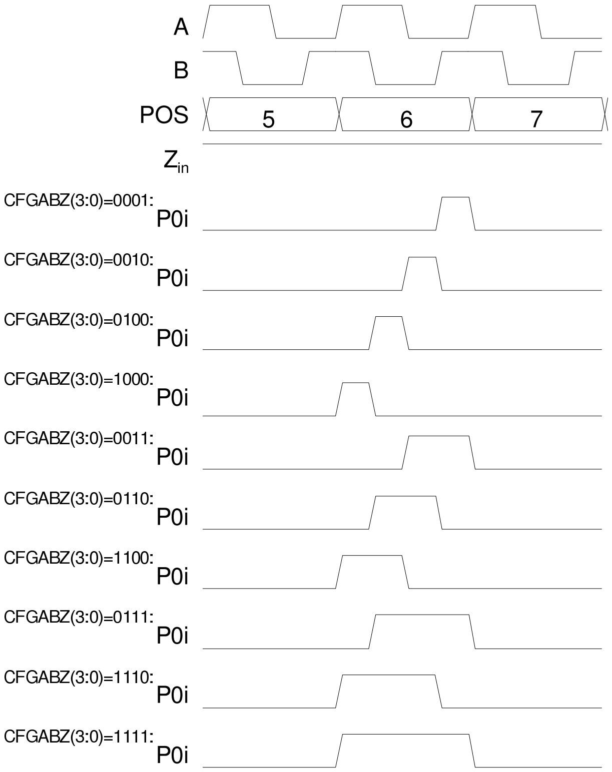


Figure 8: Function of zero signal logic CFGABZ(3:0) (Example for CFGZPOS(7)=1, CFGZPOS(6:0)=0x6)

Setup Example 1
Incremental ABZ output with a zero signal of 180° synchronous with the A signal at PA:
CFGABZ = "0000 1100"

Setup Example 2
Incremental ABZ output with a zero signal of 270° which can be synchronized externally with a 90° zero pulse for PA = 1 und PB = 1:
CFGABZ = "1100 0111"

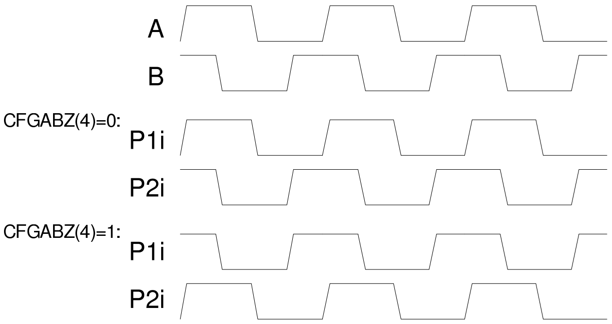


Figure 9: Function of CFGABZ(4)

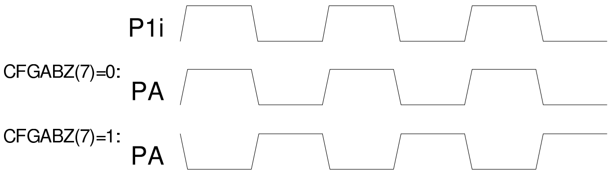


Figure 10: Function of CFGABZ(7)

Output Driver Configuration

The output drivers can be used as push-pull, lowside or highside drivers; the mode of operation is determined by TRIHL(1:0).

In order to avoid steep edges when transmitting via short wires the slew rate can be set using SSR to suit the length of the cable. This can result in a limiting of the maximum permissible output frequency if at the same time the RS422 specification is to be adhered to (for example, to 300 kHz at a slew rate of 300 ns; the tolerances in Electrical Characteristics, numbers 506/507, must be observed).

The driver output short-circuit current can be set by SIK and can be minimized when connecting to logic or to an external 24 V line driver. If the outputs are used as RS422-compatible 5 V drivers, it is recommended that SIK = 11 to keep the power dissipation of iC-MQ low.

TRIHL	Adr 0x1E, bit 1:0
Code	Function
00	Push-pull operation
01	Highside driver mode (P channel open drain)
10	Lowside driver mode (N channel open drain)
11	Not permitted

Table 49: Output Drive Mode

SSR	Adr 0x1E, bit 3:2
Code	Function
00	Nominal value 12 ns
01	Nominal value 25 ns
10	Nominal value 80 ns
11	Nominal value 220 ns
Note	See Elec. Char. Nos. 506/507

Table 50: Output Slew Rate

SIK	Adr 0x1E, bit 5:4
Code	Function
00	typ. 2 mA, linking logic or driver ICs
01	typ. 8 mA
10	typ. 40 mA
11	typ. 100 mA, recommended for RS422
Note	See Elec. Char. Nos. 503/504

Table 51: Output Short-Circuit Current

Minimum Phase Distance

The minimum phase distance for A/B/Z and CPD/CPU/CP output signals can be preselected using MTD(3:0). This setting limits the maximum possible output frequency for safe transmission to counters which cannot debounce spikes or only permit a low input frequency.

When preselecting the minimum edge distance the configuration of the RS422 output drivers (with regard to the driver current and slew rate) and the length of cable used must be taken into account.

MTD	Adr 0x1D, bit 7:4	
Code	*Mode ABZ*: t_{MTD}	*Mode 191/193: tclk()lo*
0x0	220 ns	110 ns
0x1	410 ns	205 ns
0x2	600 ns	300 ns
0x3	800 ns	400 ns
0x4	1.0 µs	500 ns
0x5	1.2 µs	600 ns
0x6	1.4 µs	700 ns
0x7	1.6 µs	800 ns
0x8	220 ns	50 ns
0x9	410 ns	50 ns
0xA	600 ns	50 ns
0xB	800 ns	50 ns
0xC	1.0 µs	50 ns
0xD	1.2 µs	50 ns
0xE	1.4 µs	50 ns
0xF	1.6 µs	50 ns
Note	All timing specifications are nominal values, see Elec. Char. No. 515 for tolerances.	

Table 52: Minimum Phase Distance

ERROR MONITORING AND ALARM OUTPUT

iC-MQ monitors the input signals, the internal interpolator and the sensor supply controller via which the input signal levels are stabilized. If the sensor supply tracking unit reaches its control limits this can be interpreted as an end-of-life message, for example.

Three separate error masks stipulate whether error events are signaled as an alarm via the current-limited open drain I/O pin ERR (mask EMASKA), whether they cause the RS422 line drivers to shutdown or not (mask EMASKO) or whether they are stored in the EEPROM (mask EMASKE).

The display logic (via EPH) and the minimum alarm indication time (via EMTD) can be set for I/O pin ERR; an internal pull-up current source can be switched in via EPU. ERR pin also has an input function for switching iC-MQ to test mode (see page 33) and for the acceptance of a system error message in normal operation (only for EPH = 0).

EPH	Adr 0x15, bit 2
Code	Pin Logic
0	Low on error (otherwise Z)
1	Z on error (otherwise low)

Table 53: Alarm Input/Output Logic

EMTD	Adr 0x15, bit 5:3		
Code	Indication Time	Code	Indication Time
0x0	0 ms	0x4	50 ms
0x1	12.5 ms	0x5	62.5 ms
0x2	25 ms	0x6	75 ms
0x3	37.5 ms	0x7	87.5 ms

Table 54: Minimum Alarm Indication Time

EPU	Adr 0x17, bit 2
Code	Function
0	No internal pull-up active
1	Internal 300 µA pull-up current source active

Table 55: Pull-Up Enable for Alarm Output ERR

PDMODE	Adr 0x18, bit 6
Code	Function
0	Line driver active when no error persists
1	Line driver active only after cycling power

Table 56: Driver Activation

EMASKA	Adr 0x15, bit 1:0; Adr 0x14, bit 7:0
Bit	Error event
9	Line count error (wrong count of sine periods between two zero pulses)
8	Temporal tracking error (out-of-sync: position output differs from actual angle, e.g. after cycling power)
7	Loss of tracking (excessive input frequency)
6	Configuration error* (SDA or SCL pin error, no acknowledge signal from EEPROM or invalid check sum)
5	Excessive temperature warning
4	Ungated index enable signal Z_{In} (comparated X1/X2 inputs for CFGABZ and CFGZPOS adjustment)
3	Control error 2: range at max. limit
2	Control error 1: range at min. limit
1	Signal error 2: clipping due to excessive input level
0	Signal error 1: loss of signal (poor input level or s/c phase out of range)
Code	Function
1	Enable: event will be displayed
0	Disable: event will not be displayed
Notes	*) The line drivers remain high impedance (tristate) when cycling power.

Table 57: Error Event Mask for Alarm Output

EMASKO	Adr 0x17, bit 1:0; Adr 0x16, bit 7:0
Bit	Error event
9	Line count error (wrong count of sine periods between two zero pulses)
8	Temporal tracking error (out-of-sync: position output differs from actual angle, e.g. after cycling power)
7	Loss of tracking (excessive input frequency)
6	Configuration error* (ROM bit with fixed value = 1) SDA or SCL pin error, no acknowledge signal from EEPROM or invalid check sum
5	Excessive temperature warning
4	System error: I/O pin ERR pulled to low by an external error signal (only permitted with EPH = 0)
3	Control error 2: range at max. limit
2	Control error 1: range at min. limit
1	Signal error 2: clipping due to excessive input level
0	Signal error 1: loss of signal (poor input level or s/c phase out of range)
Code	Function
1	Enable: event triggers tri-state
0	Disable: event does not cause tri-state
Notes	*) The line drivers remain high impedance (tristate) when cycling power.

Table 58: Error Event Mask for Driver Shutdown

Error Protocol

Out of the errors enabled by EMASKE both the first (under ERR1) and last error (under ERR2) which occur after the iC-MQ is turned on are stored in the EEPROM.

The EEPROM also has a memory area in which all occurring errors can be stored (ERR3). Only the fact that an error has occurred can be recorded, with no information as to the time and count of appearance of that error given. Error recording can be used to statistically evaluate the causes of system failure, for example.

EMASKE	Adr 0x18, bit 5:0; Adr 0x17, bit 7:4
Bit	Error event
9	Line count error (wrong count of sine periods between two zero pulses)
8	—
7	Loss of tracking (excessive input frequency)
6	—
5	Excessive temperature warning
4	System error: I/O pin ERR reads low by an external error signal (only permitted with EPH = 0)
3	Control error 2: range at max. limit
2	Control error 1: range at min. limit
1	Signal error 2: clipping due to excessive input level
0	Signal error 1: loss of signal (poor input level or s/c phase out of range)
Code	Function
1	Enable: event will be latched
0	Disable: event will not be latched

Table 59: Error Event Mask for EEPROM Savings

ERR1 **ERR2** **ERR3**	Adr 0x31, bit 1:0; Adr 0x30, bit 7:0 Adr 0x32, bit 3:0; Adr 0x31, bit 7:2 Adr 0x33, bit 5:0; Adr 0x32, bit 7:4
Bit	Error Event
6:0	Assignation according to EMASKE
Code	Function
0	No event
1	Registered error event

Table 60: Error Protocol

Line Count Error

The line count error feature is particularly interesting for encoder systems. The disc is checked anew with each zero pulse, with the number of sine cycles counted until the next zero pulse occurs. If the direction of rotation is changed, the check is aborted.

The line count is then stored under LINECNT minus 1, i.e. for a code disc with 256 lines LINECNT records a value of 255. If the counted line number does not match the number already stored in LINECNT, a line count error is set. In mode System Test signal TP1 indicates when the line count check is first ended.

Temperature Monitoring

If the temperature warning threshold is exceeded an excessive temperature message is generated which is processed in the temperature monitor block (T_w corresponds to T_2).

Exceeding the temperature warning threshold can be signaled at pin ERR or used to shut down the line drivers (via mask EMASKO). The temperature warning is deleted when the temperature drops below T_w $-\mathrm{T}_{hys}$.

If the temperature shutdown threshold $T_{off} = T_w + \Delta T$ is exceeded the line drivers are shut down independent of EMASKO.

REVERSE POLARITY PROTECTION

iC-MQ is protected against a reversal of the supply voltage and has short-circuit-proof, error-tolerant line drivers. A defective device cable or one wrongly connected is tolerated by iC-MQ. All circuitry components which draw the monitored supply voltage from VDDS and GNDS are also protected.

The following pins are also reverse polarity protected: PA, NA, PB, NB, PZ, NZ, ERR, VDD, GND and ACO.

Conditions: This is based on the condition that GNDS only receives load currents from VDDS. The maximum voltage difference between GNDS and another pin should not exceed 6 V, the exception here being pin ERR (see *Test Mode* page 33).

TEST MODE

iC-MQ switches to test mode when a voltage greater than VTMon is applied to pin ERR (precondition: EMODE(0) = 1). In response iC-MQ transmits its setup settings as current-modulated data using error signal I/O pin ERR either directly from the RAM (for EMODE2 = 1) or after re-reading the EEPROM (for EMODE2 = 0). Should the voltage at the ERR pin fall below VTMoff test mode is terminated and data transmission aborted.

The clock rate for the data output is determined by ENFAST. Two clock rates can be selected: 780 ns for ENFAST = 1 or 3.125 µs for ENFAST = 0 (see Electrical Characteristics, B12, for clock frequency and tolerances).

Data is output in Manchester code via two clock pulses per bit. To this end the lowside current source switches between a Z state (OFF = 0 mA) and an L state (ON = 2 mA).

The bit information lies in the direction of the current source switch:
Zero bit: change of state Z → L (OFF to ON)
One bit: Change of state L → Z (ON to OFF)

Transmission consists of a start bit (a one bit), 8 data bits and a pause interval in Z state (the timing is identical with an EEPROM access via the I^2C interface).

Example: byte value = 1000 1010
Transmission including the start bit: 1 1000 1010
In Manchester code: LZ LZZL ZLZL LZZL LZZL

Decoding of the data stream:

ZZZZZZ LZ LZ ZL ZL ZL LZ ZL LZ ZL ZZZZZZ
Pause 1 1 0 0 0 1 0 1 0 Pause

EMODE	Adr 0x15, bit 7:6	
Code	Function during test mode	Function following test mode
00	Normal operation	Normal operation
01	Transmission of error and OEM data*	Repeated read out of EEPROM
10	Normal operation	Repeated read out of EEPROM
11	Transmission of EEPROM contents (0x0-0x7F)	Repeated read out of EEPROM
Notes	*) Selectable address ranges: EMODE2 = 0: EEPROM addresses 0x24 to 0x7F EMODE2 = 1: RAM addresses 0x3B to 0x43	

Table 61: Test Mode

EMODE2	Adr 0x18, bit 7	
Code	Register selection	Address range for EMODE = 01
0	Reading/sending external configuration data (DEVID is device address)	EEPROM address range 0x24-0x7F
1	Sending internal configuration data (ENSL = 1)	RAM address range 0x3B-0x43

Table 62: Register And Address Selection For Test Mode

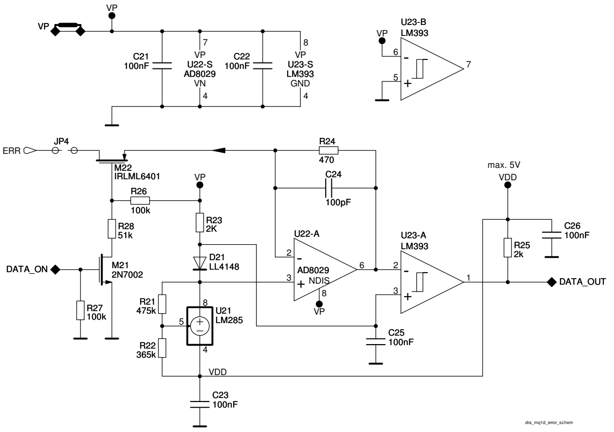


Figure 11: Example circuit for the decoding and conversion of the current-modulated signals to logic levels.

Quick programming in the single master system

For the purpose of signal conditioning it is possible to reprogram iC-MQ quickly. If test mode is quit and EMODE ≠ 00, iC-MQ reads the configuration data in again. In place of the standard EEPROM (DEVID 0x50) an EEPROM with a different device address can be read in which can be stored under DEVID (address 0x00, bit 6:0).

In operating modes *Mode ABZ*, *System Test* and *Mode 191/193* the content of the EEPROM is read in its entirety. For other modes the address area is limited to 0x0-0x31 so that the configuration time for either calibration or IC testing is shortened.

If the setup is switched to test mode during the readin procedure, readin is aborted and only repeated once test mode has been terminated.

Quick programming in the multimaster system

Fast programming of iC-MQ, byte for byte, is possible with a multimaster-competent programming device. To this end the integrated I^2C slave mode must be enabled by ENSL; iC-MQ then reacts to the device ID 0x55.

If no EEPROM is connected, iC-MQ automatically sets the I^2C slave mode enable (after a maximum of 150 ms, see Electrical Characteristics, D11) and deactivates the digital section (ENSL = 1 and END = 0 are set). Any number of bytes can be written at any one time; the received data is accepted directly into the RAM register. The conditions given in the following table must be taken into consideration here. After programming END = 1 must be set to restart sine-to-digital conversion in the selected mode of operation.

EXAMPLE APPLICATIONS

Figure 12 is a circuit diagram of an optical encoder with an incremental output of quadrature signals as RS422-compatible differential signals which can be terminated by 100 Ω at the controller end. By way of an alternative the magnetic encoder in Figure 13 uses magnetoresistive sensor bridges. An external overvoltage protection circuit may be realized employing TVS diodes plus a PolyFuse in the VDD line, for instance.

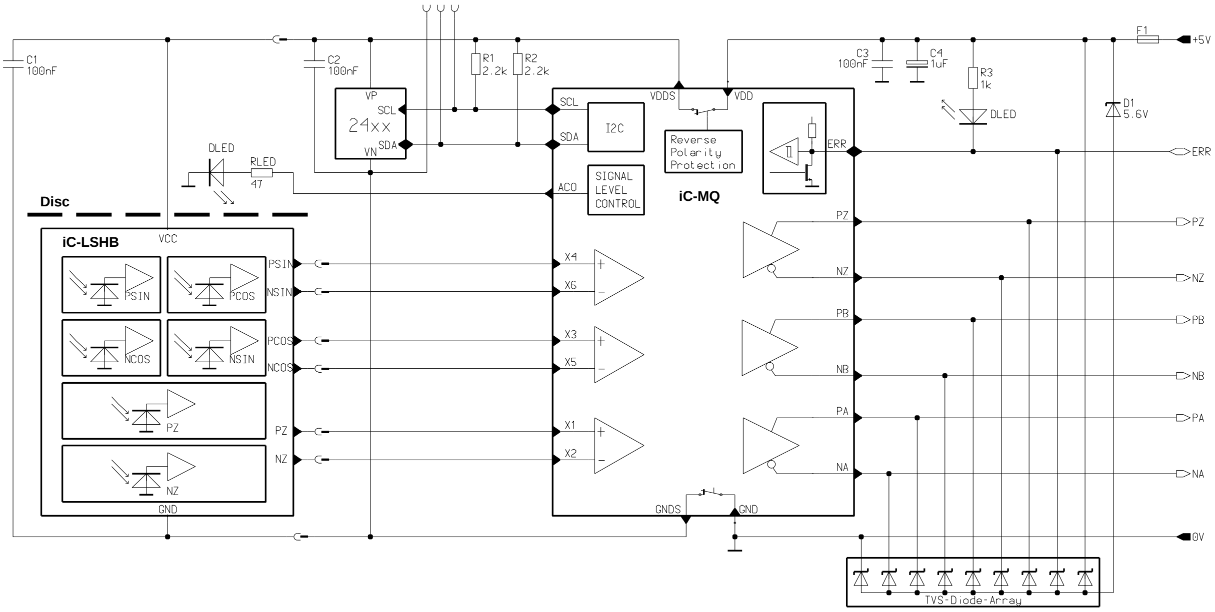


Figure 12: Example application with an optical encoder

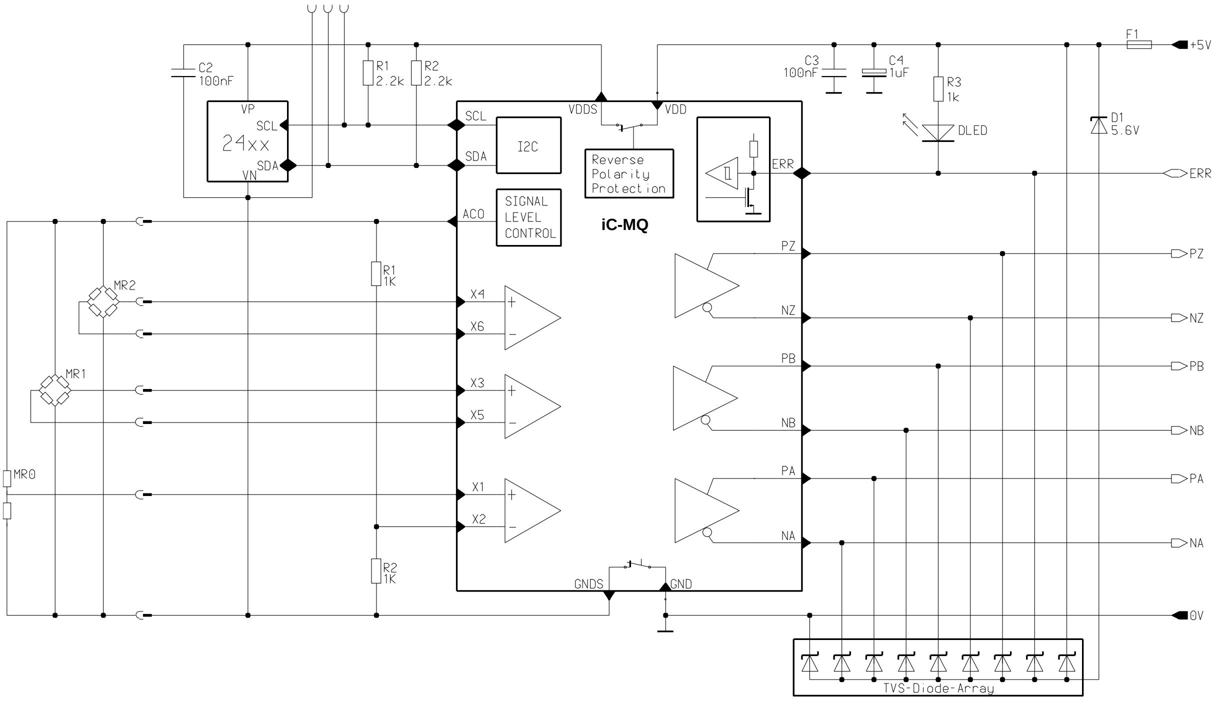


Figure 13: Example application with a magnetic encoder

When iC-MQ is used in 24 V systems, with supply voltages of 5 V to 30 V for example, it can be combined with iC-DL which acts as a line driver with an integrated line adaptation feature (Figure 14).

A reduced driving capability of iC-MQ is sufficient (SIK = 00) to operate iC-DL so that the current required is reduced at the 5 V end. If an LDO voltage regulator is selected, the circuit is suitable for a supply range of 4.5 V to 30 V without any changes having to be made.

The wiring of the iC-DL error message output (pin NER) to the PLC is not necessary if the iC-MQ error mask is set for output shutdown (EMASKO). In the event of error the pull-down current sources ensure that a low signal is produced at the iC-DL inputs on all lines which the controller recognizes as an error. If there is an overload at the outputs, via its temperature protection unit iC-DL itself makes sure that the driver outputs are shutdown (tristate) - which the controller also classes as an error. In addition iC-MQ can transmit the overload to the error memory as a system error when information is returned to the bidirectional I/O pin ERR (as shown).

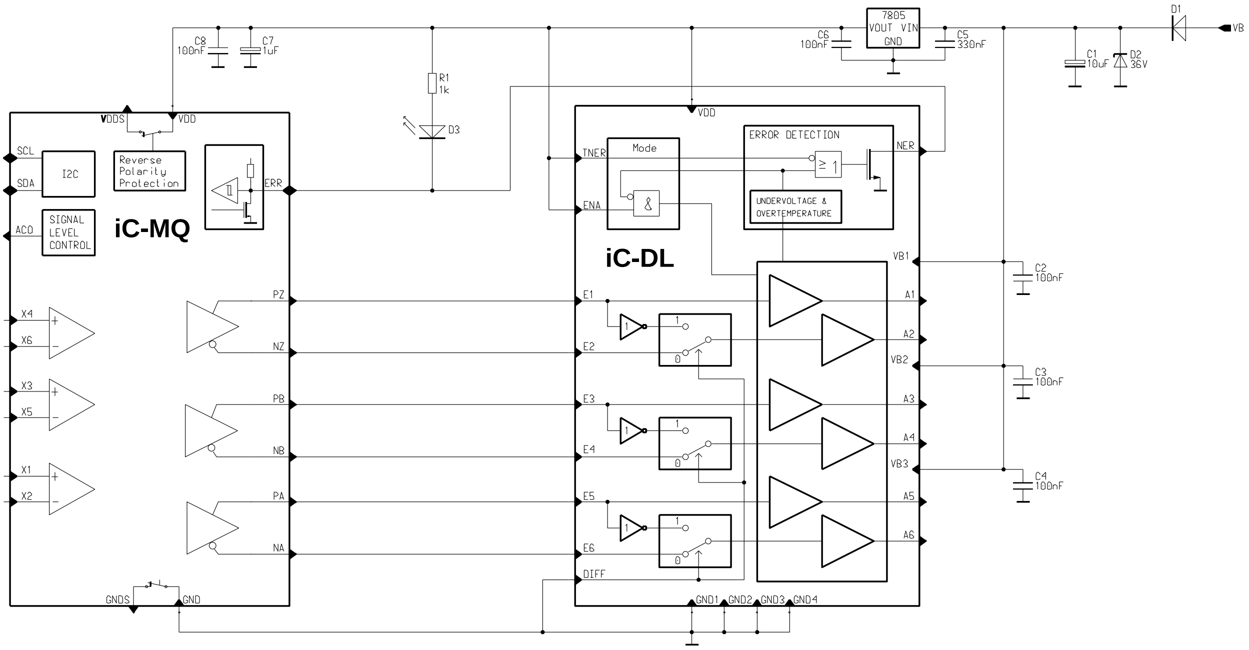


Figure 14: Example application with a 24 V line driver

APPLICATION HINTS

In-circuit programming of the EEPROM

Access to the EEPROM is unhindered when the iC-MQ supply voltage is kept below power down reset threshold VDDoff. In this case an EEPROM which operates at a supply voltage of 2.5 V and above is required. If 3.3 V are necessary to power the EEPROM, iC-MQ's supply voltage can be raised at a maximum to power on threshold VDDon; this must occur without overshooting.

The supply voltage provided by pins VDDS and GNDS can be used to power the EEPROM; shutdown only occurs with reverse polarity. Here, the load-dependent voltage drop at both switches must be taken into account; see Vs(VDDS) and Vs(GNDS) in the Electrical Characteristics, C01 and C02.

Absolute angle accuracy and edge jitter

The precise setting of the signal conditioning unit for correction of the analog input signals is crucial to the result of interpolation; the absolute angle error obtained determines the minimum signal jitter. Here, the effect on the transition distance of the A/B output signals is not always the same but instead dependent on the absolute phase angle of the input signals. The following gives an example for an interpolation factor of 100, i.e. 400 edges per sine period.

The offset error in the cosine signal has the strongest effect on the absolute angle error at 90° and 270°; at 0° and 180° its influence on the transition distance is the most marked. With a range setting of OR1 = OR2 = 00 and VOSSC = 01 the offset error can be compensated for by an increment of 3.9 mV. If the offset has been compensated for incorrectly by one step (1 LSB), the absolute angle error would increase by ca. 0.45° and the transition distance vary by approximately +/- 0.8 %. Similar conditions apply to the sine signal, with the sole difference that the maxima would be shifted by 90°.

An error in amplitude has the strongest effect on the absolute angle error at 45°, 135°, 225° and 315°; the biggest change in the transition distance can be observed at 0°, 90°, 180° and 270°. iC-MQ can compensate for the amplitude ratio in steps of 1.5 % so that incorrect compensation by 1 LSB would increase the absolute angle error by ca. 0.42°. The transition distance would then vary by +/- 1.5 %.

A phase error between the sine and cosine signals (a deviation in phase shift from the ideal 90°) has the most marked influence on the absolute angle error at 0°, 90°, 180° and 270°. The greatest effect on the transition distance is noted at 45°, 135°, 225° and 315°. iC-MQ's phase correction feature permits a step size of 0.64° so that incorrect compensation by 1 LSB would increase the absolute angle error by ca. 0.64°. The transition distance would then vary by +/- 1.1 %.

In a perfect signal conditioning procedure it can be assumed that the residual error constitutes half a compensation step respectively. With this, in theory iC-MQ would achieve an absolute angle accuracy of ca. 0.5°, with the transition distance varying by ca. +/- 1.5 %. The linearity error of the interpolator must also be taken into consideration; this increases the absolute angle error by ca. 0.12° and the variation in transition distance by 0.4 %. With ideal, almost static input signals iC-MQ then obtains an absolute angle accuracy of 0.62° and a variation in transition distance of under 2 %.

Information on the demo board

The default delivery status of demo board EVAL MQ1D is such that it expects differential sine/cosine signals at inputs X3 to X6 with an amplitude of 125 mV, i.e.

$$\begin{aligned} V(X4) &= 2.5\,V + 0.125\,V\sin(\varphi t) \\ V(X3) &= 2.5\,V - 0.125\,V\sin(\varphi t) \\ V(X5) &= 2.5\,V + 0.125\,V\sin(90 + \varphi t) \\ V(X6) &= 2.5\,V - 0.125\,V\sin(90 + \varphi t) \end{aligned}$$

Outputs PA, NA, PB and NB generate a differential A/B signal with an angle resolution of 4 (an interpolation factor of 1). When high sine input frequencies are applied or the resolution is increased, the minimum phase distance (MTD), short-circuit current limit (SIK) and driver slew rate (SSR) must be adjusted to meet requirements. For example, a minimum phase distance of MTD = 8 should be selected with a resolution of 200 (an interpolation factor of 50) when input frequencies of up to 20 kHz are to be applied.

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We understand suitable application of our published designs to be state-of-the-art technology which can no longer be classed as inventive under the stipulations of patent law. Our explicit application notes are to be treated only as mere examples of the many possible and extremely advantageous uses our products can be put to.

ORDERING INFORMATION

Type	Package	Order Designation
iC-MQ	TSSOP20	iC-MQ TSSOP20
Evaluation Board iC-MQ		iC-MQ EVAL MQ1D

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