Product Preview CMX7032 / CMX7042 AIS Data Processor

PP/703242/2

Marine AIS data processor designed for Limiter-Discriminator based RF systems

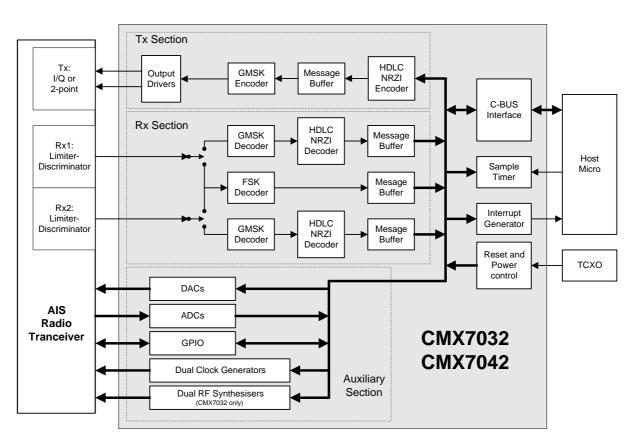
Features

- Half-Duplex GMSK and FSK Modem
- Marine AIS and DSC data formatting
- Flexible channel configuration:
 - o 2 channel simultaneous Rx
 - 1 channel Tx
- Optimal Co-channel performance
- Limiter-Discriminator Rx interface
- Auxiliary functions:
 - o 4 x (10bit) DACs
 - o 2 x (10bit) ADCs
 - o 2 x RF synthesisers (CMX7032 only)
- Supports Carrier-Sensing channel access (CSTDMA) operation
- Flexible Tx interface:
 - o I and Q or two-point modulation
 - Single and two-point modulation Tx outputs
- · C-BUS serial interface
- Flexible powersave modes
- Low power 3V to 3.6V operation
- Small VQFN and LQFP packaging
- Built on FirmASIC ® technology

Applications

- Automatic Identification System (AIS) for Marine Safety
 - Class B transponders
 - Rx only modules
 - o Tx only modules
 - o Aids-To-Navigation systems





System Overview Diagram



Brief Description

The CMX7032 and CMX7042 are highly integrated Baseband Signalling Processor ICs, that fulfil the requirements of the class B marine Automatic Identification System (AIS) transponder market, the general AIS Rx only market and Aids-to-Navigation requirements.

The AIS system allows vessels and base stations to communicate their position and other data to each other without the need for a centralised controller. This allows vessels to "see" each other and take appropriate action to avoid collision and so improve marine safety. The system uses a GMSK 9600baud data link in the Marine VHF frequency band. The system requirements are defined in ITU-M 1371-1 standard.

The CMX7032 and CMX7042 are specifically designed for use in AIS units utilising Limiter-Discriminator RF architecture. Both are half duplex in operation, comprising two parallel Limiter-Discriminator Rx paths and one I and Q or two-point modulation Tx path and configurable for AIS or marine DSC operation. The device performs signal modulation/demodulation with associated AIS functions, such as training sequence detection, NRZI conversion and HDLC processing (flags, bit stuffing/de-stuffing, CRC generate/check). Combined with the integrated Tx/Rx data buffers, the overall host μ C processing requirements are greatly reduced. Auxiliary ADCs and DACs functions are provided to further simplify the system hardware design, therefore, reducing the overall equipment size and cost. The CMX7032 and CMX7042 have identical core functionality. The CMX7032 provides maximum integration with the inclusion of two auxiliary RF synthesisers on chip. The CMX7042, without RF synthesisers, offers maximum RF system flexibility and the smallest foot-print package.

These devices utilise CML's proprietary FirmASIC ® component technology. On-chip sub-systems are configured by a Function ImageTM: this is a data file that is uploaded during device initialisation and configures the device's function and feature set. The Function ImageTM can be loaded automatically from an optional external EEPROM or from a host μ Controller over the built-in C-BUS serial interface. The device's functions and features can be enhanced by subsequent Function ImageTM releases, facilitating in-the-field upgrades.

The CMX910 (AIS class A and AIS class B processor) is also available from CML for designers preferring an I and Q modulation approach to RF design.

Resources

- CMX7032 Marine AIS data processor including two RF synthesisers (CMX7032Q1 – 64 pin VQFN package, CMX7032L9 – 64 pin LQFP package)
- CMX7042 Marine AIS data processor (CMX7042Q3 – 48 pin VQFN package, CMX7042L4 – 48 pin LQFP package)
- PE0001 Universal interface board CMX7034/CMX7042 GUI program from the CML Technical Portal (MyCML)
- PE0201 CMX703x series Evaluation board
- PE0401 CMX704x series Evaluation board
- Product Preview
- Datasheet and User manual
- Function Image™ FI-1.0



Tx Modem Functions

- Configurable modulation type
 - AIS 25kHz channel (GMSK, 9600bps, 2.4kHz deviation, BT = 0.4)
- AIS Burst mode with full AIS frame formatting (HDLC-type)
 - Bit stuffing
 - o NRZI coding
 - Training sequence and start/stop flag insertion
 - CRC generation
- AIS Raw mode (for greater flexibility)
 - o Supports arbitrary data streams for user-defined protocols
- Full support for the AIS Class B carrier-sensing channel access scheme (CS-TDMA)
- Full support for the AIS Class B Self-organising TDMA access scheme
- 160 byte (equivalent to 5 AIS slots) Tx data buffer
- Flexible Tx Interface
 - o Two-point modulation outputs, with independent gain and polarity controls
 - o I and Q modulation outputs, for use with an IQ up-converter

Rx Modem Functions

- Configurable modulation format:
 - o AIS 25kHz channel (GMSK, 9600bps, 2.4kHz deviation, BT = 0.4)
 - o DSC (de-emphasised FSK, 1200bps)
- Simultaneous reception of two AIS channels, or one AIS and one DSC channel
- AIS Burst mode with full AIS frame formatting (HDLC-type)
 - o Frame sync recognition
 - o Bit de-stuffing
 - o NRZI decoding
 - o Training sequence and start/stop flag detection
 - CRC checking
- AIS Raw mode (for greater flexibility)
 - o Supports arbitrary data streams for user-defined protocols
- DSC reception supported in raw mode
- Four 160 byte Rx data buffers can automatically store up to four 5-slot AIS bursts (2 per Rx channel)
- Rx signal input gain and polarity controls
- Time-of-arrival reporting assists with timekeeping in the absence of GPS

RF Synthesizers 100 – 600 MHz (Only available on the CMX7032)

- Two Integer-N synthesizers
- Flexible design minimizes reference spurs for low phase noise results
- Charge pump
 - o High/low soft selectable current setting to speed large frequency channel changes
 - Nominal current user defined by external resistor value
- Lock detect

Analogue I/O Functions

- Auxiliary ADC system
 - o Two 10-bit successive approximation ADCs with integrated sample and hold.
 - One Aux ADC is dedicated to RSSI measurement in a user defined window, the other is available for general use.
- Ramping auxiliary DAC
 - DAC sequences through a user-configured sequence of DAC output values to develop a specific rising/falling DAC output signal. This is useful for ramping an RF PA, and can be configured to happen automatically at the start and end of a burst.
 - Can operate as a general purpose DAC, if desired.
- Three general purpose auxiliary DACs



System Functions

- All internal subsystems are controlled via a single serial host interface to reduce host μC pin count and simplify external host driver complexity.
- Transaction oriented command/response logical host interface executes tasks supporting normal operation, device configuration, and functions to assist manufacturing calibration trimming of external circuits.
- Internal system clock derived from RF synthesizer reference oscillator and eliminates the need for additional XTAL or baseband clock oscillator.
- Two user programmable auxiliary clock synthesisers generate clocks for external system use and eliminate the need of multiple external clock sources.
- User selected method for loading a Function Image[™] either from the host µC via C-BUS or from an optional external serial EEPROM.
- Integrated regulator supplies all internal voltages from a single 3.3V regulated supply.
- Powersave facilities minimize total system power.

AIS system formats

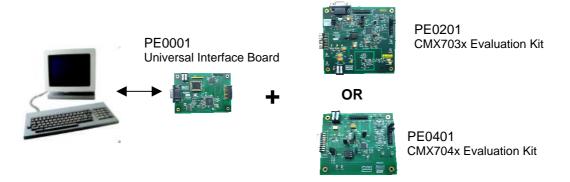
The AIS system uses two basic channel access mechanisms – Self Organising Time Division Multiple Access (SOTDMA) and Carrier-Sensing Time Division Multiple Access (CSTDMA). The CMX7032 is compatible with both systems and offers additional features, which simplify the implementation of CSTDMA. The SOTDMA system is detailed in ITU-M 1371-1 and IEC 61993-2 while the CSTDMA is detailed in IEC 62287.

The CSTDMA system is used in the implementation of the Class B AIS. This requires the Receiver to monitor the first part of a slot for an existing AIS transmission from another station before deciding to use the slot for its own transmission or aborting and selecting a different slot.

The SOTDMA system is used in the Class A and Base Station AIS as well as the Class B-SOTDMA AIS standard.

Product Support

An evaluation support package is available to assist with the design-in process. The PE0001 is a universal interface board for connection of the target device evaluation board PE0201 or PE0401 to a standard PC, for quick and easy evaluation of the desired product. A specific GUI program is available for down load from the CML Technical Portal (MyCML at www.cmlmicro.com) for use with the PE0001. The PE0201 and PE0401 boards are specific to the CMX7032 and CMX7042 devices, respectively.







About FirmASIC®

CML's proprietary *FirmASIC*[™] component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC* [®] combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC* [®] device are determined by uploading its Function Image[™] during device initialisation. New Function Images[™] may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC* [®] devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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