

C-13-2500/C-FDFB-SLC2



Features

- Duplex LC Single Mode Transceiver
- Small Form Factor Multi-sourced 2x5 Pin Package
- 1310nm, DFB Laser
- SONET /SDH STM-16 Compliant
- Single +3.3V Power Supply
- LVPECL/CML Differential level Inputs and Outputs
- LVTTTL or LVPECL logic level signal-detect output choice
(C-13-2500-FDFB-SLC for LVPECL and C-13-2500C-FDFB-SLC for LVTTTL)
- LVTTTL disable input
- Temperature Range: 0 to 70° C
- Class 1 Laser International Safety Standard IEC 825 Compliant
- Complies with Bell Core TA-NWT-000983

General Operating

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.135	3.3	3.465	V
Total Current	I_{cc}			300	mA
Inrush Current	I_{cc}'			30	mA
Power Supply Noise Rejection ^a		100			mV _{p-p}
Operating Temperature (case)	T_{op}	0		70	°C
Storage Temperature	T_{st}	-40		85	°C
Data Rate OC48/STM-16	DR		2488		Mb/s

a) 20Hz to 155MHz

Transmitter Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Optical Power	P_{op}	-5		0	dBm
Average Launch power of off Tx	P_{off}			-30	dBm
Extinction Ratio (dynamic)	ER	8.2			dB
Eye Mask					SONET/SDH compliant
Optical Jitter generation	Jgen			0.002	UI
Optical Rise time ^b	t_r		130		ps
Optical Fall time ^b	t_f		130		ps
Mean Wavelength	λ	1260	1310	1360	nm
Maximum RMS width (s)	$\Delta\lambda$			1	nm
Relative Intensity Noise	RIN			-120	dB/Hz

b) 20%-80% values

Transmitter Electrical

Parameter	Symbol	Min	Typical	Max	Unit
Input Differential	R_{in}	80	100	120	Ohm
PECL Single Ended data input swing	V_{in}	200		800	mV _{p-p}
PECL Differential data input swing	V_{in}	400		1600	mV _{p-p}
TxFault_Fault	V_{fault}	2		V_{cc}	V
TxFault_Normal	V_{normal}	V_{ee}		0.8	V
TxDisable_Disable	V_d	2		V_{cc}	V
TxDisable_Enable	V_{en}	V_{ee}		$V_{ee}+0.8$	V

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Receiver Specifications					
Parameter	Symbol	Min	Typical	Max	Unit
Receive Power Low ^d	$R_{sens,low}$		-20	-18	dBm
Receive Power High	$R_{sens,high}$			0	dBm
Damage Threshold for Receiver	$P_{In,damage}$			0	dBm
Wavelength	λ	1100		1600	nm
LOS Assert		-28			dBm
LOS De-assert				-18	dBm
LOS hysteresis		1			dB

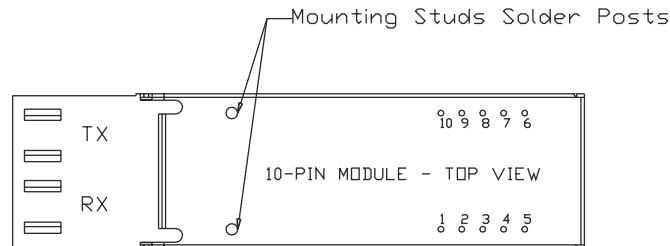
d) at 10^{-10} BER, PRBS 2²³-1

Electrical Output					
Parameter	Symbol	Min	Typical	Max	Unit
PECL Single ended data output swing	V_{out}	250		500	mV _{p-p}
PECL Differential data output swing	V_{out}	500		1000	mV _{p-p}
Data output rise time	T_r		130		ps
Data output fall time	T_f		130		ps

Timing and Electrical					
Parameter	Symbol	Min	Typical	Max	Unit
Tx Disable Negate time	t_{on}			1	ms
Tx Disable assert time	t_{off}			10	μ s
Time to initialize, including reset of TX fault	t_{init}			300	ms
Tx fault Assert time	t_{fault}			100	μ s
Tx Disable to reset	t_{reset}	10			μ s
LOS Assert time	$t_{loss,on}$			100	μ s
LOS De-assert time	$t_{loss,off}$			100	μ s
Serial ID Clock Rate	f_{serial_clock}			100	KHz
RX_LOS Voltage (high)		2		$V_{ee}+0.3$	V
RX_LOS Voltage (low)		0		0.8	V
LOS output voltage-Fault	$V_{LOS\ fault}$	2		V_{cc}	V
LOS output voltage-Normal	$V_{LOS\ normal}$	V_{ee}		$V_{ee}+0.3$	V
MOD_DEF (0:2)-High	V_h	2		V_{cc}	V
MOD_DEF (0:2)-Low	V_l	V_{ee}		$V_{ee}+0.3$	V

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Outline Drawing



Pinout Definitions

Pin	Symbol	Notes
1	RxGND	Directly connect this pin to the receiver ground plane
2	RxVcc	+3.3V dc power for the receiver section
3	SD	Active high on this indicates a received optical signal (LVTTTL or LVPECL)
4	RD-	Receiver Data out Bar(LVPECL/CML)
5	RD+	Receiver Data out (LVPECL/CML)
6	TxVcc	+3.3V dc power for the transmitter section
7	TxGND	Directly connect this pin to the transmitter ground plane
8	TxDIS	Transmitter disable (LVTTTL)
9	TD+	Transmitter Data In (LVPECL/CML)
10	TD-	Transmitter Data In Bar (LVPECL/CML)
Attaching Posts		The attaching posts are at the case potential and may be connected chassis ground. They are not isolated from circuit ground.

Recommended Circuit Schematics

Inputs to the C-1x-2500/C-Fx-SLCx series transmitters are AC coupled and internally terminated through 50 ohm to AC ground. These transceivers can operate with LVPECL or CML logic levels. The input signal must have at least a 200 mV peak to peak (single ended) signal swing. Output from the receiver section of the module is also AC coupled and is expected to drive into 50 ohm load. Different termination strategies may be required depending on the particular Serializer/Deserializer chip set used. The C-1x-2500/C-Fx-SLCx series product family are designed with AC coupled data inputs and outputs to provide the following advantages:

- Close positioning of SERDES with respect to transceiver; allow for shorter line lengths and at gigabit speeds reduces EMI.
- Minimum number of external components.
- Internal termination reduces the potential for unterminated stubs which would otherwise increase jitter and reduce transmission margin.

Figure 1 & 2 illustrates the recommended transmit and receive data line terminations for SERDES with CML and LVPECL Inputs/outputs respectively.

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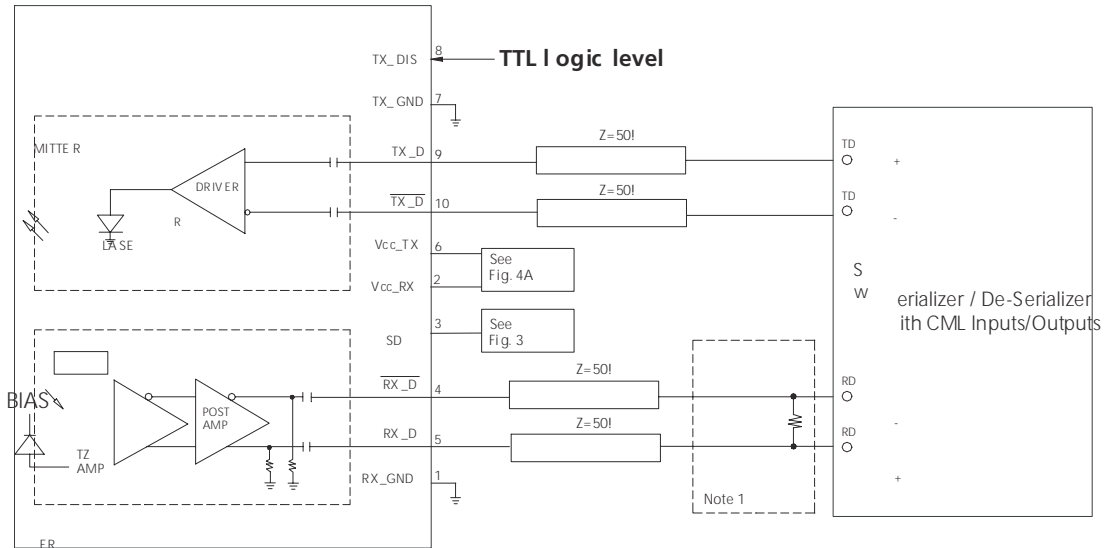


Figure 1. Recommended TRANSMIT and RECEIVE Data Termination for SERDES with CML I/Os
Note 1. Consult SERDES manufacturer's data sheet and application data for appropriate receiver input biasing network. Some deserializer inputs are internally terminated and may not need external termination resistors.

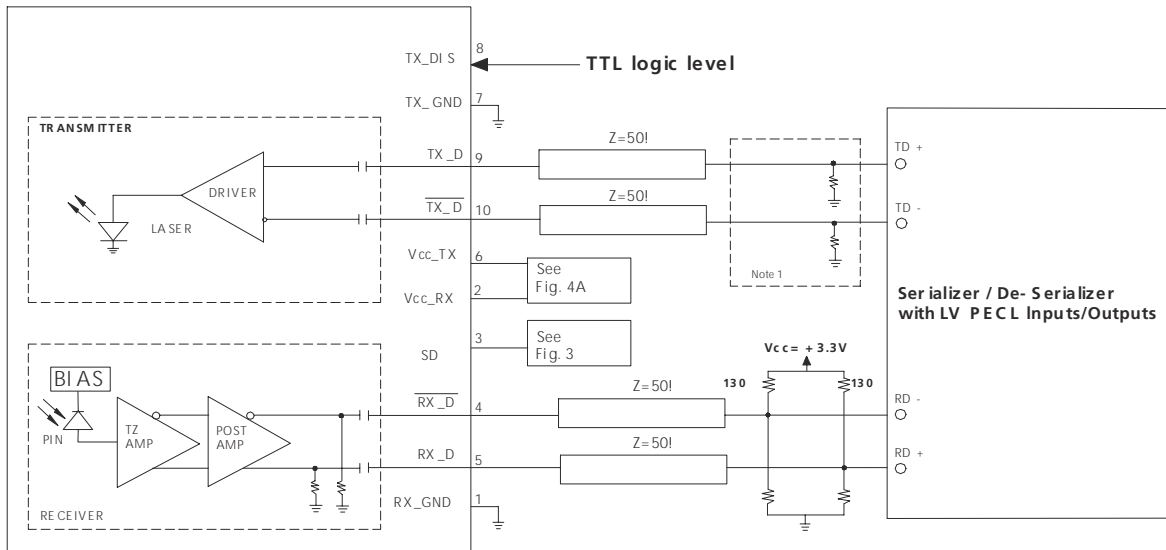


Figure 2. Recommended TRANSMIT and RECEIVE Data Terminations for SERDES with LV PECL I/Os.
Note 1. Consult SERDES manufacturer's data sheet and application data for appropriate receiver input biasing network. Some deserializer inputs are internally terminated and may not need external termination resistors.

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SIGNAL DETECT

The C-13-2500-F-SLC/C-13-2500C-F-SLC transceivers are equipped with LVTTTL / LVPECL signal detect outputs. The standard LVTTTL output eliminates the need for a LVPECL to LVTTTL level shifter in most applications.

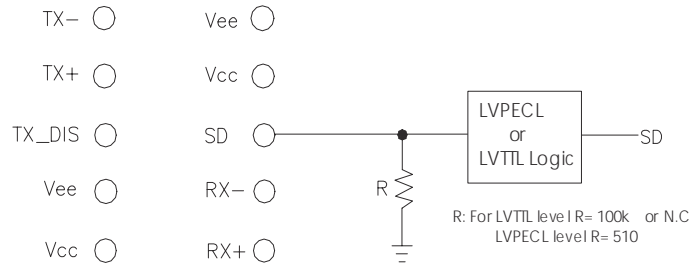
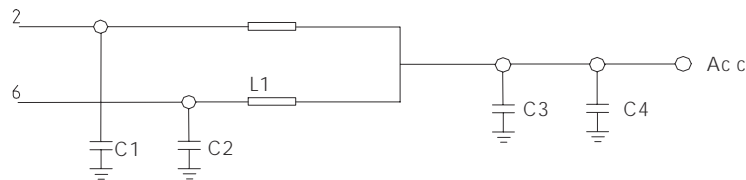


Figure 3: Signal Detect

POWER COUPLING

A suggested layout for power and ground connections is given in figure 4B below. Connections are made via separate voltage and ground planes. The mounting posts are at case ground and should not be connected to circuit ground. The mounting posts are at case ground and should not be connected to circuit ground. The ferrite bead should provide a real impedance of 50 to 100 ohms at 100 to 1000MHz. Bypass capacitors should be placed as close to the 10-pin connector as possible.



VALUES:
 C 1, C 2 = 1000pF,
 C 3, = 0.1 uF
 C 4, = 10 uF,
 L1, L2 = Real impedance of 50 to
 100 Ohms to 1000 MHz.

Figure 4A: Suggested Power Coupling-Electrical Schematic

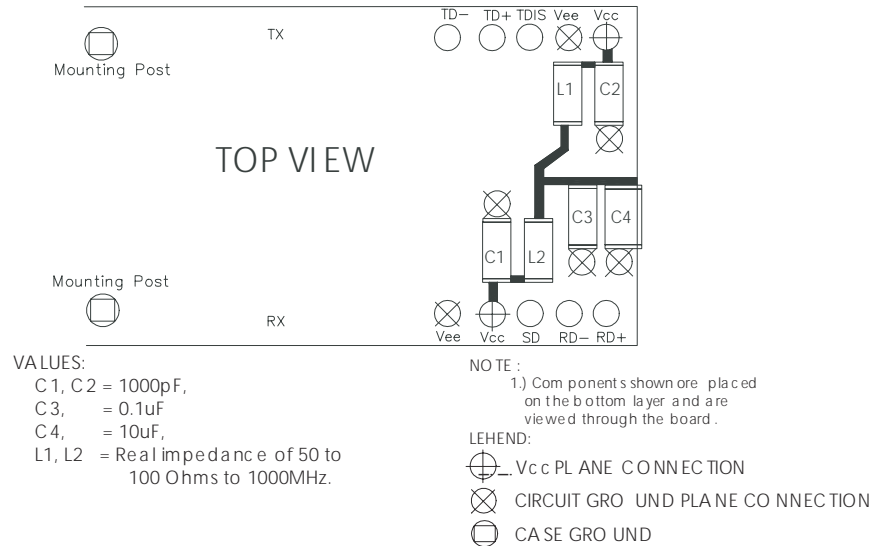
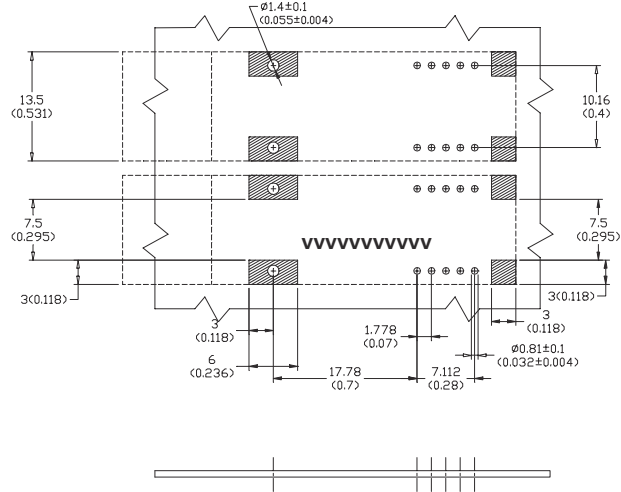


Figure 4B: Suggested Power Coupling-Component Placement

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Recommended Board layout Hole Pattern

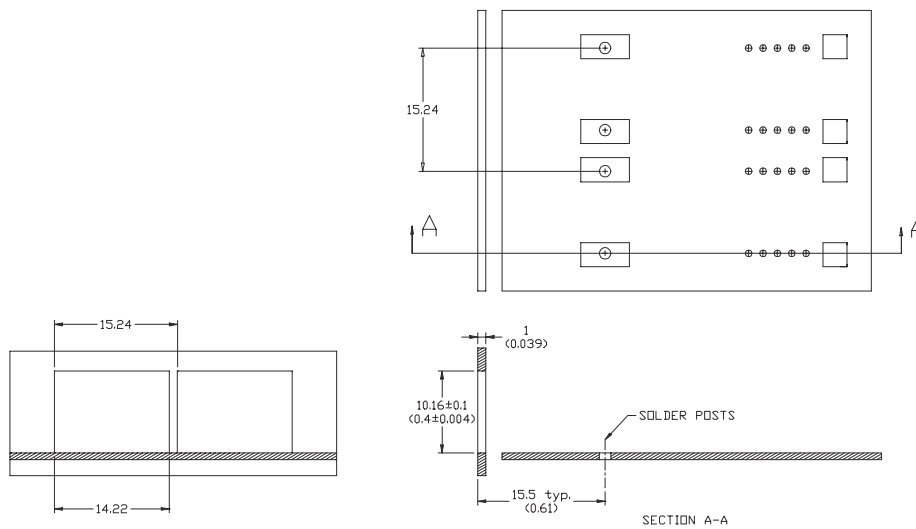


DIMENSION IN MILLIMETER (IN CHES)

NOTES:

1. THIS FIGURE DESCRIBE THE RECOMMAND CIRCUIT BOARD LAYOUT FOR THE SFF TRANSCEIVER.
2. THE HATCHED AREAS ARE KEEP-OUT AREAS RESERVED FOR HOUSING STANDOFF. NO METAL TRACES OR GROUND CONNECTION IN KEEP-OUT AREAS.
3. THE MOUNTING STUDS SHOULD BE SOLDERED TO CHASSIS GROUND FOR MECHANICAL INTEGRITY.

Recommended Panel mounting



DIMENSION IN MILLIMETER (IN CHES)

Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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