

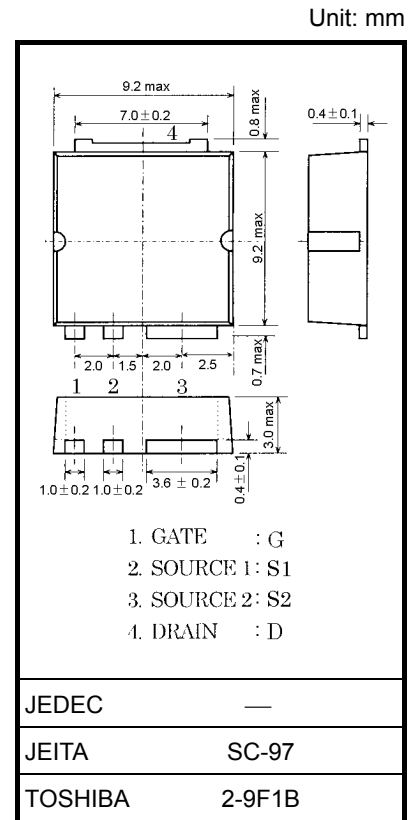
2SK4034

Switching Regulator, DC-DC Converter Applications
Motor Drive Applications

- Low drain-source ON-resistance: $R_{DS(ON)} = 4.2 \text{ m}\Omega$ (typ.)
- High forward transfer admittance: $|Y_{fs}| = 110 \text{ S}$ (typ.)
- Low leakage current: $I_{DSS} = 100 \text{ }\mu\text{A}$ ($V_{DS} = 60 \text{ V}$)
- Enhancement mode: $V_{th} = 1.5 \text{ to } 2.5 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	60	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)		V_{DGR}	60	V
Gate-source voltage		V_{GSS}	± 20	V
Drain current	DC (Note 1)	I_D	75	A
	Pulse ($t \leq 1 \text{ ms}$) (Note 1)	I_{DP}	300	
Drain power dissipation ($T_c = 25^\circ\text{C}$)		P_D	125	W
Single pulse avalanche energy (Note 2)		E_{AS}	322	mJ
Avalanche current		I_{AR}	75	A
Repetitive avalanche energy (Note 3)		E_{AR}	12.5	mJ
Channel temperature		T_{ch}	150	$^\circ\text{C}$
Storage temperature range		T_{stg}	-55 to 150	$^\circ\text{C}$



Weight: 0.74 g (typ.)

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	1.0	$^\circ\text{C/W}$

Note: Use the S1 pin to return the gate signal to source. Board traces should be designed so the main current flows to the S2 pin.

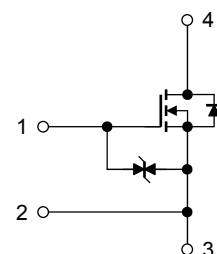
Note 1: Ensure that the channel temperature does not exceed 150°C .

Note 2: $V_{DD} = 25 \text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 78 \text{ }\mu\text{H}$, $R_G = 25 \text{ }\Omega$, $I_{AR} = 75 \text{ A}$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

Note 4: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



This transistor is an electrostatic-sensitive device. Handle with care.

Electrical Characteristics (Note 5) (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 10	μA
Drain cut-off current		I_{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	60	—	—	V
		$V_{(BR)DSX}$	$I_D = 10 \text{ mA}, V_{GS} = -20 \text{ V}$	35	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$	1.5	—	2.5	V
Drain-source ON-resistance		$R_{DS(ON)}$	$V_{GS} = 10 \text{ V}, I_D = 38 \text{ A}$	—	4.2	5.8	$\text{m}\Omega$
			$V_{GS} = 4.5 \text{ V}, I_D = 38 \text{ A}$	—	5.5	10	$\text{m}\Omega$
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10 \text{ V}, I_D = 38 \text{ A}$	55	110	—	S
Input capacitance		C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	12400	—	pF
Reverse transfer capacitance		C_{rss}		—	410	—	
Output capacitance		C_{oss}		—	1100	—	
Switching time	Rise time	t_r		—	15	—	ns
	Turn-on time	t_{on}		—	35	—	
	Fall time	t_f		—	45	—	
	Turn-off time	t_{off}		Duty $\leq 1\%$, $t_w = 10 \mu\text{s}$	—	250	
Total gate charge (gate-source plus gate-drain)		Q_g	$V_{DD} \approx 48 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 75 \text{ A}$	—	196	—	nC
Gate-source charge		Q_{gs}		—	148	—	
Gate-drain ("miller") charge		Q_{gd}		—	48	—	

Note 5: The S1 and S2 pins should be grounded together, except when measuring the switching time.

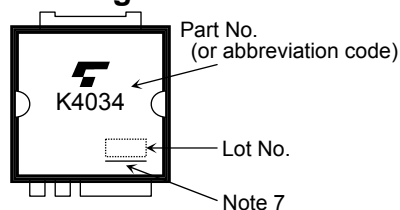
Source-Drain Ratings and Characteristics (Note 6) (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1, Note 6)		I_{DR1}	—	—	—	75	A
Pulse drain reverse current (Note 1, Note 6)		I_{DRP1}	—	—	—	300	A
Continuous drain reverse current (Note 1, Note 6)		I_{DR2}	—	—	—	1	A
Pulse drain reverse current (Note 1, Note 6)		I_{DRP2}	—	—	—	4	A
Forward voltage (diode)		V_{DS2F}	$I_{DR1} = 75 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-1.5	V
Reverse recovery time		t_{rr}	$I_{DR} = 75 \text{ A}, V_{GS} = 0 \text{ V}, dI_{DR}/dt = 50 \text{ A}/\mu\text{s}$	—	70	—	ns
Reverse recovery charge		Q_{rr}		—	77	—	nC

Note 6: I_{DR1}, I_{DRP1} : Current flowing between the drain and S2 pins. Ensure that the S1 pin is left open.
 I_{DR2}, I_{DRP2} : Current flowing between the drain and S1 pins. Ensure that the S2 pin is left open.

The S1 and S2 pins should be grounded together, unless otherwise noted.

Marking

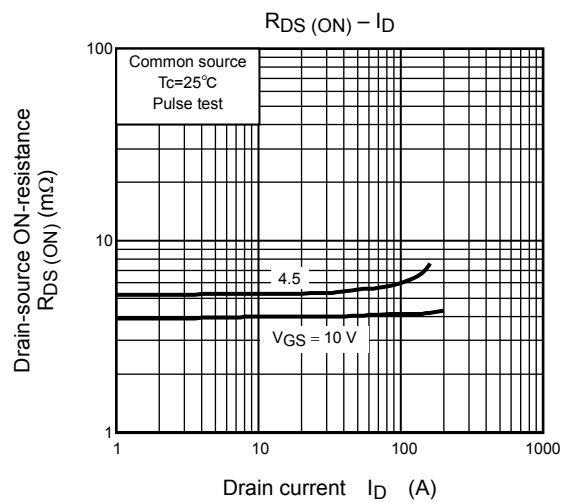
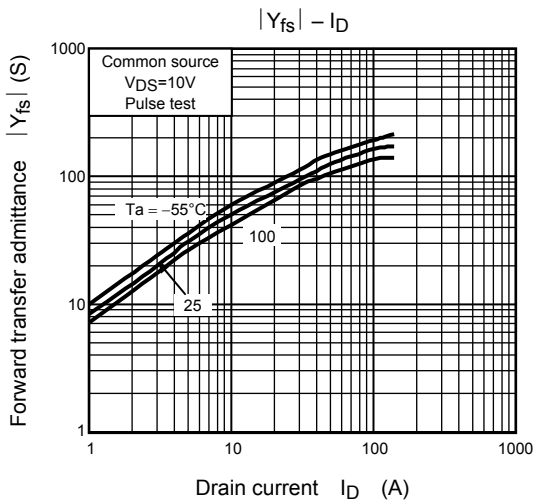
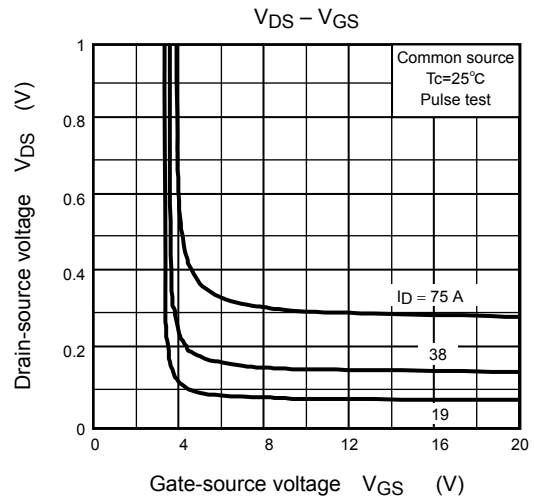
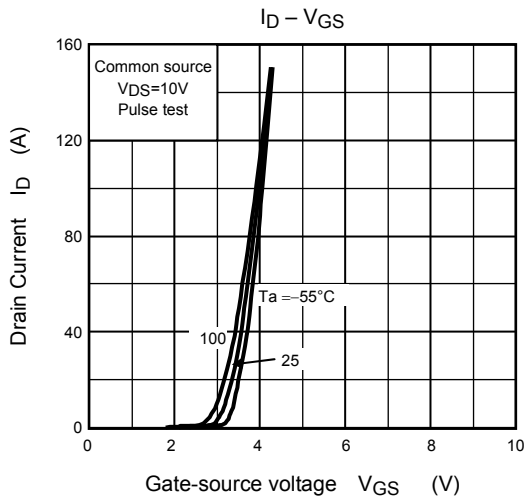
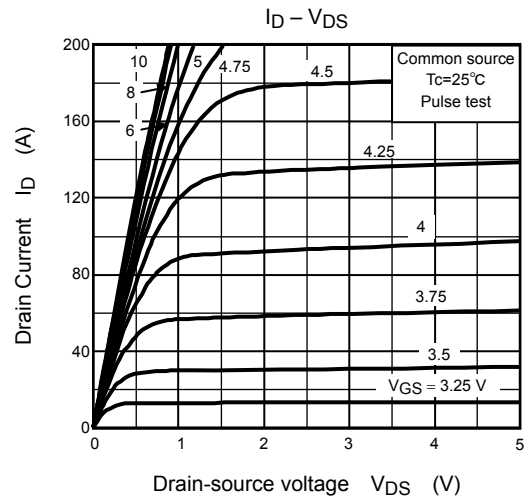
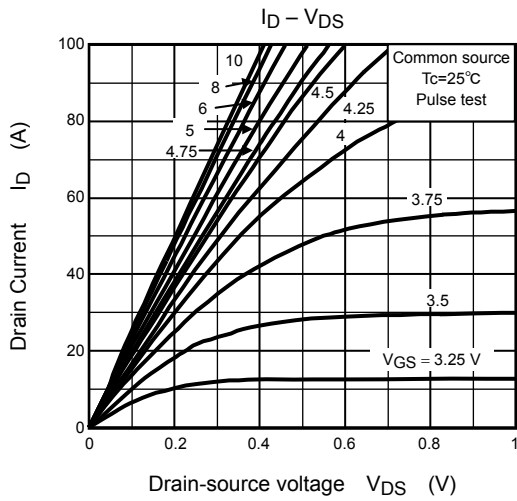


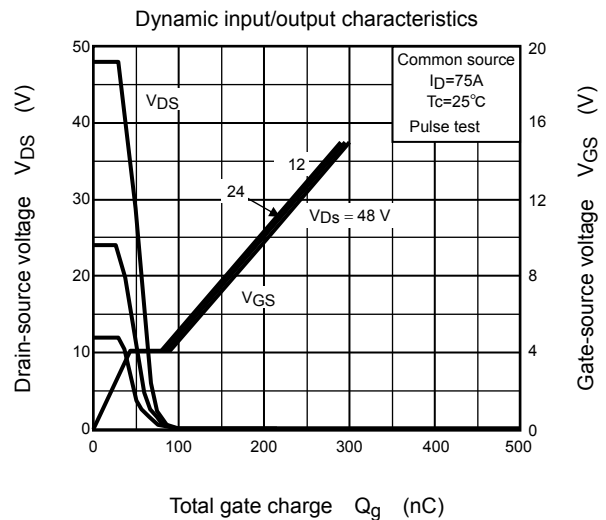
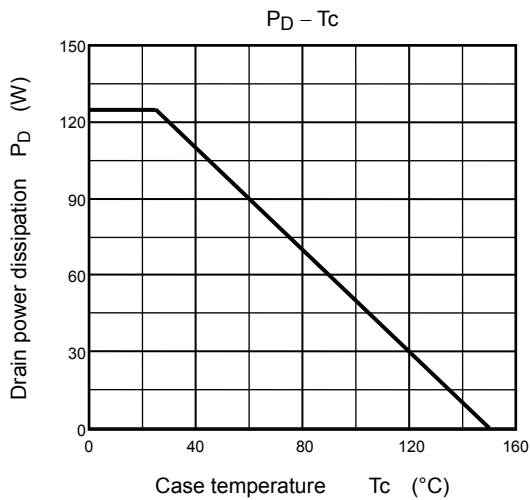
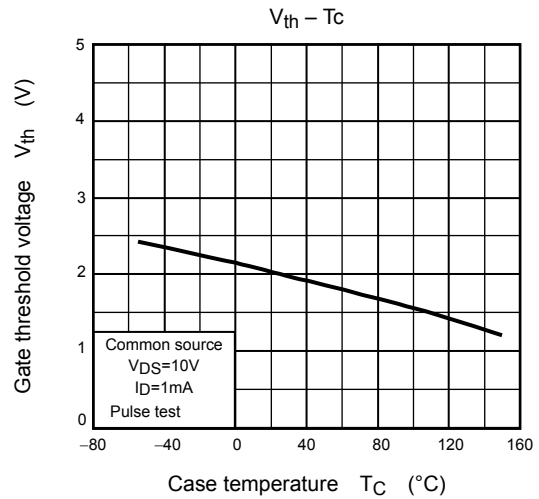
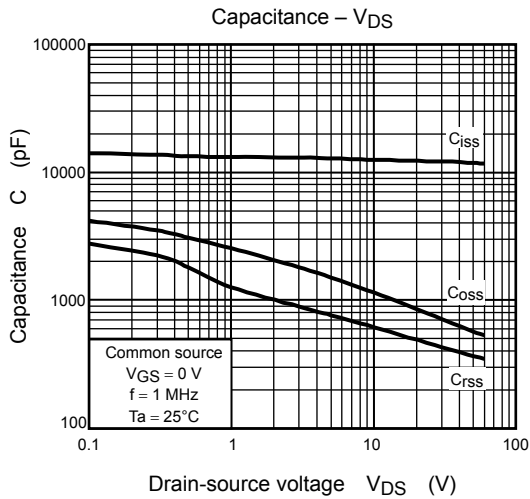
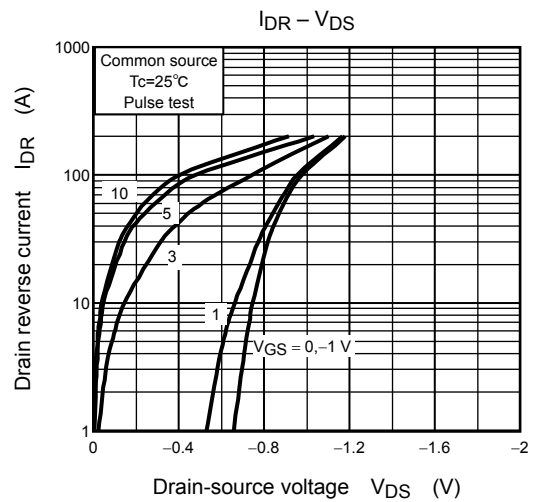
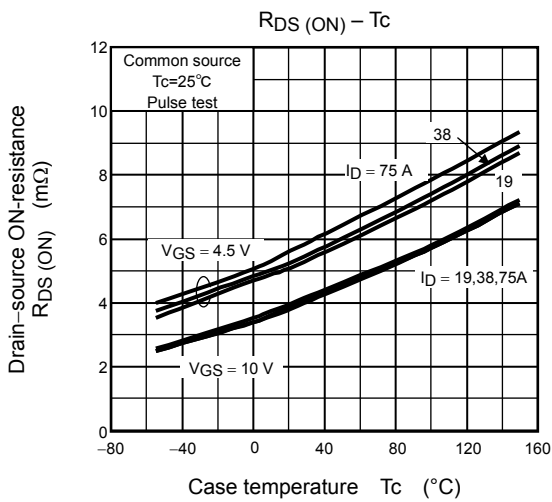
Note 7: A line under a Lot No. identifies the indication of product Labels.

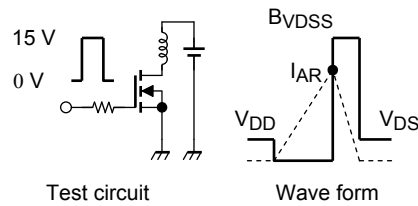
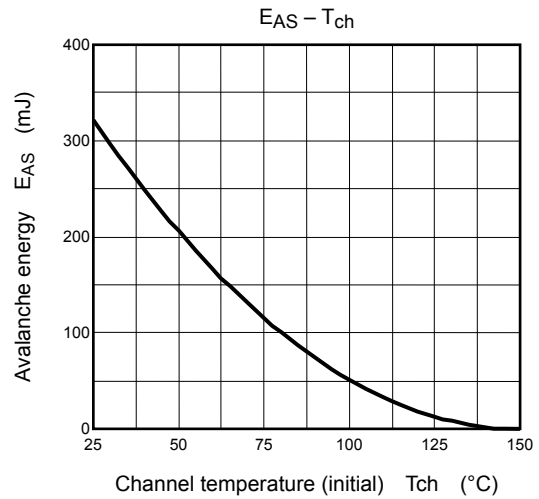
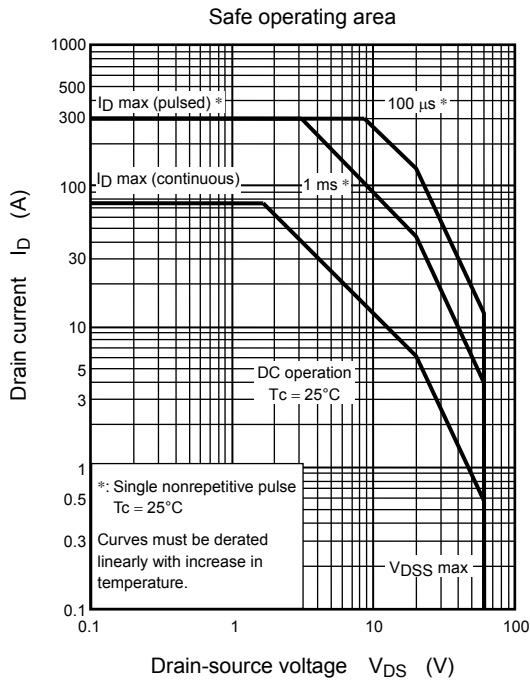
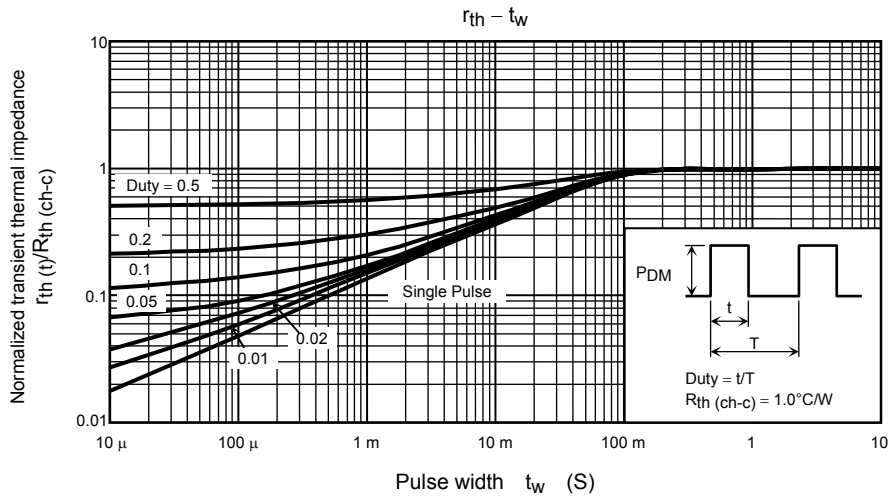
Not underlined: [[Pb]]/INCLUDES > MCV

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$R_G = 25 \Omega$
 $V_{DD} = 25 \text{ V}, L = 78 \mu\text{H}$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{BVDSS}{BVDSS - V_{DD}} \right)$$

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