

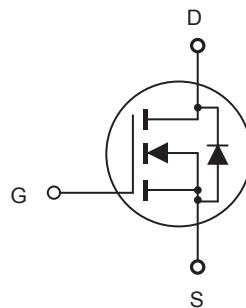
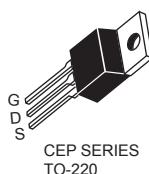


CEP3120/CEB3120

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- 30V, 40A, $R_{DS(ON)} = 15\text{m}\Omega$ @ $V_{GS} = 10\text{V}$.
 $R_{DS(ON)} = 22\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead free product is acquired.
- TO-220 & TO-263 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous@ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	I_D	40 28	A
Drain Current-Pulsed ^a	I_{DM}	160	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P_D	43 0.29	W W/ $^\circ\text{C}$
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$



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Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}} = 0\text{V}, I_{\text{D}} = 250\mu\text{A}$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 30\text{V}, V_{\text{GS}} = 0\text{V}$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{\text{GS}} = 20\text{V}, V_{\text{DS}} = 0\text{V}$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{\text{GS}} = -20\text{V}, V_{\text{DS}} = 0\text{V}$			-100	nA
On Characteristics^c						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{GS}} = V_{\text{DS}}, I_{\text{D}} = 250\mu\text{A}$	1		3	V
Static Drain-Source	$R_{\text{DS(on)}}$	$V_{\text{GS}} = 10\text{V}, I_{\text{D}} = 20\text{A}$		11	15	$\text{m}\Omega$
On-Resistance		$V_{\text{GS}} = 4.5\text{V}, I_{\text{D}} = 15\text{A}$		17	22	$\text{m}\Omega$
Dynamic Characteristics^d						
Input Capacitance	C_{iss}	$V_{\text{DS}} = 15\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		895		pF
Output Capacitance	C_{oss}			215		pF
Reverse Transfer Capacitance	C_{rss}			160		pF
Switching Characteristics^d						
Turn-On Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}} = 15\text{V}, I_{\text{D}} = 10\text{A}, \square$ $V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 3\Omega$		11	22	ns
Turn-On Rise Time	t_{r}			7	14	ns
Turn-Off Delay Time	$t_{\text{d(off)}}$			31	62	ns
Turn-Off Fall Time	t_{f}			5	10	ns
Total Gate Charge	Q_{g}	$V_{\text{DS}} = 15\text{V}, I_{\text{D}} = 10\text{A}, V_{\text{GS}} = 10\text{V}$		21	27	nC
Gate-Source Charge	Q_{gs}			2		nC
Gate-Drain Charge	Q_{gd}			6		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^b	I_{s}				40	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{\text{GS}} = 0\text{V}, I_{\text{s}} = 20\text{A}$			1.3	V

Notes :

- a.Repetitive Rating : Pulse width limited by maximum junction temperature. \square
- b.Surface Mounted on FR4 Board, $t \leq 10 \text{ sec.} \square$
- c.Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\% \square$
- d.Guaranteed by design, not subject to production testing. \square

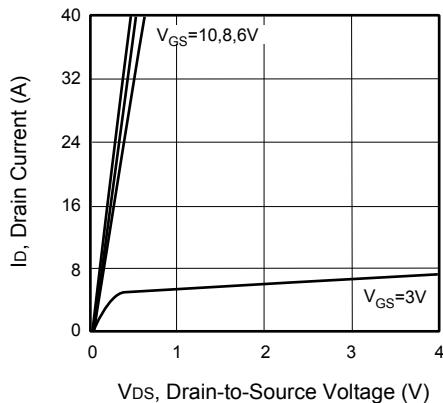


Figure 1. Output Characteristics

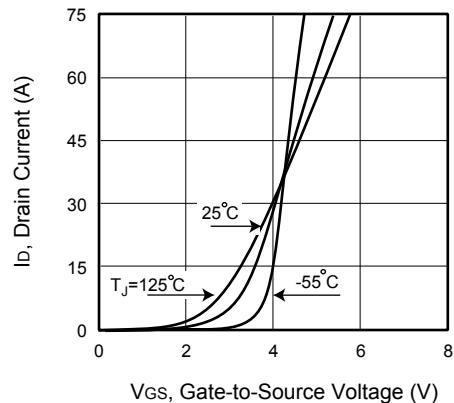


Figure 2. Transfer Characteristics

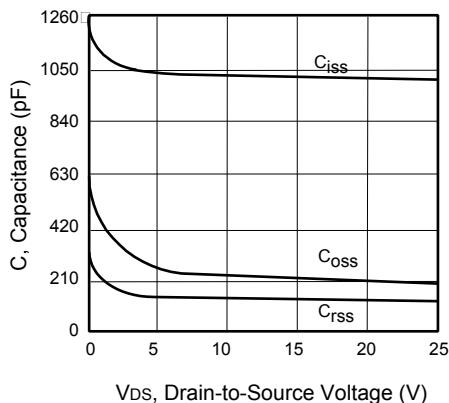


Figure 3. Capacitance

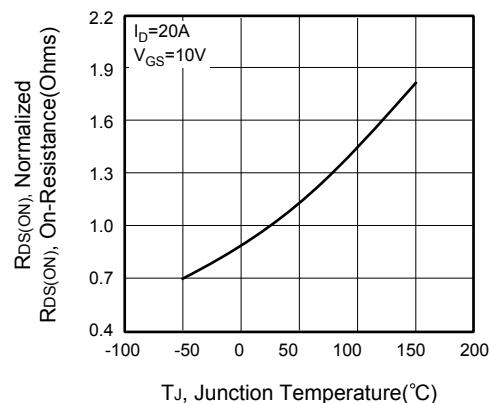


Figure 4. On-Resistance Variation with Temperature

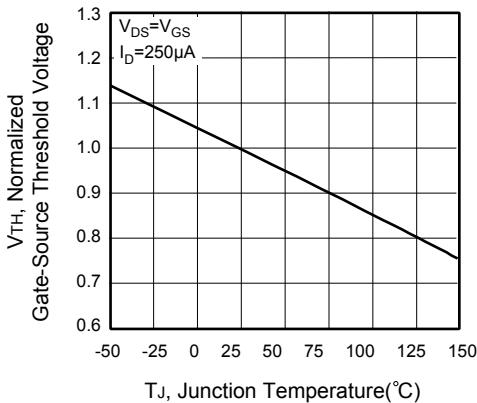


Figure 5. Gate Threshold Variation with Temperature

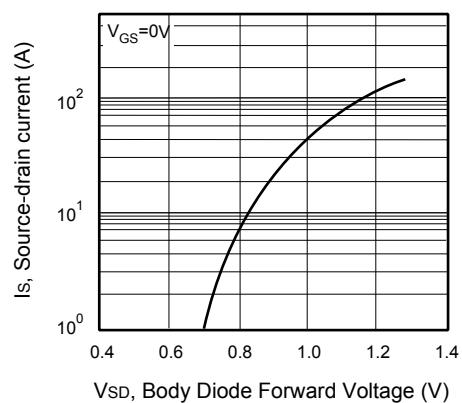


Figure 6. Body Diode Forward Voltage Variation with Source Current



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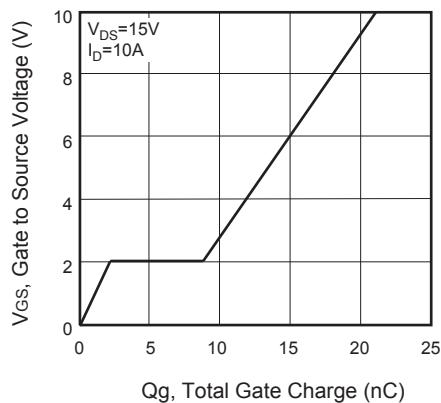


Figure 7. Gate Charge

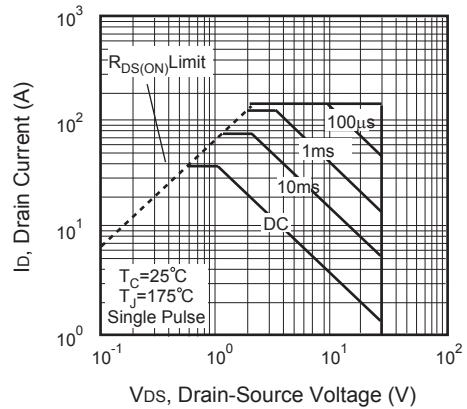


Figure 8. Maximum Safe Operating Area



Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

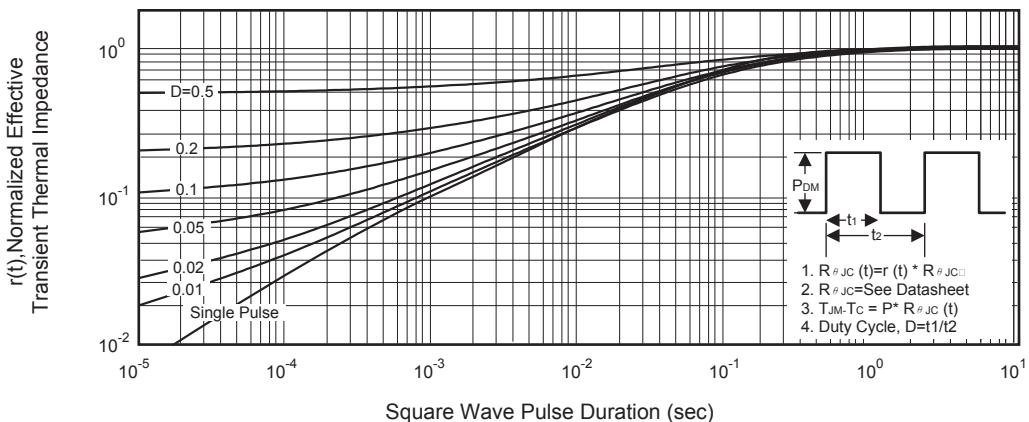


Figure 11. Normalized Thermal Transient Impedance Curve