Flash-ROM Module 8MByte (2Mx32Bit), 80Pin-SMM, 3.3V Design
Part No. HMF2M32F4VA

GENERAL DESCRIPTION

The HMF2M32F4VA is a high-speed flash read only memory (FROM) module containing 2,097,152 words organized in a x32bit configuration. The module consists of four 1M x 16 FROM mounted on a 80-pin stackable type, double - sided, FR4-printed circuit board.

Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Output enable (/OE) and write enable (/WE) can set the memory input and output. The host system can detect a program or erase operation is complete by observing the Ready Pin, or reading the DQ7(Data # Polling) and DQ6(Toggle) status bits. When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single + 3.0V DC power supply and all inputs and outputs are LVTTL-compatible.

FEATURES

- Part Identification
  - HMF2M32F4VA : Socket 5mm
- Access time: 80, 90, 120ns
- High-density 8MByte design
- High-reliability, low-power design
- Single + 3.0V ± 0.3V power supply
- All in/outputs are LVTTL-compatible
- FR4-PCB design
- 80-pin Designed by
  40-pin Fine Pitch Connector (x 2EA)
- Minimum 1,000,000 write/erase cycle
- Sector erases architecture

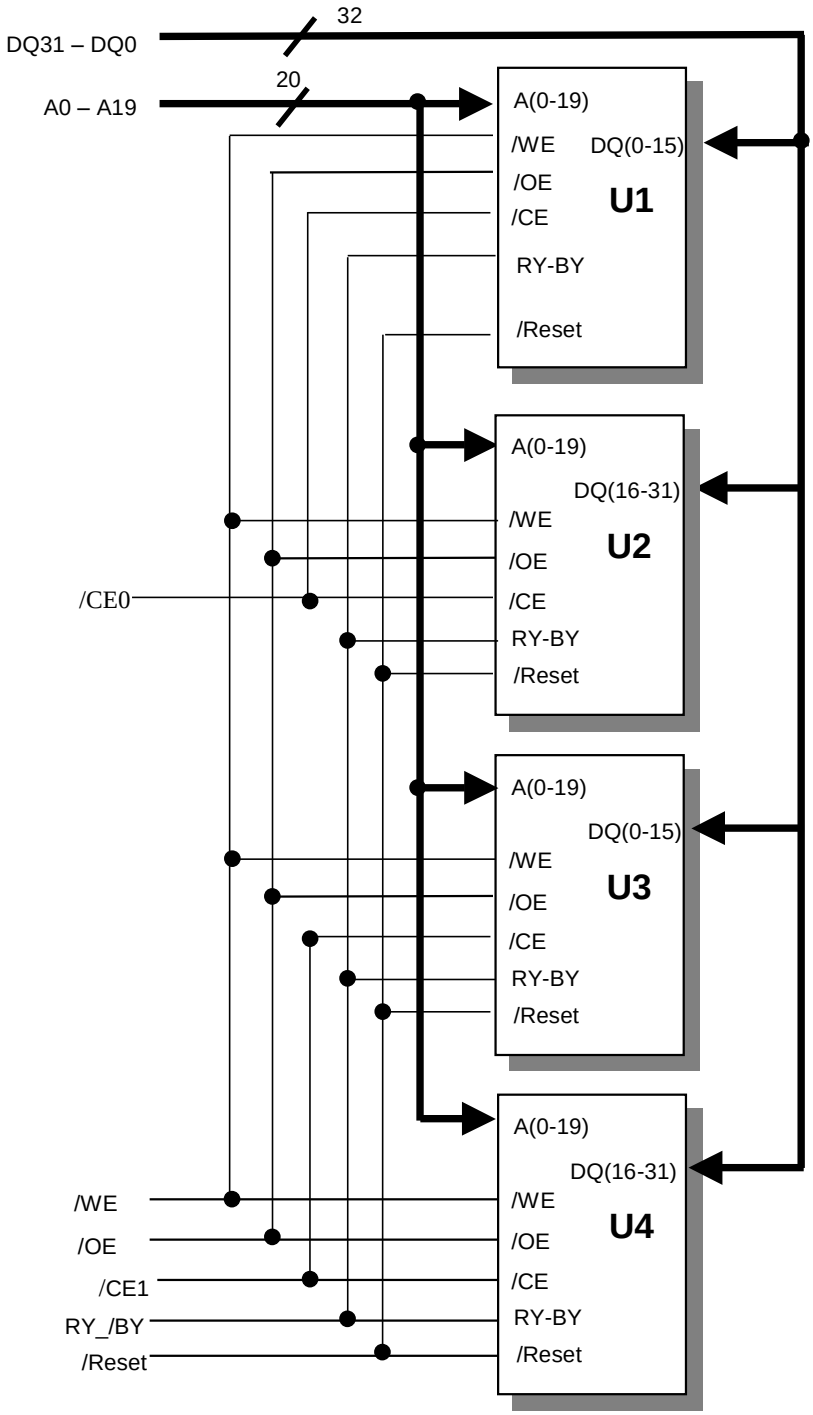
OPTIONS MARKING

- Timing
  - 80ns access -80
  - 90ns access -90
  - 120ns access -120
- Packages
  - 80-pin SMM F

PIN ASSIGNMENT

P1				P2			
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vcc	21	Vcc	1	Vcc	21	Vcc
2	/CE0	22	DQ15	2	DQ16	22	NC
3	NC	23	DQ7	3	DQ24	23	NC
4	NC	24	DQ14	4	DQ17	24	/BYTE
5	NC	25	DQ6	5	DQ25	25	/OE
6	RY_/BY	26	DQ13	6	DQ18	26	/CE1
7	Vss	27	Vss	7	Vss	27	Vss
8	/RESET	28	DQ5	8	DQ26	28	A16
9	/WE	29	DQ12	9	DQ19	29	A0
10	A19	30	DQ4	10	DQ27	30	A18
11	A8	31	DQ11	11	DQ20	31	A17
12	A9	32	DQ3	12	DQ28	32	A7
13	A10	33	DQ10	13	DQ21	33	A6
14	Vss	34	Vss	14	Vss	34	Vss
15	A11	35	DQ2	15	DQ29	35	A5
16	A12	36	DQ9	16	DQ22	36	A4
17	A13	37	DQ1	17	DQ30	37	A3
18	A14	38	DQ8	18	DQ23	38	A2
19	A15	39	DQ0	19	DQ31	39	A1
20	Vcc	40	Vcc	20	Vcc	40	Vcc

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	/RESET	DQ (/BYTE=L)	POWER
STANDBY	X	H	X	Vcc±0.3V	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
READ	L	L	H	H	D_{OUT}	ACTIVE
WRITE or ERASE	X	L	L	H	D_{IN}	ACTIVE

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	$V_{IN,OUT}$	-0.5V to Vcc+0.5V
Voltage with respect to ground Vcc	V_{CC}	-0.5V to +4.0V
Storage Temperature	T_{STG}	-65°C to +150°C
Operating Temperature	T_A	-40°C to +85°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
Vcc for ± 10% device Supply Voltages	Vcc	2.7V	3.0	3.6V
Ground	V_{SS}	0	0	0

DC AND OPERATING CHARACTERISTICS ($0^oC \leq T_A \leq 70\ ^oC$)

PARAMETER	TEST CONDITIONS		SYMBOL	MIN	MAX	UNIT
Input Leakage Current	Vcc=Vcc max, V_{IN}= GND to Vcc		I_{L1}	-10	1.0	µA
Output Leakage Current	Vcc=Vcc max, V_{OUT}= GND to Vcc		I_{L0}	-10	1.0	µA
Output High Voltage	I_{OH} = -2.0mA, Vcc = Vcc min		V_{OH}	0.85x Vcc	-	V
Output Low Voltage	I_{OL} = 4.0mA, Vcc =Vcc min		V_{OL}	-	0.45	V
Vcc Active Read Current (1)	/CE = V_{IL}, /OE = V_{IH},	5MHZ	I_{CC1}	-	64	mA
		1MHZ		-	16	
Vcc Active Write Current (2)	/CE = V_{IL}, /OE=V_{IH}		I_{CC2}	-	120	mA
Vcc Standby Current	/CE, /RESET=Vcc±0.3V		I_{CC3}	-	20	µA
Low Vcc Lock-Out Voltage			V_{LKO}	2.3	2.5	V

Notes: 1. The Icc current listed includes both the DC operating current and the frequent component (at 5MHz).

2. Icc active while embedded algorithm (program or erase) is in progress

3. Not 100% tested

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Block Erase Time	-	0.7	15	sec	Excludes 00H programming prior to erasure
Chip Erase Time		25		sec	
Word Programming Time	-	11	360	μs	Excludes system-level overhead
Chip Programming Time	-	12	36	sec	

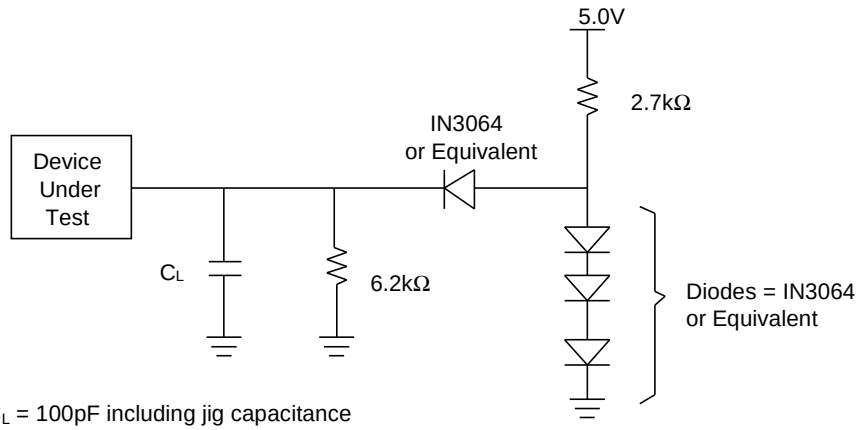
TSOP CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	TYP.	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes : Capacitance is periodically sampled and not 100% tested.

TEST SPECIFICATIONS

TEST CONDITION	VALUE	UNIT
Output load	1TTL gate	
Input rise and full times	5	ns
Input pulse levels	0 to 3	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V



Note : C_L = 100pF including jig capacitance

AC CHARACTERISTICS

u Read Only Operations Characteristics

PARAMETER	DESCRIPTION	SPEED						UNIT
		- 80		-90		-120		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	80		90		120		ns
t_{ACC}	Address Access time		80		90		120	ns
t_{CE}	Chip Enable to Access time		80		90		120	ns
t_{OE}	Output Enable time		30		35		50	ns
t_{DF}	Chip Enable to Output High-Z		25		30		30	ns
t_{OEH}	Output Enable Hold Time	0		0		0		ns
t_{QH}	Output Hold Time From Addresses, /CE or /OE	0		0		0		ns

u Erase/Program Operations

Alternate /WE Controlled Writes

PARAMETER	DESCRIPTION	- 80		-90		-120		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time (1)	80	-	90	-	120	-	ns
t_{AS}	Address Setup Time	0	-	0	-	0	-	ns
t_{AH}	Address Hold Time	45	-	45	-	50	-	ns
t_{DS}	Data Setup Time	35	-	45	-	50	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	ns
t_{OES}	Output Enable Setup Time	0	-	0	-	0	-	ns
t_{GHWL}	Read Recover Time Before Write	0	-	0	-	0	-	ns
t_{CS}	/CE Setup Time	0	-	0	-	0	-	ns
t_{CH}	/CE Hold Time	0	-	0	-	0	-	ns
t_{WP}	Write Pulse Width	35	-	35	-	50	-	ns
t_{WPH}	Write Pulse Width High	30	-	30	-	30	-	ns
t_{PGM}	Programming Operation	11		11		11		ns
t_{BERS}	Block Erase Operation (2)	0.7	-	0.7	-	0.7	-	ns
t_{VCS}	Vcc set up time	50	-	50	-	50	-	ns
t_{RB}	Write Recover Time Before RY_/BY	0	-	0	-	0	-	ns

Notes : : 1. Not 100% tested

2 . The duration of the program or erase operation varies and is calculated in the internal algorithms.

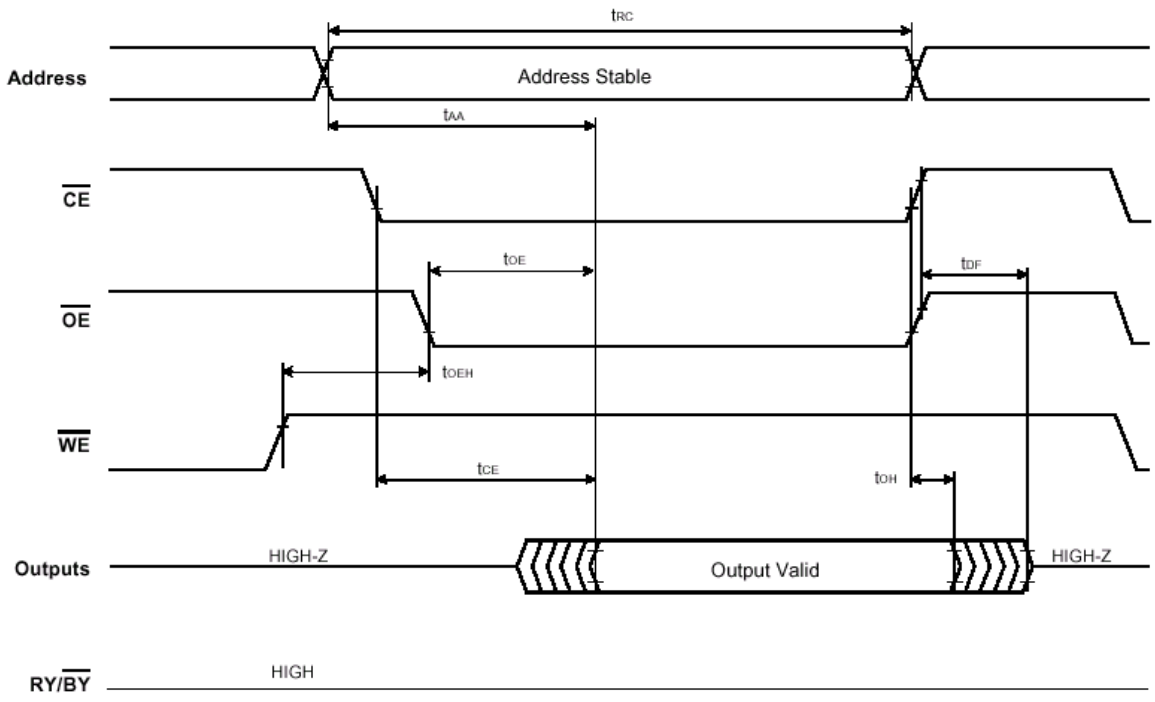
u Erase/Program Operations
Alternate /CE Controlled Writes

PARAMETER	DESCRIPTION	- 80		-90		-120		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time(1)	80	-	90	-	120	-	ns
t_{AS}	Address Setup Time	0	-	0	-	0	-	ns
t_{AH}	Address Hold Time	45	-	45	-	50	-	ns
t_{DS}	Data Setup Time	35	-	45	-	50	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	ns
t_{OES}	Output Enable Setup Time	0	-	0	-	0	-	ns
t_{GHWL}	Read Recover Time Before Write	0	-	0	-	0	-	ns
t_{WS}	/WE Setup time	0	-	0	-	0	-	ns
t_{WH}	/WE Hold time	0	-	0	-	0	-	ns
t_{PGM}	/CE Pulse Width	35		35		50		ns
t_{CPH}	/CE Pulse Width High	30						
t_{WHWH1}	Programming Operation	11						us
t_{WHWH2}	Sector Erase Operation	0.7						sec

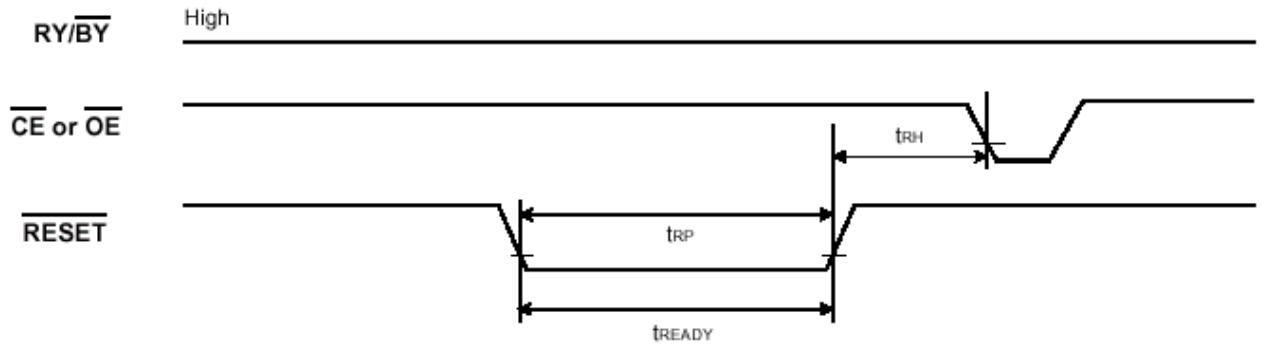
Notes : 1. Not 100% tested

2 . This does not include the preprogramming time

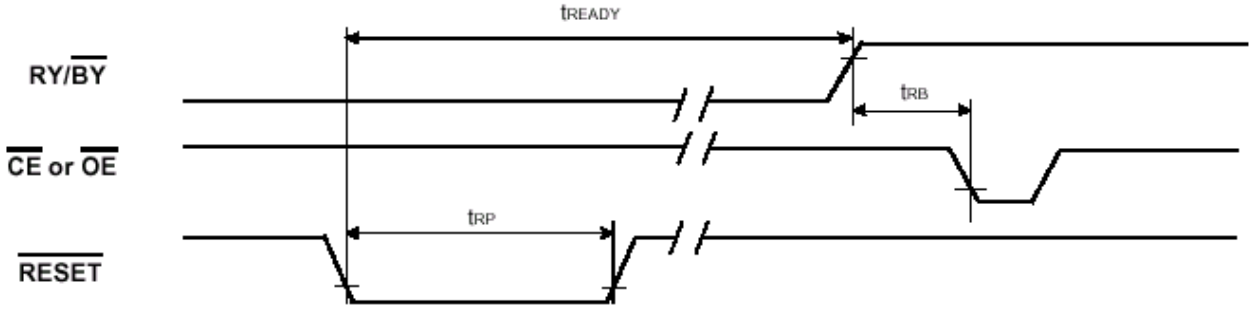
u READ OPERATIONS TIMING



u RESET TIMING



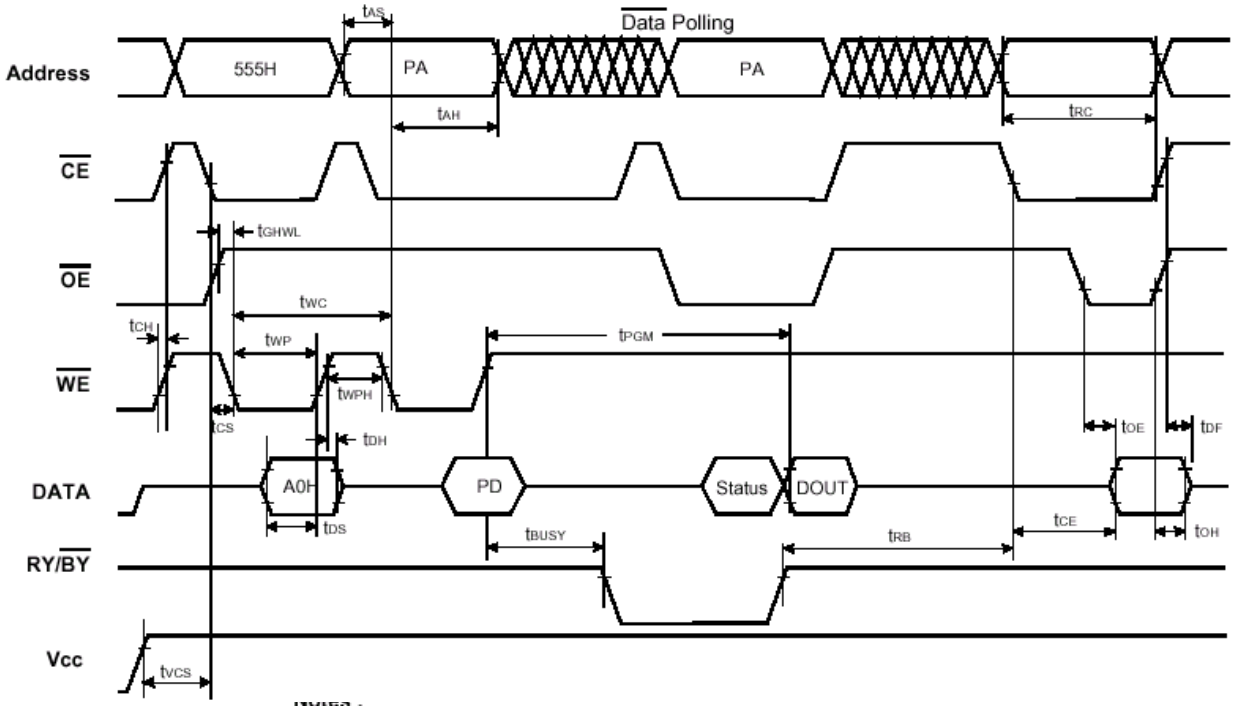
Reset Timings NOT during Internal Routine



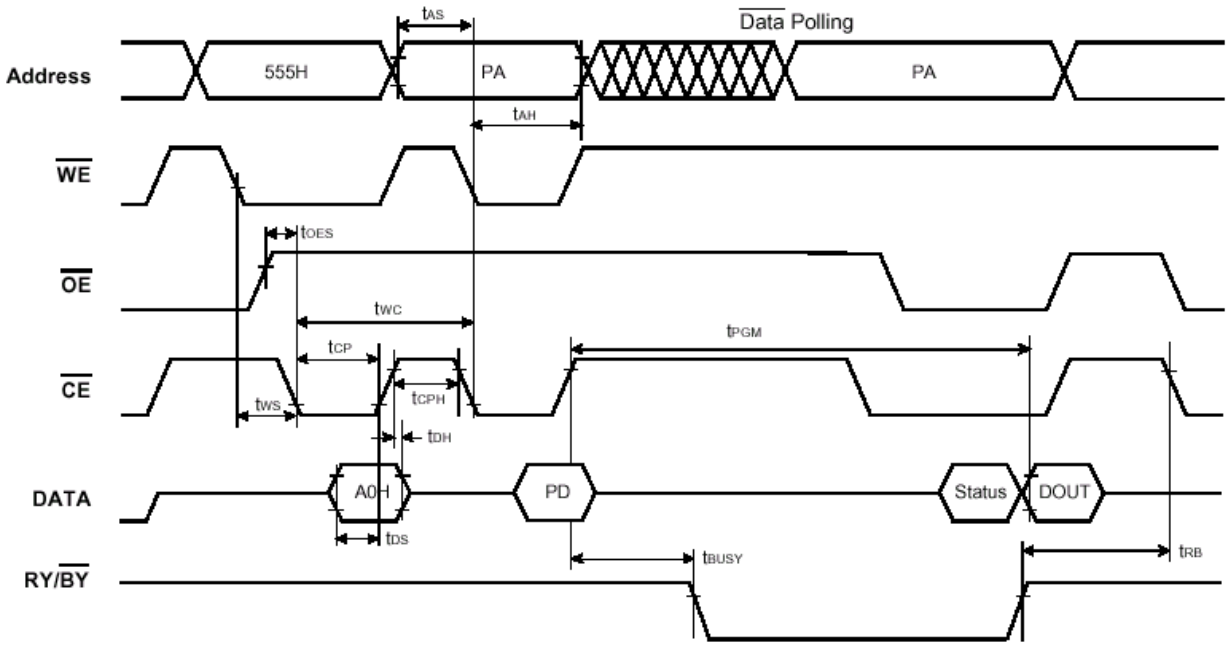
Reset Timings during Internal Routine

u PROGRAM OPERATIONS TIMING

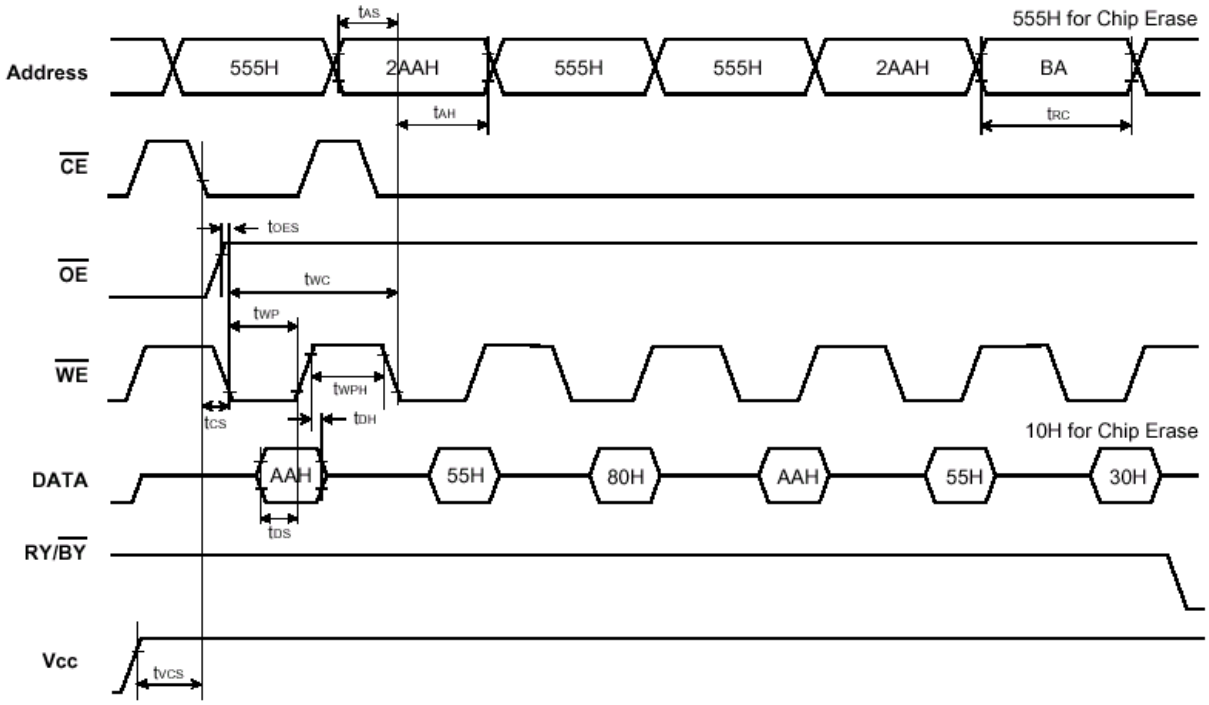
Alternate /WE Controlled Writes



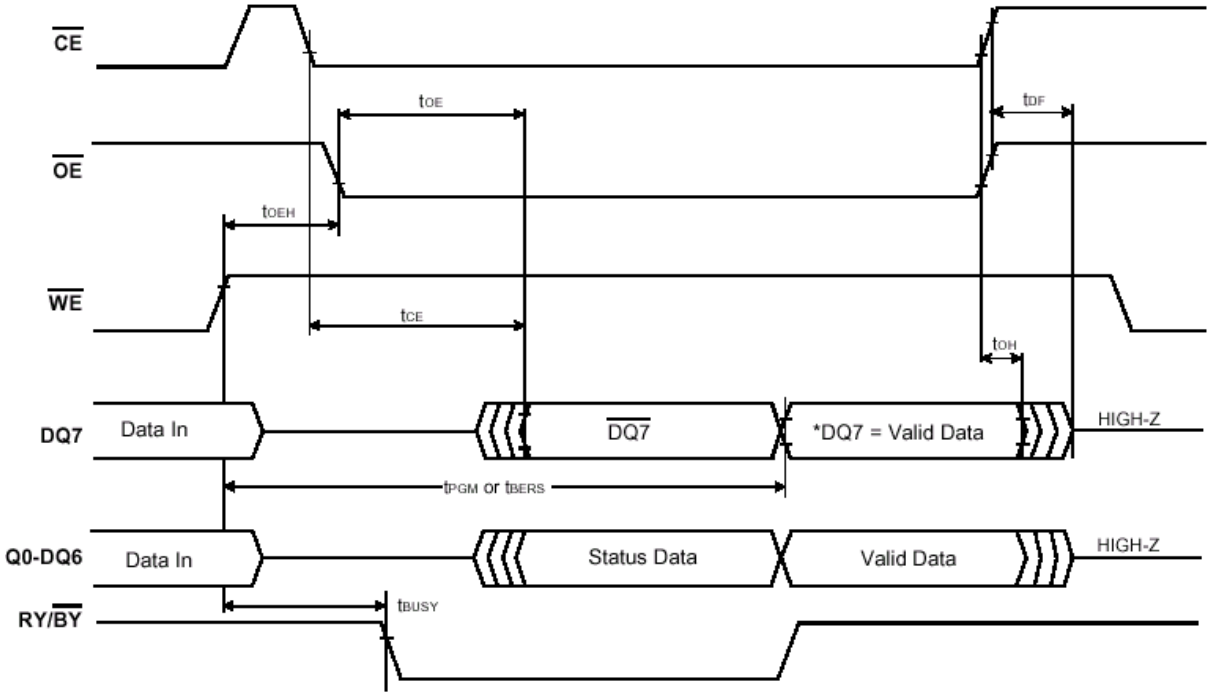
Alternate /CE Controlled Writes



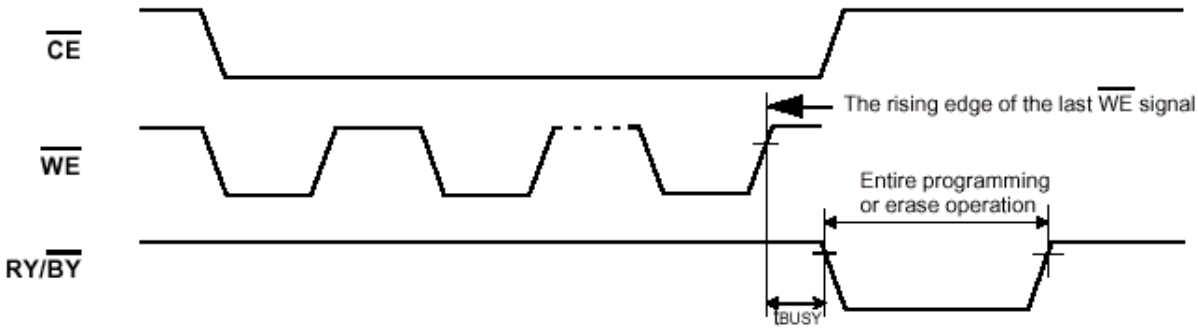
u CHIP/BLOCK ERASE OPERATION TIMINGS



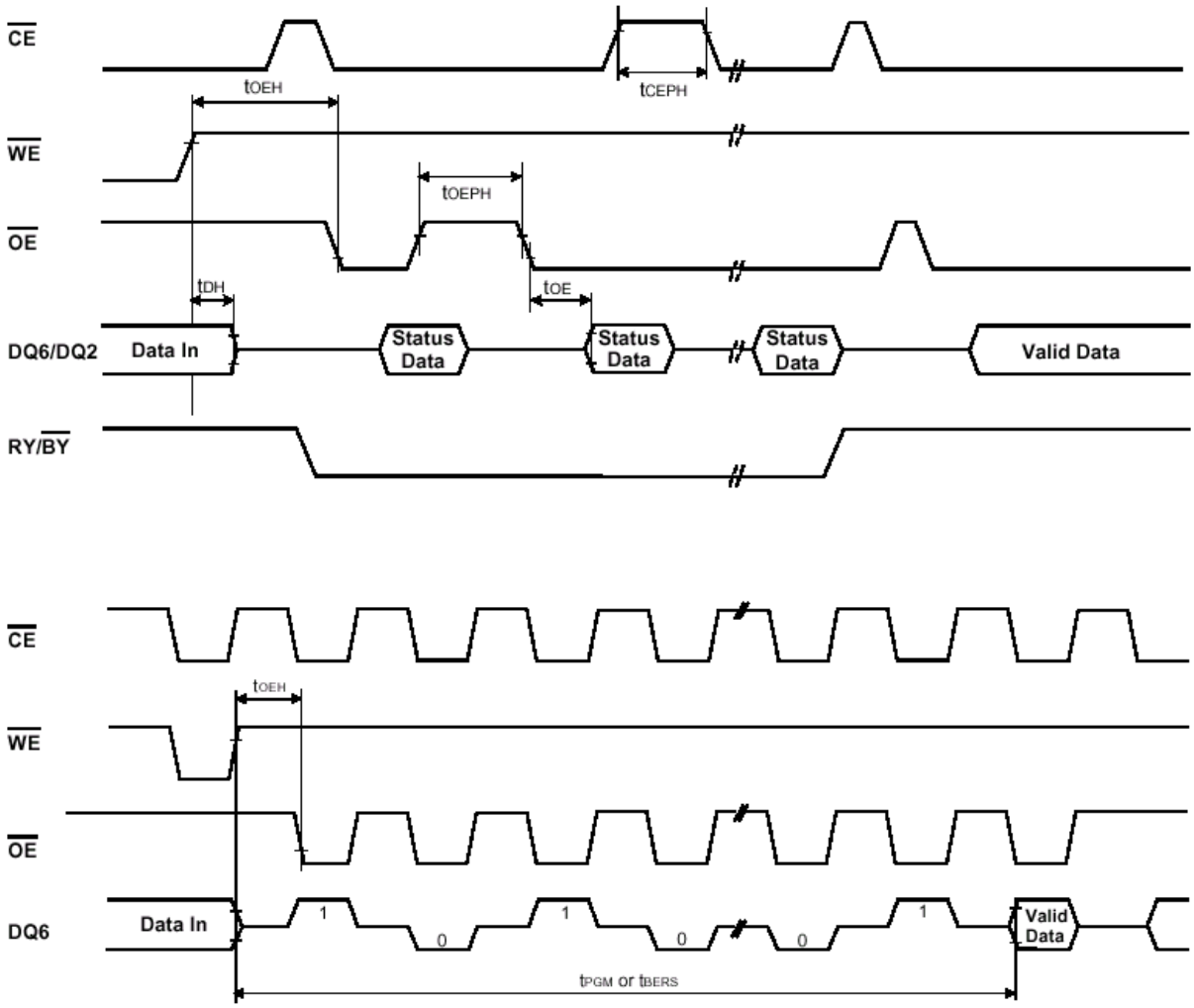
u DATA# POLLING TIMES DURING INTERNAL ROUTINE OPERATION



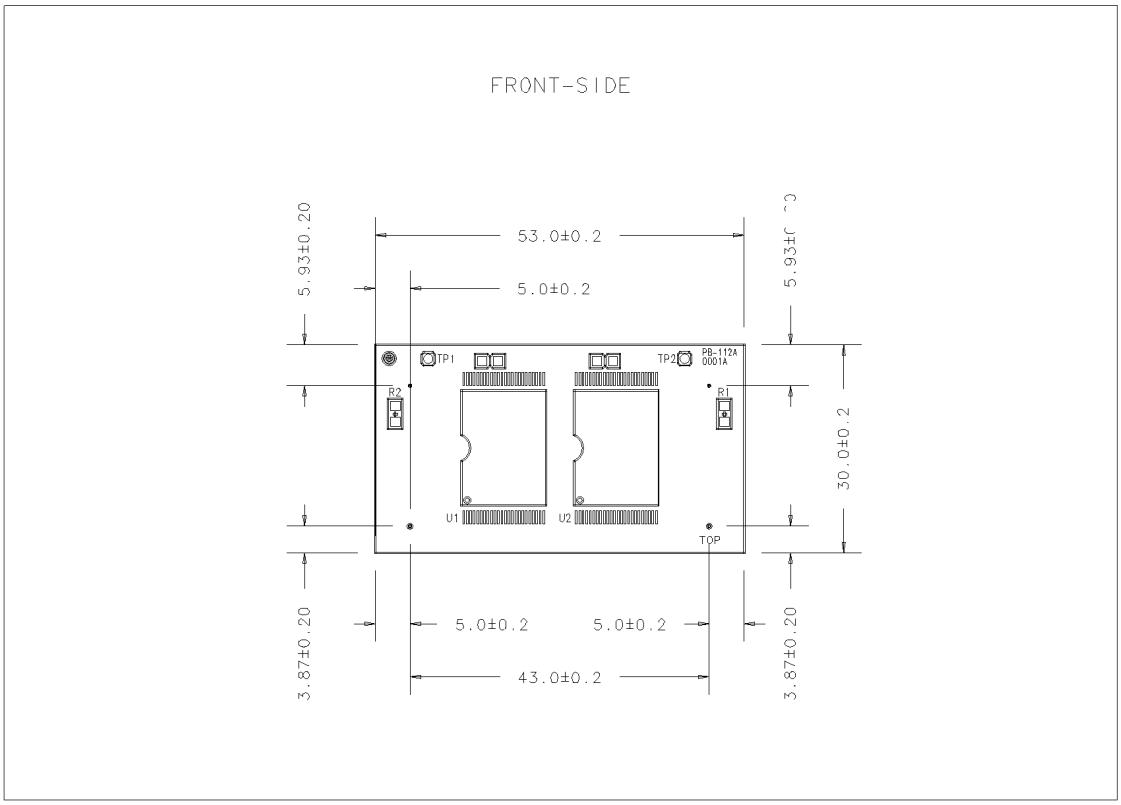
u RY_ /BY TIMEING DURING ERASE / PROGRAM OPERATION

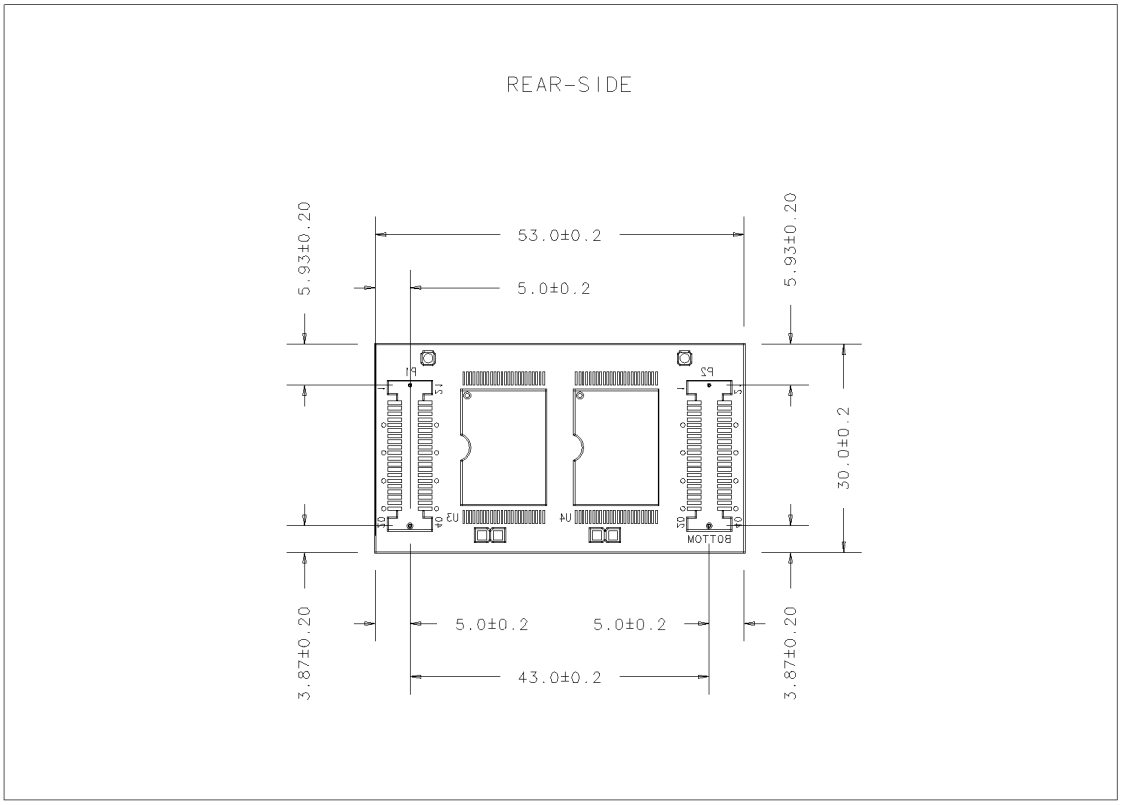


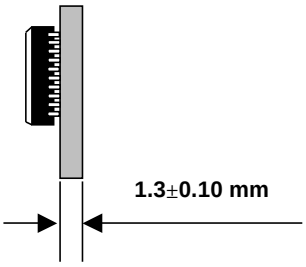
u TOGGLE# BIT DURING INTERNAL ROUTINE OPERATION



PACKAGE DIMENSIONS







ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMF2M32F4VA-80	8MByte	x 32	80Pin –SMM	4EA	3.3V	80ns
HMF2M32F4VA-90	8Mbyte	x 32	80Pin –SMM	4EA	3.3V	90ns
HMF2M32F4VA-120	8Mbyte	x 32	80Pin –SMM	4EA	3.3V	120ns