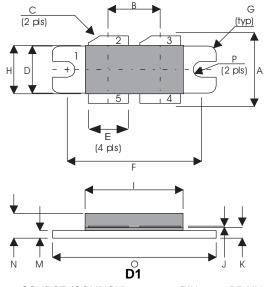


### ROHS COMPLIANT METAL GATE RF SILICON FET

#### MECHANICAL DATA



SOURCE (COMMON) PIN 2 PIN 1 **DRAIN 1** PIN 3 DRAIN 2 PIN 4 GATE 2 PIN 5 GATE 1

DIM	Millimetres	Tol.	Inches	Tol.
Α	15.24	0.50	0.600	0.020
В	10.80	0.13	0.425	0.005
С	45°	5°	45°	5°
D	9.78	0.13	0.385	0.005
E	8.38	0.13	0.330	0.005
F	27.94	0.13	1.100	0.005
G	1.52R	0.13	0.060R	0.005
Н	10.16	0.15	0.400	0.006
1	21.84	0.23	0.860	0.009
J	0.10	0.02	0.004	0.001
K	1.96	0.13	0.077	0.005
М	1.02	0.13	0.040	0.005
N	4.45	0.38	0.175	0.015
0	34.04	0.13	1.340	0.005
Р	1.63R	0.13	0.064R	0.005

# **GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET** 300W - 50V - 175MHz**PUSH-PULL**

### **FEATURES**

- SUITABLE FOR BROAD BAND APPLICATIONS
- SIMPLE BIAS CIRCUITS
- ULTRA-LOW THERMAL RESISTANCE
- BeO FREE
- LOW Crss
- HIGH GAIN 20 dB MINIMUM

### **APPLICATIONS**

 VHF/UHF COMMUNICATIONS from 1 MHz to 175 MHz

$\overline{P_D}$	Power Dissipation	875W (438W -A Version)
$BV_DSS$	Drain – Source Breakdown Voltage *	125V
$BV_{GSS}$	Gate – Source Breakdown Voltage*	±20V
I <sub>D(sat)</sub>	Drain Current*	18A
T <sub>stg</sub>	Storage Temperature	−65 to 150°C
Tj	Maximum Operating Junction Temperature	200°C

<sup>\*</sup> Per Side

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Issue 2

### **ELECTRICAL CHARACTERISTICS** (T<sub>case</sub> = 25°C unless otherwise stated)

Parameter		Test Conditions		Min.	Тур.	Max.	Unit
	PER SIDE						
BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0	I <sub>D</sub> = 100mA	125			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 125V	$V_{GS} = 0$			6	mA
I <sub>GSS</sub>	Gate Leakage Current	V <sub>GS</sub> = 20V	$V_{DS} = 0$			6	μΑ
V <sub>GS(th)</sub>	Gate Threshold Voltage*	I <sub>D</sub> = 10mA	$V_{DS} = V_{GS}$	1		7	V
9 <sub>fs</sub>	Forward Transconductance*	V <sub>DS</sub> = 10V	I <sub>D</sub> = 3A	4.8			mhos
V <sub>GS(th)m</sub>	Gate Threshold Voltage  atch  Matching Between Sides	I <sub>D</sub> = 10mA	$V_{DS} = V_{GS}$			0.1	V
		TOT	AL DEVICE				
G <sub>PS</sub>	Common Source Power Gain	P <sub>O</sub> = 300W		20			dB
η	Drain Efficiency	$V_{DS} = 50V$	I <sub>DQ</sub> = 1.2A	60			%
VSWR	Load Mismatch Tolerance	f = 175MHz		20:1			_
		Р	ER SIDE				•
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 50V$	$V_{GS} = -5V f = 1MHz$			360	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 50V$	$V_{GS} = 0$ $f = 1MHz$			150	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	$V_{DS} = 50V$	$V_{GS} = 0$ $f = 1MHz$			9	pF

<sup>\*</sup> Pulse Test: Pulse Duration = 300  $\mu s$ , Duty Cycle  $\leq$  2%

### THERMAL DATA

R <sub>THj-case</sub>	Thermal Resistance Junction – Case	Max. 0.2°C / W
,		0.4 °C / W -A Version

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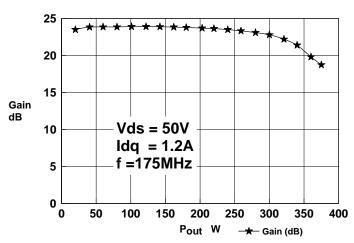


Figure 1 – Gain vs. Power Output.

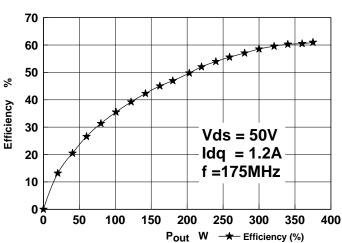


Figure 2 – Efficiency vs. Power Output.

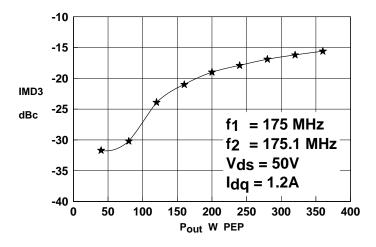


Figure 3 - IMD vs. Power Output

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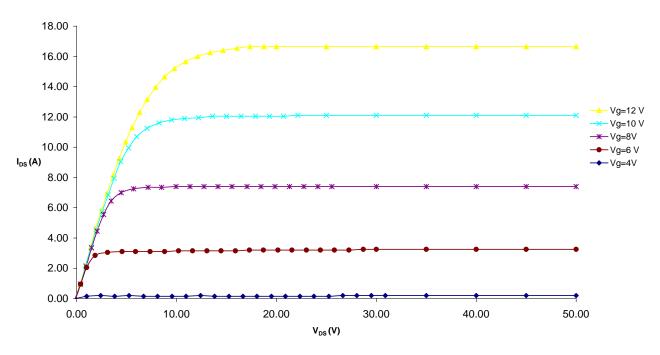


Figure 4 – Typical IV Characteristics.

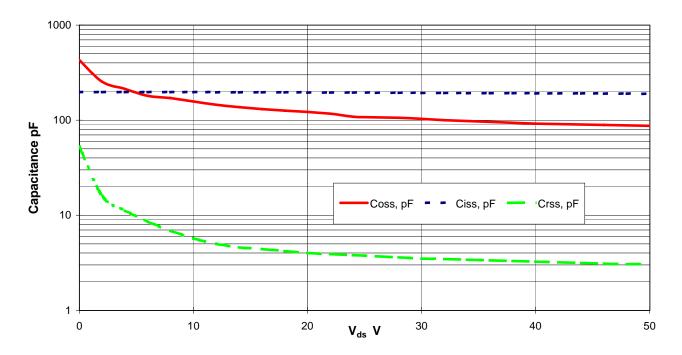
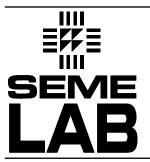


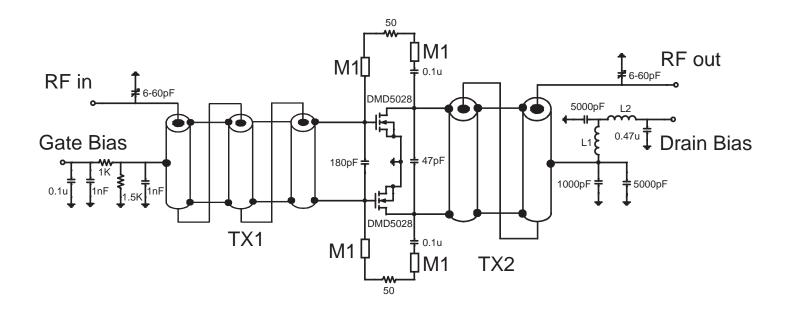
Figure 5 - Typical CV Characteristics.

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### DMD5028 175MHz TEST FIXTURE

TX1 9:1 transformer. 3 turns of 062-25 semi-rigid coax around 75-26 powdered iron core

TX2 4:1 transformer. 2 turns of 090-25 semi-rigid coax around 100-8 powdered iron core

L1 10 turns 16awg enamelled wire, 5mm internal diameter

L2 0.5 turns 16 awg enamelled wire on A1 x 1 2-hole core

M1 microstrip line, 20mm long, 1mm wide on 0.062in thick G10 substrate

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