FAIRCHILD SEMICONDUCTOR®

February 2007

# FAN7384
# Half-Bridge Gate-Drive IC

## Features

- Floating Channel for Bootstrap Operation to +600V
- Typically 250mA/500mA Sourcing/Sinking Current Driving Capability for Both Channels
- Extended Allowable Negative $V_S$ Swing to -9.8V for Signal Propagation at $V_{DD}$=$V_{BS}$=15V
- Matched Propagation Delay Below 50ns
- Output In-Phase with Input Signal
- 3.3V and 5V Input Logic Compatible
- Built-in Shoot-Through Prevention Logic
- Built-in Common Mode dv/dt Noise Canceling Circuit
- Built-in UVLO Functions for Both Channels
- Built-in Cycle-by-Cycle Shutdown Function
- Built-in Soft-Off Function
- Built-in Bi-Directional Fault Function
- Built-in Short-Circuit Protection Function

## Applications

- Motor Inverter Driver
- Normal Half-Bridge and Full-Bridge Driver
- Switching Mode Power Supply

## Description

The FAN7384 is a monolithic half-bridge gate-drive IC designed for high voltage, high speed driving MOSFETs and IGBTs operating up to +600V.

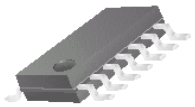
Fairchild's high-voltage process and common-mode noise canceling technique provide stable operation of high-side drivers under high-dv/dt noise circumstances.

An advanced level-shift circuit allows high-side gate driver operation up to $V_S$ = -9.8V (typical) for $V_{BS}$ =15V.

The UVLO circuits prevent malfunction when $V_{DD}$ and $V_{BS}$ are lower than the specified threshold voltage.

Output drivers typically source/sink 250mA/500mA, respectively, which is suitable for half-bridge and full-bridge applications in motor drive systems.

**14-SOP**



## Ordering Information

| Part Number | Package | Pb-Free | Operating Temperature Range | Packing Method |
|---|---|---|---|---|
| FAN7384M(1) | 14-SOP | Yes | -40°C ~ 125°C | Tube |
| FAN7384MX(1) | | | | Tape & Reel |

**Note:**

1. These devices passed wave soldering test by JESD22A-111.

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## Typical Application Diagrams

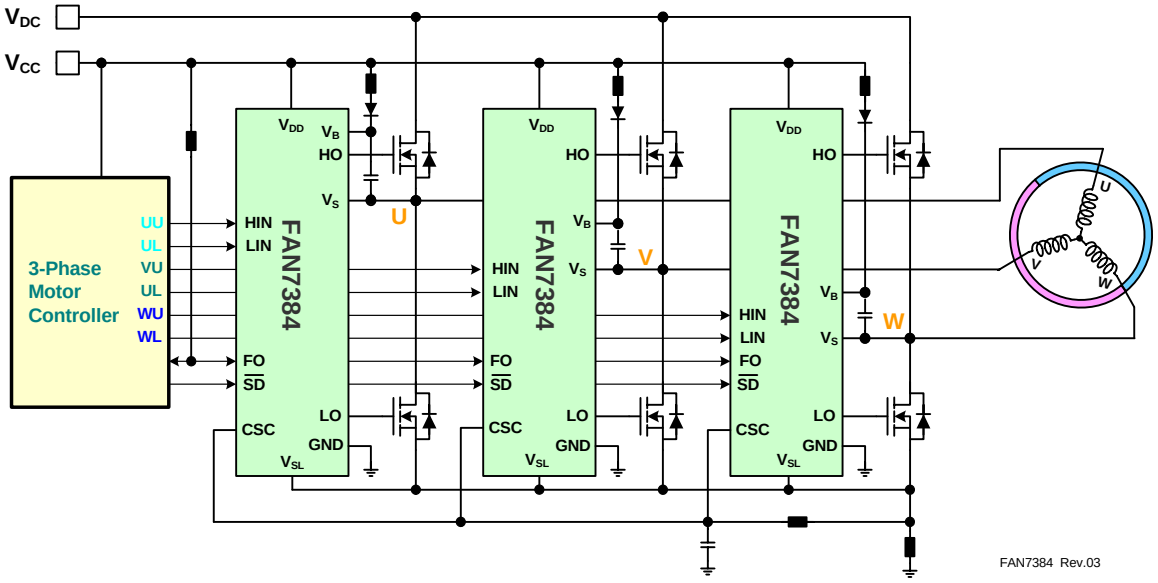


**Figure 1. 3-Phase Motor Drive Application**

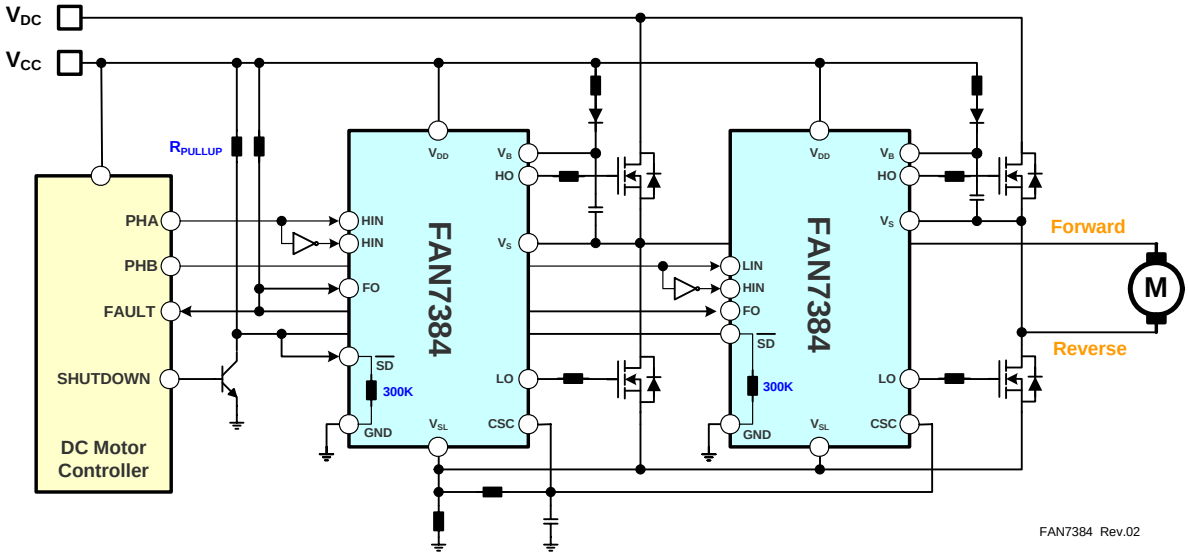


**Figure 2. DC Motor Drive Application**

## Internal Block Diagram

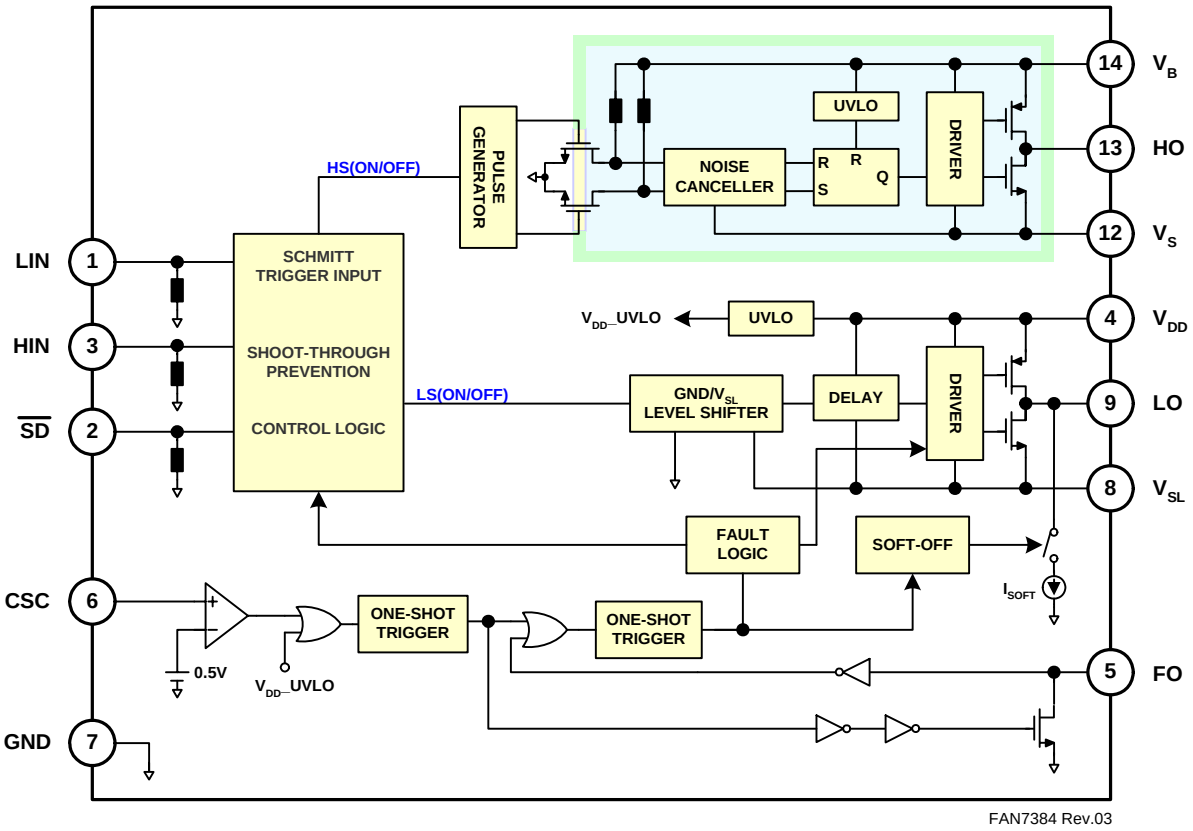


**Figure 3. Functional Block Diagram**

## Pin Configuration

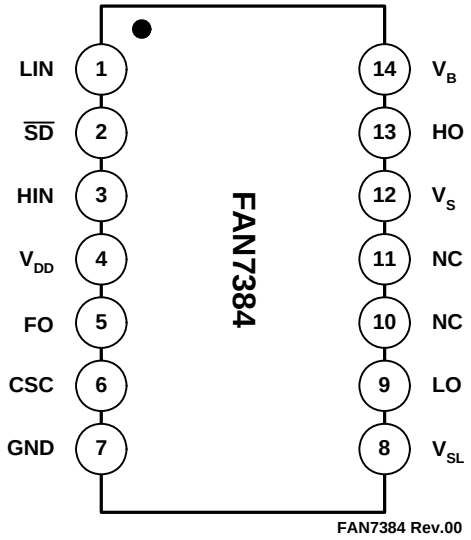


**Figure 4. Pin Configuration (Top View)**

## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| 1 | LIN | Logic Input for low-side gate driver |
| 2 | $\overline{SD}$ | Shutdown control input with active low |
| 3 | HIN | Logic Input for high-side gate driver |
| 4 | $V_{DD}$ | Low-side power supply voltage |
| 5 | FO | Bi-direction fault pin with open drain |
| 6 | CSC | Short-circuit current detection input |
| 7 | GND | Ground |
| 8 | $V_{SL}$ | Low-side supply offset voltage |
| 9 | LO | Low-side gate driver output |
| 10 | NC | Not connection |
| 11 | NC | Not connection |
| 12 | $V_S$ | High-side floating supply offset voltage |
| 13 | HO | High-side gate driver output |
| 14 | $V_B$ | High-side floating supply voltage |

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## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A$=25°C, unless otherwise specified.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_S$ | High-side offset voltage $V_S$ | $V_B$-25 | $V_B$+0.3 | V |
| $V_B$ | High-side floating supply voltage $V_B$ | -0.3 | 625 | V |
| $V_{HO}$ | High-side floating output voltage | $V_S$-0.3 | $V_B$+0.3 | V |
| $V_{DD}$ | Low-side and logic-fixed supply voltage | -0.3 | 25 | V |
| $V_{IN}$ | Logic input voltage (HIN, LIN, $\overline{SD}$) | -0.3 | $V_{DD}$+0.3 | V |
| $V_{CSC}$ | Current sense input voltage | -0.3 | $V_{DD}$+0.3 | V |
| $V_{FO}$ | Fault output voltage | -0.3 | $V_{DD}$+0.3 | V |
| $dV_S/dt$ | Allowable offset voltage slew rate | | 50 | V/ns |
| $P_D$[(2)(3)(4)] | Power dissipation | | 1.0 | W |
| $\theta_{JA}$ | Thermal resistance, junction-to-ambient | | 110 | °C/W |
| $T_J$ | Junction temperature | | 150 | °C |
| $T_S$ | Storage temperature | -55 | 150 | °C |

**Notes:**

2. Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
3. Refer to the following standards:
   JESD51-2: Integral circuits thermal test method environmental conditions - natural convection
   JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
4. Do not exceed $P_D$ under any circumstances.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_B$ | High-side floating supply voltage | | $V_S$+13 | $V_S$+20 | V |
| $V_S$ | High-side floating supply offset voltage | | 6-$V_{DD}$ | 600 | V |
| $V_{DD}$ | Supply voltage | | 13 | 20 | V |
| $V_{HO}$ | High-side output voltage | | $V_S$ | $V_B$ | V |
| $V_{LO}$ | Low-side output voltage | | GND | $V_{DD}$ | V |
| $V_{IN}$ | Logic input voltage (HIN, LIN, $\overline{SD}$) | | GND | $V_{DD}$ | V |
| $V_{FO}$ | Fault output voltage | | -0.3 | $V_{DD}$+0.3 | V |
| $T_A$ | Ambient temperature | | -40 | 125 | °C |

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## Electrical Characteristics

$V_{BIAS}$ ($V_{DD}$, $V_{BS}$) = 15.0V, $T_A$ = 25°C, unless otherwise specified. The $V_{IN}$ and $I_{IN}$ parameters are referenced to GND. The $V_O$ and $I_O$ parameters are referenced to $V_S$ and GND and are applicable to the respective outputs HO and LO.

| Symbol | Characteristics | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **LOW SIDE POWER SUPPLY SECTION** | | | | | | |
| $I_{QDD}$ | Quiescent $V_{DD}$ supply current | $V_{LIN}$=0V or 5V | | 600 | 800 | µA |
| $I_{PDD}$ | Operating $V_{DD}$ supply current | $f_{LIN}$=20kHz, rms value | | 950 | 1300 | µA |
| $V_{DDUV+}$ | $V_{DD}$ supply under-voltage positive going threshold | $V_{DD}$=Sweep | 10.9 | 11.9 | 12.9 | V |
| $V_{DDUV-}$ | $V_{DD}$ supply under-voltage negative going threshold | $V_{DD}$=Sweep | 10.4 | 11.4 | 12.4 | V |
| $V_{DDHYS}$ | $V_{DD}$ supply under-voltage lockout hysteresis | $V_{DD}$=Sweep | | 0.5 | | V |
| **BOOTSTRAPPED POWER SUPPLY SECTION** | | | | | | |
| $V_{BSUV+}$ | $V_{BS}$ supply under-voltage positive going threshold | $V_{BS}$=Sweep | 10.6 | 11.5 | 12.4 | V |
| $V_{BSUV-}$ | $V_{BS}$ supply under-voltage negative going threshold | $V_{BS}$=Sweep | 10.1 | 11.0 | 11.9 | V |
| $V_{BSHYS}$ | $V_{BS}$ supply under-voltage lockout hysteresis | $V_{BS}$=Sweep | | 0.5 | | V |
| $I_{LK}$ | Offset supply leakage current | $V_B$=$V_S$=600V | | | 10 | µA |
| $I_{QBS}$ | Quiescent $V_{BS}$ supply current | $V_{HIN}$=0V or 5V | | 50 | 90 | µA |
| $I_{PBS}$ | Operating $V_{BS}$ supply current | $f_{HIN}$=20kHz, rms value | | 400 | 600 | µA |
| **GATE DRIVER OUTPUT SECTION** | | | | | | |
| $V_{OH}$ | High-level output voltage, $V_{BIAS}$-$V_O$ | $I_O$=0mA (No Load) | | | 100 | mV |
| $V_{OL}$ | Low-level output voltage, $V_O$ | $I_O$=0mA (No Load) | | | 100 | mV |
| $I_{O+}$ | Output HIGH short-circuit pulse current | $V_O$=0V, $V_{IN}$=5V with PW<10µs | 200 | 250 | | mA |
| $I_{O-}$ | Output LOW short-circuit pulsed current | $V_O$=15V, $V_{IN}$=0V with PW<10µs | 420 | 500 | | mA |
| $V_S$ | Allowable negative $V_S$ pin voltage for IN signal propagation to $H_O$ | | | -9.8 | -7.0 | V |
| $V_{SL}$-GND | $V_{SL}$-GND/GND-$V_{SL}$ voltage educability | | -7.0 | | 7.0 | V |
| **SHUTDOWN CONTROL SECTION ($\overline{SD}$)** | | | | | | |
| $\overline{SD}$+ | Shutdown "1" input voltage | | | | 1.2 | V |
| $\overline{SD}$- | Shutdown "0" input voltage | | 2.5 | | | V |
| **LOGIC INPUT SECTION (HIN, LIN)** | | | | | | |
| $V_{IH}$ | Logic "1" input voltage | | 2.5 | | | V |
| $V_{IL}$ | Logic "0" input voltage | | | | 1.2 | V |
| $V_{INHYS}$ | Logic input hysteresis voltage | | | 0.5 | | V |
| $I_{IN+}$ | Logic "1" input bias current | $V_{IN}$=5V | 10 | 15 | 20 | µA |
| $I_{IN-}$ | Logic "0" input bias current | $V_{IN}$=0V | | | 2.0 | µA |

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## Electrical Characteristics (Continued)

$V_{BIAS}$ ($V_{DD}$, $V_{BS}$) = 15.0V, $T_A$ = 25°C, unless otherwise specified. The $V_{IN}$ and $I_{IN}$ parameters are referenced to GND. The $V_O$ and $I_O$ parameters are referenced to GND and $V_S$ is applicable to HO and LO.

| Symbol | Characteristics | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **SHORT-CIRCUIT PROTECTION** | | | | | | |
| $V_{CSCREF}$ | Short-circuit detector reference voltage | | 0.47 | 0.50 | 0.53 | V |
| $I_{CSCIN}$ | Short-circuit input current | $V_{CSCIN}$=1V, $R_{CSCIN}$=100KΩ | 5 | 10 | 15 | µA |
| $I_{SOFT}$ | Soft turn-off source current | $V_{DD}$=15V | 5 | 10 | 15 | mA |
| $-V_{CSC}$ | Negative CSC pin immunity(5) | Voltage on CSC pin up to -12V, Time<2µs | | | -20 | V |
| **FAULT DETECTION SECTION** | | | | | | |
| $V_{FINH}$ | Fault input high level voltage | | 2.5 | | | V |
| $V_{FINL}$ | Fault input low level voltage | | | | 1.2 | V |
| $V_{FINHYS}$ | Fault input hysteresis voltage(5) | | | 0.5 | | V |
| $V_{FOH}$ | Fault output high level voltage | $V_{CSC}$=0V, $R_{PULL-UP}$=4.7KΩ | 4.7 | | | V |
| $V_{FOL}$ | Fault output low level voltage | $V_{CSC}$=1V, $I_{FO}$=2mA | | | 0.8 | V |
| $t_{FO}$ | Fault output pulse width | $V_{CSCIN}$=1V | | 60 | 100 | µs |

**Note:**

5. These parameters guaranteed by design.

## Dynamic Electrical Characteristics

$T_A$=25°C, $V_{BIAS}$ ($V_{DD}$, $V_{BS}$) = 15.0V, $V_S$ = GND, $C_{Load}$ = 1000pF unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{on}$ | Turn-on propagation delay | $V_S$=0V | | 180 | 260 | ns |
| $t_{off}$ | Turn-off propagation delay | $V_S$=0V or 600V (5) | | 170 | 240 | ns |
| $t_r$ | Turn-on rise time | | | 50 | 100 | ns |
| $t_f$ | Turn-off fall time | | | 30 | 80 | ns |
| MT | Delay matching | | | | 50 | ns |
| DT | Dead-time | | 80 | 120 | 170 | ns |
| $t_{UVFLT}$ | Under-voltage filtering time(5) | | | 16 | | µs |
| $t_{CSCFLT}$ | CSC pin filtering time(5) | | | 300 | | ns |
| $t_{CSCFO}$ | Time from CSC triggering to FO(5) | | | 350 | | ns |
| $t_{CSCLO}$ | Time from CSC triggering to low-side gate output(5) | From $V_{CSC}$=1V to starting gate turn-off | | 600 | | ns |
| $t_{SDFO}$ | Shutdown to FO propagation delay(5) | | | 60 | | ns |
| $t_{SDOFF}$ | Shutdown to HIGH/LOW-side gate off(5) | | | 100 | | ns |

**Note:**

5. These parameters guaranteed by design.

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## Typical Characteristics

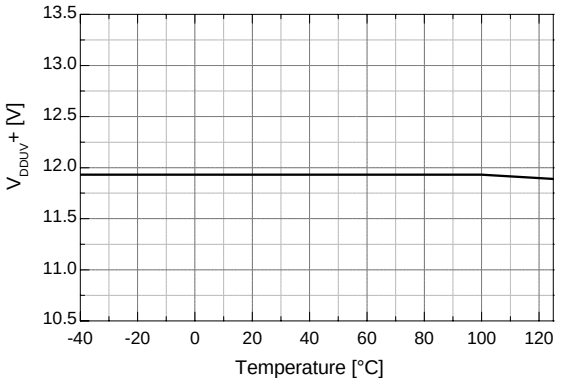


**Figure 5. $V_{DD}$ UVLO (+) vs. Temperature**

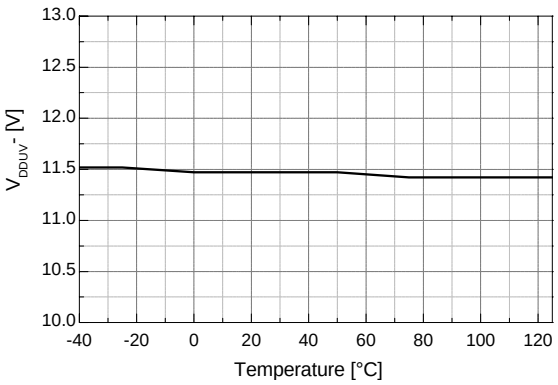


**Figure 6. $V_{DD}$ UVLO (-) vs. Temperature**

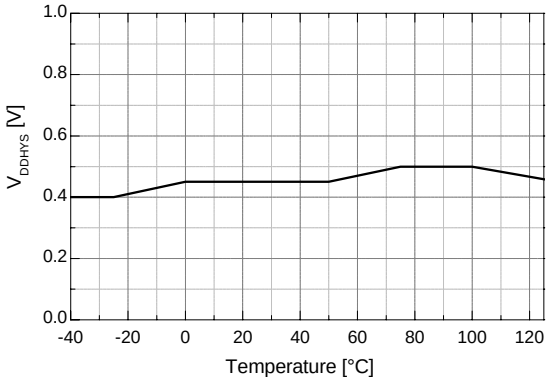


**Figure 7. $V_{DD}$ UVLO Hysteresis vs. Temperature**

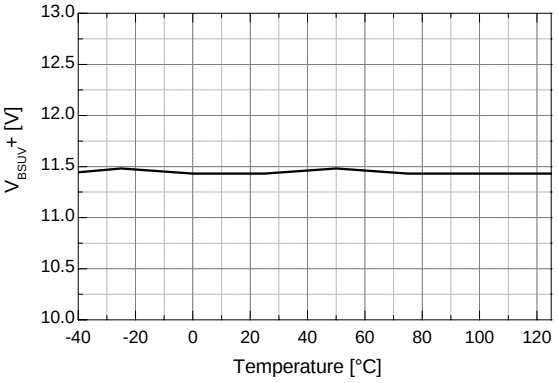


**Figure 8. $V_{BS}$ UVLO (+) vs. Temperature**

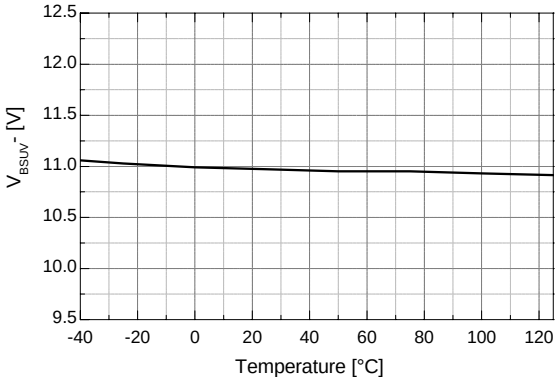


**Figure 9. $V_{BS}$ UVLO (-) vs. Temperature**

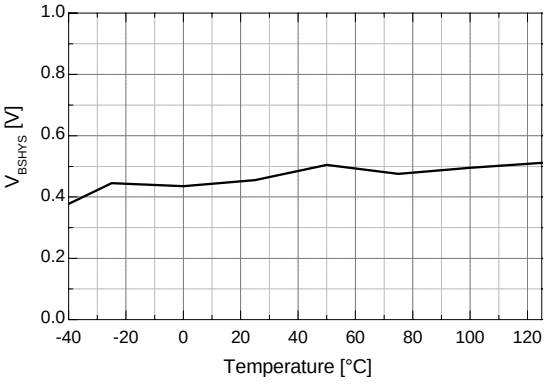


**Figure 10. $V_{BS}$ UVLO Hysteresis vs. Temperature**

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## Typical Characteristics (Continued)

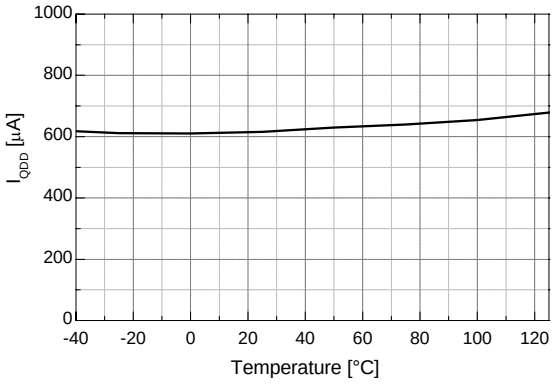


**Figure 11. $V_{DD}$ Quiescent Current vs. Temperature**

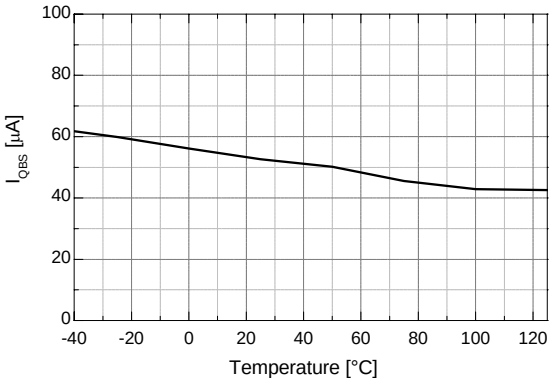


**Figure 12. $V_{BS}$ Quiescent Current vs. Temperature**

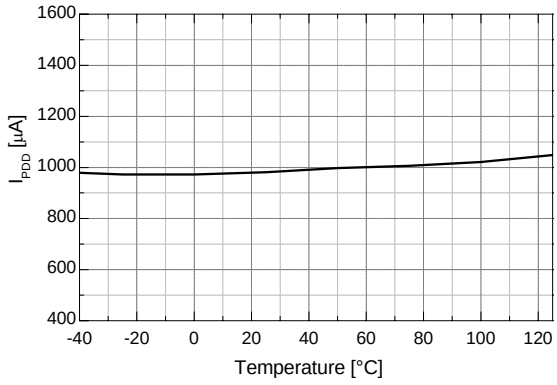


**Figure 13. $V_{DD}$ Operating Current vs. Temperature**

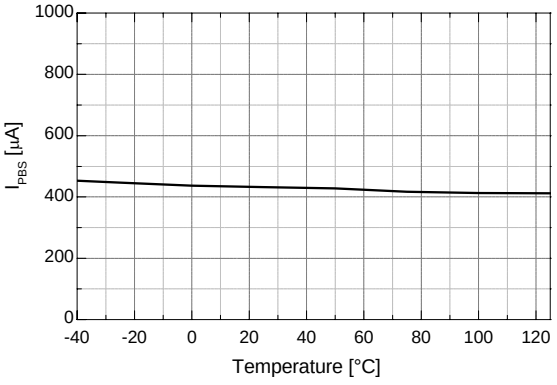


**Figure 14. $V_{BS}$ Operating Current vs. Temperature**

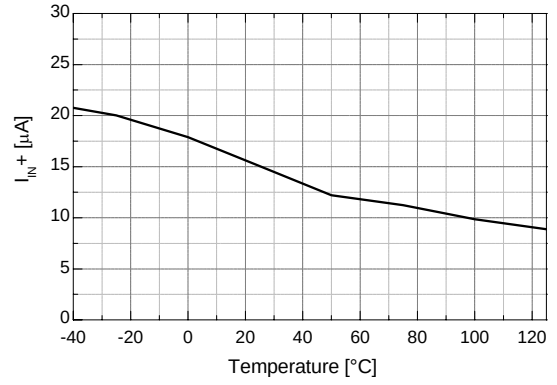


**Figure 15. Logic Input Current vs. Temperature**

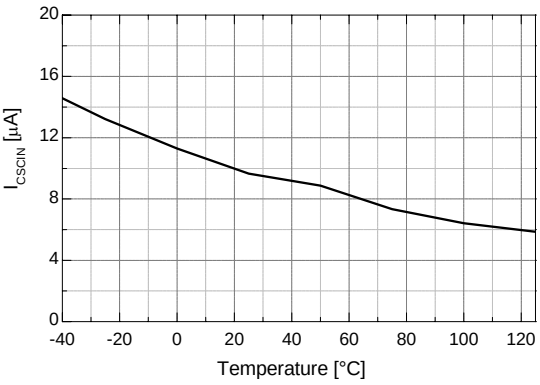


**Figure 16. $I_{CSCIN}$ vs. Temperature**

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## Typical Characteristics (Continued)

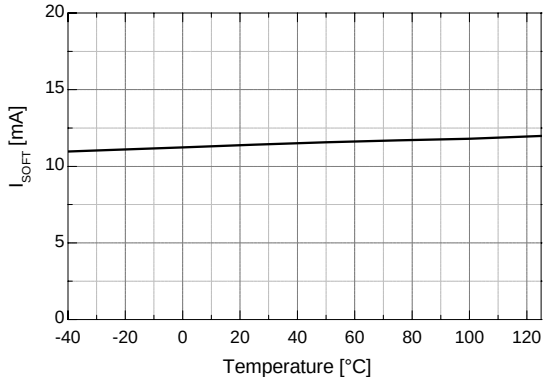


**Figure 17. $I_{SOFT}$ vs. Temperature**

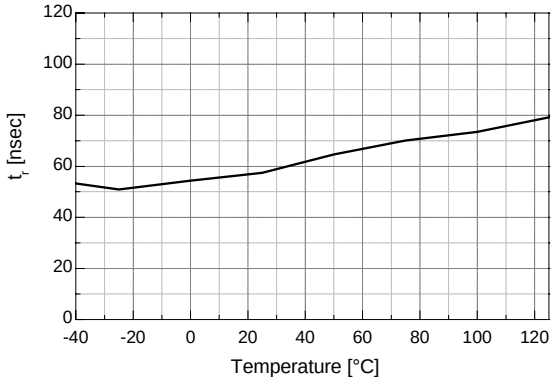


**Figure 18. Turn-on Rising Time vs. Temperature**

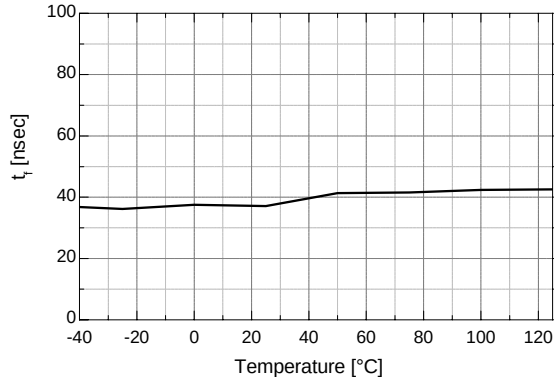


**Figure 19. Turn-off Falling Time vs. Temperature**

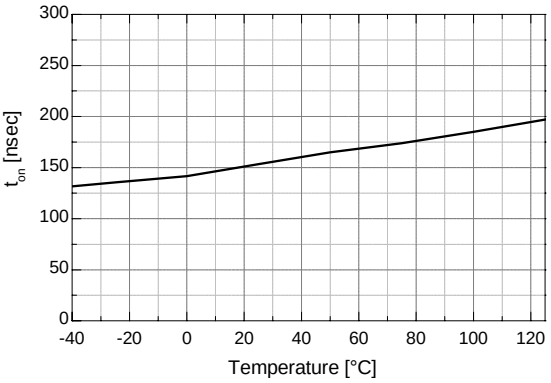


**Figure 20. Turn-on Delay Time vs. Temperature**

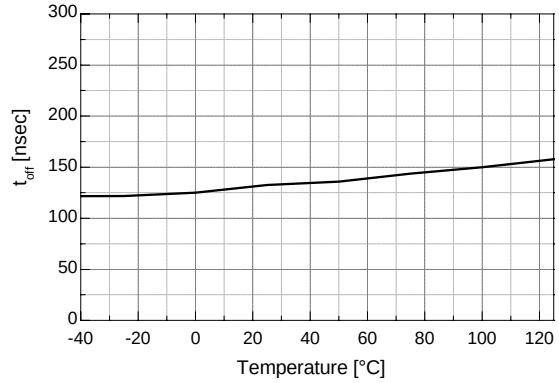


**Figure 21. Turn-off Delay Time vs. Temperature**

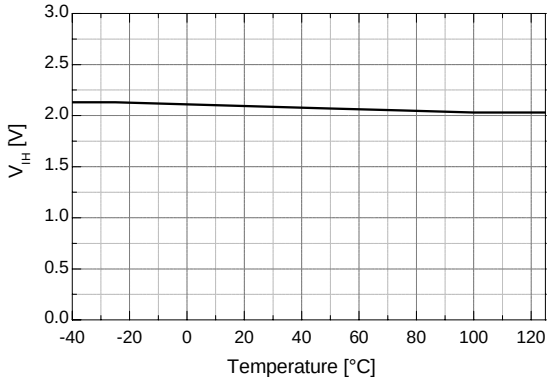


**Figure 22. Logic Input High Voltage vs. Temperature**

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## Typical Characteristics (Continued)

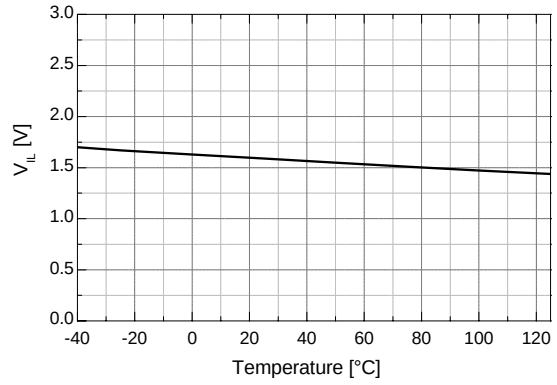


**Figure 23. Logic Input Low Voltage vs. Temperature**

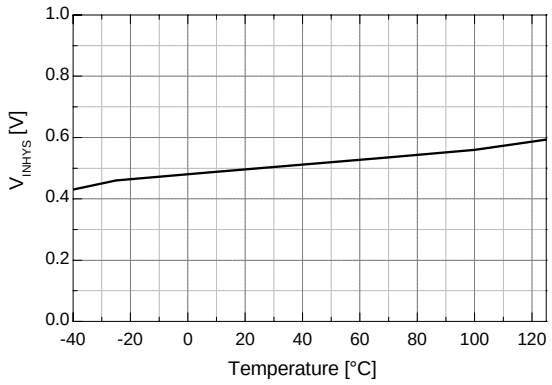


**Figure 24. Logic Input Hysteresis vs. Temperature**

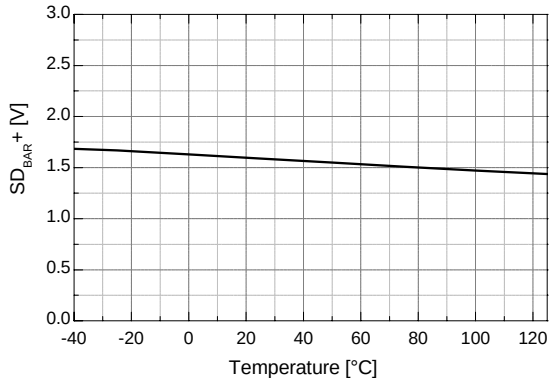


**Figure 25. $\overline{SD}$ Positive Threshold vs. Temperature**

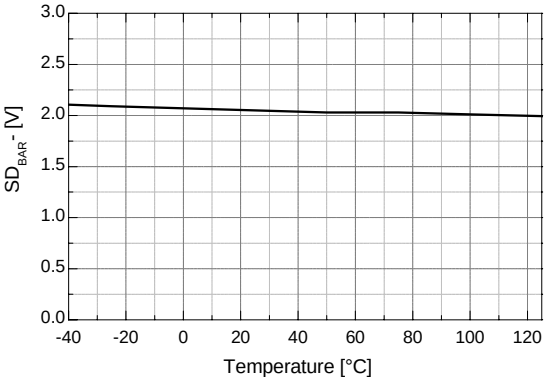


**Figure 26. $\overline{SD}$ Negative Threshold vs. Temperature**

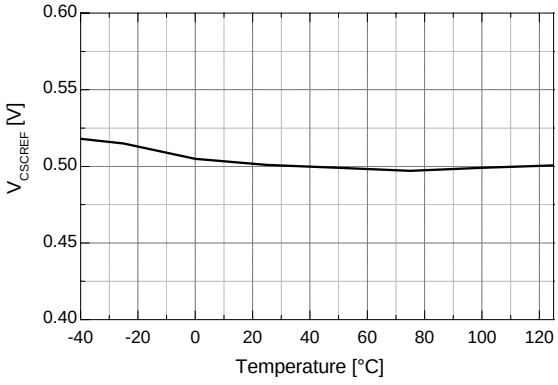


**Figure 27. $V_{CSCREF}$ vs. Temperature**

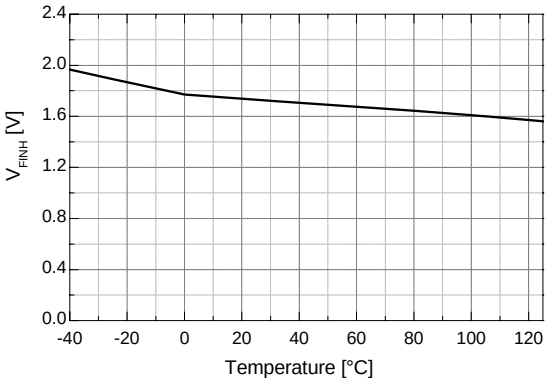


**Figure 28. Fault Input High Voltage vs. Temperature**

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## Typical Characteristics (Continued)

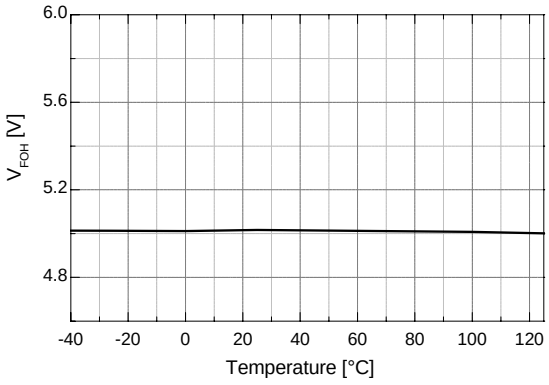


**Figure 29. Fault Output High Voltage vs. Temperature**

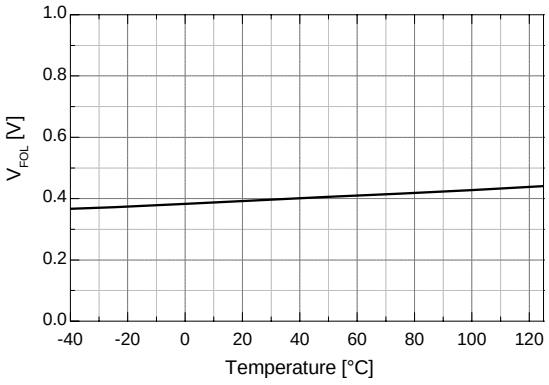


**Figure 30. Fault Output Low Voltage vs. Temperature**

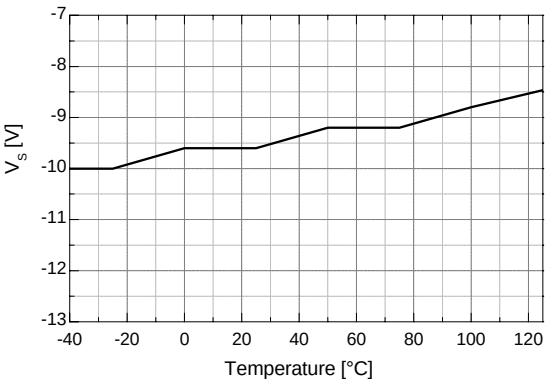


**Figure 31. Allowable Negative $V_S$ Voltage for Signal Propagation to High Side vs. Temperature**

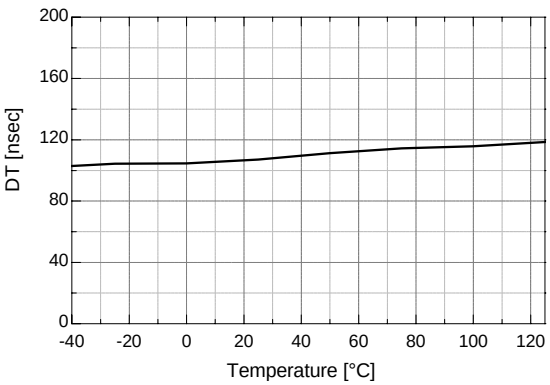


**Figure 32. Dead Time vs. Temperature**

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## Switching Time Definitions

The overall switching timing waveforms definition of FAN7384 as shown Figure 33.

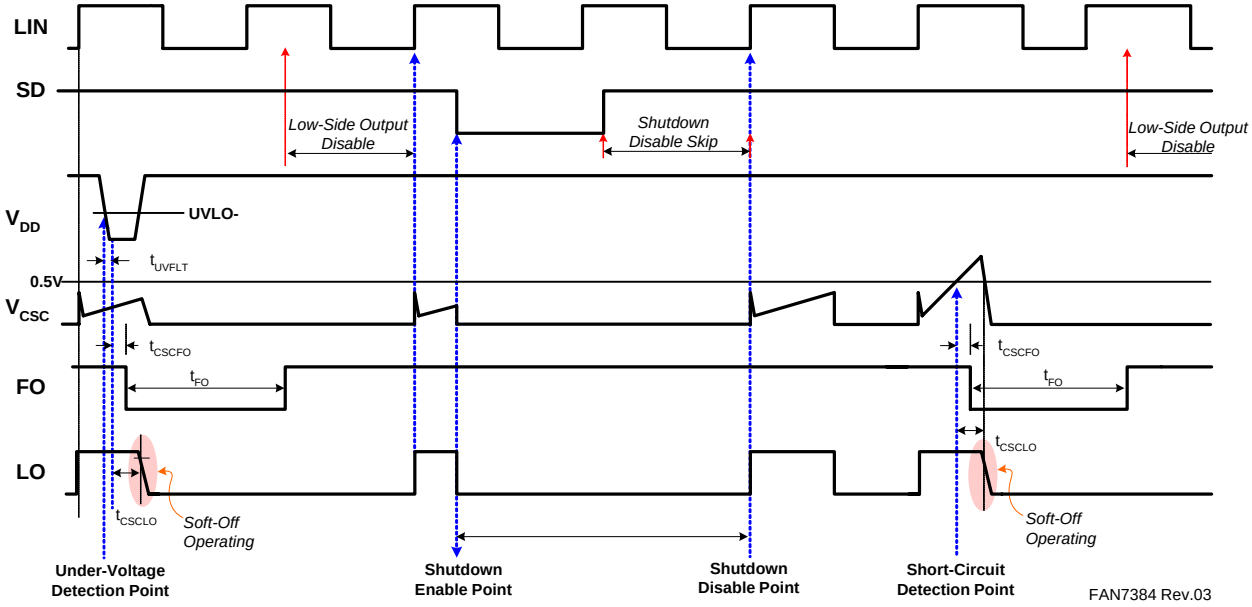


**Figure 33. Switching Timing Waveforms Definition**

# Typical Application Information

## 1. Protection Function

### 1.1 Under-Voltage Lockout (UVLO)

The high- and low-side drivers include under-voltage lockout (UVLO) protection circuitry that monitors the supply voltage ($V_{DD}$) and bootstrap capacitor voltage ($V_{BS}$) independently. It can be designed to prevent malfunction when $V_{DD}$ and $V_{BS}$ are lower than the specified threshold voltage. Moreover, the UVLO hysteresis prevents chattering during power supply transitions. If the supply voltage ($V_{DD}$) maintains an under-voltage condition over under-voltage filtering times (typically 16μs), the fault and soft-off circuits are activated, as shown Figure 34.

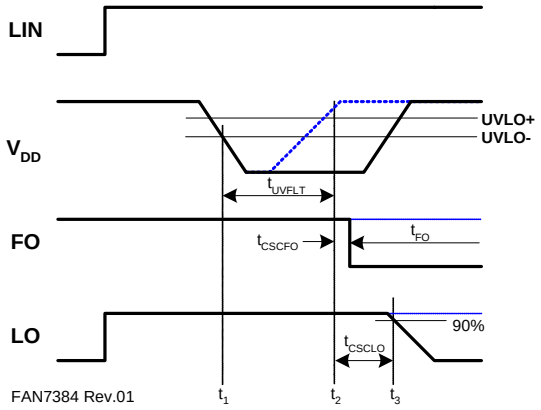


**Figure 34. Waveforms for Under-Voltage Lockout**

### 1.2 Shoot-Through Prevention Function

The FAN7384 has a shoot-through prevention circuitry that monitors the high- and low-side inputs. It can be designed to prevent outputs of high- and low-side turning on at same time, as shown Figure 35 and 36.

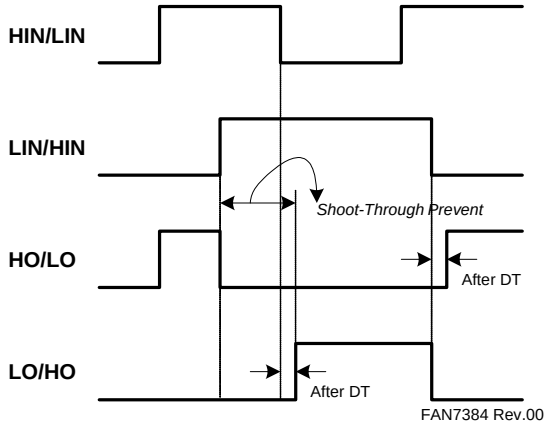


**Figure 35. Waveforms for Shoot-Through Prevention**

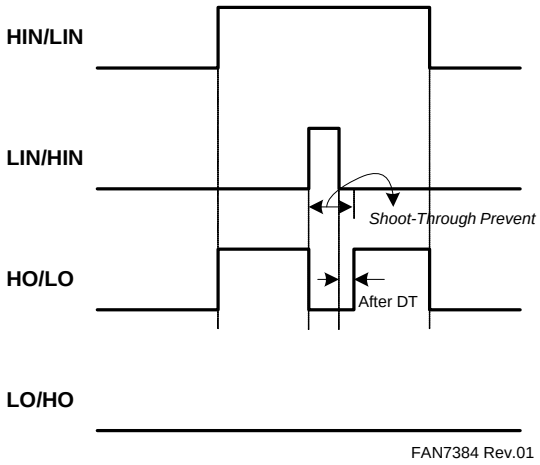


**Figure 36. Waveforms for Shoot-Through Prevention**

### 1.3 Over-Current Protection Function

The FAN7384 has over-current detection circuitry that monitors the current-by-current sensing resistor connected from the low-side switch source ($V_{SL}$) to ground.

It is a built-in time-filler from the over-current event to prevent malfunction from a noise source, such as leading-edge pulse in inductive load application, as shown Figure 37.

The sensing current is calculated as follows:

$$I_{CS} = \frac{V_{CSCREF}}{R_{CS}}[A] \quad (1)$$

where,

$V_{CSCREF}$: Reference voltage of current sense comparator

$R_{CS}$: Current sensing resistor

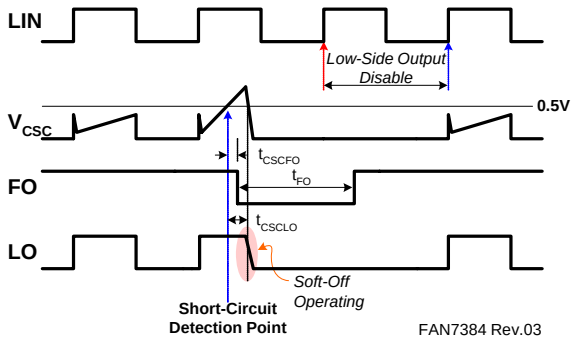


**Figure 37. Waveforms for Short-Circuit Protection**

## 2. Layout Considerations

For optimum performance, considerations must be taken during printed circuit board (PCB) layout.

### 2.1 Supply Capacitors

If the output stages are able to quickly turn on a switching device with a high value of current, the supply capacitors must be placed as close as possible to the device pins ($V_{DD}$ and GND for the ground-tied supply, $V_B$ and $V_S$ for the floating supply) to minimize parasitic inductance and resistance.

### 2.2 Gate-Drive Loop

Current loops behave like antennae, able to receive and transmit noise. To reduce the noise coupling/emission and improve the power switch turn-on and off performance, gate-drive loops must be reduced as much as possible.

### 2.3 Ground Plane

To minimize noise coupling, the ground plane should not be placed under or near the high-voltage floating side.

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## Package Dimensions

### 14-SOP

Dimensions are in millimeters unless otherwise noted.

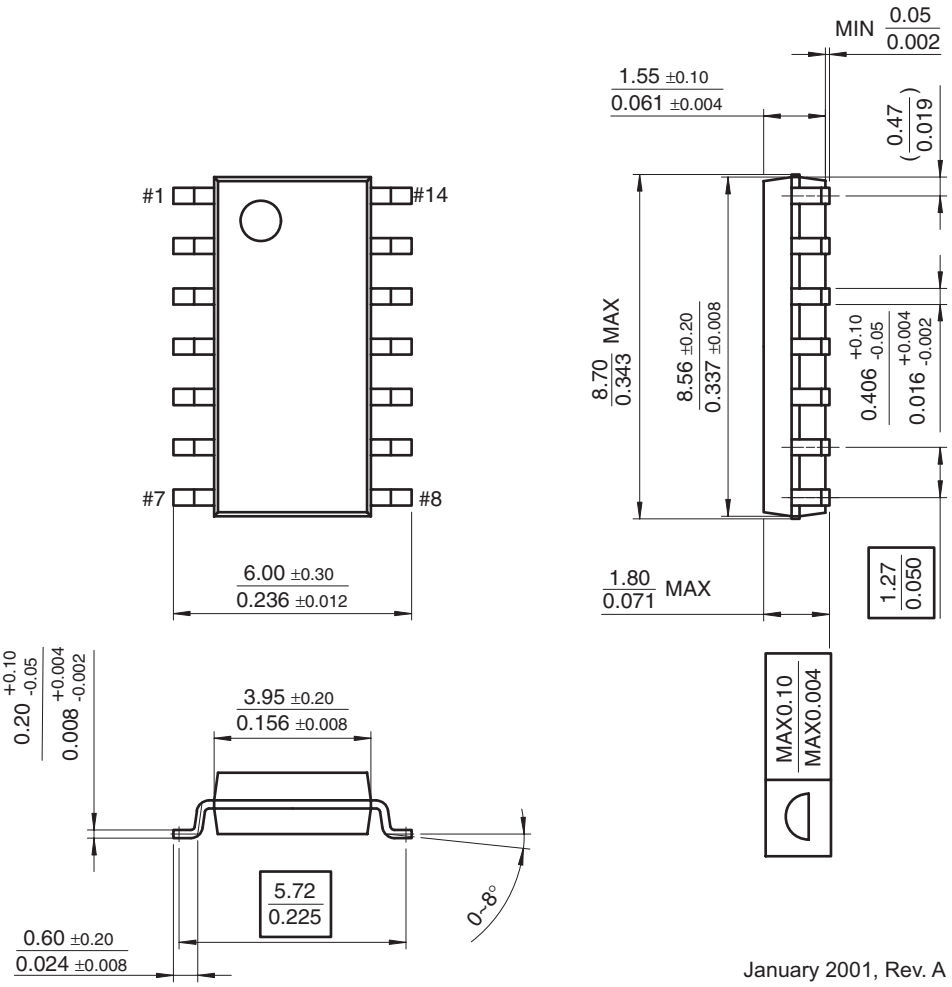


**Figure 38. 14-Lead Small Outline Package (SOP)**

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