PJ04N03D

25V N-Channel Enhancement Mode Field Effect Transistor

FEATURES

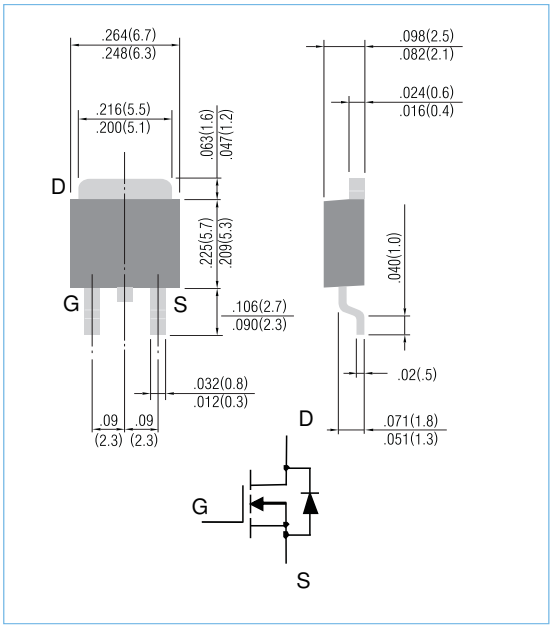
- $R_{DS(ON)}$,V_{GS}@10V,I_{DS}@30A=4mΩ
- $R_{DS(ON)}$,V_{GS}@5.0V,I_{DS}@24A=6mΩ

- Advanced trench process technology
- High Density Cell Design For Uitra Low On-Resistance
- Specially Designed for DC/DC Converters and Motor Drivers
- Fully Characterized Avalanche Voltage and Current
- In compliance with EU RoHS 2002/95/EC directives

MECHANICALDATA

- Case : TO-252 Molded Plastic
- Terminals : Solderable per MIL-STD-750,Method 2026
- Marking : 04N03D

TO-252 Unit: inch (mm)



Maximum RATINGS and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		Symbol	Limits	Units
Drain-Source Voltage		V_{DS}	25	V
Gate-Source Voltage		V_{GS}	±20	V
Continous Drain Current	T_C=25°C	I_D	80	A
Pulsed Drain Current (1)		I_{DM}	220	A
Avalanche Energy L=0.1mH,I_D=53A,V_{DD}=25V		E_{AS}	140	mJ
Power Dissipation	T_C=25°C	P_D	100	W
	T_C=75°C		66	
Operating Junction and Stroage Temperature Range		T_J,T_{STG}	-55 to +175	°C
Junction-to-Case		$R_{\Theta JC}$	1.5	°C/W
Junction-to-Ambient		$R_{\Theta JA}$	50	

NOTE : Pulse width limited by maximum junction temperature

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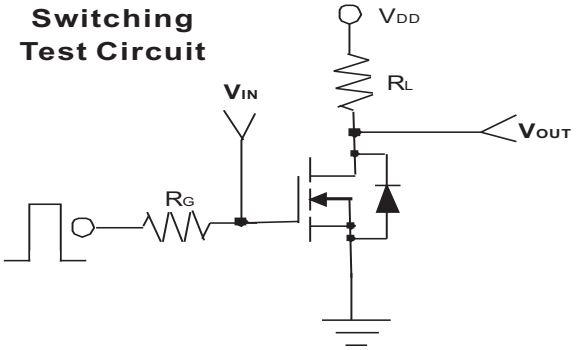
ELECTRICAL CHARACTERISTICS (T_A=25oC,Unless Otherwise Noted)

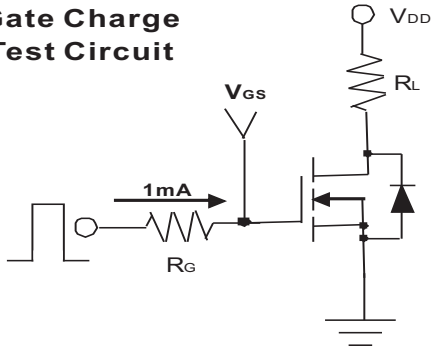
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250μA	25	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	1	-	3	V
Drain-Source On-state Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=30A	-	3.6	4.0	mΩ
		V_{GS}=5V,I_D=24A	-	4.8	6.0	mΩ
Gate-Body Leakage	I_{GSS}	V_{DS}=0V,V_{GS}=±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V	-	-	1	μA
		V_{DS}=20V,V_{GS}=0V,T_J=125°C	-	-	25	μA
On-State Drain Current	$I_{D(ON)}$	V_{DS}=10V,V_{GS}=10V	65	-	-	A
Forward Transconductance	gfs	V_{DS}=5V,I_D=24A	15	-	-	S
DYNAMIC						
Total Gate Charge	Q_G	V_{DS}=15V,V_{GS}=5V,I_D=30A	-	26.4	-	nC
		V_{DS}=15V,V_{GS}=10V I_D=30A	-	58.2	-	nC
Gate-Source Charge	Q_{GS}		-	5.4	-	nC
Gate-Drain Charge	Q_{GD}		-	11.6	-	nC
Turn-On Delay Time	td(on)	V_{DS}=15V,I_D=1A,V_{GS}=10V R_{GS}=3.6Ω	-	17.6	22	nS
Rise Time	tr		-	11.8	18	nS
Turn-Off Delay Time	td(off)		-	48.6	72	nS
Fall Time	tf		-	19.2	26	nS
Input Capacitance	C_{ISS}	V_{GS}=0V,V_{DS}=15V f=1MHz	-	2950	-	pF
Output Capacitance	C_{OSS}		-	520	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	430	-	pF
Gate Resistance	Rg	V_{GS}=15mV,V_{DS}=0V,f=1MHz	-	1.2	-	Ω
Source-Drain Diode						
Continuous Current	I_S		-	-	80	A
Forward Voltage	V_{SD}	I_F=30A,V_{GS}=0V	-	-	1.3	V

NOTE : Plus Test: Pluse Width ≤ 300us, Duty Cycle ≤ 2%.

Switching Test Circuit



Gate Charge Test Circuit



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Typical Characteristics Curves (Ta=25℃, unless otherwise noted)

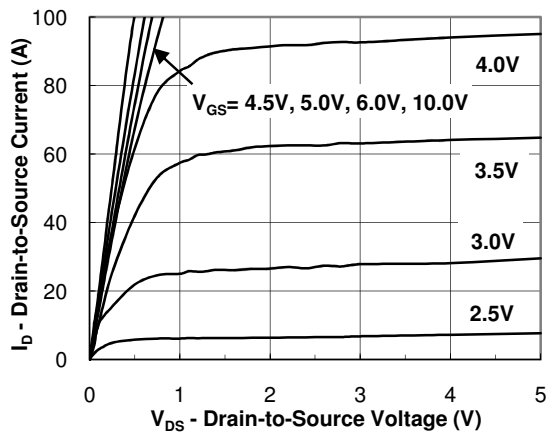

Fig.1 Output Characteristic

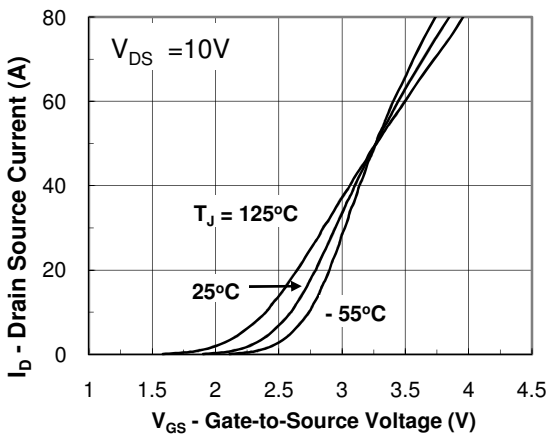

Fig.2 Transfer Characteristic

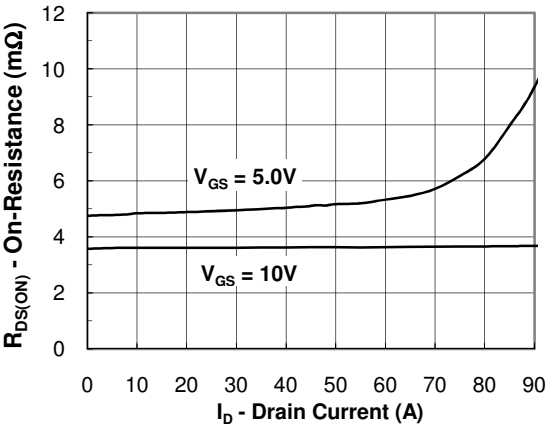

Fig.3 On Resistance vs Drain Current

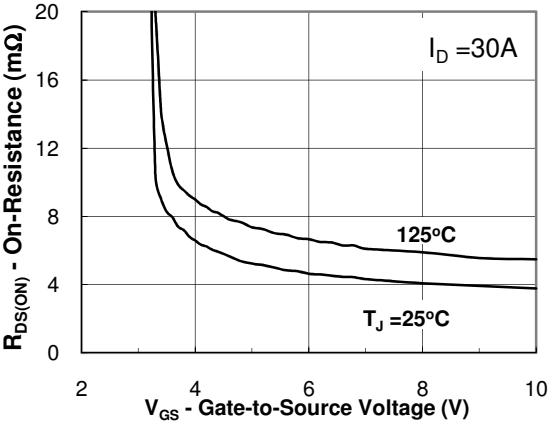

Fig.4 On Resistance vs Gate to Source Voltage

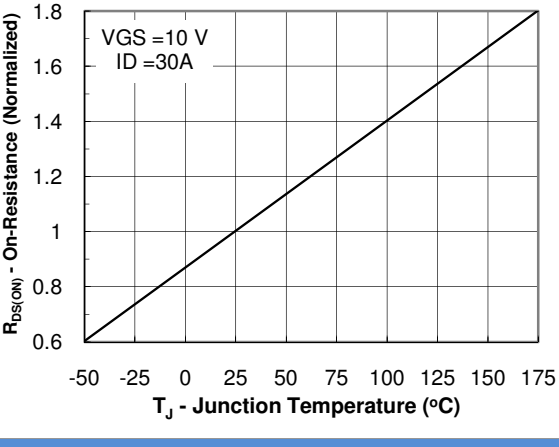

Fig.5 On Resistance vs Junction Temperature

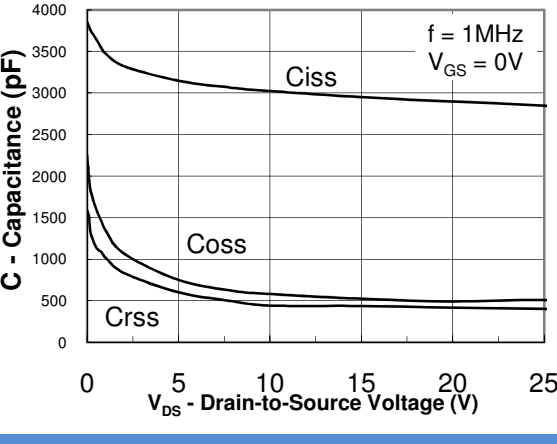

Fig.6 Capacitance

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Typical Characteristics Curves (Ta=25℃, unless otherwise noted)

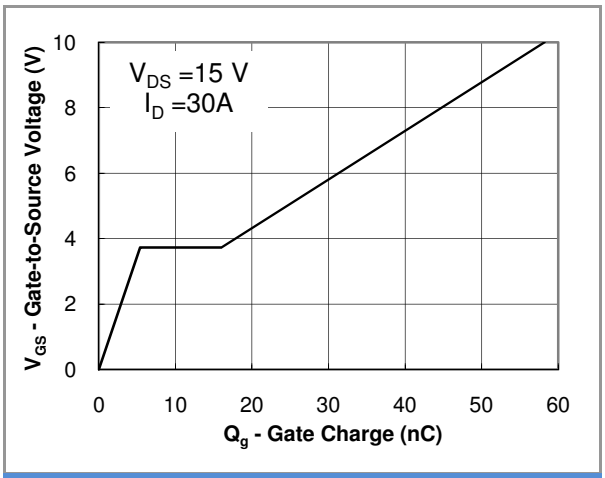

Fig. 7 Gate Charge Waveform

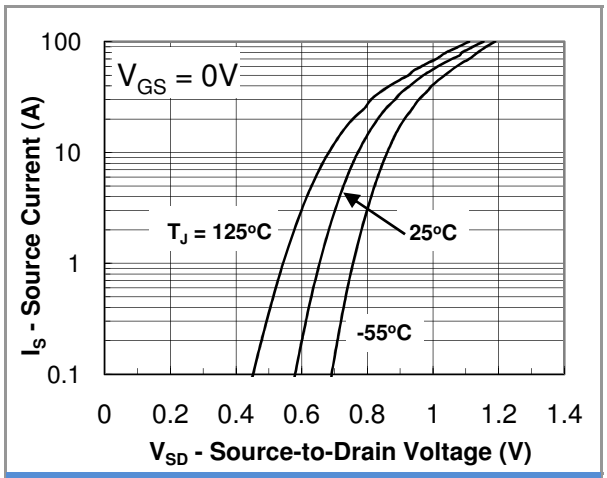

Fig.8 Source-Drain Diode Forward Voltage

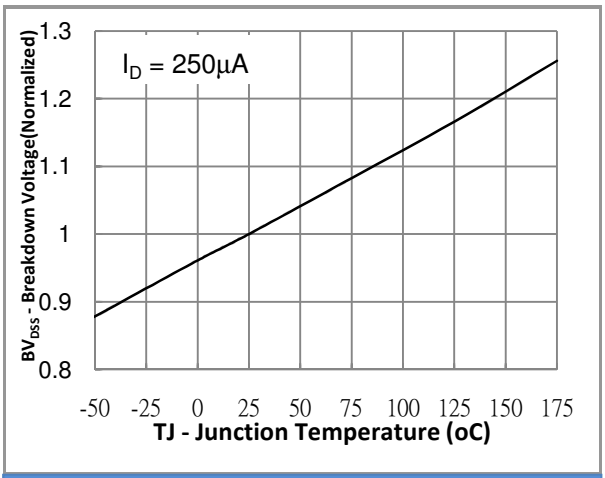

Fig.9 Breakdown Voltage vs Junction Temperature

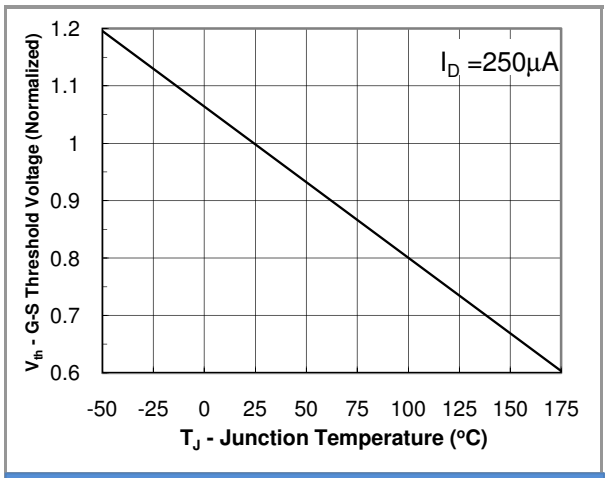

Fig.10 Threshold Voltage vs Junction Temperature

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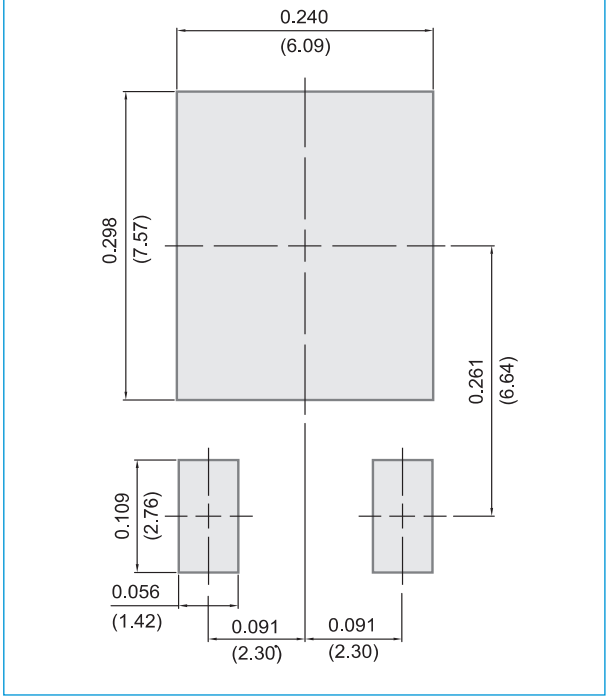
MOUNTING PAD LAYOUT

TO-252 Unit: inch (mm)



ORDER INFORMATION

- Packing information
  T/R - 3K per 13" plastic Reel

LEGAL STATEMENT