1.1 General

MB86046B is a home bus protocol controller (HBPC) for the home bus interface that complies with the "Home Bus System Standard Specifications (ET-2101) (EIAJ/REEA)" established in September, 1988.

MB86046B is a general-purpose controller usable for various services. Practically:

(1) This controller introduces sophisticated timing-control technique for easier software development while dealing with basic functions in specified layers 1 and 2.

(2) The "hardware macro" for the standard home bus interface is designed by taking system configuration flexibility into consideration. This controller is normally supplied as the "HBPC" (Custom IC for home bus interface) but will be incorporated into a macro.

(3) The noise guard function that is particularly required for system reliability is provided.

MB86046B has such excellent functions as an optimum controller to connect telephone devices, security devices, AVC devices, etc. to the home bus.

The reader should read the "Home Bus System Standard Specifications (ET-2101) (EIAJ/REEA) in advance.

1.2 Features

This IC supports the following functions:

Layer 1

- Transmission speed (9600 bps)
- Signal waveform (AMI)
- Duty (50%)
- Signal logic (negative logic)
- Collision detection and control (priority code, source address)
- Home bus data sending direction control function
- Short message interrupt detection and control
- Packet sending start point identification
- Basic format identification is possible.
- Single character sending/receiving function (start-stop synchronization)

Layer 2

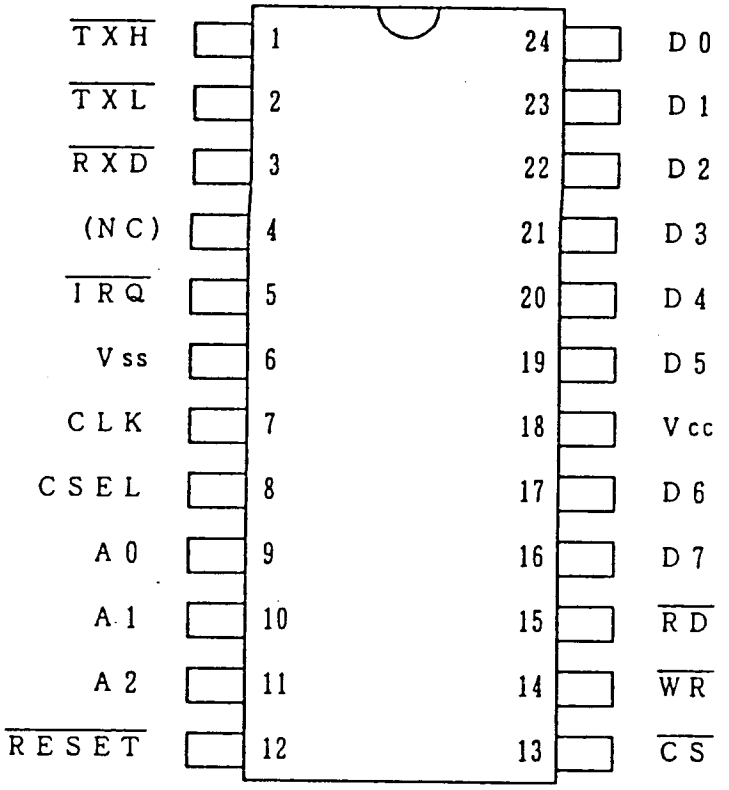
- Message length code read and count function
- Parity generation
- Broadcasting/individual call identification function
- ACK/NAK transmission register is provided.
- Error detection, data receive error, read/write lost data error, framing error, parity error, ACK/NAK error
- Dummy code

Others

- State monitoring function
- I/O TTL compatible
- Single +5 V power supply
- 24-pin dip-switch (plastic)

2.1 Pin Assignment

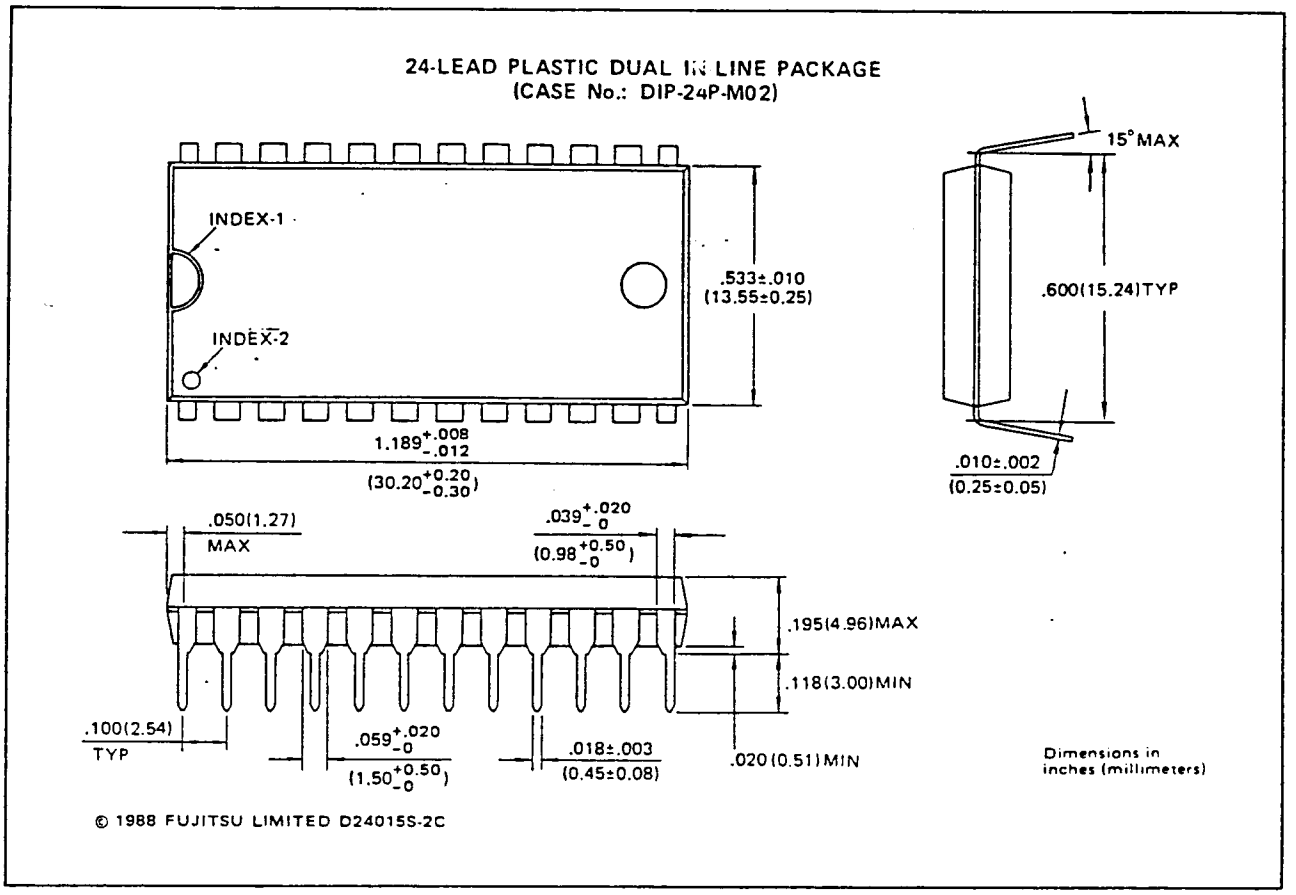
TOP VIEW



2.2 I/O Pins and Their Functions

Pin No.	Pin name	Symbol	IO	Function
3	HB data input	$\overline{RXD}$	I	Home bus control signal input pin
1	HB data (+) direction	$\overline{TXH}$	O	Home bus control signal output pin. The (+) direction data is output. The start bit is always output from this pin.
2	HB data (-) direction	$\overline{TXL}$	O	Home bus control signal output pin. The (-) direction data is output.
9-11	Register address	A_0-A_2	I	Internal register select pin. Either TXDR, RXDR, AKR, CCR, STR1, STR2, MDR, or MLC is selected with A_2, A_1, and A_0.
14	Write	$\overline{WR}$	I	When $\overline{WR}$ is set to "L" in the $\overline{CS}$ = "L" state, the CPU can write data in this IC.
15	Read	$\overline{RD}$	I	When $\overline{RD}$ is set to "L" in the $\overline{CS}$ = "L" state, data of this IC is output to the CPU data bus.
13	Chip select	$\overline{CS}$	I	Chip select signal pin. When $\overline{CS}$ = "L", data transfer to or from the CPU is enabled.
12	Reset	$\overline{RESET}$	I	When $\overline{RESET}$ is set to "L", all sending and receiving operations end. The resetting period should be held for at least 3.2 s.
24-19 17-16	Data I/O	D_0-D_5 D_6-D_7	I/O	8-bit bidirectional three-state I/O pin. When $\overline{CS}$ = "H", this is put in the high-impedance state.
5	Interrupt	$\overline{IRQ}$	O	Interrupt request pin for CPU. When an interrupt occurs, the signal is set to "L".
7	Clock input	CLK	I	Basic clock input pin. A clock of 4.9152 MHz to 614.4 kHz can be input.
8	Clock select	CSEL	I	Basic clock input select pin. When CSEL = "L", 4.9152 MHz is selected. When CSEL = "H", 614.4 kHz is selected.
6	Power supply	Vss	I	GND pin
18		Vcc	I	+5 V power pin

2.3 External Dimensions (MB86046B)



3.1 Block Diagram

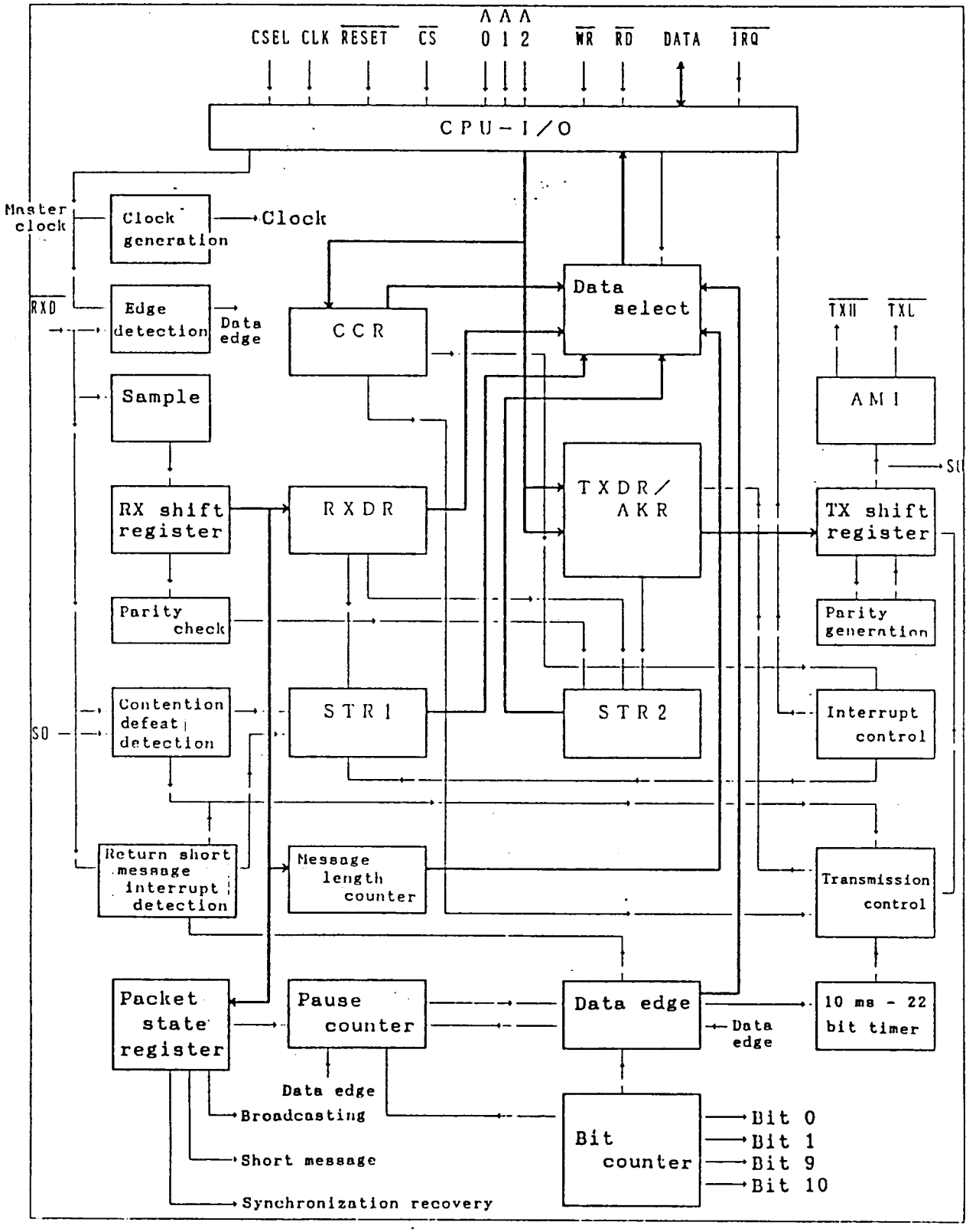


Figure 3.1 MB86046B block diagram

3.2 Start Bit Detect Function

This function eliminates noise and shows a received data error (RDE) for an incorrect message by setting the start bit detecting range.

The start bit detect function has two functions; position detection and width detection. The detect range is as follows:

- ① in Figure 3.2 is the period when the state counter is "2"
- ② through ⑧ in Figure 3.2 is the −13 µs and +26 µs period where the start bit should have been positioned
- ⑨ in Figure 3.2 is the period when the state counter is "0"

In other periods (e.g. MDR = "1"), the start bit is ignored. The sampling cycle is approximately 1.6 µs (1/614.4 kHz) for both position and width detections. (Example: 13.0 µs = 1.627 µs x 8 clocks)

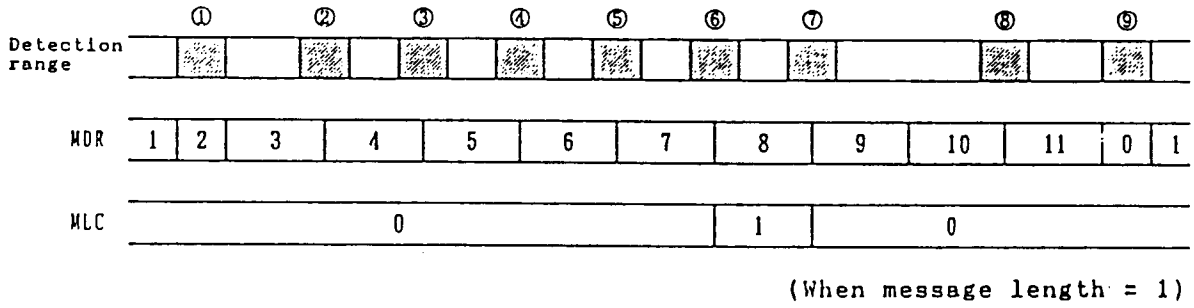


Figure 3.2 Start bit detect position

3.2.1 Position detect function

When the start bit does not come into the range of 13 μs (-) and 26 μs (+) where the start bit should be positioned (in Figure 3.3), this function judges the start bit as noise and ignores it.

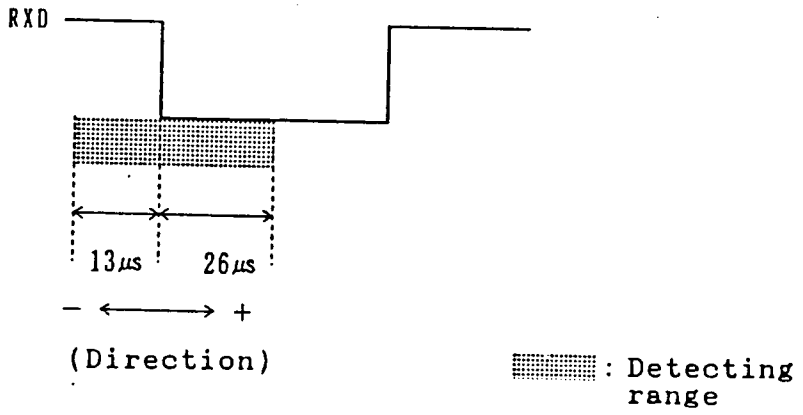


Figure 3.3 Start bit position detect range (for ② through ⑧ in Figure 3.2)

Notes for position detection:

A margin is provided after the start bit as shown in Figure 3.3 for start bit position detection. Because a case as shown in Figure 3.4 is taken into consideration.

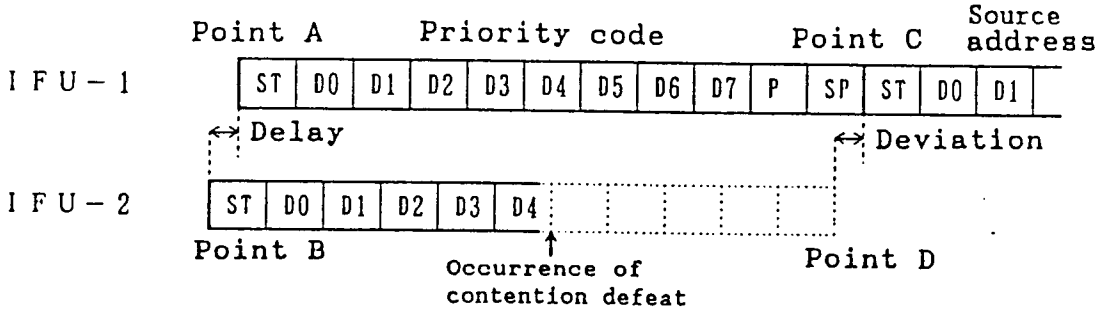


Figure 3.4 "Deviation" in contension

Figure 3.4 shows a case that IFU-2 starts sending first then IFU-1 starts sending and IFU-2 is defeated in contention with the priority code.

In this case, the top of the priority code viewed from IFU-2 is not point A but point B.

Similarly, the source address position is point D. However, IFU-2 failed contention with the priority code, so the source address position is point C.

Accordingly, a "deviation" between point C and point D is generated for IFU-2. This deviation is dependent upon the delay with the priority code. The home bus report specifies this delay as 13 μs or less.

The range after the start bit is set to 26 μs (in the + direction) for this IC, taking into account the cable delay time, so that this IC can correctly receive the start bit in such a case.

Also, the time "deviation" is considered for the ACK/NAK position where the sender and receiver are replaced by each other.

3.2.2 Width detect function

This function detects the start bit width. If the wide is larger or smaller, this function judges the start bit as noise and ignores it. If a longer noise that exceeds the detect range comes in when the state counter is "2", a received data error occurs.

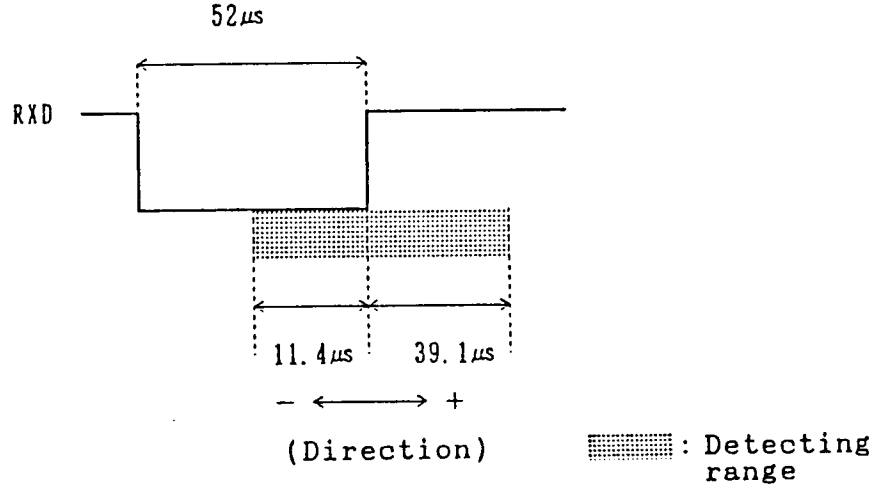
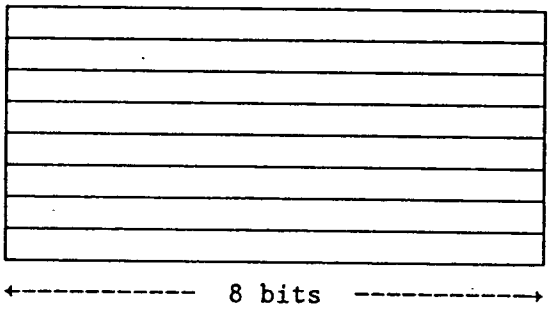


Figure 3.5 Start bit width detect range

3.3 Internal Register Functions

This IC has eight 8-bit long registers.



Register name	Address	Access
TXDR	00H	W
RXDR	01H	R
AKR	02H	W
CCR	03H	R/W (Mode 1) W (Mode 2)
STR1	04H	R
STR2	05H	R
MDR	06H	R
MLC	07H	R

3.3.1 TXDR (Transmission data register)

This is a write-only 8-bit register for sending.

Data other than ACK/NAK to be sent to the bus is written in this register. Writing data in this register automatically starts sending when sending is enabled.

This register is a write-only register. The read value is undefined. (Initial value: Undefined)

3.3.2 RXDR (Received data register)

This is a read-only 8-bit register for receiving.

The received data including ACK/NAK is put in this register. (Initial value: 00H)

3.3.3 AKR (ACK/NAK transmission register)

This is a write-only 8-bit register for ACK/NAK sending.

When a value is written in this register, data is sent to the next ACK/NAK sending enabled period. ACK/NAK can be sent for local sending. For broadcasting, short message interrupt, and errors (received data error and write lost data error) that do not require when ACK/NAK sending, ACK/NAK is not sent even though data has been set. Data is cleared for each packet, so data that spreads over packets is not sent. This register is for write only. The read value is undefined. (Initial value: Undefined)

3.3.4 Control code register (CCR)

This register has two modes; mode 1 and mode 2.

In mode 1, read and write are possible. In mode 2, this register is a write-only flag register. When write is performed, upper four bits are used to select a mode. 0H selects mode 1, while 6H selects mode 2. The lower 4-bit data is written in the register.

When read is performed, the contents is mode 1 are always read regardless of the upper four bits. The contents in mode 2 cannot be read.

When this register is reset, the RES flag only is valid and other flags (SMI, RIM, TIM) are ignored. In other words, when 0FH (SMI, RES, RIM, TIM=1) is written in the CCR upon resetting, this IC judges that 04H (RES=1) is written.

* Mode 1 (Upper 4 bits are set to 0H). (Initial value: 00H)

	7	6	5	4	3	2	1	0	Address	Access
CCR	0	0	0	0	SMI	RES	RIM	TIM	03H	R/W

[Bit 3] SMI (short message interrupt flag)

When this flag is '1', a short message interrupt is generated in the section where short message interrupt is enabled (MDR=8 for long message).

Since the short message interrupt operation works regardless of sending or receiving, the long message being sent locally can be interrupted. To start sending by short message interrupt, data (priority code) should be written in TXDR in addition to this flag. This flag is set to '0' when the state counter (MDR) changes from "0" to "1". (Initial value: 0)

[Bit 2] RES (reset flag)

When this flag changes from '1' to '0', all states are reset to the initial ones and the operation is stopped. For instance, if this flag is set to '0' during sending, sending is canceled at that point and remaining bits are not sent. The operation is started when this flag changes from '0' to '1'. (Synchronization recovery period is set.)

The initial value of this flag is '0'. This flag should be set to '1' from the CPU when resetting is made with the RESET pin or when operation of this IC is started upon power on. (Initial value: 0)

[Bit 1] RIM (receive interrupt mask flag)

This flag masks the IRQ pin output (interrupt) only. The INTR flag of STR1 is not affected.

When this flag is '0', the IRQ pin output (interrupt) due to factor related to receiving (reception, short message interrupt, received data error, read lost data error, framing error, parity error or ACK/NAK error) is masked. When this flag is '1', the IRQ pin output is not masked.

This flag is set to '1' (i.e. the interrupt mask is reset) when the state counter (MDR) changes from "0" to "1" or when the synchronization recovery period is reset by timeout.

When synchronization is not set after resetting or after receiving a received data error, this IC automatically sets this flag to '0' (i.e. interrupt masked state) so that any interrupt will not be caused by undefined received data. This flag therefore does not have to be rewitten.

Setting this flag to '1' forcibly from the CPU can generate interrupt by undefined received data. (Initial value: 0)

[Bit 0] TIM (transmission interrupt mask flag)

This flag masks the IRQ pin output (interrupt) only. The INTR flag of STR1 is not affected.

When this flag is '0', the IRQ pin output (interrupt) due to a factor related to sending (sending, contention defeat, or write lost data error) is masked. When this flag is '1', the IRQ pin output is not masked.

This flag is set '1' (i.e. the interrupt mask is reset) when the state counter (MDR) changes from "0" to "1" or when the synchronization recovery period is reset by timeout. (Initial value: 0)

* Mode 2 (Upper four bits are set to 6H.)

This mode should be used for special purposes or for future expansion of functions. Normally, this mode should not be used.

	7	6	5	4	3	2	1	0	Address	Access
CCR	0	1	1	0	-	-	WBRC	LMES	03H	W

[Bit 1] WBRC (broadcasting)

When '1' is set in this flag, this IC treats the packet being sent or received as the "broadcasting" packet. When '0' is set, this IC treats the packet being sent or received as the "individual call" packet.

Although this flag cannot be read, completion of write can be checked with the broadcasting flag (BRC) because this flag rewrites the broadcasting flag (BRC) value.

Note:

This IC sets the broadcasting flag (BRC) value when the state counter changes from "3" to "4". Rewrite the broadcasting flag value with the WBRC flag later.

[Bit 0] LMES (long message)

When this flag is set to '1', this IC treats the packet being sent or received as the "long message" packet. When '0' is set, this IC treats the packet being sent or received as the "short message" packet.

This flag cannot be read nor directly checked.

Note:

This IC judges the short message or long message when the state counter changes from "3" to "4". Rewrite the long message or short message with the LMES flag later.

3.3.5 STR1 (status register 1)

This is a read only flag register that shows the state on the bus or of the packet. (Initial value: 00H)

	7	6	5	4	3	2	1	0	Address	Access
STR1	INTR	RSMI	CD	TX	ERR	BRC	RXRDY	TXRDY	04H	R

[Bit 7] INTR (interrupt flag)

This flag is set to '1' to indicate interrupt to the CPU when data I/O interrupt is required.

This flag is set to '0' when STR1 is read, when the state counter (MDR) changes from "0" to "1", or when the state counter (MDR) changes from "0" to "2" in the synchronization recovery period.

The difference between this flag and IRQ pin is that the IRQ pin uses negative logic while this flag uses positive logic and that the IRQ pin is masked with the mask flags (RIM, TIM) while this flag is not masked. (Initial value: 0)

[Bit 6] RSMI (short message interrupt flag)

This flag is set to '1' when short message interrupt is detected (i.e. when the stop bit is set to "0" in the data of the long message).

This flag is set to '0' when the state counter (MDR) changes from "0" to "1" or when the state counter (MDR) changes from "0" to "2" in the synchronization recovery period.

The long message is judged by using "bit 0 and bit 1 of the priority code". (See Table 4.1.)

When this flag is set to '1' (i.e. when short message interrupt occurs), the framing error (FE) flag is not set. (Initial value: 0)

[Bit 5] CD (contention defeat flag)

This flag is set to '1' when "contention failure" occurs. "Contention defeat" occurs when the received data is different from the sent data in bits of "priority code" and "source address". Therefore, "contention defeat" occurs when the start bit, parity bit, or stop bit is different.

This flag is set to '0' when the state counter (MDR) changes from "0" to "1" or when the state counter (MDR) changes from "0" to "2" in the synchronization recovery period. (Initial value: 0)

[Bit 4] TX (transmission flag)

This flag is set to '1' when data is sent. However, this flag is not set to '1' when ACK/NAK is sent after data receiving.

This flag is set to '0' when the state counter (MDR) changes from "0" to "1" or when the state counter changes from "0" to "2" in the synchronization recovery period. Upon contention defeat, this flag is set to '0' when the state counter changes next. (Initial value: 0)

[Bit 3] ERR (error flag)

This flag is an ORed result of error flags (RDE, WLD, RLD, FE, PE, AKE) of status register 2. This flag is set to '1' when any error flag of status register 2 is set to '1'.

This flag is set to '0' when status register 2 is read, when the state counter (MDR) changes from "0" to "1", or when the state counter (MDR) changes from "0" to "2" in the synchronization recovery period. (Initial value: 0)

[Bit 2] BRC (broadcasting flag)

This flag is set to '1' when the message being received is a "broadcasting packet". This flag is set to '0' when the message being received is an "individual packet".

This flag is set to the value of "bit 6 of the priority code" when the state counter (MDR) changes from "3" to "4". (See Table 3.1.)

This flag is set to '0' when the state counter (MDR) changes from "0" to "1" or when the state counter (MDR) changes from "0" to "2" in the synchronization recovery period. (Initial value: 0)

[Bit 1] RXRDY

This flag is set to '1' when data transfer to the CPU is enabled.

This flag is set to '0' when the CPU reads RXDR, when the state counter (MDR) changes from "0" to "1", or when the state counter (MDR) changes from "0" to "2" in the synchronization recovery period. (Initial value: 0)

[Bit 0] TXRDY

This flag is set to '1' when data can be received from the CPU.

This flag is set to '0' when the CPU writes data in TXDR. (* Initial value: 0)

* This flag is set to '0' after power is turned on. This flag is set to '1' immediately after '1' is written to the RES flag field (during IC activation).

3.3.6 STR2 (status register 2)

This is a read-only flag register that indicates an error on the bus or of the packet.

Bit 7 through bit 2 are error flags, which are set when an error occurs. The clear condition for each error flag is as follows:

- RDE and WLD are set to '0' when this register is read or when the state counter (MDR) changes from "0" to "2" in the synchronization recovery period.

- RLD, FE, PE, and AKE are set to '0' when this register is read, when the state counter (MDR) changes from "0" to "1", or when the state counter (MDR) changes from "0" to "2" in the synchronization recovery period. (Initial value: 01H)

  Note:

  Read this register after checking that the error flag (ERR) of status register 1 has been applied.

	7	6	5	4	3	2	1	0	Address	Access
STR2	RDE	WLD	RLD	FE	PE	AKE	0	DRE	05H	R

[Bit 7] RDE (received data error flag)

This flag is set to '1' when the start bit cannot be detected in the start bit detecting range (See 3.2) in the packet, when data is put when the state counter (MDR) is "0" (i.e. at the position where data is not present normally), or when the state counter is "2" and a long noise (longer than the width detecting range) is input.

This flag does not operate when the start bit has not been normally detected in ACK/NAK.

When a received data error occurs, the synchronization recovery period is started. (Initial value: 0)

[Bit 6] WLD (write lost data flag)

This flag is set to '1' when the next character data is not written in the transmission data register (TXDR) before the parity bit of the character being sent ends (approximately 1.04 ms).

Sending is stopped when a write lost data error occurs. In this case, data is lost in mid-session. A received data error also occurs and the synchronization recovery period is started. (Initial value: 0)

[Bit 5] RLD (read lost data flag)

This flag is set to '1' when next data is input from the bus while data is present in the received data register (RXDR). (In this case, the RXDR value is replaced with a new one.)

Reading STR2 sets this flag to "0". The basic reason of the error is, however, that RXDR has not been read. This flag is set for each character until RXDR is read. (Initial value: 0)

[Bit 4] FE (framing error flag)

This flag is set to '1' when "0" is detected as the stop bit in the long message excluding the data portion. In the data portion of the long message, the short message interrupt flag (RSMI) is set to '1' and this flag does not work. (Initial value: 0)

[Bit 3] PE (parity error flag)

This flag is set to '1' when a parity error is detected. Even-number parity is used. (Initial value: 0)

[Bit 2] AKE (ACK/NAK error flag)

This flag is set to '1' when the ACK/NAK start bit cannot be detected from the start bit detecting range (See 3.2). (Initial value: 0)

[Bit 0] DRE (synchronization recovery period)

This flag is set to '1' and the synchronization recovery period starts immediately after resetting or when a received data error (RDE) or write lost data error (WLD) occurs. (The state counter changes from "0" to "2".)

When synchronization recovers and the synchronization recovery period ends, this flag is set to '0' and the normal mode is started. (Initial value: 1)

The synchronization recovery period ends when either of the following conditions is set:

① When the period data is not present on the bus continues for 10 ms + 22 bits

② When a normal packet (without parity error (PE)) is received in the synchronization recovery period.

3.3.7 MDR (state counter)

This register indicates the state of the packet being received on the bus.

This is a read-only 8-bit register in a range of 0 (00H) to 11 (0BH).

Figures 3.6 through 3.9 show examples of state counter change patterns.

Figure 3.6 shows the state counter changes for the individual packet. The counter changes from "0" to "11" in order.

Figure 3.7 shows the state counter changes for the broadcasting packet. The counter changes from "0" to "9" in order. States "10" and "11" are not provided because ACK/NAK is not provided.

Figure 3.8 shows that a packet is put in the synchronization recovery period. The difference from Figure 3.6 is that state "1" of the state counter is missing and the state counter changes from "0" to "2". When the accepted packet is a broadcasting packet, states "10" and "11" are eliminated as shown in Figure 3.7.

Figure 3.9 shows an ACK/NAK error. A feature is that state "10" is continuing twice. (The state "10" period continues by two characters.)

As another case, the state ends in the mid-session and the counter returns to zero due to an error or short message interrupt.

Table 3.1 lists the state counter values and the states. (Initial value: 00H)

Note:

The state counter value is succeeded from the previous value during the start bit to detect the position and width. (See 3.2.)

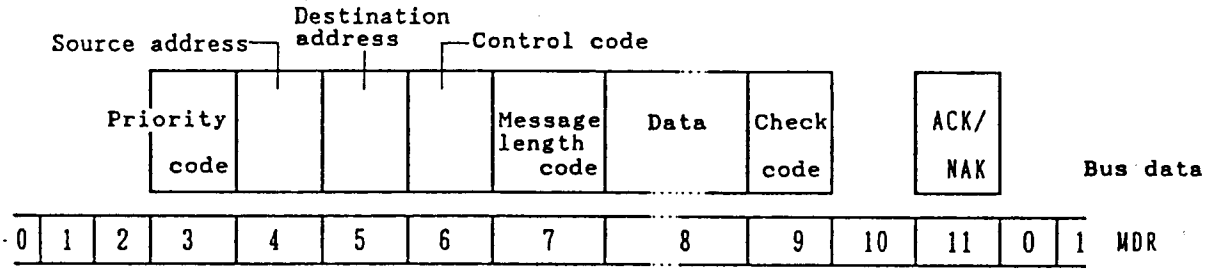


Figure 3.6 Individual packet

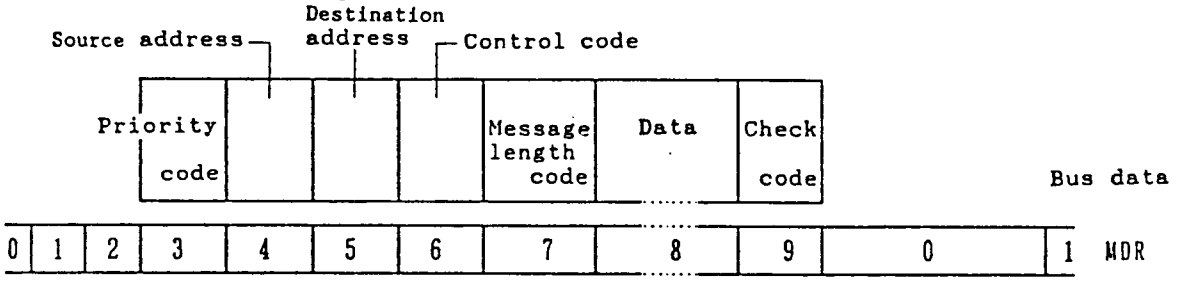


Figure 3.7 Broadcasting packet

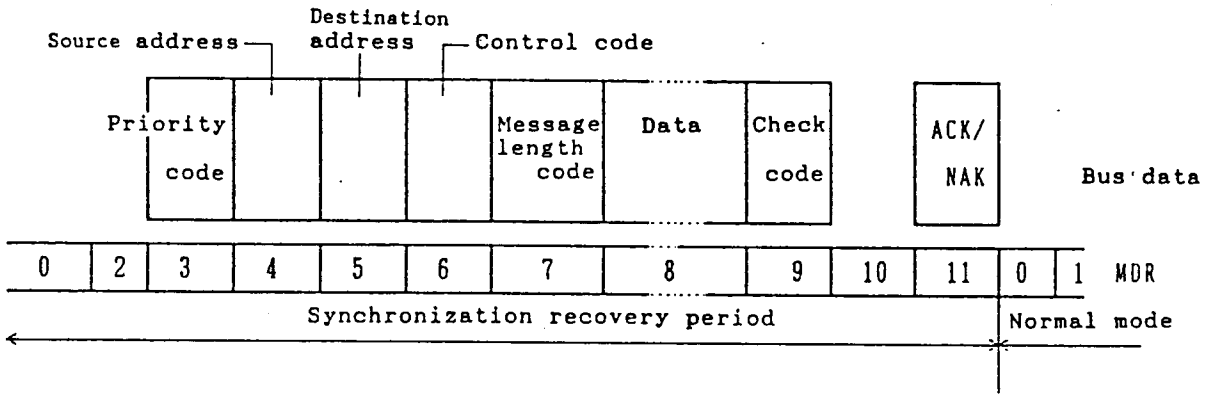


Figure 3.8 A packet put in the synchronization recovery period

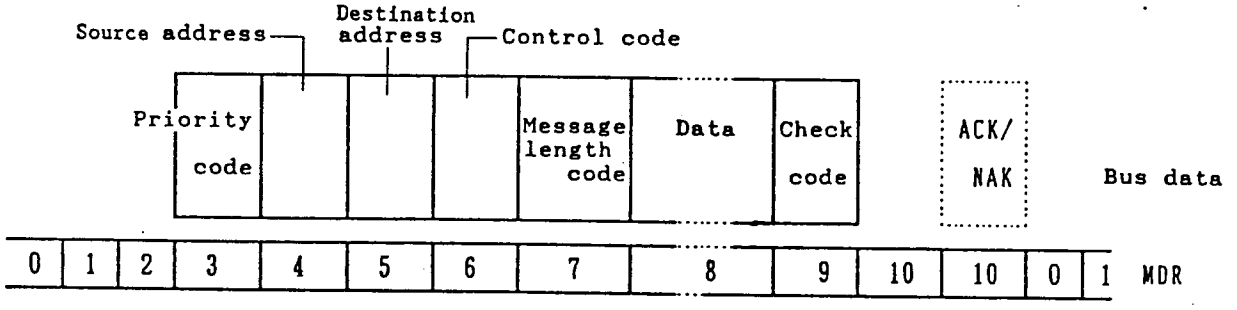
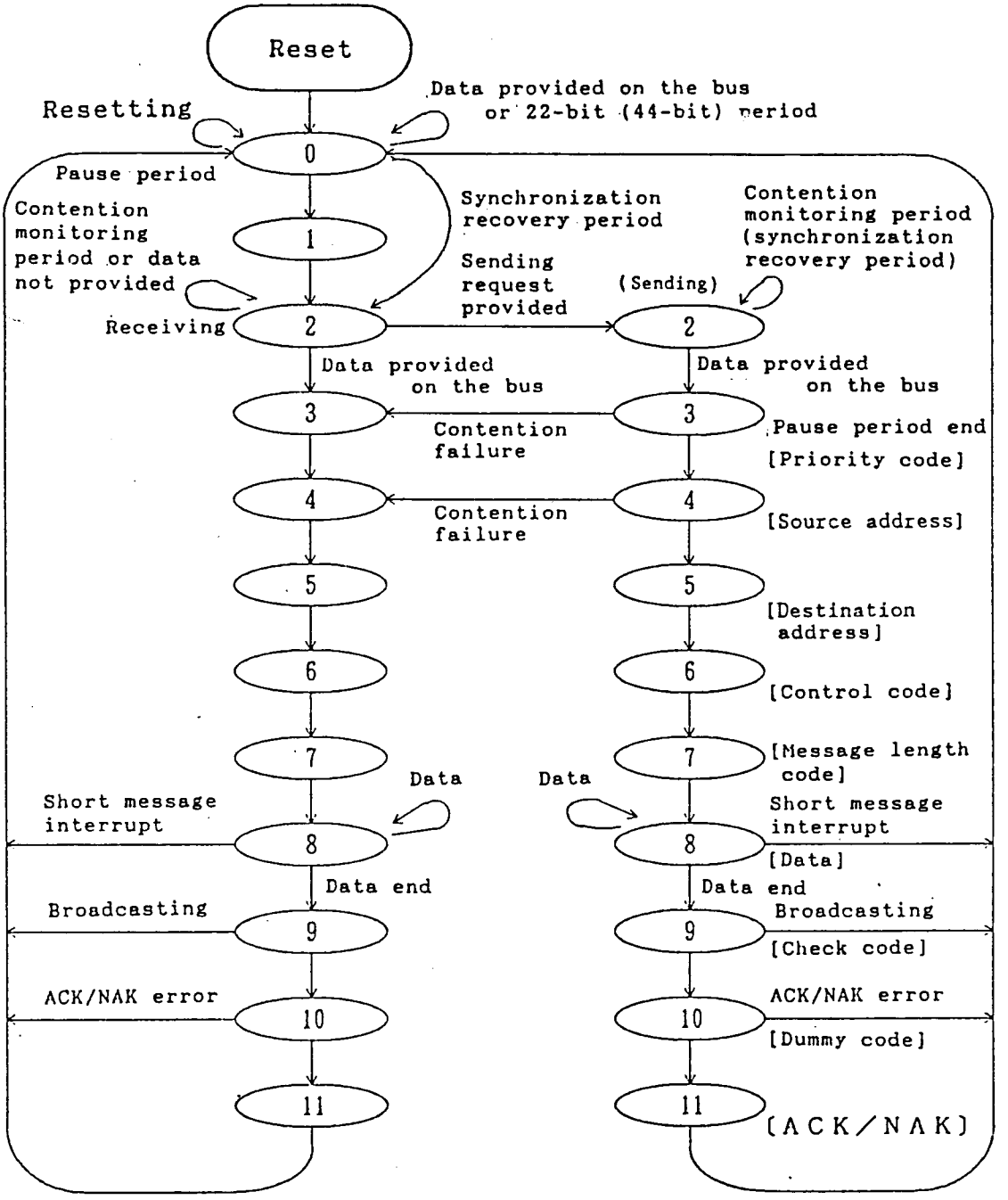


Figure 3.9 ACK/NAK error

Table 3.1 State counter values and states

State counter value	State	Time
0	Data end detection (first half of the pause period)	22 bits: individual packet 44 bits: broadcasting packet
1	Data receiving operation stop (second half of the pause period)	10 ms (96 bits) - 22 bits - 208 μs (2 bits)
2	Synchronization recovery monitoring time	2 bits (208 μs)
	Data input waiting (bus empty)	0
	Synchronization recovery operation	Maximum 10 ms (96 bits) - 22 bits
3	Priority code period	11 bits
4	Source address period	11 bits
5	Destination address period	11 bits
6	Control code period	11 bits
7	Message length code period	11 bits
8	Data period	Data amount x 11 bits
9	Check code period	11 bits
10	Dummy code period	11 bits: normal 22 bits: ACK/NAK error
11	ACK/NAK period	11 bits



Note:

- The state counter (MDR) returns to 0 for a "received data error" or "write lost data".
- Enclosed by ( ) is a state counter (MDR) value.

Figure 3.10 State changes (state counter)

3.3.8 MLC (message length counter)

This is a read-only 8-bit register that counts the message length. It is a down-counter in the range of 1 (01H) to 256 (00H).

The message length counter is always "0" unless it is at the data portion (MDR = 8). (Initial value: 00H)

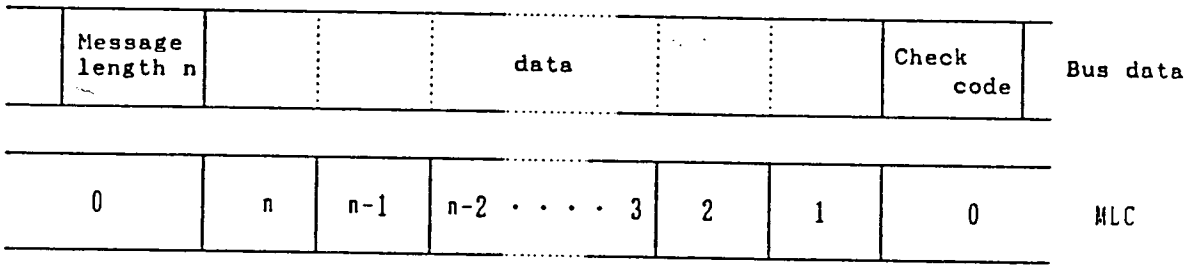


Figure 3.11 MLC (message length counter) operation

4.1 Explanation of Operation

4.1.1 Sending operation (See Figures 4.1 and 4.2.)

(1) Writing data in the transmission data register (TXDR) sets TXRDY to "0" and sending becomes ready. (①)

Transmission data can be rewritten but cannot be cleared before sending is actually started on the bus.

(2) When sending is enabled (when the pause period ends or when data is set with MDR = 2), sending is automatically started. (②)

(3) The TXRDY flag and INTR flag are set to '1', the IRQ pin is set to 'L', and interrupt is generated. The next transmission data (source address) from the CPU is requested. (③)

(4) Sending is continued in the same manner until the check code is sent. During sending, synchronization for each character is not performed.

(5) Sending or receiving is stopped (④) for one character of the dummy code, then ACK/NAK is received.

The sending operation is thus performed.

One-packet data write ends at the check code write position (⑤). The transmission data written thereafter becomes the first character of the next packet. (The priority code is sent after the pause period.)

Receiving is performed along with sending, so interrupt due to receiving (⑥) occurs after "priority code" sending.

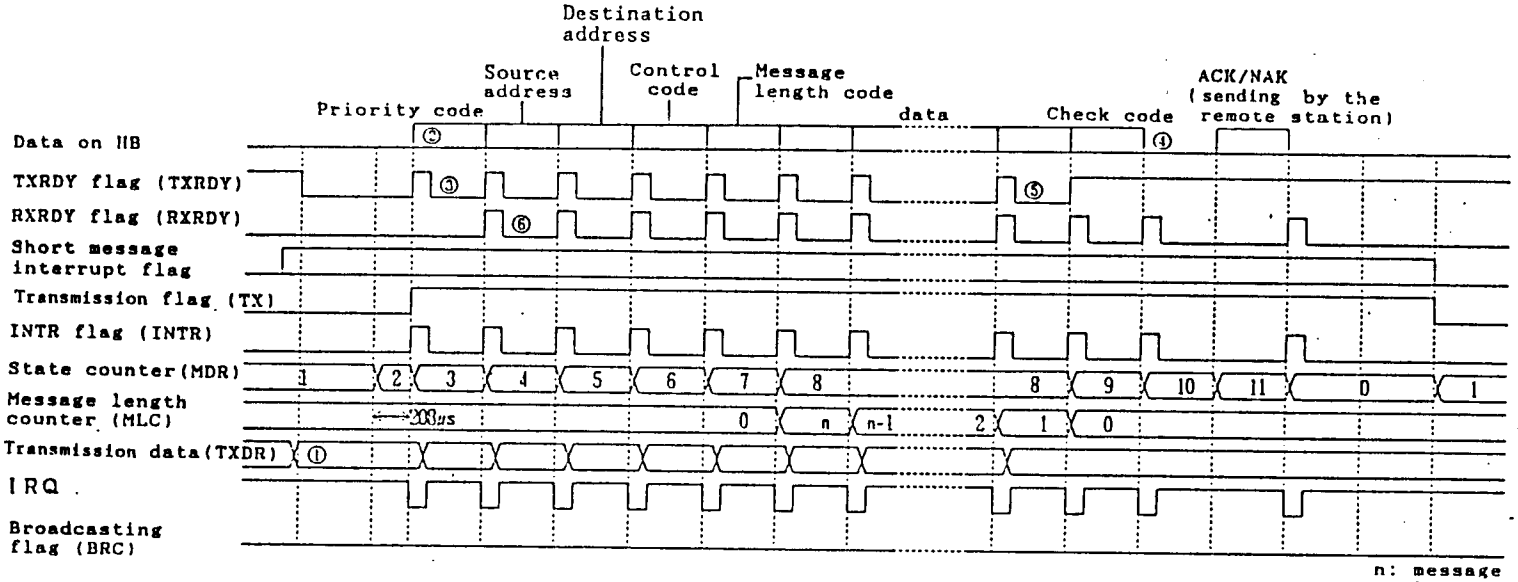


Figure 4.1 Data sending operation (individual)

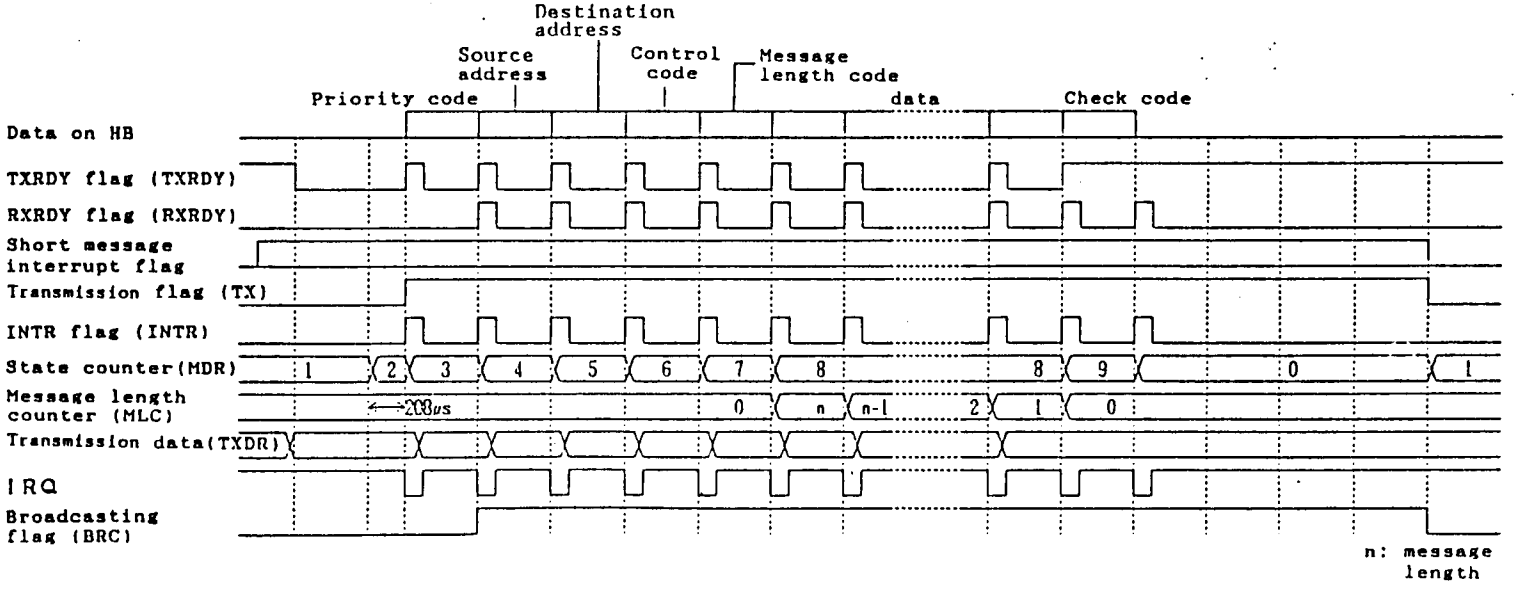


Figure 4.2 Data sending operation (broadcasting)

4.1.2 Receiving operation (See Figures 4.3 and 4.4.)

(1) Entry of data starts the receiving operation.

(2) After a character is received, the RXRDY flag and INTR flag are set to '1' and the IRQ pin is set to 'L'. Interrupt is generated and data entry is prompted to the CPU. (⑦)

Since the received data is transferred to the CPU after receiving a character, the first character (priority code) is transferred to the CPU when MDR = 4.

(3) Receiving is repeated in the same manner. Upon receiving, synchronization is performed with the start bit for each character.

(4) The final received data (ACK/NAK for individual, check code for broadcasting) is transferred to the CPU when MDR = 0. (⑧)

Long message or broadcasting is judged with bits 0 and 1 or bit 6 of the "priority code" upon sending or receiving.

Table 4.1 Conditions of long message and broadcasting

Priority code		Long message
bit 0	bit 1	
0	0	x
0	1	x
1	0	x
1	1	o

Priority code	Broadcasting
bit 6	
0	x
1	o

Note:

At o, long message or broadcasting is judged.

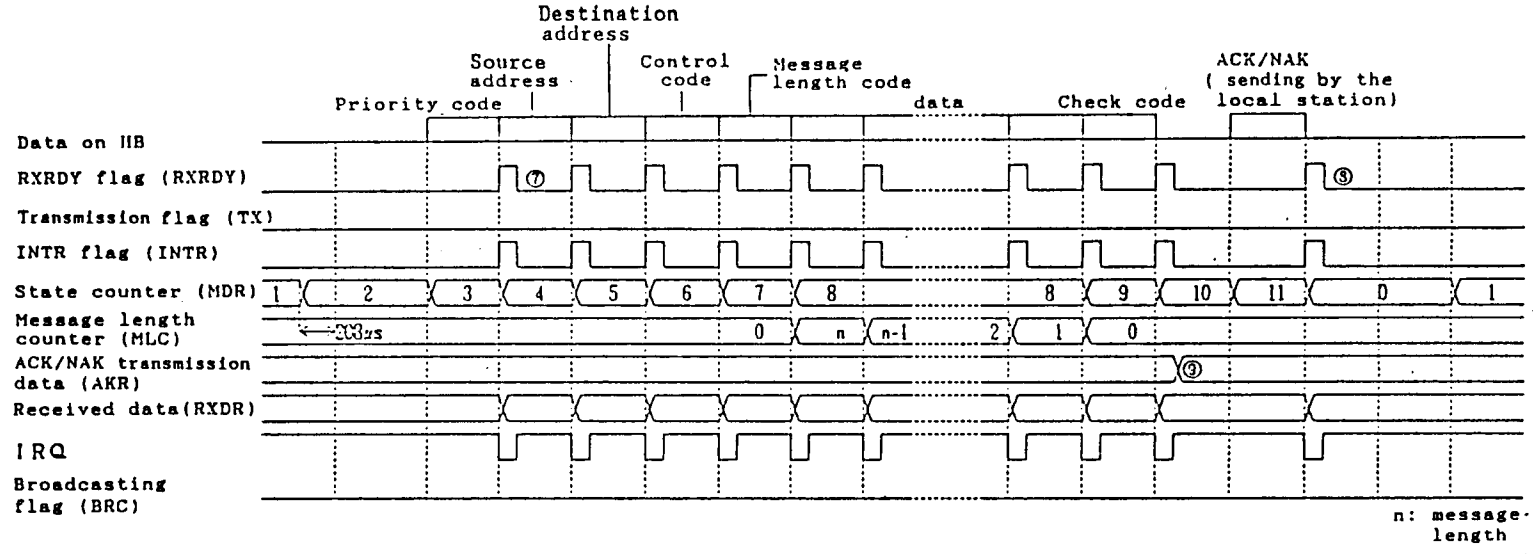


Figure 4.3 Data receiving operation (individual)

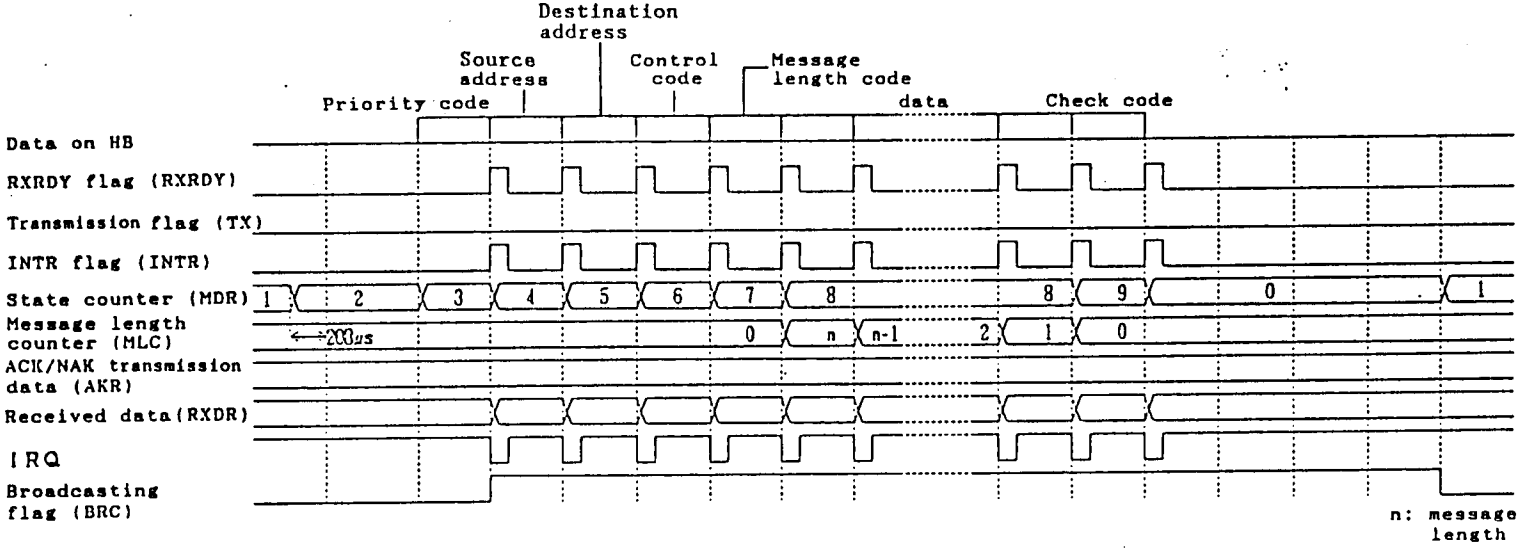


Figure 4.4 Data receiving operation (broadcasting)

4.1.3 ACK/NAK sending operation (See Figures 4.3 and 4.4.)

(1) Writing data in the ACK/NAK transmission register (AKR) makes ACK/NAK sending ready. (⑨) ACK/NAK data is set whenever it is written during sending or receiving. (MDR = "3" to "10": Data in the dummy code for "10")

Same as other sending data, the ACK/NAK transmission register (AKR) can be rewritten but cannot be cleared.

(2) Sending is automatically performed in the ACK/NAK period. Data is not sent even though it has been set in the case of broadcasting, short message interrupt, or received data error. ACK/NAK sending uses AKR. Same as other data, the received ACK/NAK data is put in RXDR.

Data written in the ACK/NAK transmission register is cleared (i.e. ACK/NAK sending itself is canceled) when the state counter (MDR) changes from "0" to "1" or when the state counter (MDR) changes from "0" to "2" in the synchronization recovery period. In other words, data is cleared for each packet.

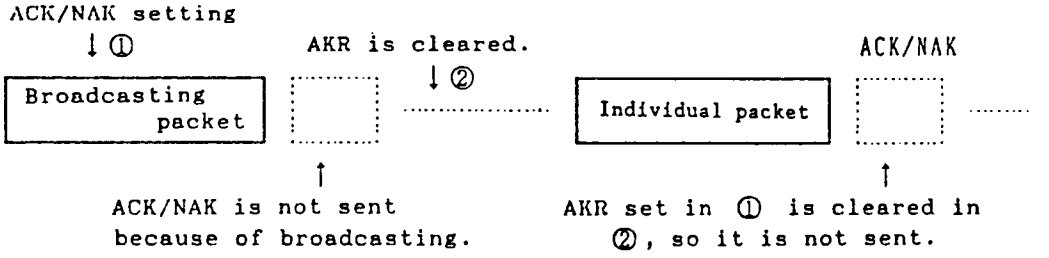


Figure 4.5 ACK/NAK sending operation

4.1.4 Pause period

The phase period is 22 bits + 10 ms (96 bits) for broadcasting and 10 ms (96 bits) for individual packet.

Figure 4.6 shows the relationship between the pause period and state counter (MDR).

The period when the state counter (MDR) is "0" in the pause period is 22 bits for individual packet and 44 bits for broadcasting before the next state (MDR=1) is set. In this period, the packet end is indicated.

Because the end of the packet in which the "message length code" does not match the actual data length should be detected and synchronization should be adjusted immediately after resetting.

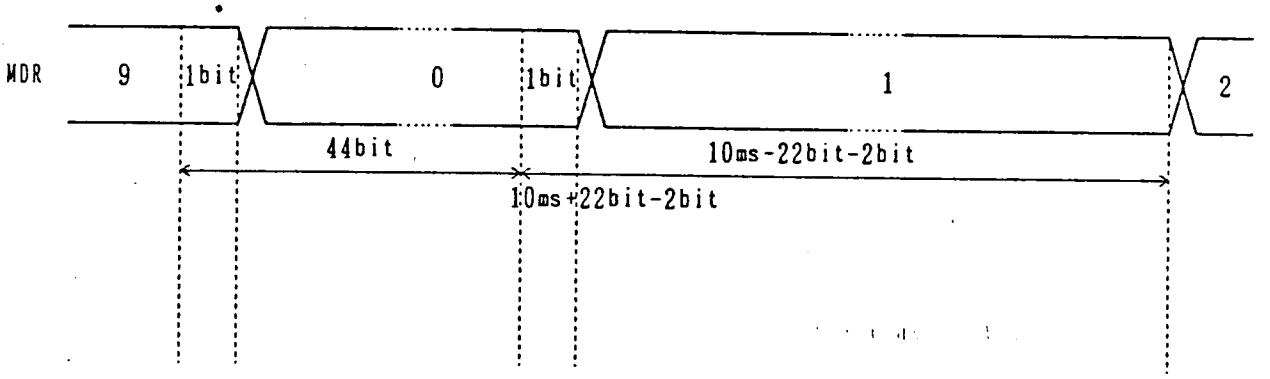
While the state counter (MDR) is "1", data is not received.

As shown in Figure 4.6, the length of the portion in which the state counter is "0" is different between the broadcasting and individual packets depending on the dummy code and ACK/NAK. The length of the portion in which the state counter is "1" is same between the broadcasting and single packets. The reason the entire length is -2 bits is that the synchronization recovery monitoring time (2 bits = 208 μs) is included in state "2" of the state counter.

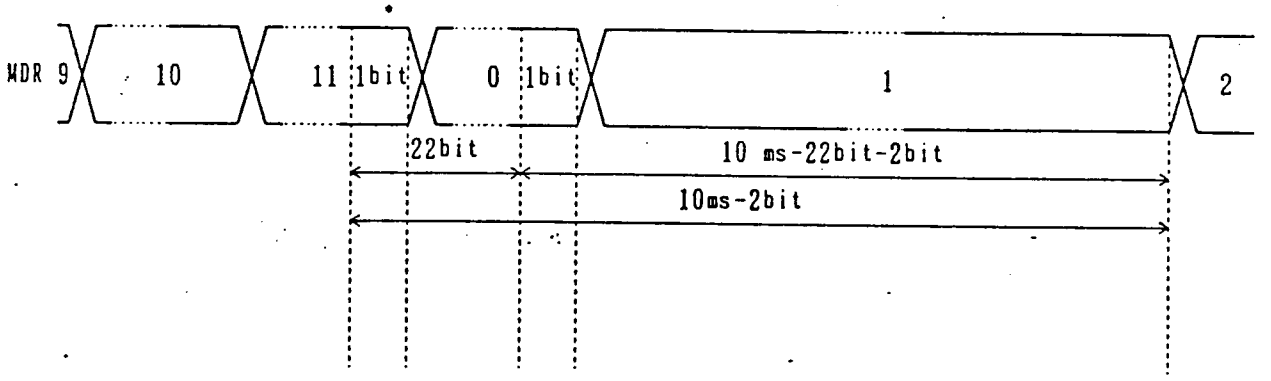
Note:

Synchronization recovery monitoring time: This is the monitoring period to perform collision accurately. When another terminal starts sending during this period, sending can be started accordingly.

i) Broadcasting



ii) Individual



Note:

This period (1 bit) is caused by the delay of the changing position of the state counter because of width detection.

Figure 4.6 Pause period operation

4.1.5 Contention

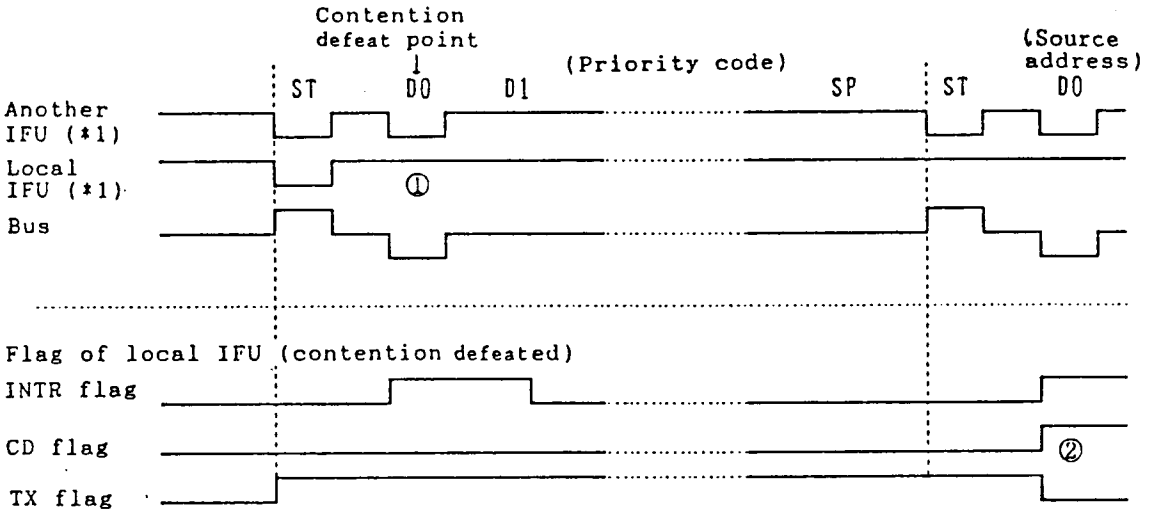
When the sending start of another IFU is detected within the synchronization recovery monitoring time, sending is started accordingly (only in case the transmission data has been written in the transmission data register (TXDR) and contention is performed.

Figure 4.7 shows contention defeat of the local IFU with priority code D0.

As shown in the figure, when contention defeat is detected (Figure 4.7 ①), the corresponding bit and following bits are not sent. Then, the interrupt flag (INTR) and contention defeat flag (CD) are set to '1' at the same time and the transmission flag (TX) is set to '0' to post the contention defeat and sending cancelation. (Figure 4.7 ②)

When contention defeat is detected, this IC stops sending in the mid-session but does not resend the data.

Collision is detected with all bits including the start (ST), parity (P), and stop (SP) bits of the "priority code" and "source address".



*1 Actually divided to TXH and TXL and output.

Figure 4.7 Contention operation

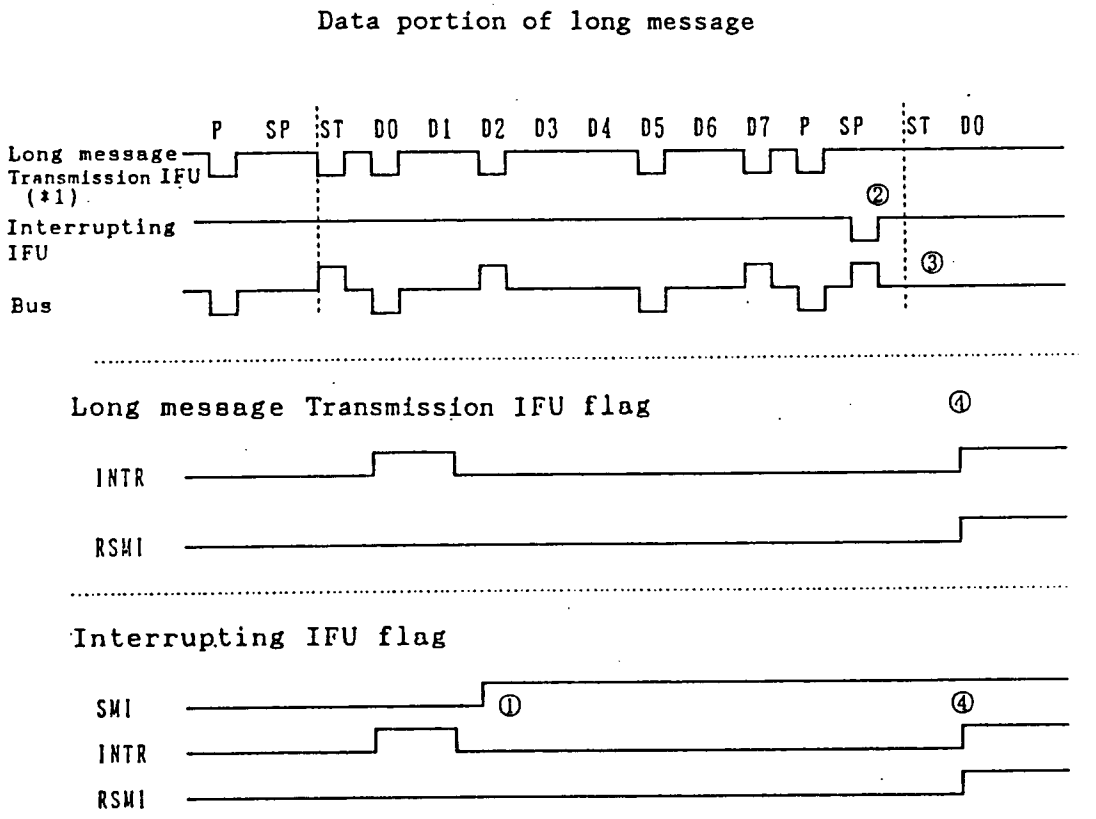
4.1.6 Short message interrupt operation

When the short message interrupt flag (SMI) is set to '1' (Figure 4.8 ①), short message interrupt (Figure 4.8 ②: '0' is output to the data stop bit.) at the data portion of the long message and the pause period (10 ms + 22 bits) is started.

Then, the interrupt flag (INTR) and return short message interrupt flag (RSMI) are set to '1' at the same time and occurrence of short message interrupt is posted. (Figure 4.8 ④)

The long message sending IFU which is interrupted stops sending of the next character (Figure 4.8 ③) and starts the pause period (10 ms + 22 bits). Then, the interrupt flag (INTR) and return short message interrupt flag (RSMI) are set to '1' at the same time and occurrence of interrupt is posted. (Figure 4.8 ④)

When interrupted, this IC stops sending in the mid-session but does not resend data.



*1 Actually divided to TXH and TXL and output.

Figure 4.8 Short message interrupt operation

4.1.7 Synchronization recovery period operation

This period is used for synchronization recovery when synchronization for each packet is changed (received data error) due to noise, etc. or after resetting.

The synchronization recovery period is started when the reset flag (RES) is changed from 0 to 1 (upon software resetting) or when a received data error occurs.

In this synchronization recovery period, receiving is performed but sending is not performed.

i) When the message is larger than the message length

Figure 4.9 shows a case that the message is larger than the message length and 1 byte of data is additionally contained. (Figure 4.9 ①) Therefore, the received data error is set to "1". (Figure 4.9 ②)

The pause period (10 ms + 22 bits) is started from point ③ that is 1 character after ① (i.e. 11 bits after).

Sending is not performed in the synchronization recovery period even though transmission data has been set. Data is sent after synchronization recovery. (Figure 4.9 ④)

As shown in Figure 4.9, the state counter (MDR) changes from 0 to 2 in the synchronization recovery period.

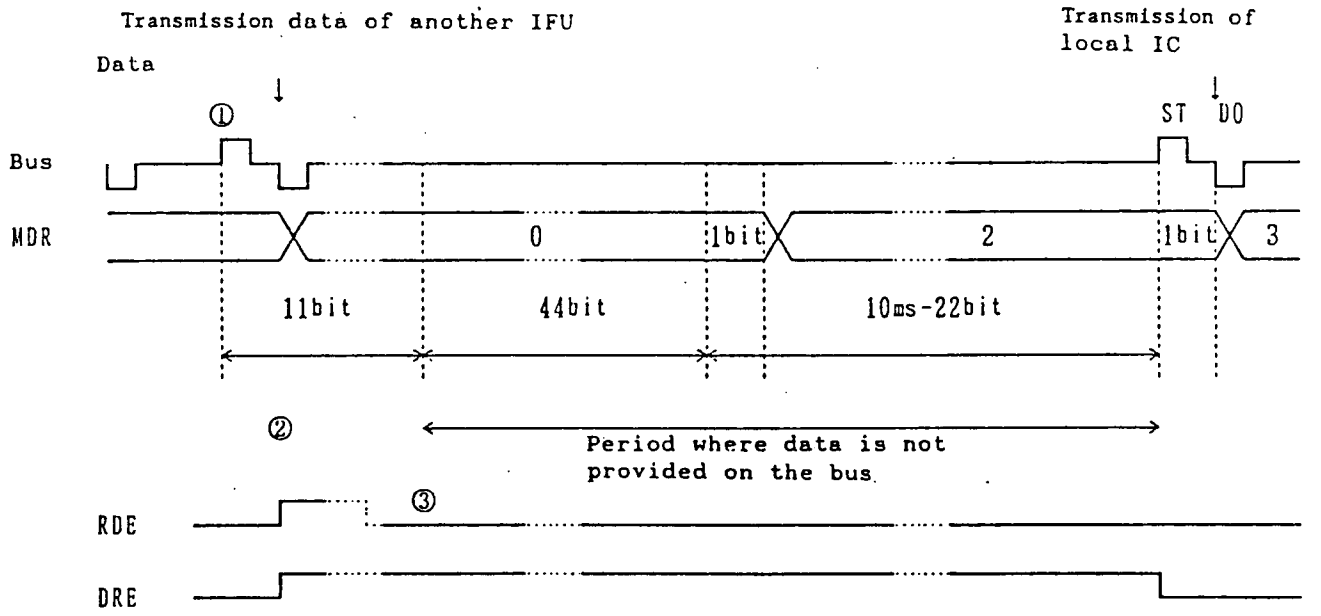


Figure 4.9 When the message is larger than the message length

ii) When the message is smaller than the message length

Figure 4.10 shows a case that the message is smaller than the message length. This figure shows a case that the state counter is "6" and next data has not come (Figure 4.10 ①).

In this case, a received data error occurs at Figure 4.10 ② and the synchronization recovery period is started. The pause period (10 ms + 22 bits) is started from Figure 4.10 ①. Sending is not performed in the synchronization recovery period even though transmission data has been set. Data is sent after synchronization recovery.

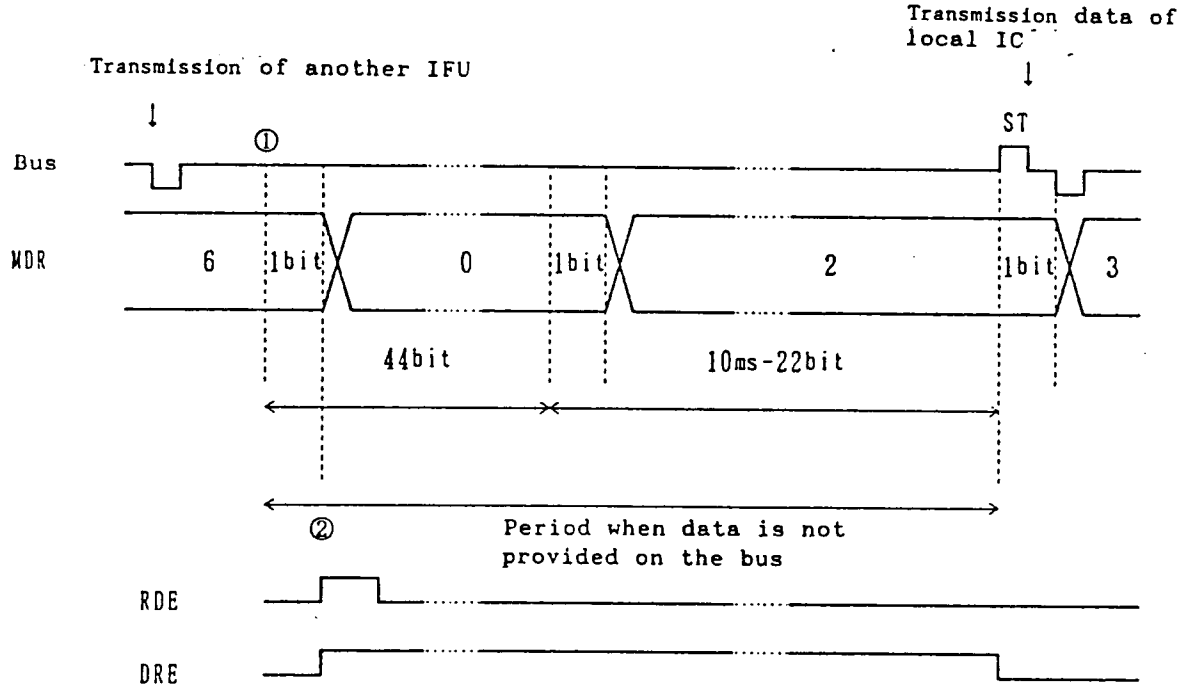


Figure 4.10 When the message is smaller than the message length

iii) When data comes when the state counter is "0"

Figure 4.11 shows a case that data (including noise) comes when the state counter is "0".

In this case, data comes at Figure 4.11 ① and RDE and DRE rise within 12 bits (Figure 4.11 ③).

The pause period is 10 ms + 22 bits after the data end (Figure 4.11 ②: Not related to the position where RDE and DRE rise). In this case, sending is not performed in the synchronization recovery period even though transmission data has been set. Data is sent after synchronization recovery.

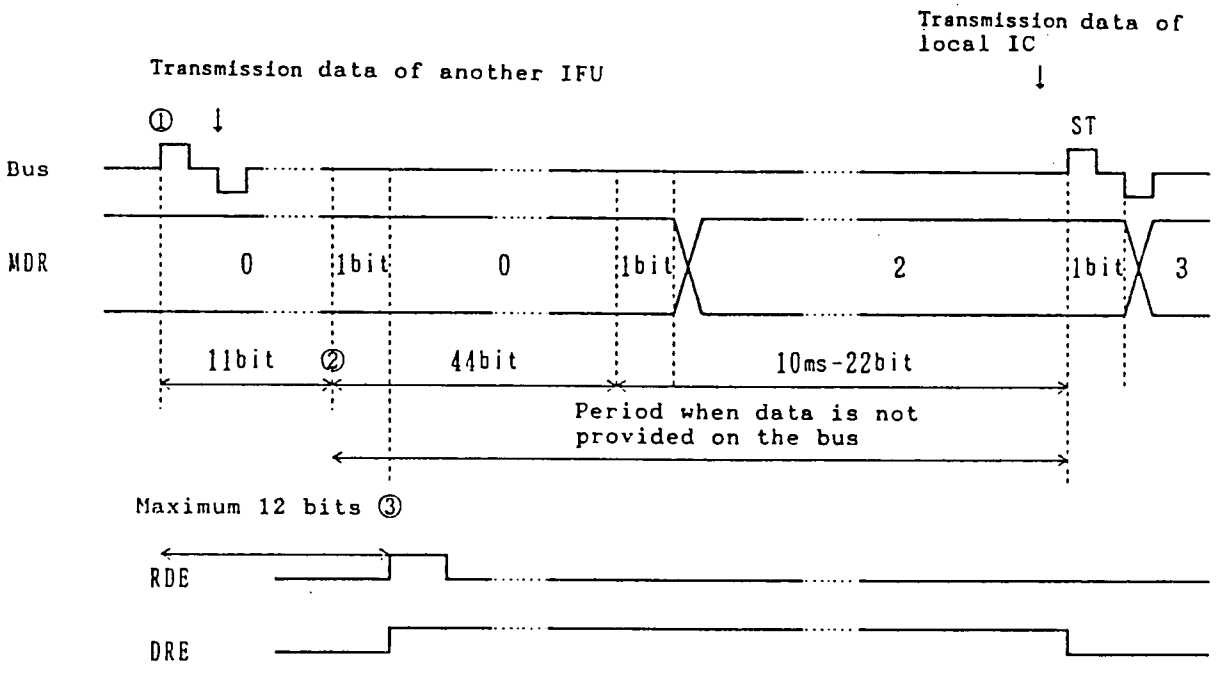


Figure 4.11 When data comes while the state counter is "0"

4.1.8 Synchronization recovery operation

Completion of synchronization recovery in this IC is judged by detecting the following two states:

(1) The period when data is not provided on the bus is 10 ms + 22 bits.

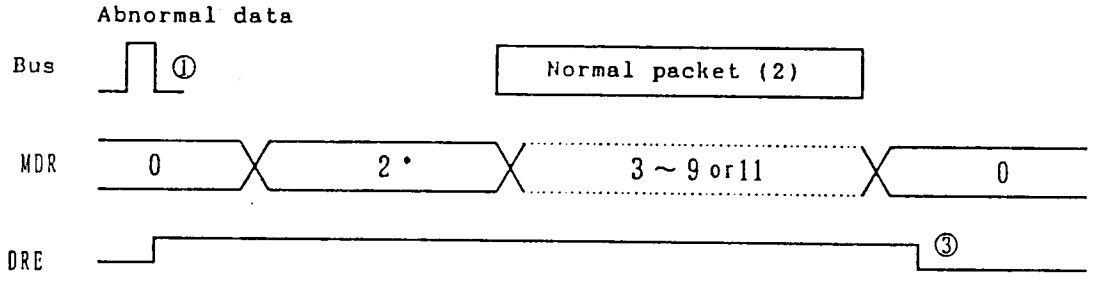
(2) When a normal packet (without parity error (PE)) is received in the synchronization recovery period.

(1) is the method shown in Figure 4.11, etc. This method identifies completion of synchronization recovery when the period without data continues for 10 ms + 22 bits.

(2) is the method shown in Figure 4.12. When data (noise, etc.) comes at Figure 4.12 ①, the packet comes before the pause period ends (Figure 4.12 ②) and the packet has no parity error. In this case, the synchronization recovery period is ended (Figure 4.12 ③) assuming completion of synchronization recovery.

With the method in (2), synchronization recovery can be rapidly performed when individual packets continue and a 10 ms + 22 bits space cannot be provided.

The synchronization recovery operation is repeated until either (1) or (2) is set up.



*1 Length before the pause period ends

Figure 4.12 When the synchronization recovery period ends with one-packet reception

4.1.9 Operation for error

This IC detects the following six errors:

i) Received data error (RDE)

ii) Write lost data error (WLD)

iii) Read lost data error (RLD)

iv) Framing error (FE)

v) Parity error (PE)

vi) ACK/NAK error (AKE)

When a received data error (RDE) occurs, the flag is set to '1' to post the error to the CPU with interrupt. At the same time, the state counter (MDR) is set to "0" and the synchronization recovery period (DRE) is set to '1' to start the synchronization recovery period.

The write lost data error (WLD) and read lost data error (RLD) are checked for when next data is sent or received. The flag is set to '1' and the error is posted to the CPU with interrupt.

For a read lost data error (RLD), the receiving operation is continued. For the write lost data error (WLD), sending is stopped and the synchronization recovery period is started. In this case, a received data error also occurs.

When a framing error (FE) or parity error (PE) occurs, the flag is set to '1' and the error is posted to the CPU with interrupt. The receiving operation is continued.

When an ACK/NAK error occurs, the flag is set to '1' and the error is posted to the CPU with interrupt. When this error occurs, the state counter (MDR) changes from "10" to "10" and from "10" to "0". When ACK/NAK cannot be detected, the MDR = 10 period continues for 22 bits.

Any error flag is cleared when status register 2 is read, when the state counter (MDR) changes from "0" to "1", or when the state counter (MDR) changes from "0" to "2" in the synchronization recovery period.

4.1.10 Interrupt operation

The following five interrupt causes are provided for this IC:

i) Transmission data input
ii) Received data output
iii) Short message interrupt
iv) Contention defeat
v) Error

Detection of an interrupt cause can be judged with the TXRDY flag, RXRDY flag, return short message interrupt flag, contention defeat flag, error flag, or status register 2. Interrupt is reset by reading the interrupt flag (INTR) (i.e. reading STR1) for any cause.

As a function that masks the interrupt signal (IRQ), there are the sending and receiving interrupt mask flags (RIM, TIM). There flags have a function that does not undefined received data in the synchronization recovery period to the CPU and a function that controls interrupt of undefined received data in the synchronization recovery period by letting the user rewrite.

These flags disables interrupt after the received data error is set to "1" then sets to "0" one character later and before synchronization is set. Upon software resetting, this flag is also set to "0" and interrupt is disabled until synchronization is set.

Figure 4.13 shows operations of the sending and receiving interrupt mask flags upon software resetting. Software resetting is performed at Figure 4.13 ①. In this case, the packet end is searched while the state counter is "0" when data is provided, then the synchronization recovery period ends at the point 10 ms + 22 bits later (Figure 4.13 ②) and interrupt is applied thereafter.

In other words, interrupt is not generated in packet 1, but interrupt is generated in packet 2 as the normal state.

For the period when interrupt is disabled, interrupt can be forcibly generated by setting the receiving interrupt flag to '1' and data can be received. (IC receives data even when interrupt is not generated.) Data received at that point is not always correct.

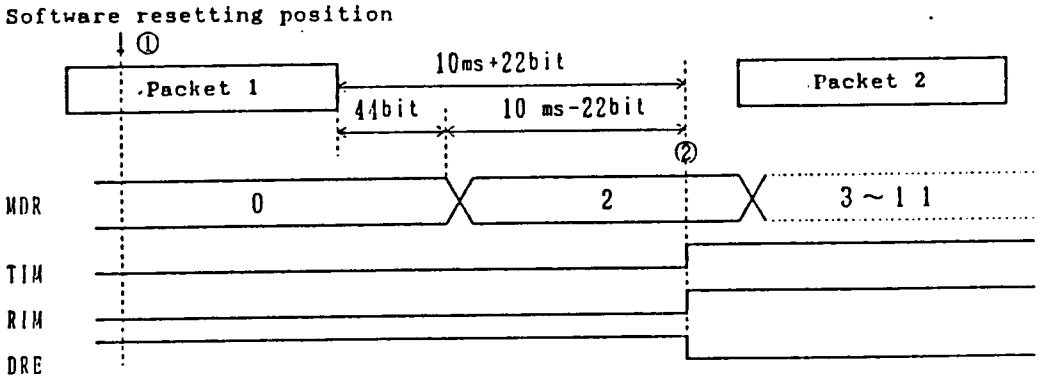


Figure 4.13 Sending/receiving interrupt mask flag operation upon resetting

4.2 Explanation of Operation

4.2.1 When sending is requested during receiving

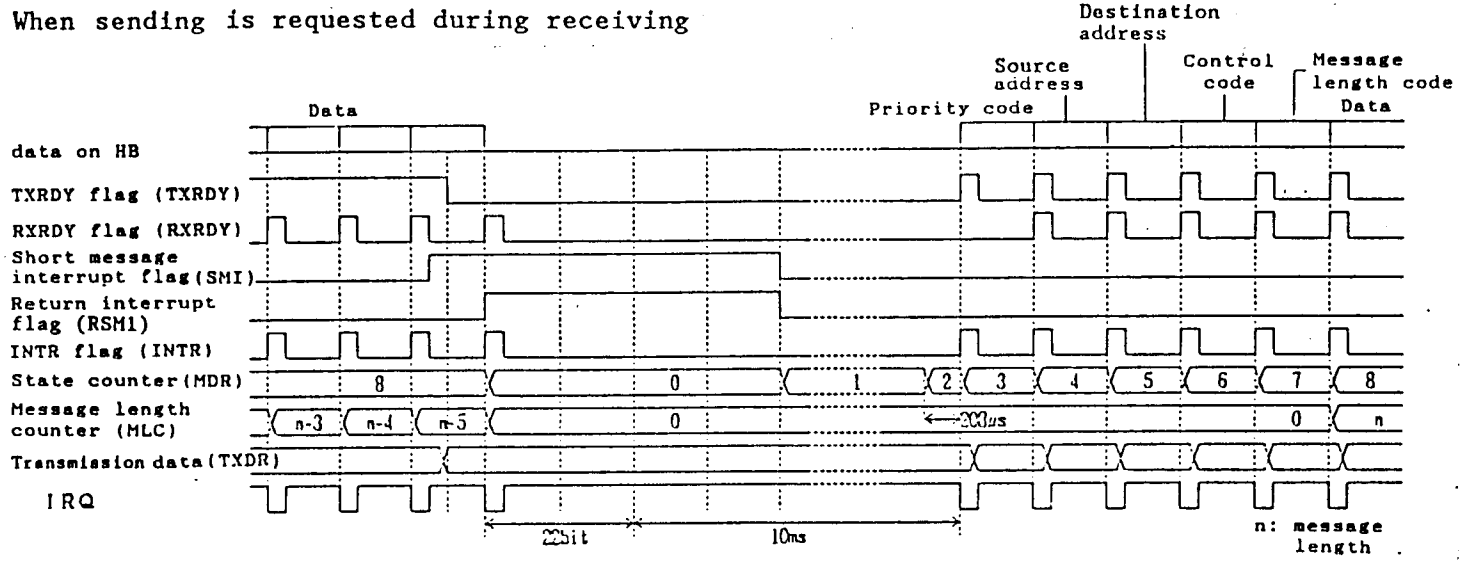


Figure 4.14 When sending is requested during receiving of long message

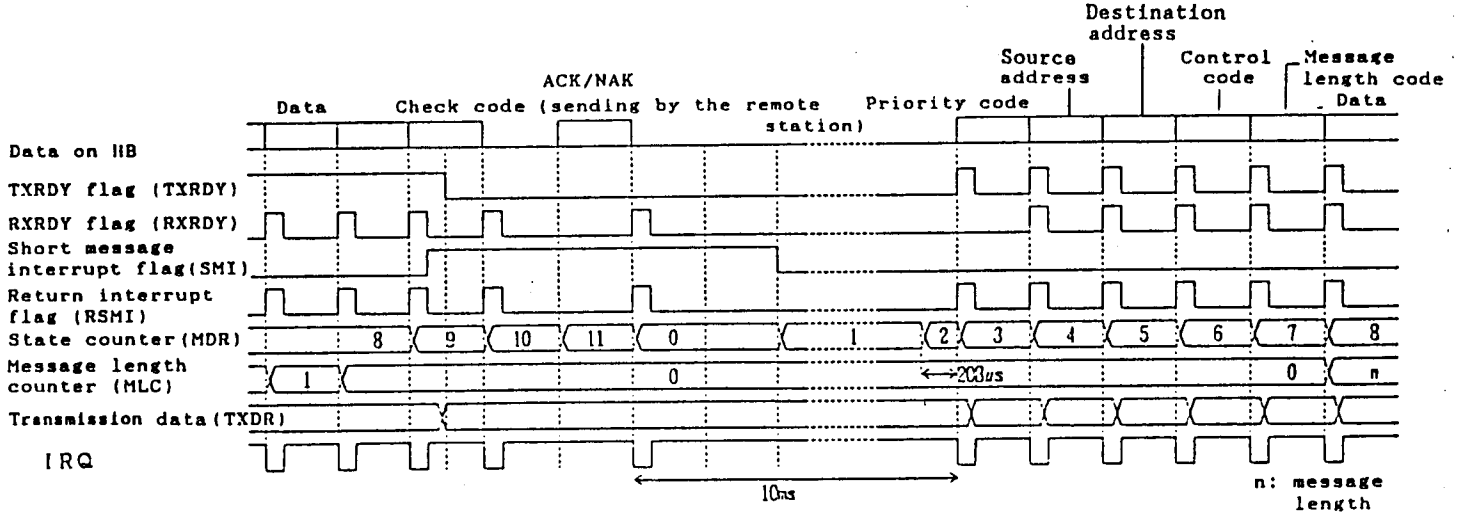


Figure 4.15 When sending is requested during receiving of short message

4.2.2 When interrupt occurs during sending

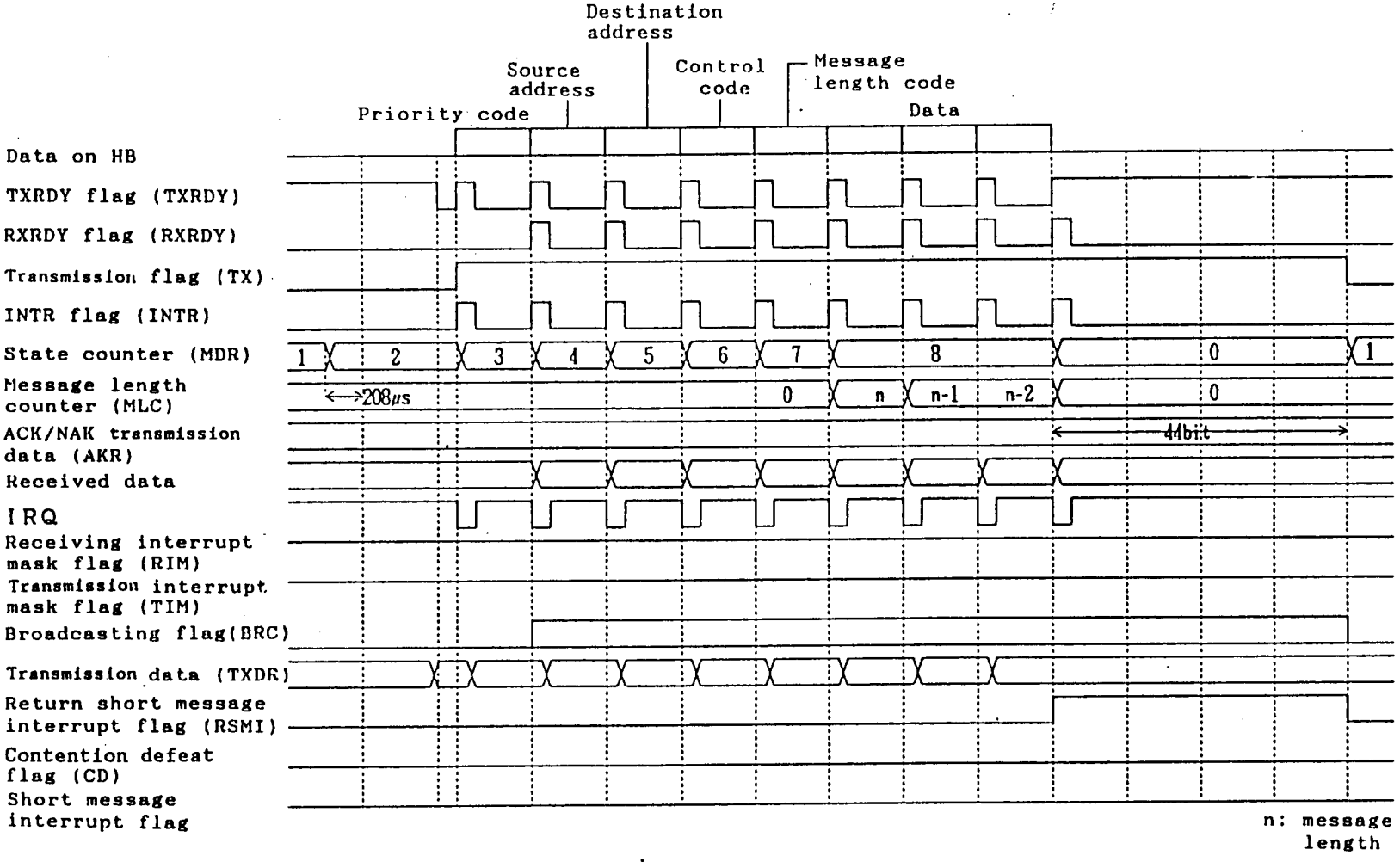


Figure 4.16 When interrupt occurs during sending

4.2.3 When interrupt occurs during receiving

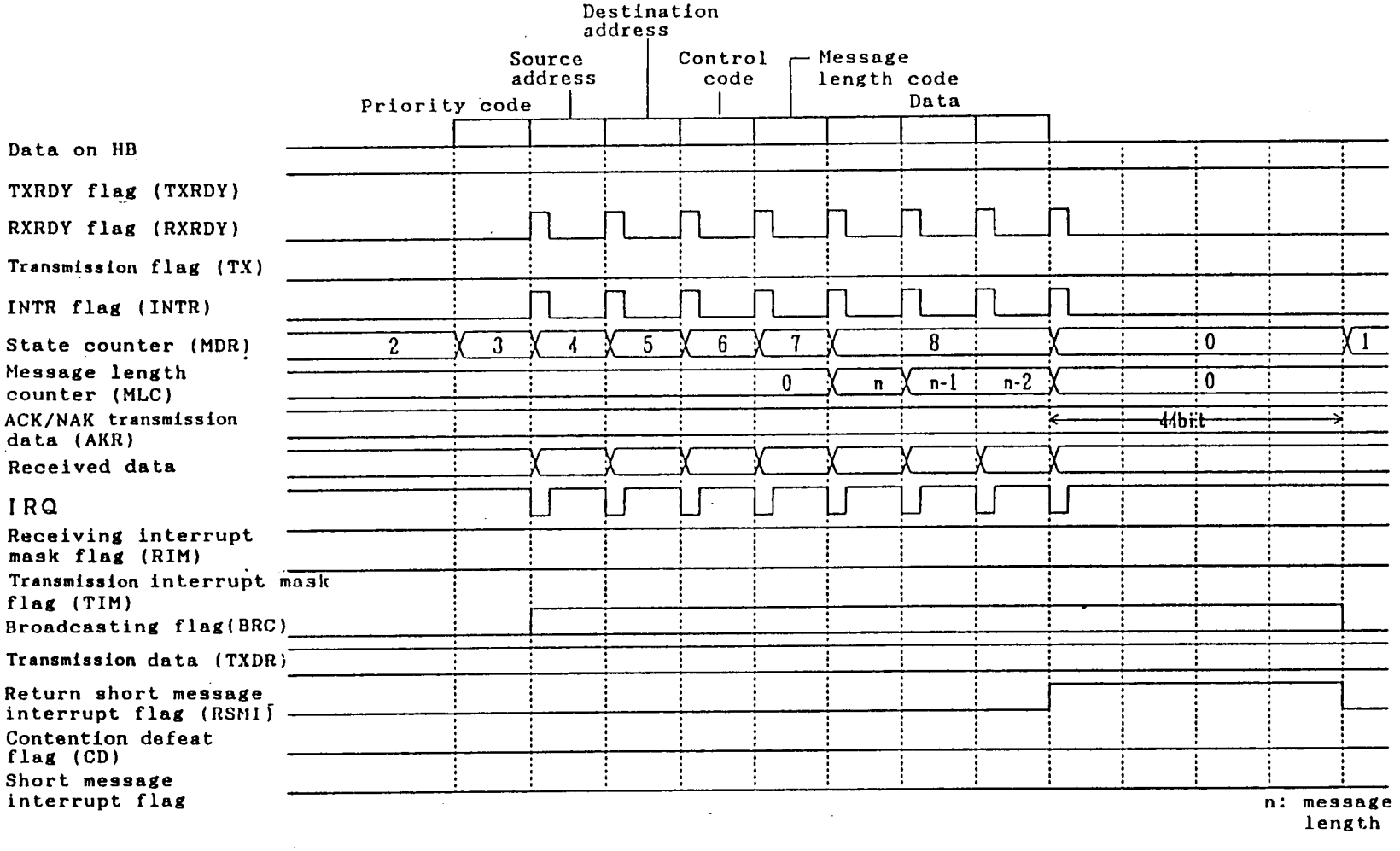


Figure 4.17 When interrupt occurs during receiving

4.2.4 Contention defeat

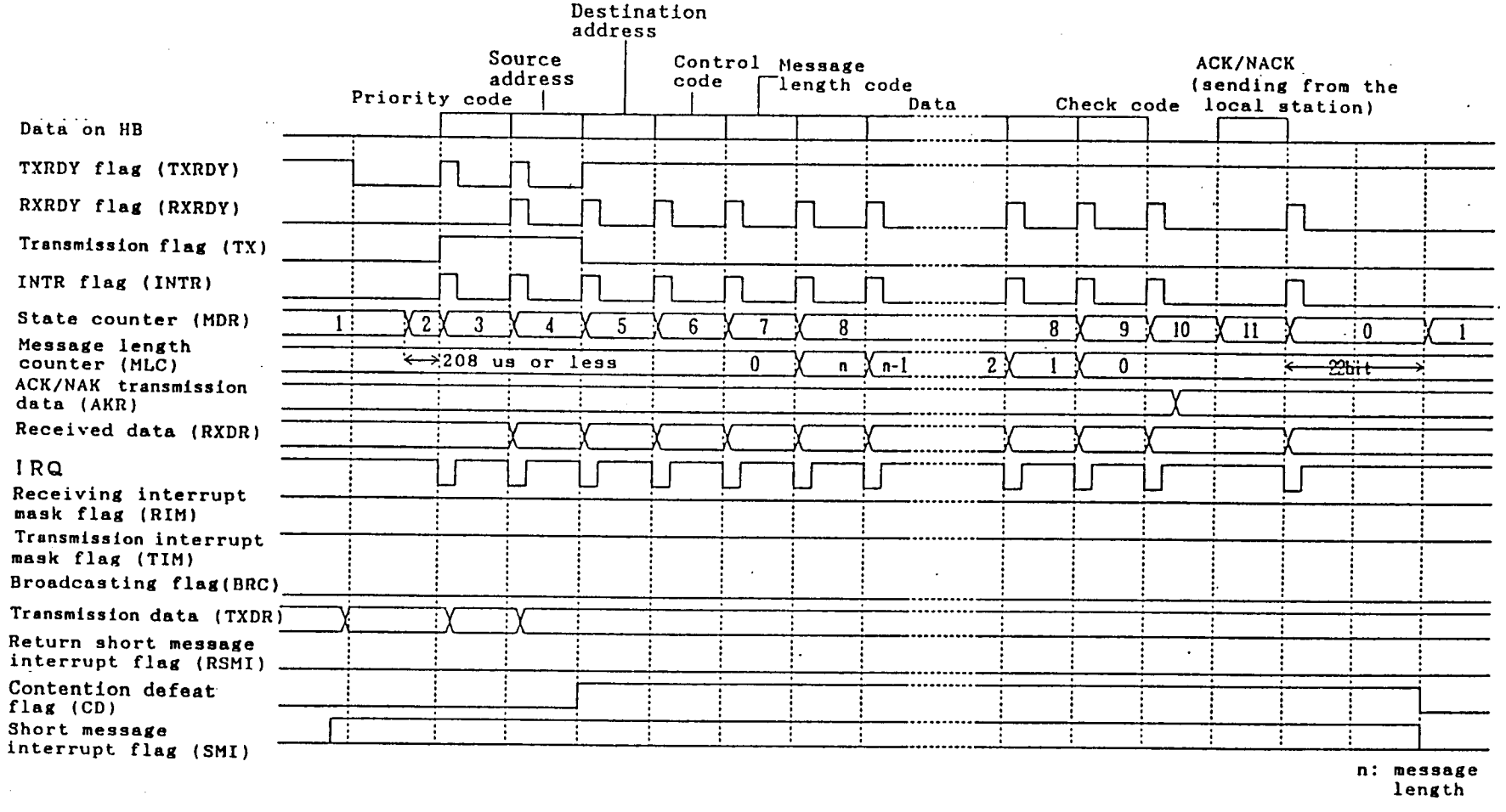


Figure 4.18 Contention defeat

4.2.5 When write lost data occurs

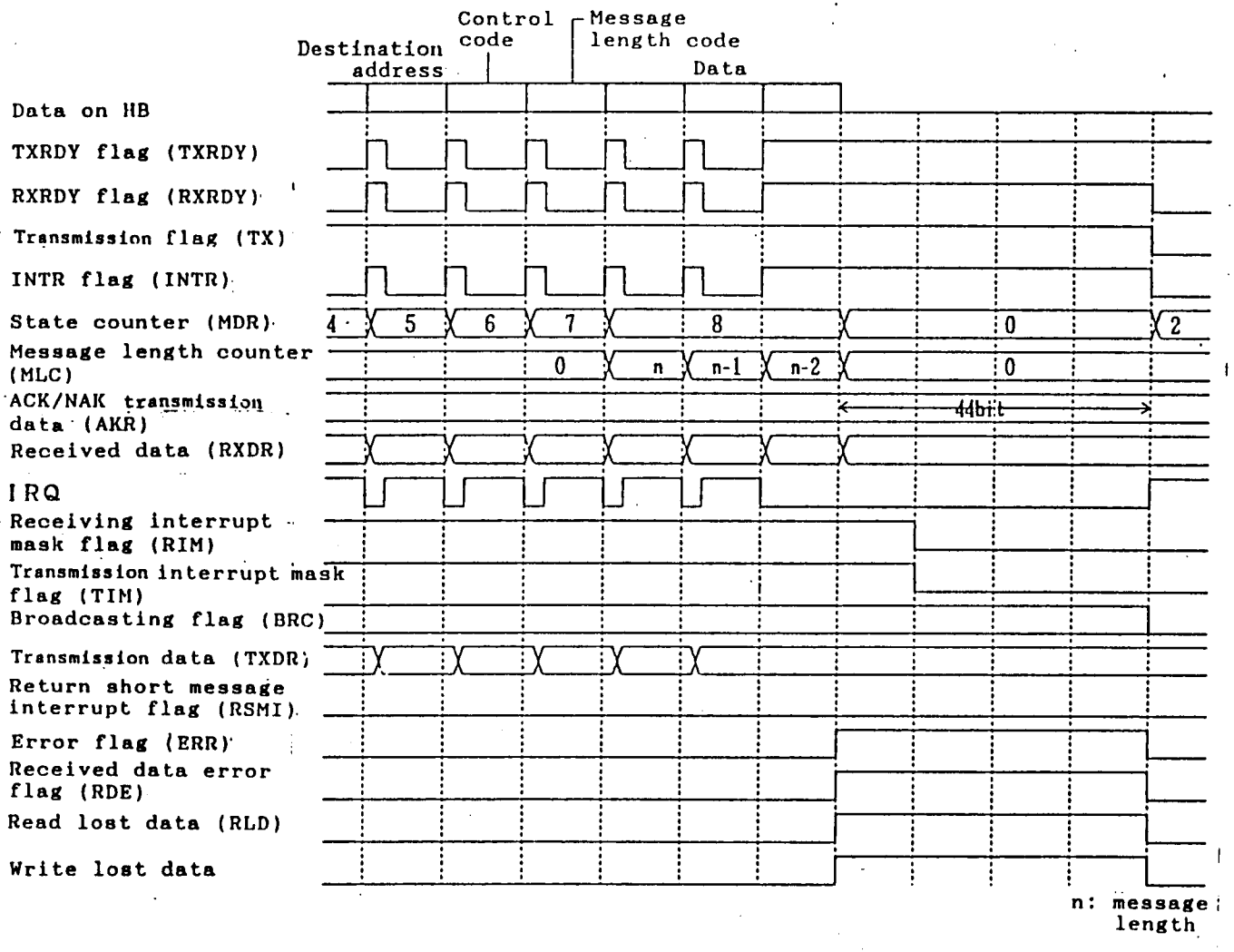


Figure 4.19 When write lost data occurs

4.2.6 Receiving operation after resetting

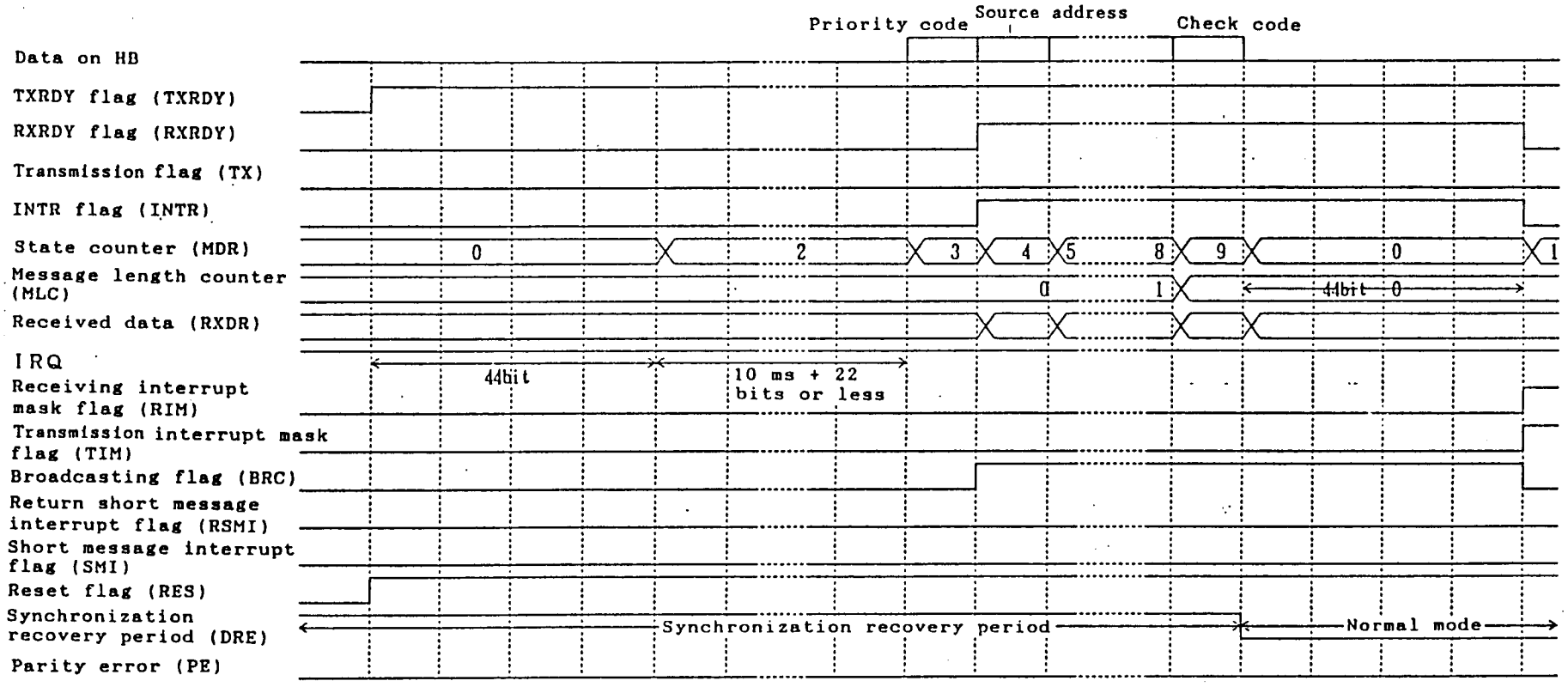


Figure 4.20 Synchronization recovery with receiving after resetting

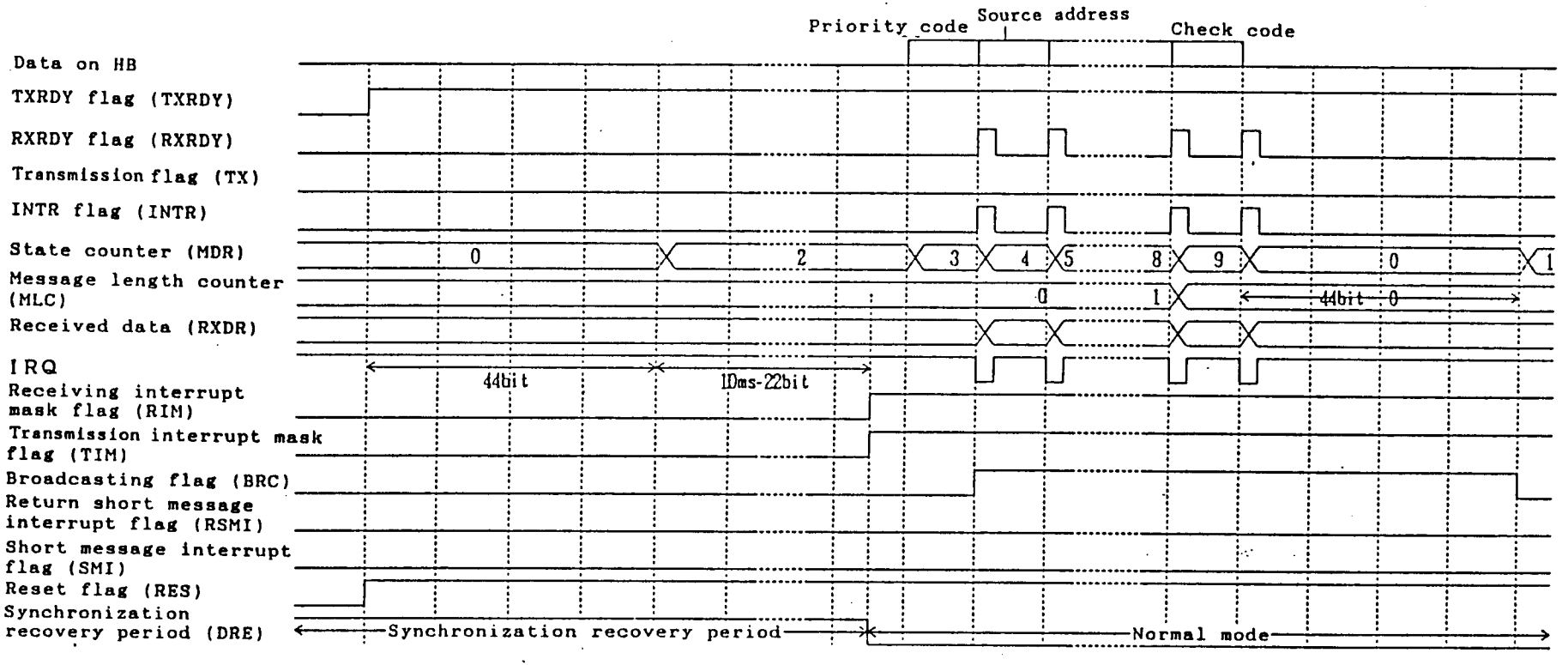


Figure 4.21 Synchronization recovery with timeout after resetting

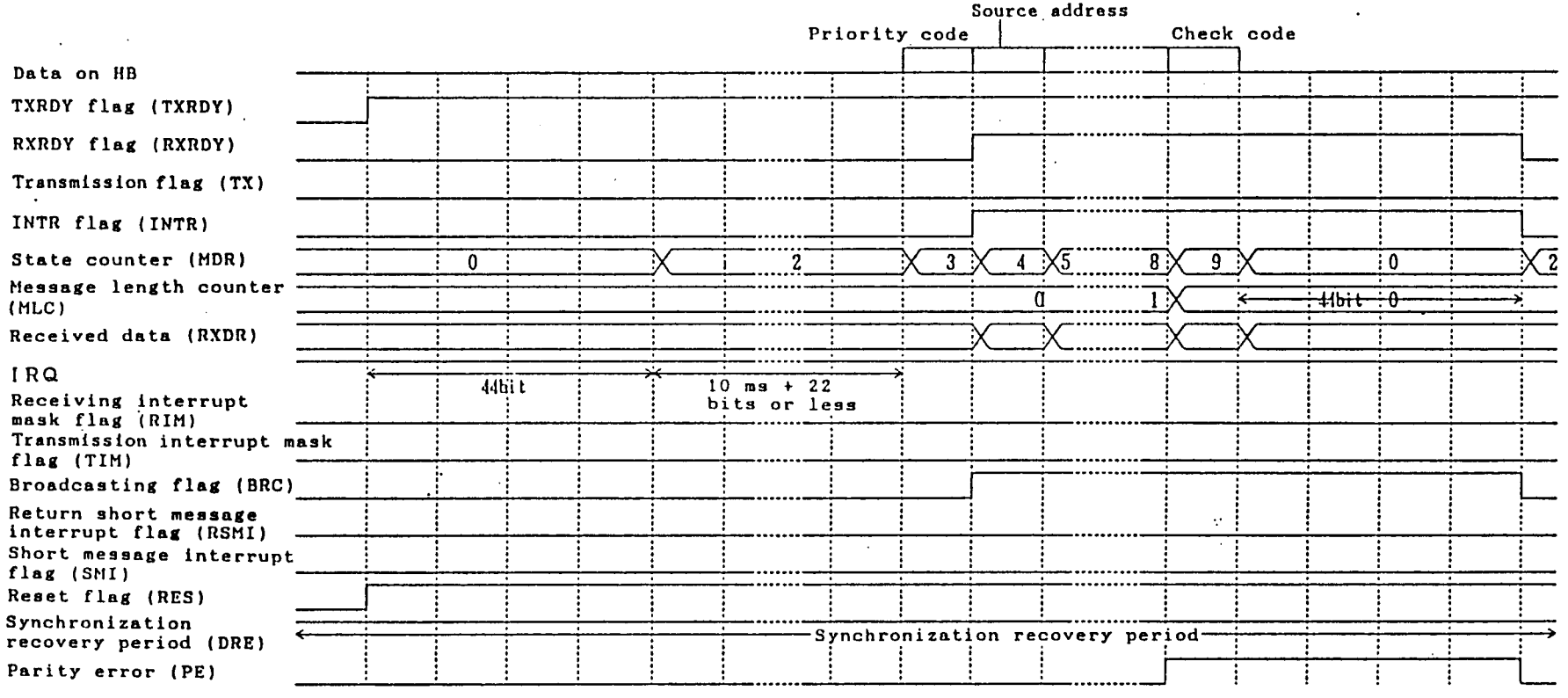


Figure 4.22 Synchronization recovery not performed with parity error after resetting

4.3 Operating Parts

4.3.1 When sending is started

Figures 4.23, 4.24, and 4.25 show sending starting.

Figure 4.23 shows that the local IFU starts sending according to sending started by another IFU within the synchronization recovery monitoring time (2 bits) at the end of the pause period. In this case, contention occurs on the bus.

Figure 4.24 shows sending from the point at which the pause period (including the synchronization recovery monitoring time) ends because data was written when MDR = 1.

Figure 4.25 shows starting sending at the approximately same time as transmission data is written when MDR = 2 (bus empty). The INTR flag and MDR change when ST changes to DO. The broadcasting flag rises when ST of the source address changes to DO.

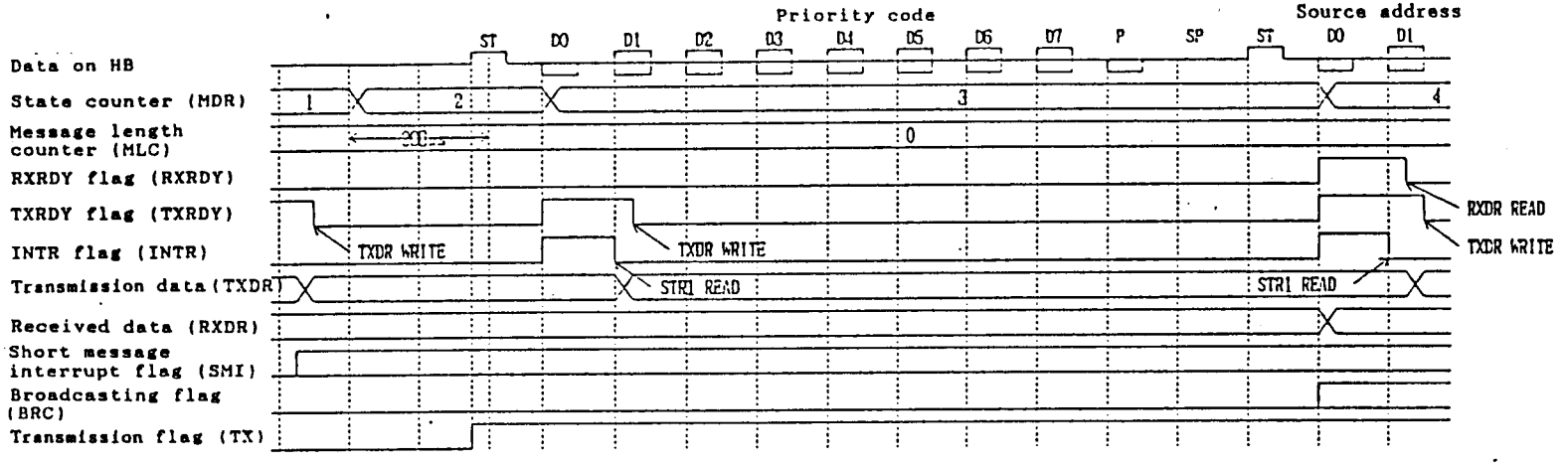


Figure 4.23 When sending is started along with sending from another IFU within the synchronization recovery monitoring time

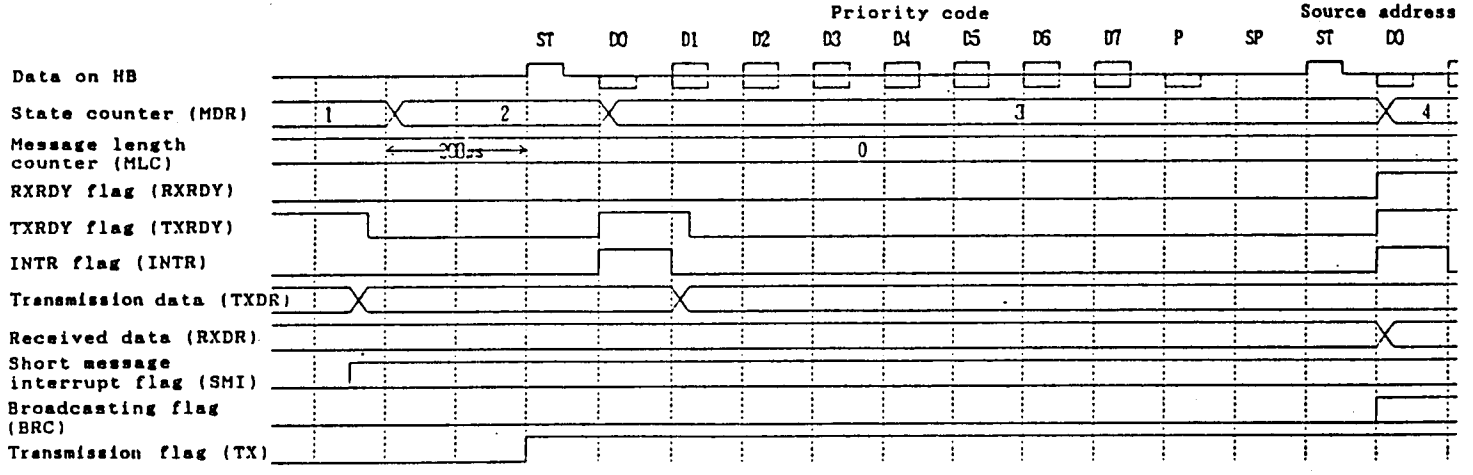


Figure 4.24 When sending is started after the pause period

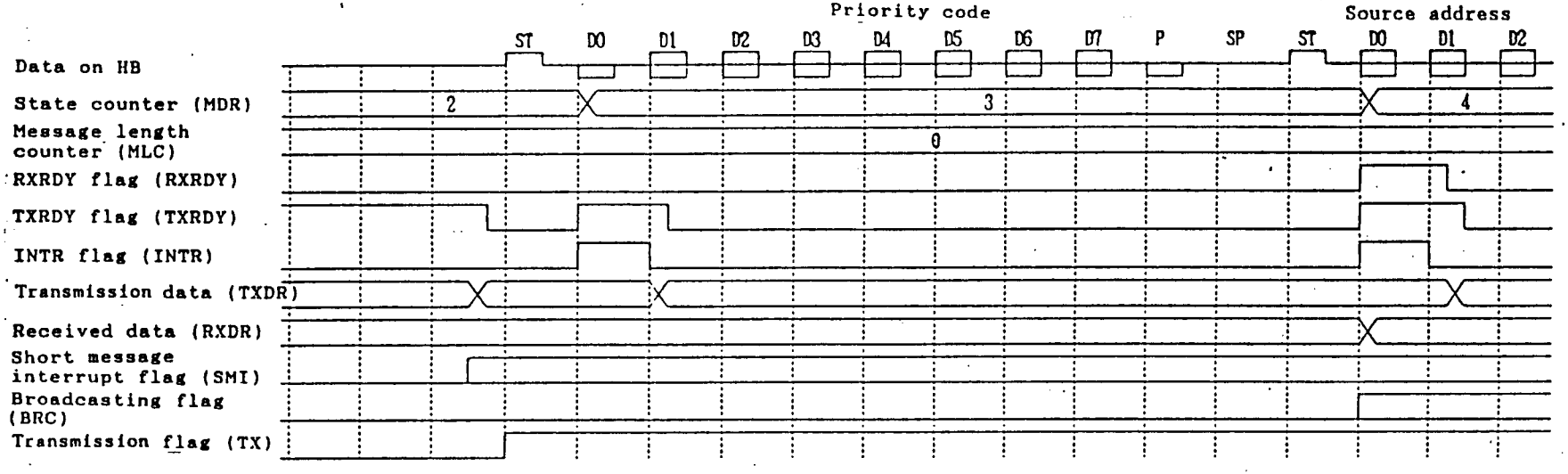


Figure 4.25 When sending is started while the bus is empty

4.3.2 Message length code and data

Figure 4.26 follows Figures 4.23, 4.24, and 4.25 and shows the message length code through data. At the first character of data, the message length (n) is set in the message length counter (MLC).

Figure 4.27 shows the message length code through data upon receiving. Compared with Figure 4.26, TXRDY is 'H', transmission data has not been set, and the transmission flag (TX) is 'L', which are the differences.

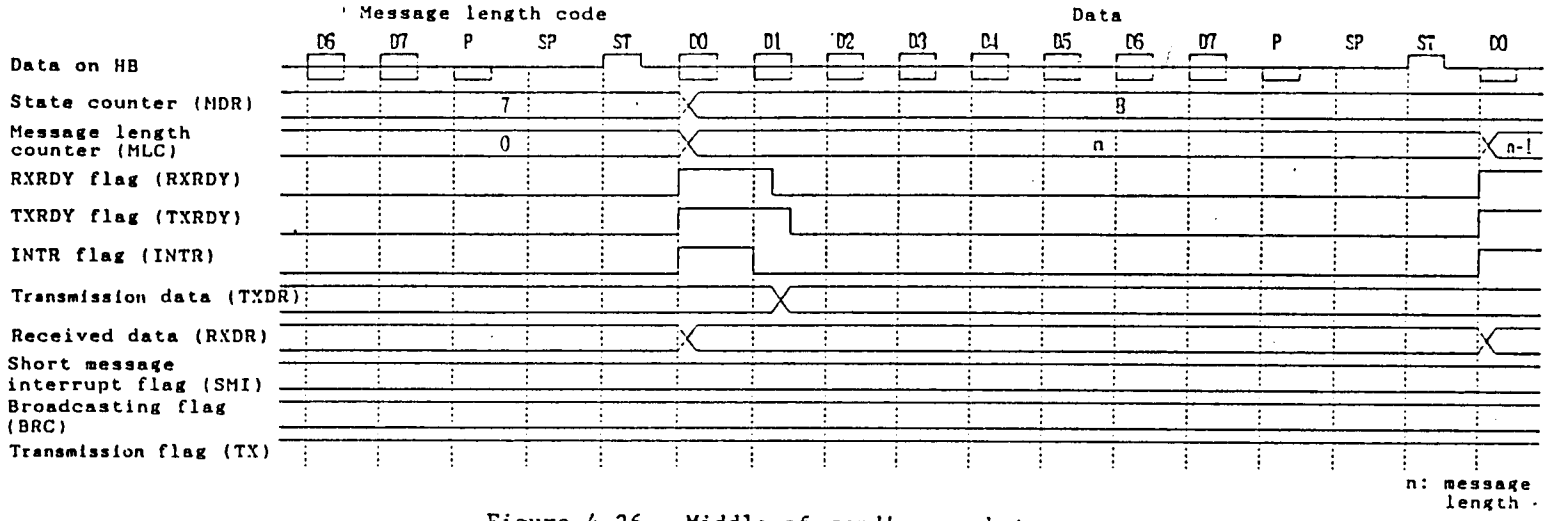


Figure 4.26 Middle of sending packet

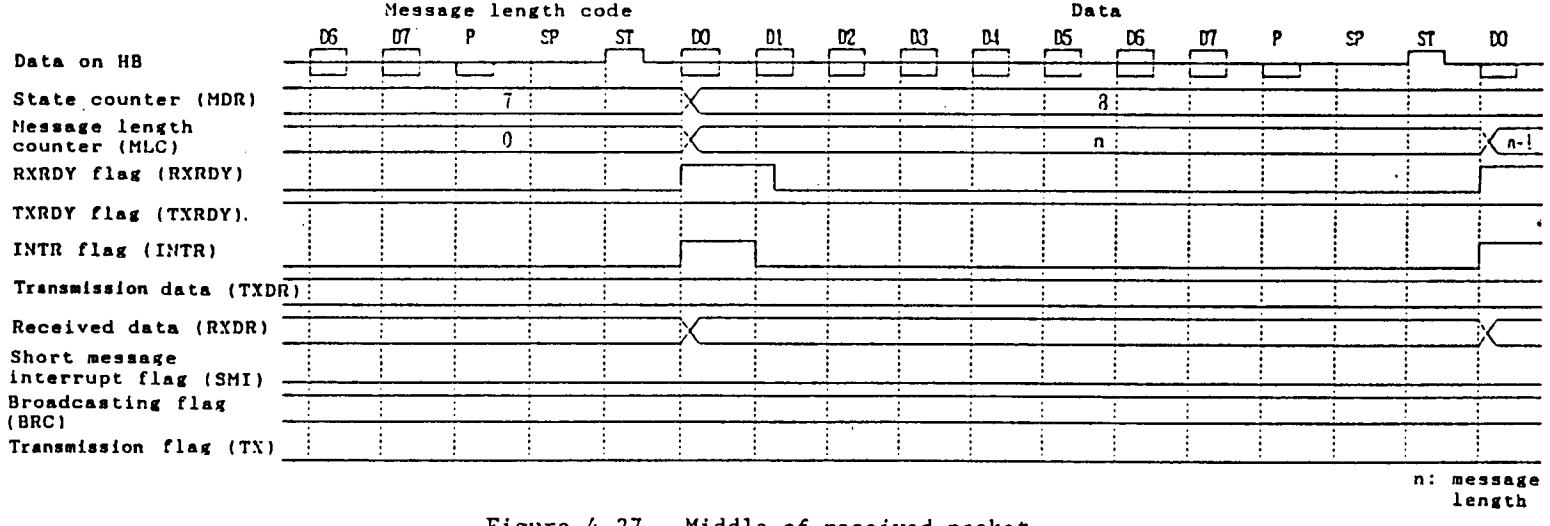


Figure 4.27 Middle of received packet

4.3.3 Check code (in sending)

Figures 4.28 and 4.29 show the check code in sending.

Figure 4.28 shows the case of broadcasting packet.

Figure 4.29 shows the case of individual packet.

In Figure 4.29, MDR changes from 9 to 10 and from 10 to 11. Interrupt is disabled at the MDR = 11 portion. Figure 4.29 shows the transmission flag (TX) rises to indicate local sending during ACK/NAK receiving.

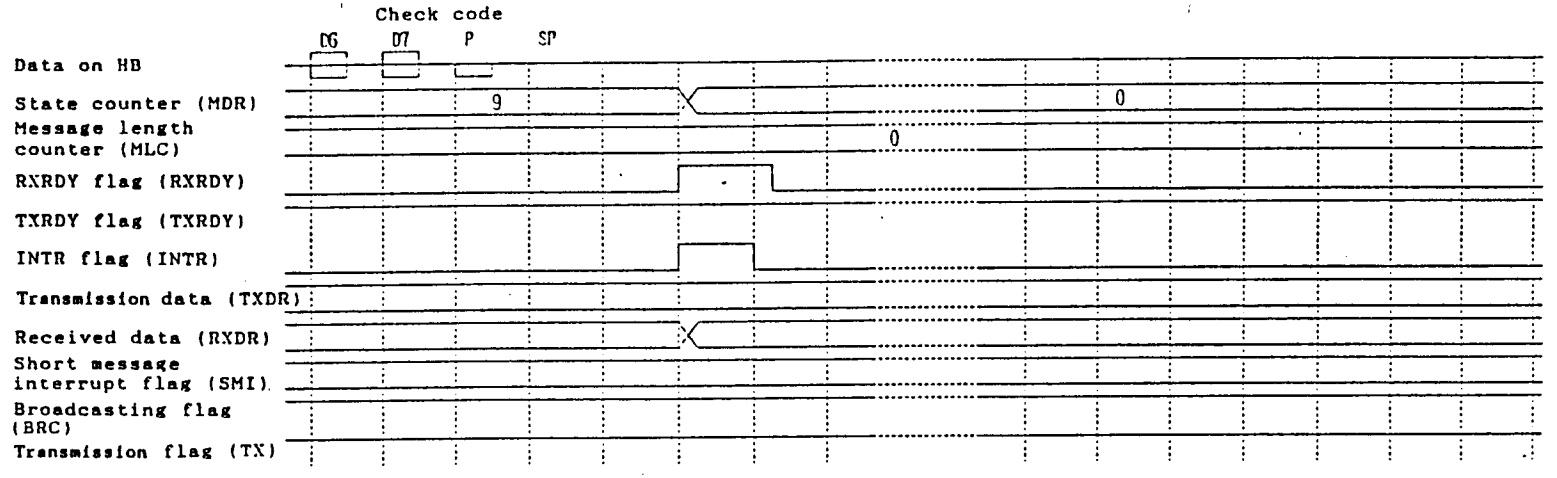


Figure 4.28 End of sending packet (broadcasting)

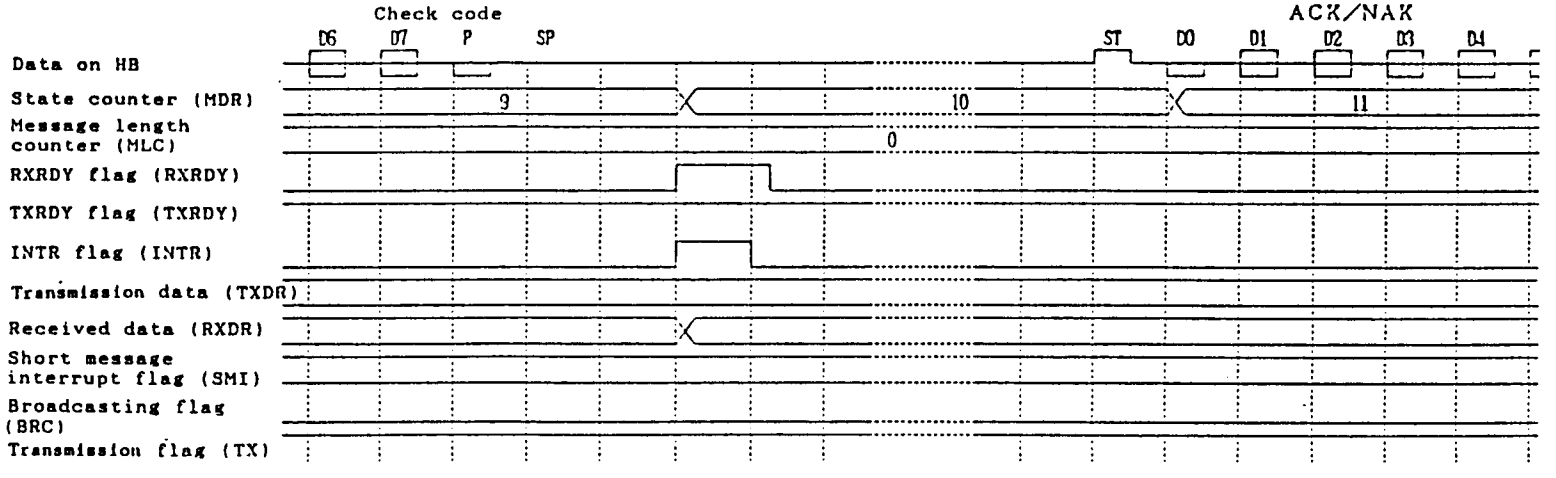


Figure 4.29 Check code through ACK/NAK operation of sending packet

4.3.4 Check code (in receiving)

Figure 4.30 shows the check code portion upon receiving a individual packet. ACK/NAK data is written in AKR when MDR = 10. Then, ACK/NAK sending occurs.

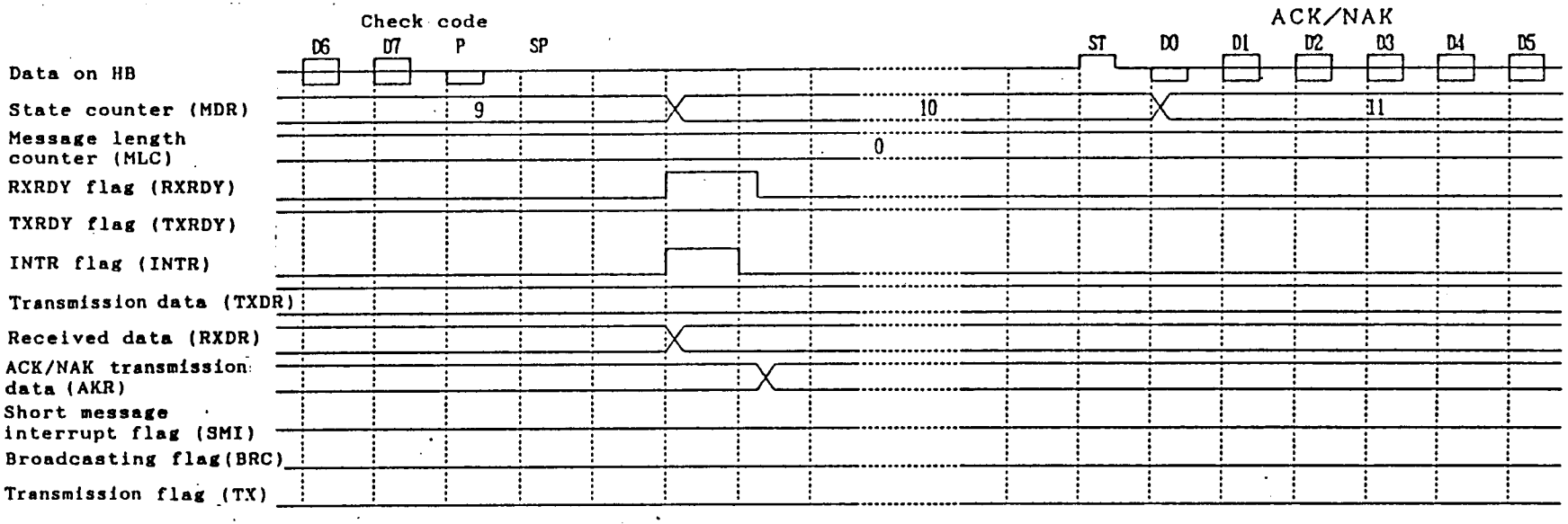


Figure 4.30 Check code through ACK/NAK operation of received packet

4.3.5 Packet sending/receiving

Figures 4.31 and 4.32 follow Figures 4.29 and 4.30.

Figure 4.31 shows individual packet sending.

Figure 4.32 shows individual packet receiving.

In Figure 4.31, the transmission flag (TX) falls when MDR changes from 0 to 1.

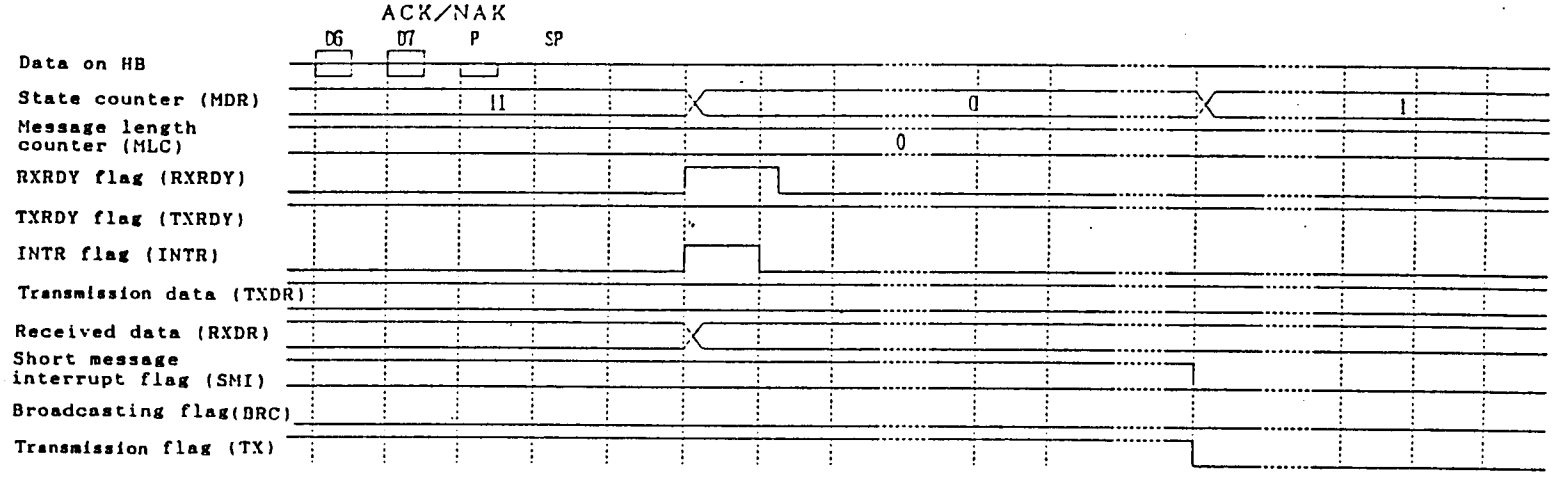


Figure 4.31 End of sending packet (individual)

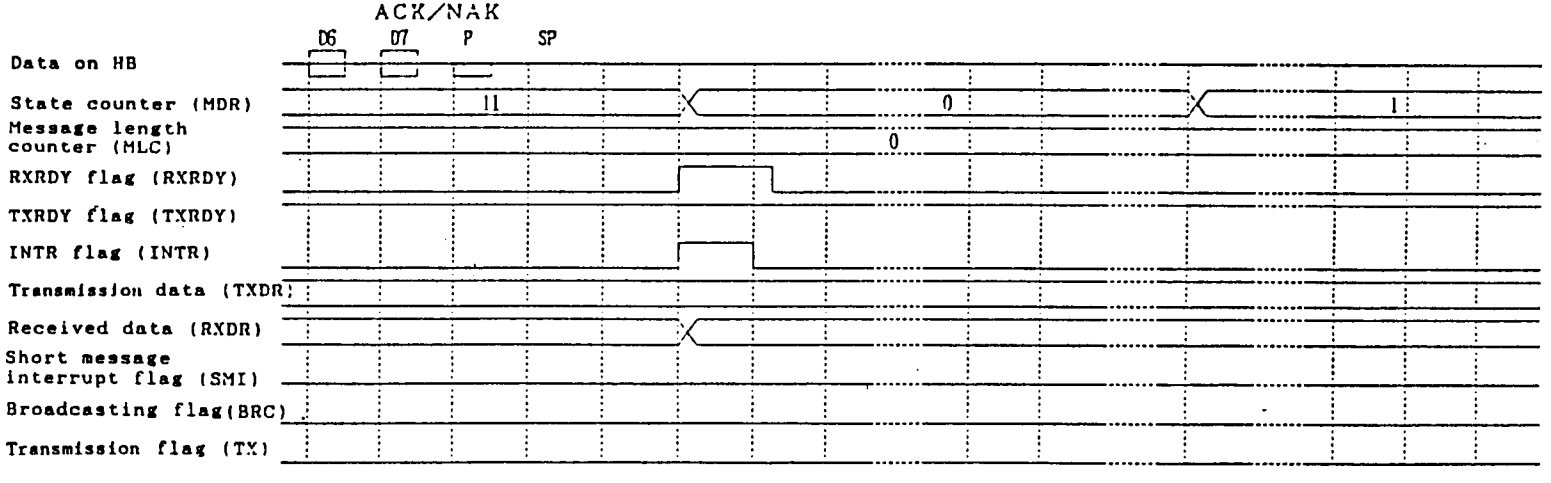


Figure 4.32 End of received packet (individual)

4.3.6 Short message interrupt

Figures 4.33 and 4.35 show short message interrupt.

Figure 4.33 shows short message interrupt which is applied to long message. Since the SMI flag is set to 'H' near the 6th bit (D6) of data, the SP bit of data is set to 0 (TXH = 'L'). Therefore, short message interrupt is applied and the pause period is started. In this case, MDR changes from 8 to 0 and MLC changes from n to 0. RSMI rises when MDR changes from 8 to 0. Transmission data set near the 6th bit (D6) of data becomes the priority code of the next packet.

Figures 4.34 and 4.35 show short message interrupt applied from another IFU.

Figure 4.34 shows sending.

Figure 4.35 shows receiving. In any case, MDR changes from 8 to 0 and the pause period is started.

Figure 4.34 shows that transmission data is not set at the MDR = 0 portion because RSMI is high. If transmission data is set at this portion, it is regarded as the priority code of the next packet.

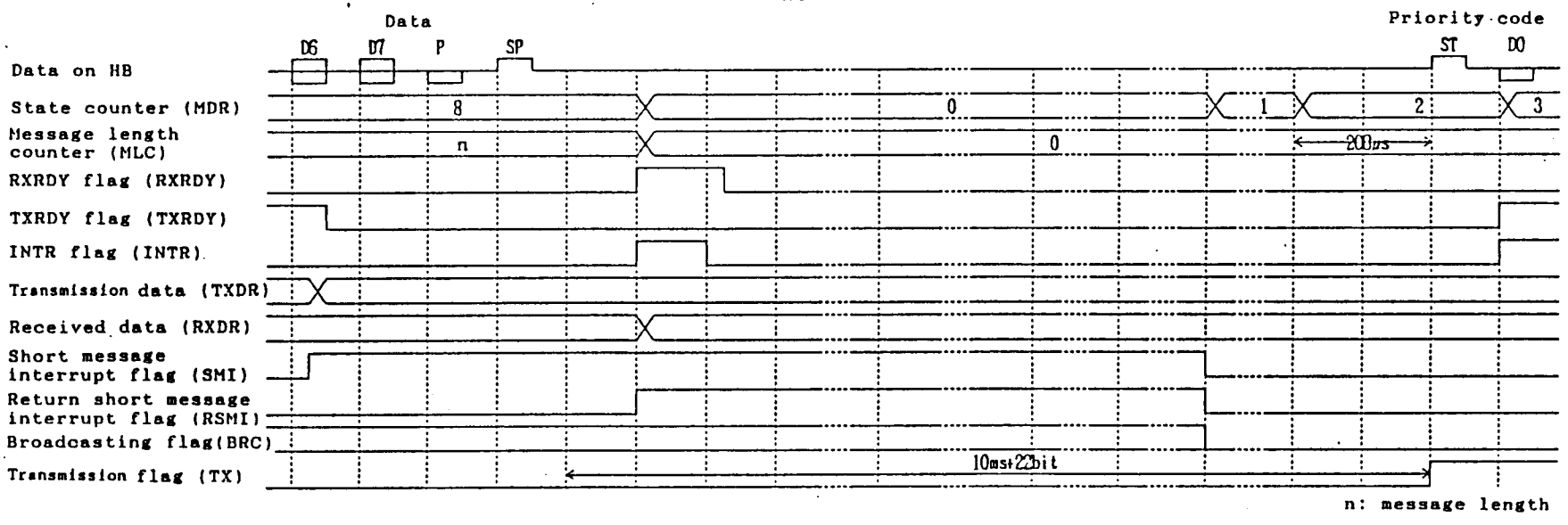


Figure 4.33 When interrupt is applied to received packet

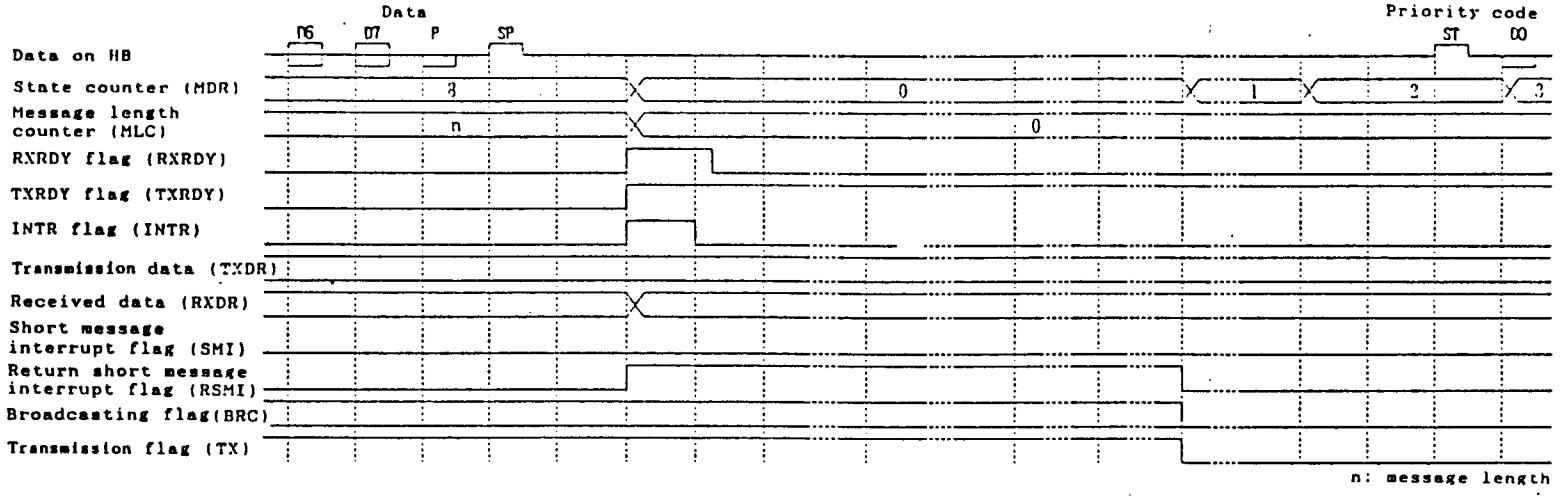


Figure 4.34 When interrupt is applied by sending packet

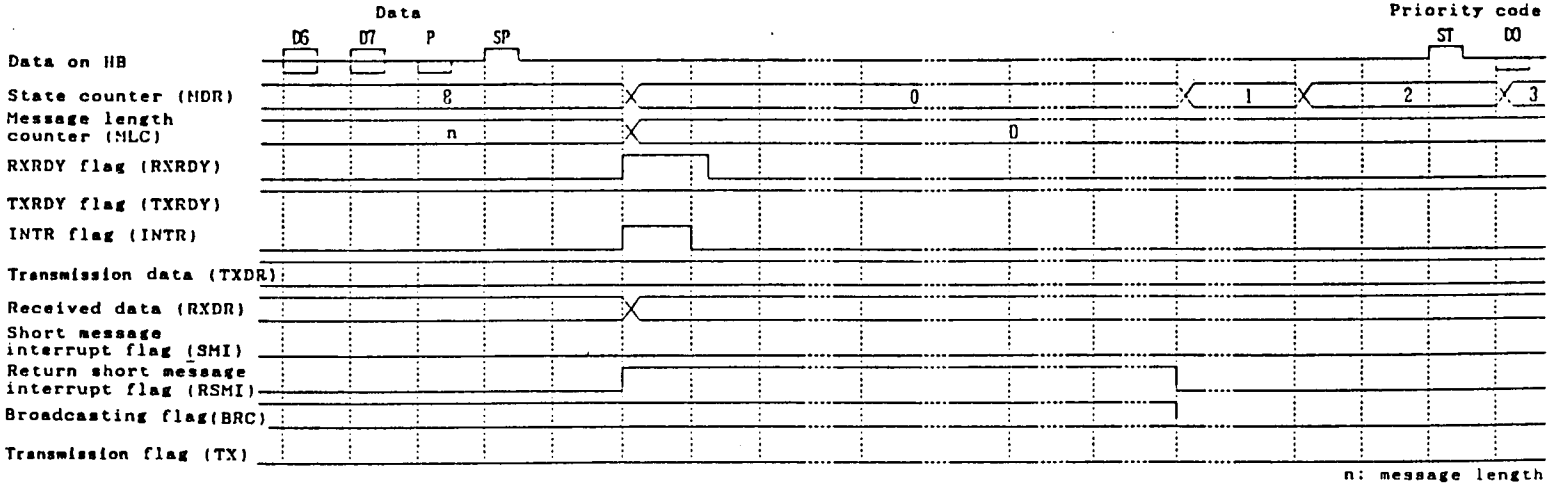


Figure 4.35 When interrupt has been applied to received packet

4.3.7 Error

Figures 4.36 and 4.37 show the parity error and framing error respectively. Both case show that an error occurs in the message length code.

The framing error does not occur at the data portion of long message because the error works as short message interrupt at this portion.

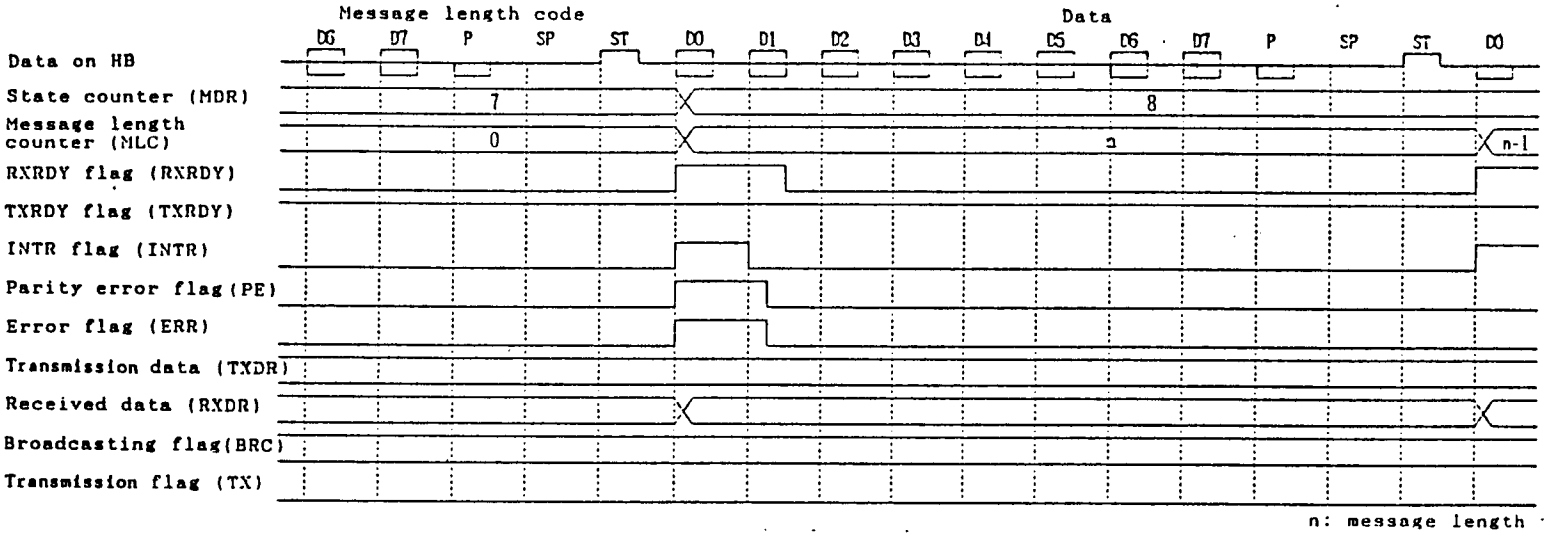


Figure 4.36 Parity error

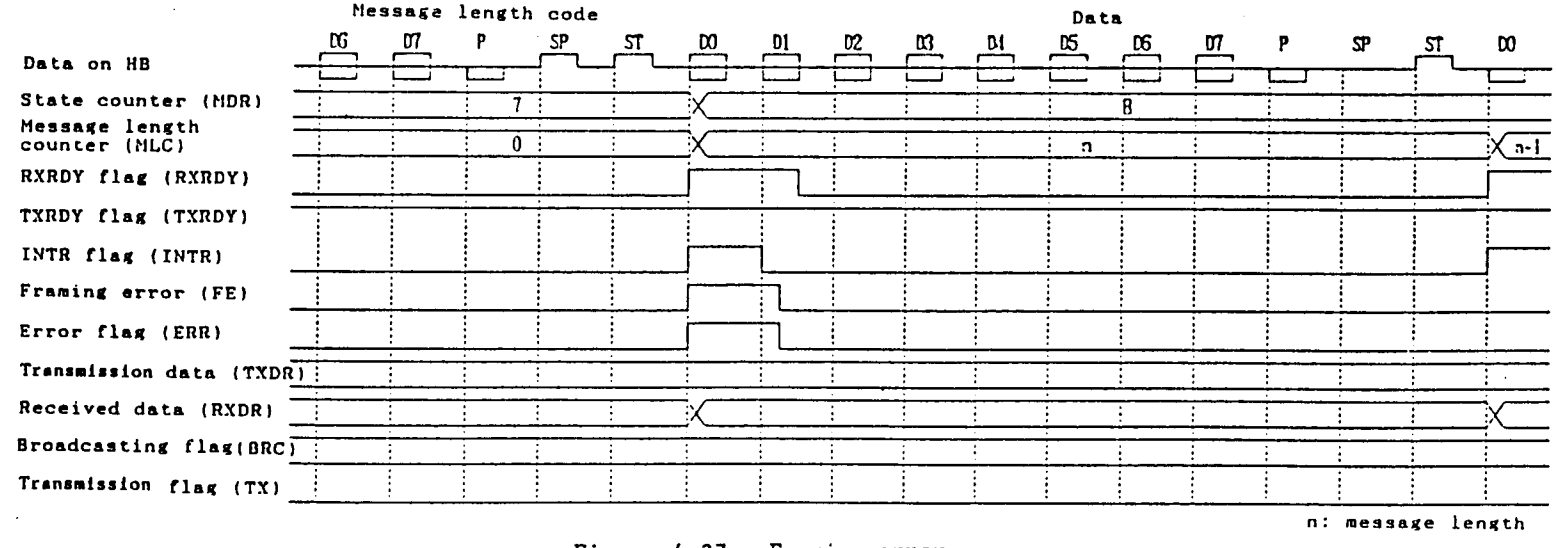


Figure 4.37 Framing error

4.3.8 Read lost data

In Figure 4.38, read lost data (RLD) occurs because the CPU has not read the received data set in (1) before the next received data is set. In this case, the contents of received data is replaced with new data and data that has been set is lost.

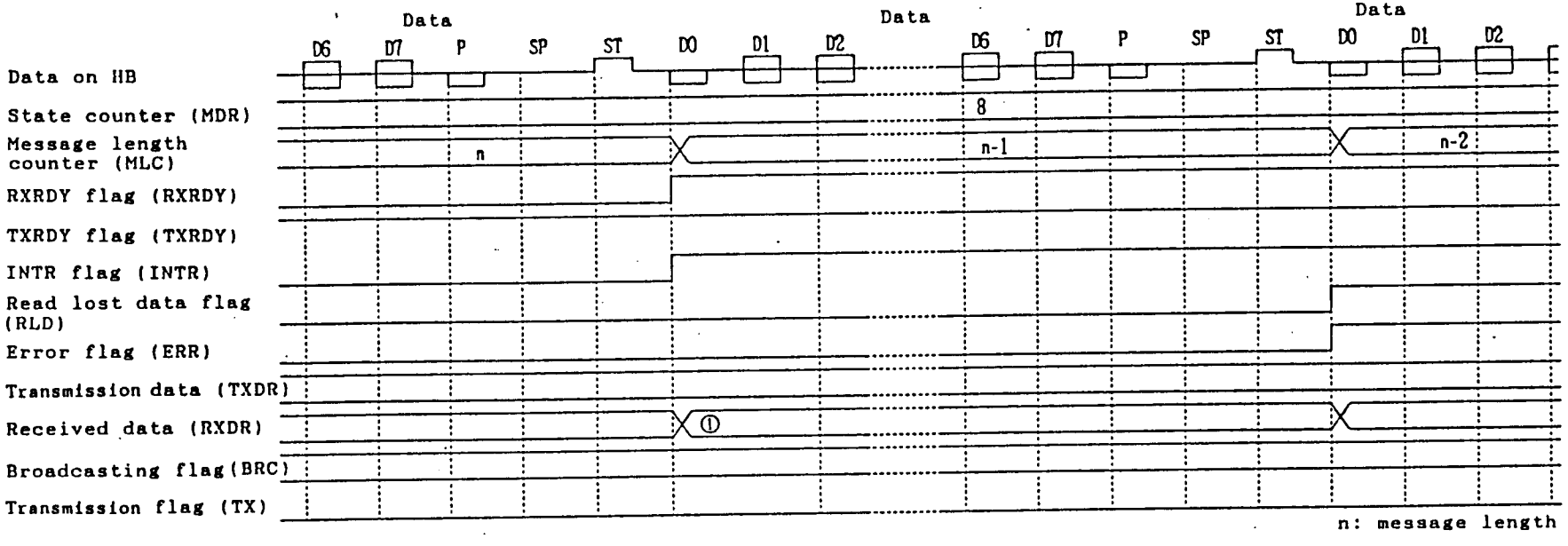


Figure 4.38 Read lost data

4.3.9 Write lost data

Figure 4.39 shows that the next transmission data is not transferred from the CPU during data sending due to some reason. In this case, write lost data (WLD) occurs and sending is stopped. In this case, MDR changes from 8 to 0 and the synchronization recovery period is started. This figure assumes that the CPU stops. Read lost data (RLD) has therefore occurred at the same time. The transmission flag (TX) is set to 'L' when MDR changes from 0 to 2.

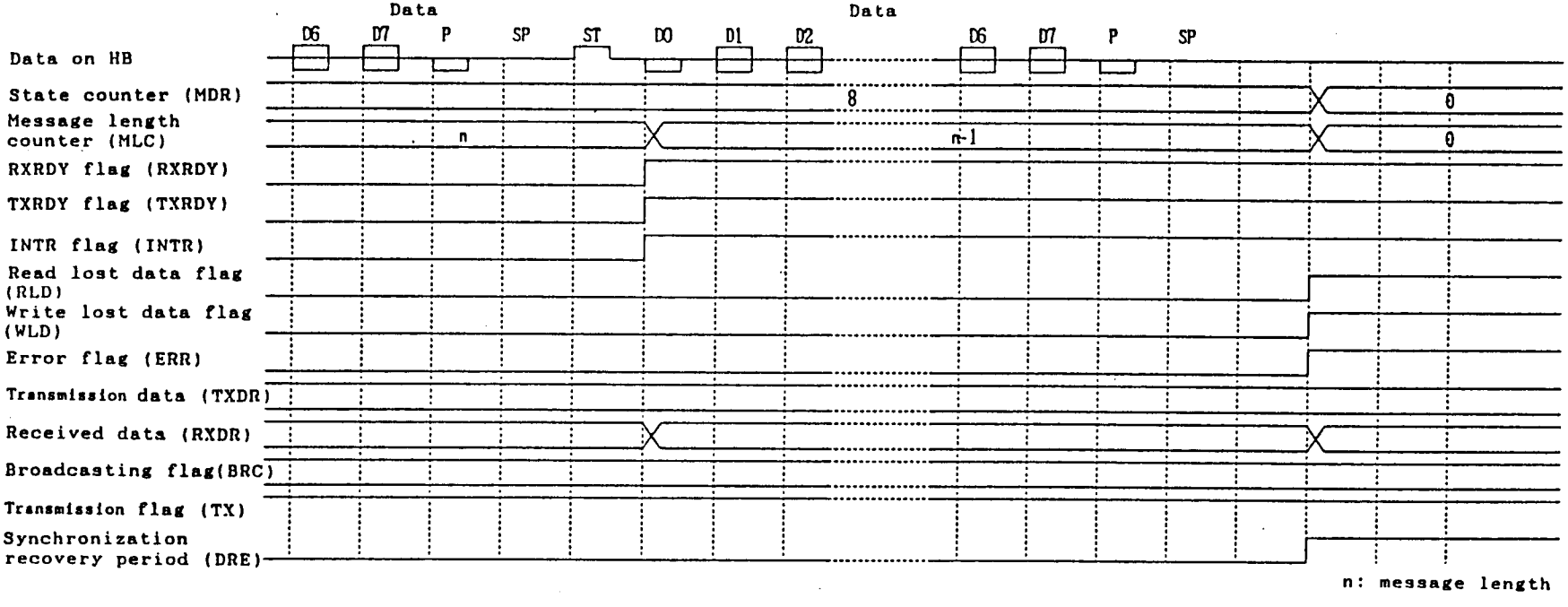


Figure 4.39 Write lost data

4.3.10 Received data error

Figure 4.40 shows a received data error. This figure shows that data does not come in data receiving. In this case, MDR changes from 8 to 0 and the synchronization recovery period is started.

Figure 4.41 shows a case that data is larger than the message length. The synchronization recovery period starts at the D0 position. One character later, the sending/receiving interrupt mask flag falls to disable interrupt. In this case, MDR changes from 0 to 2.

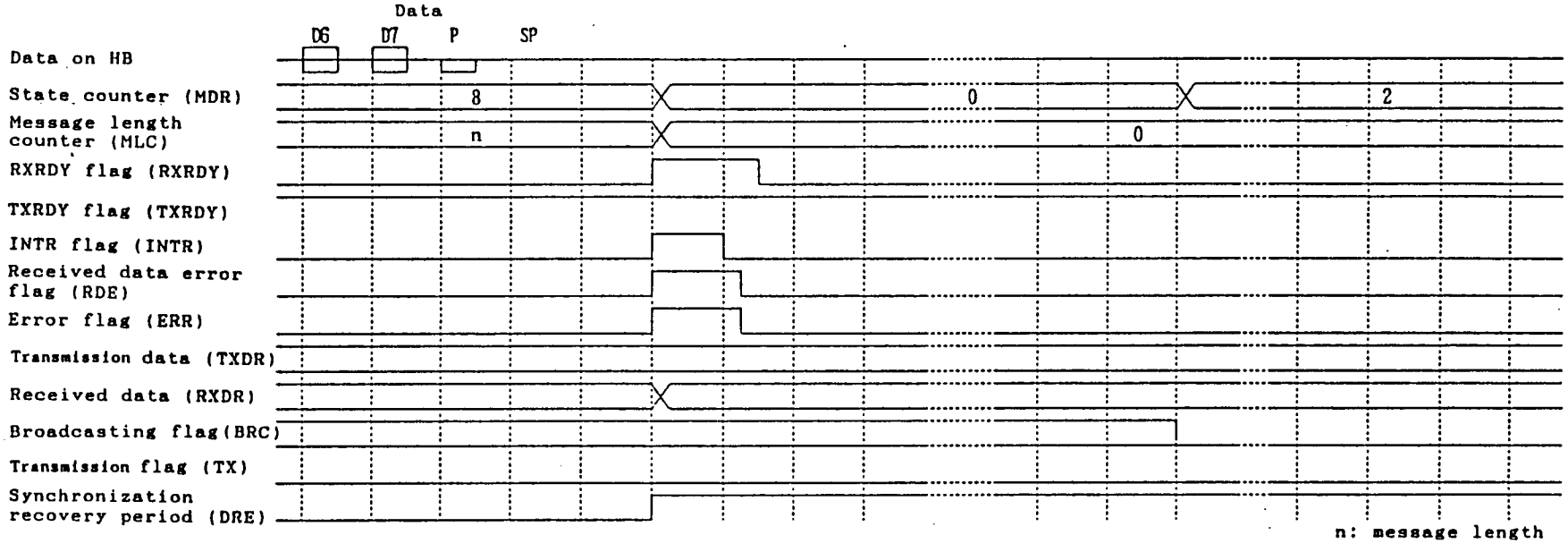


Figure 4.40 Received data error (when data is smaller)

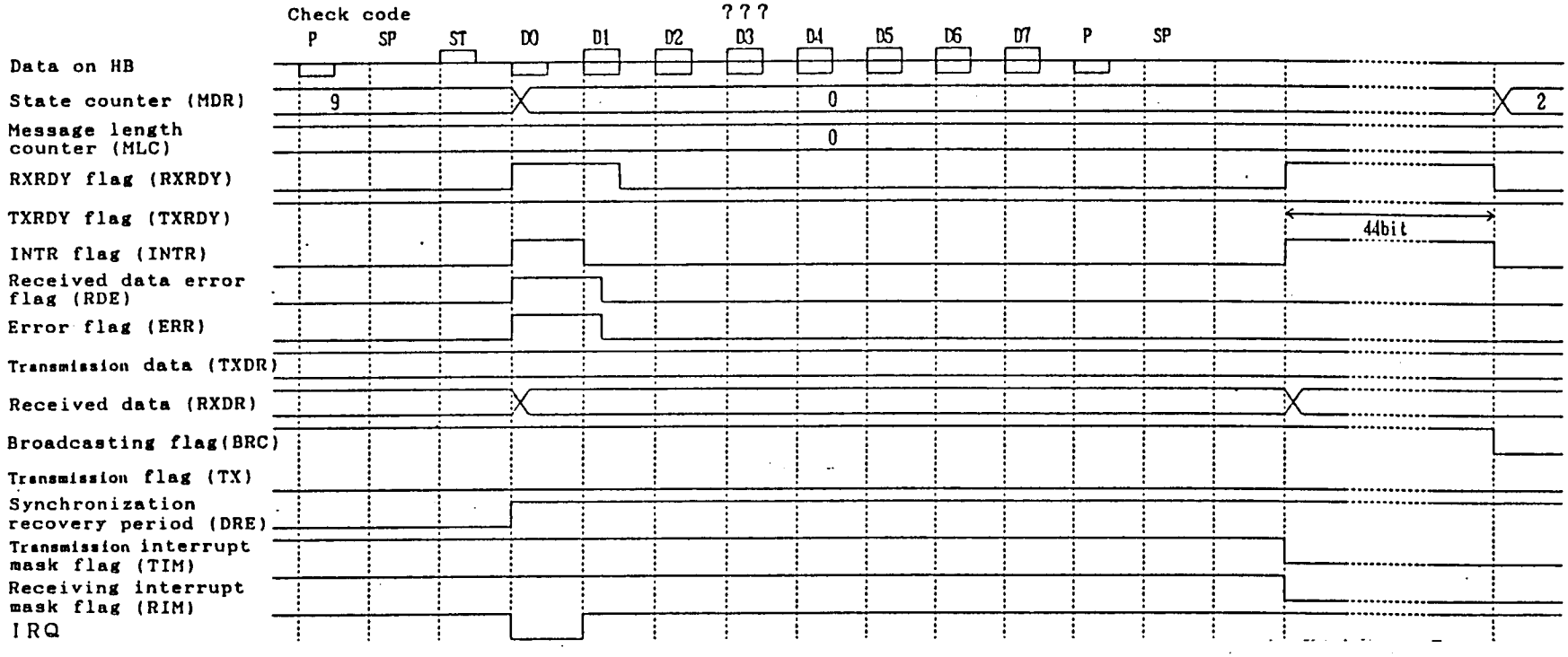


Figure 4.41 Received data error (when data is larger)

4.3.11 Contention defeat

Figure 4.42 shows contention defeat. This figure shows that contention defeat occurs in the priority code. The contention defeat falg (CD) rises when ST of the source address changes to DO. Upon contention, the transmission flag (TX) is set to 'L' at the position where the contention defeat flag (CD) rises (ST → DO) as shown in this figure. In this case, if data is written in and after the source address, the data is treated as the priority code of the next packet. The receiving operation then follows.

Figure 4.43 shows a parity error upon contention. In this case, contention defeat in the parity bit can be assumed.

When contention defeat occurs in the stop bit (i.e. when "0" is output as the stop bit), the parity error flag in Figure 4.43 is replaced with the framing error flag.

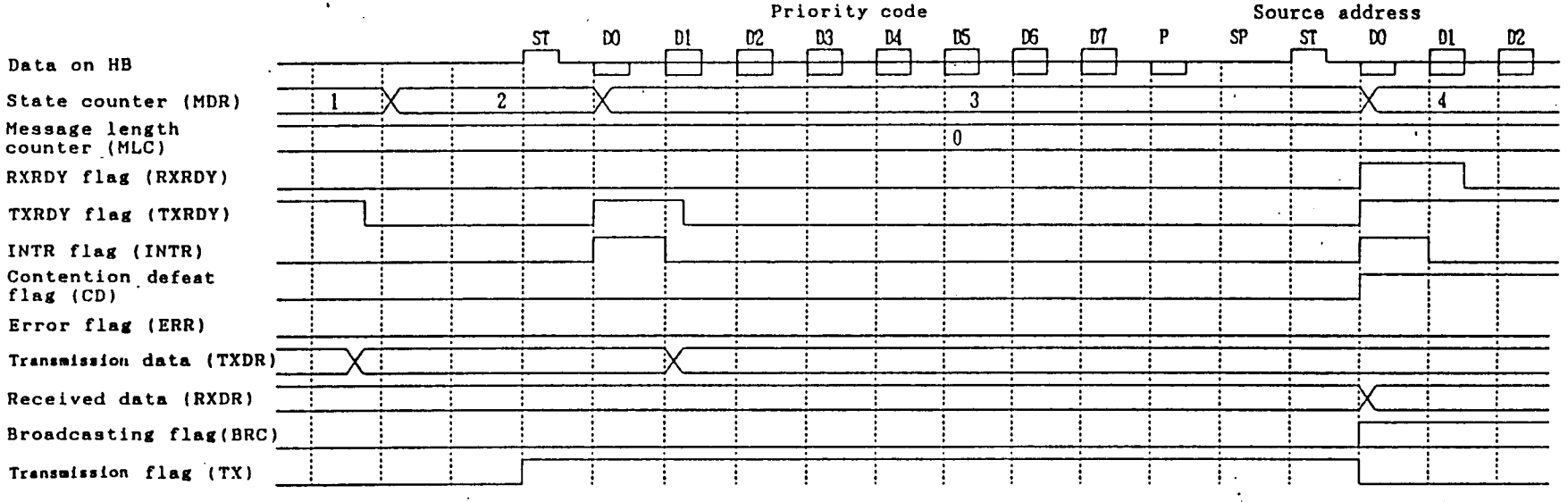


Figure 4.42 Contention defeat

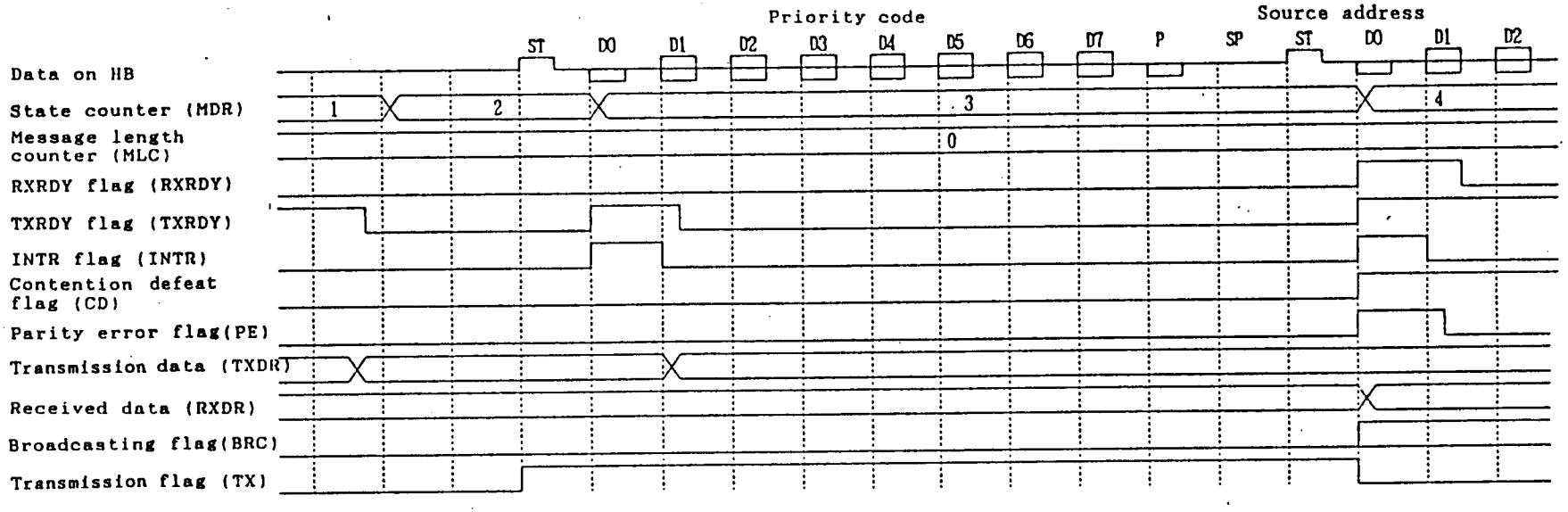


Figure 4.43 Contention defeat (parity error)

4.3.12 ACK/NAK error

Figure 4.44 shows that an ACK/NAK error occurs when ACK/NAK is not detected at the ACK/NAK detecting position. In this case, the status counter (MDR) changes from 10 to 10 and from 10 to 0. (MDR is 10 for duration of 22 bits.)

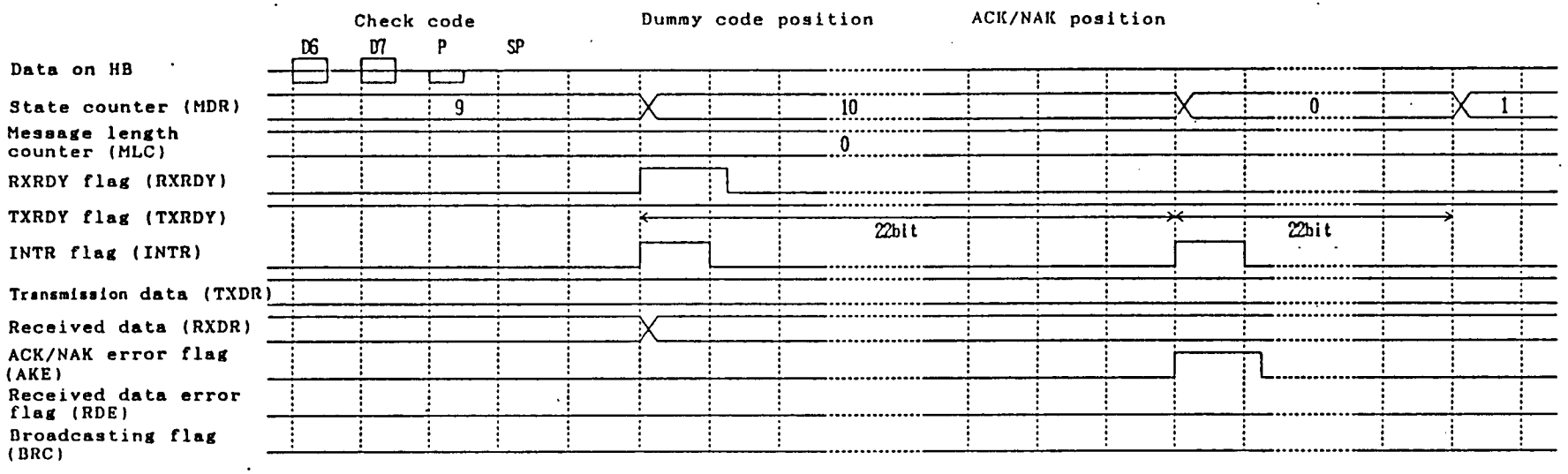


Figure 4.44 ACK/NAK error

4.3.13 After resetting

Figures 4.45 and 4.45 show the synchronization recovery period after resetting.

Figure 4.45 shows that the synchronization recovery period is ended with timeout (10 ms + 22 bits) and the normal receiving operation is started with following data.

Figure 4.46 shows that the data receiving operation is started before the synchronization recovery period ends because data comes in 10 ms + 22 bits of synchronization recovery period. In this case, the synchronization recovery period is reset by receiving a packet without parity error. During data receiving operation in the synchronization recovery period, the state counter operates.

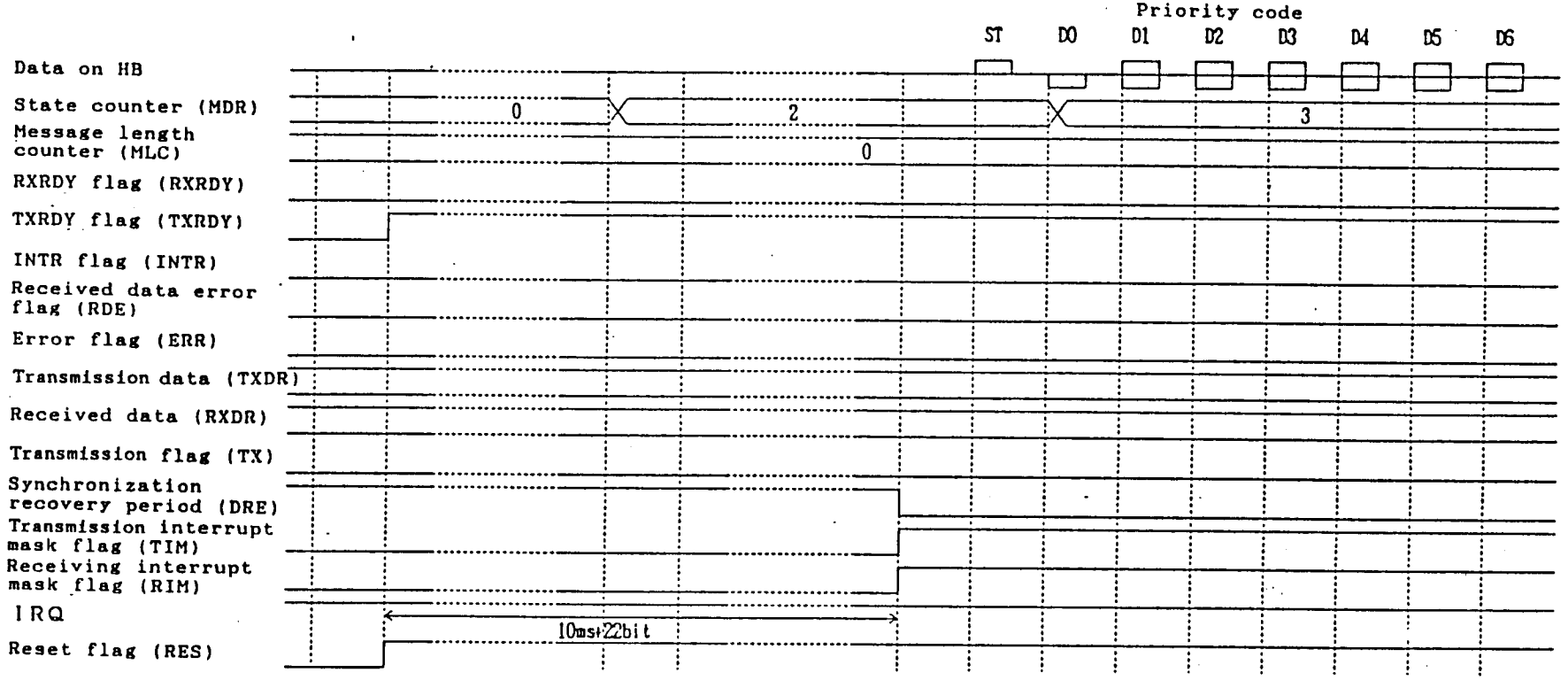


Figure 4.45 Operation after resetting (10 ms + 22 bits provided)

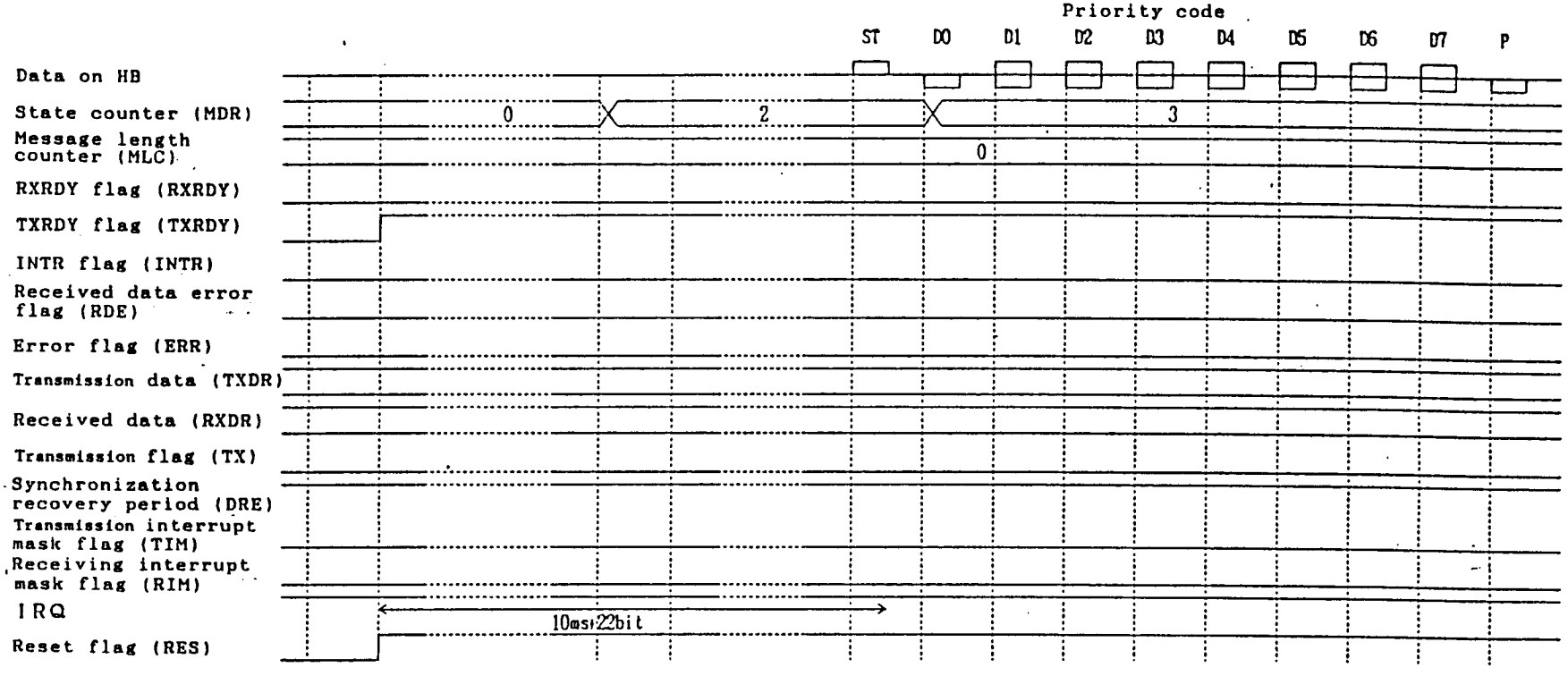


Figure 4.46 Operation after resetting (10 ms + 22 bits not provided)

5.1 Maximum Absolute Ratings

Item	Symbol	Condition	Rating		Unit
			Minimum	Maximum	
Supply voltage	Vcc	Vss = 0V	Vss-0.5	+6.0	V
Input voltage	V_I	Vss = 0V	Vss-0.5	Vcc+0.5	V
Output voltage	V_O	Vss = 0V	Vss-0.5	Vcc+0.5	V
Output current (*1)	Ios	V0 = Vcc	-	+70	mA
		V0 = 0V	-	-40	mA
Operating temperature	Top		-25	+85	°C
Storage temperature	Tstg		-40	+125	°C

*1 Vcc = 6.0 V, 1 second for 1 pin

Note:

LSI may be permanently destroyed if the controller is used exceeding the maximum absolute ratings. The controller should be used in recommended conditions. Reliability of LSI may be affected if the controller is used exceeding recommended conditions.

5.2 Recommended Operating Conditions

Item	Symbol	Condition	Standard value			Unit
			Minimum	Standard	Maximum	
Supply voltage	Vcc		4.5	5.0	5.5	V
H level input voltage	V_{IH}	TTL input	2.6	-	-	V
L level input voltage	V_{IL}		-	-	0.8	V
Operating temperature	Ta		-20	-	+70	°C

5.3 DC Characteristics

Ta = -20 to +70°C, Vcc = 5.0V ±10%, Vss = 0V

Item	Symbol	Pin	Condition	Standard value			Unit
				Minimum	Standard	Maximum	
H level outpute voltage	V_{OH}	$\overline{TXH}$, D_0-D_7, $\overline{TXL}$, $\overline{IRQ}$	I_{OH}=-0.4mA	4.0	-	Vcc	V
L level output voltage	V_{OL}		I_{OL}=-3.2mA	Vss	-	0.4	V
Input leak current	I_{LI}	(*1)	V_I=0V to Vcc	10	-	10	μA
Input leak current	I_{LZ}	D_0-D_7		10	-	10	μA
Supply current	Iccs	Vcc	Static state (*2)	-	-	0.1	mA

*1 A_0 to A_2, $\overline{RXD}$, $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, $\overline{RESET}$, CLK, CSEL

*2 V_{IH} = Vcc, V_{IL} = Vss

5.4 Input/output Capacity

Ta = 25°C

Item	Symbol	Condition	Standard value			Unit
			Minimum	Standard	Maximum	
Input pin	C_{IN}	Vcc = VI = 0V f = 1 MHz	-	-	9	pF
Output pin	C_{OUT}		-	-	9	pF
I/O pin	$C_{I/O}$		-	-	11	pF

5.5 AC Characteristics

5.5.1 Read timing

Item	Symbol	Condition	Standard value			Unit
			Minimum	Standard	Maximum	
Address setup time (until the falling edge of $\overline{RD}$)	t_{SET}		20	-	-	ns
Address hold time (from the rising edge of $\overline{RD}$)	t_{HLD}		20	-	-	ns
$\overline{RD}$ pulse width	t_{RD}		200	-	-	ns
Data delay period (from the falling edge of $\overline{RD}$)	t_{DACC}		-	-	60	ns
Data hold time (from the rising edge of $\overline{RD}$)	t_{DOH}		0	-	-	ns
IRQ release time (from the rising edge of $\overline{RD}$)	t_{IR}		1.6	-	4.8	µs
STR2 clear time (from the rising edge of $\overline{RD}$)	t_{ST}		1.6	-	4.8	µs

Figure 5.1 Read timing

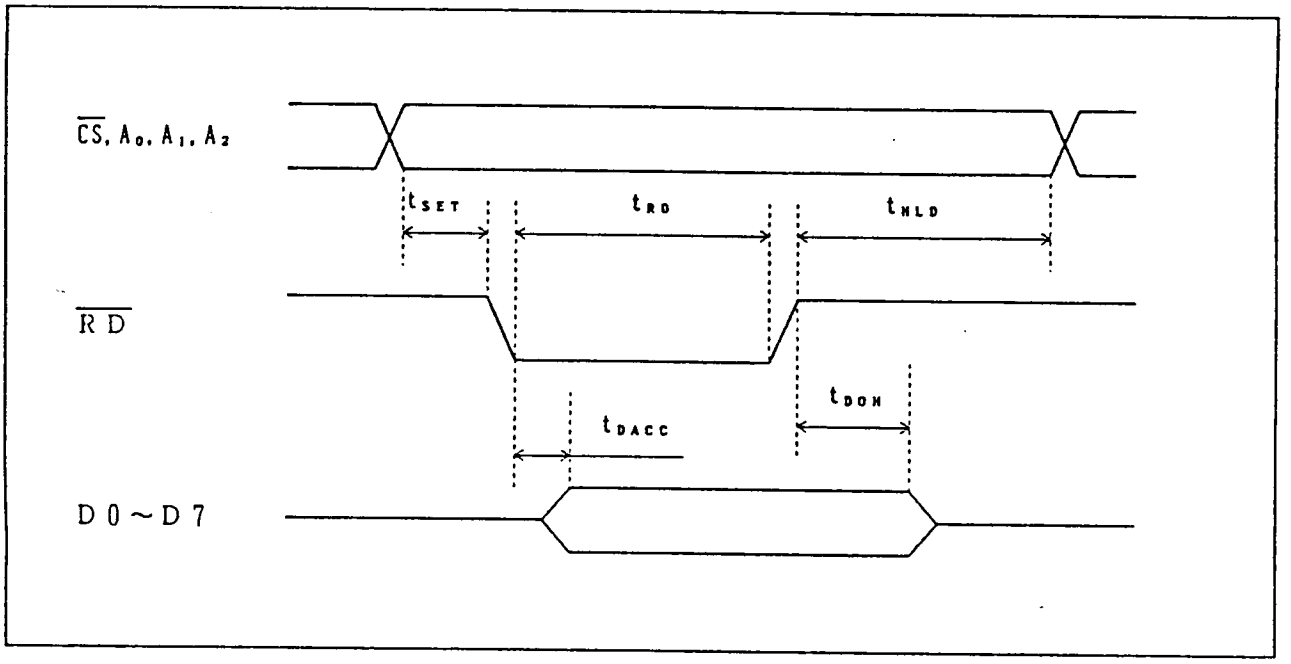


Figure 5.2 $\overline{IRQ}$ timing

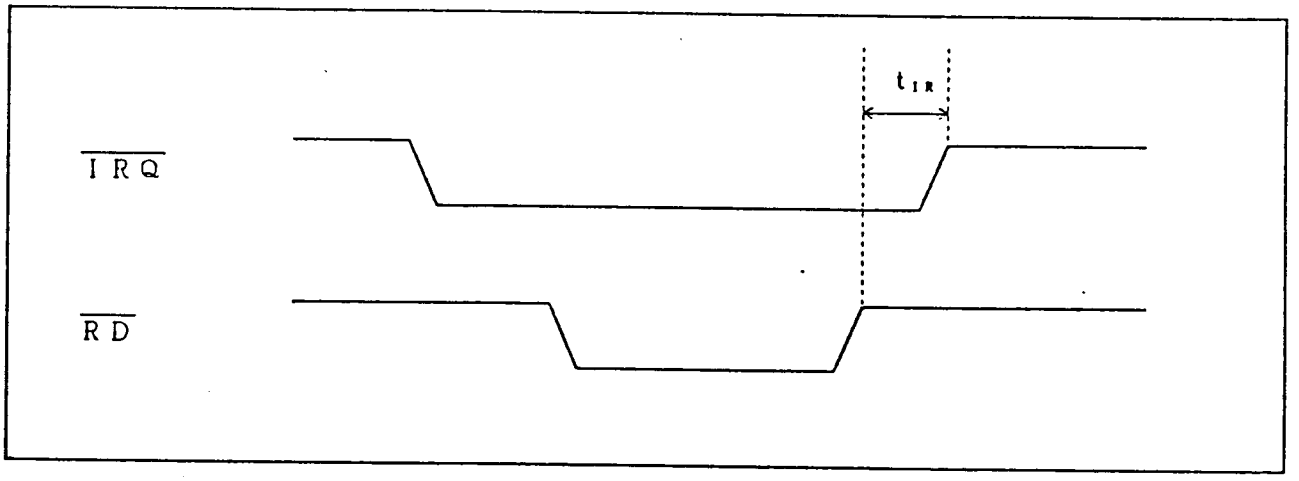
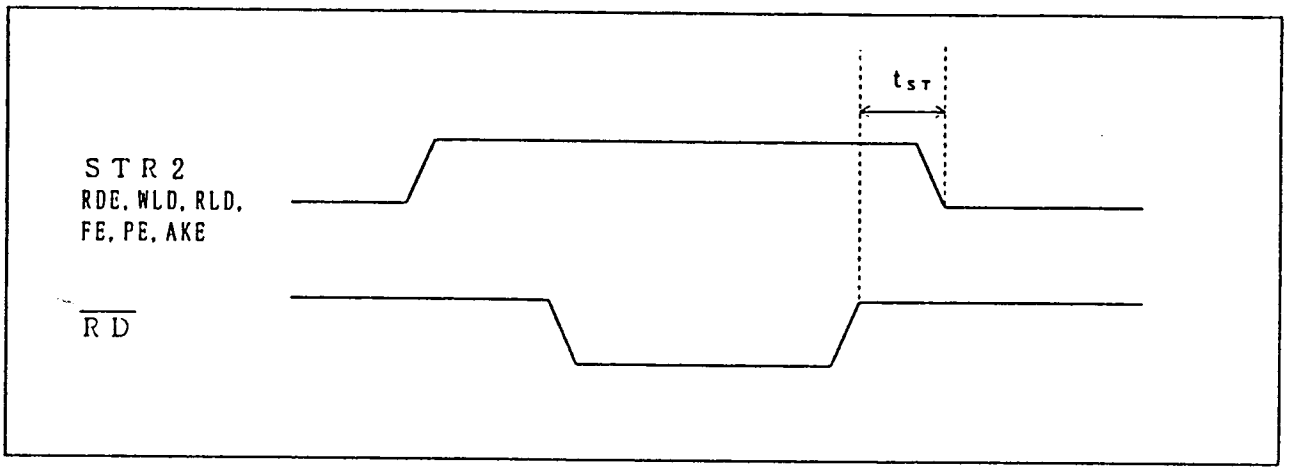


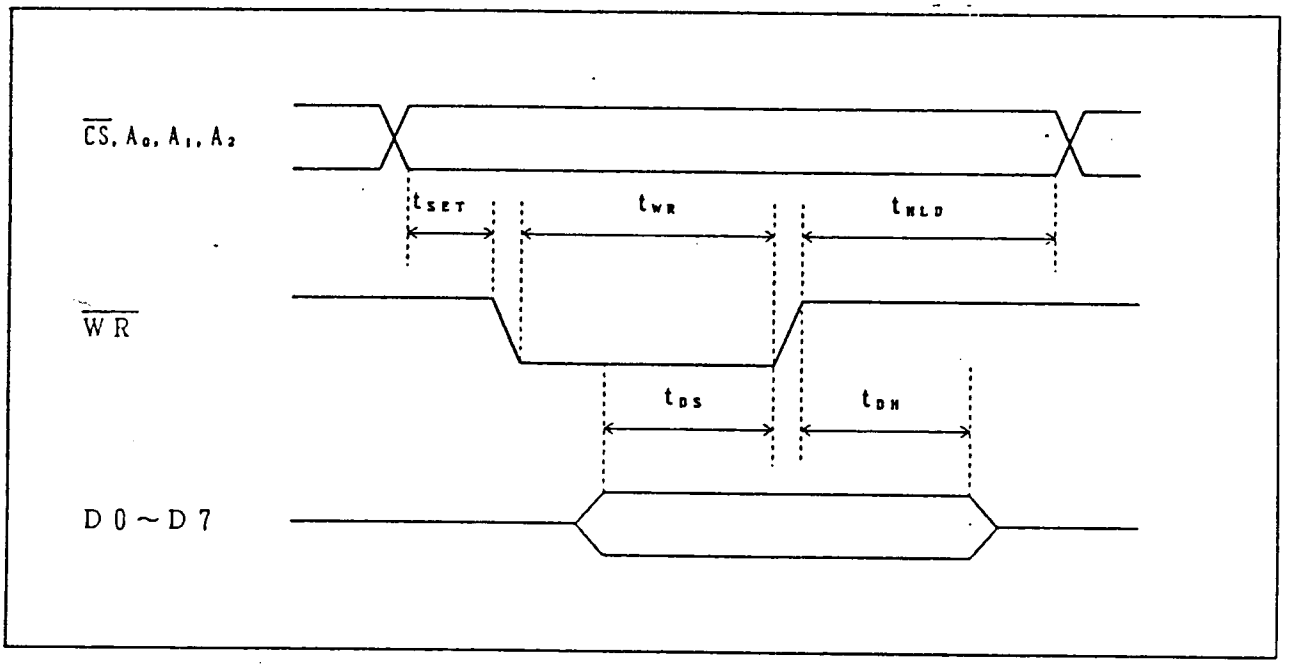
Figure 5.3 Status register 2 (RDE, WLD, RLD, FE, PE, AKE) clear timing



5.5.2 Write timing

Item	Symbol	Condition	Standard value			Unit
			Minimum	Standard	Maximum	
Address setup time (until the falling edge of $\overline{WR}$)	t_{SET}		20	-	-	ns
Address hold time (from the rising edge of $\overline{WR}$)	t_{HLD}		20	-	-	ns
$\overline{WR}$ pulse width	t_{WR}		200	-	-	ns
Data setup time (until the rising edge of $\overline{WR}$)	t_{DS}		100	-	-	ns
Data hold time (from the rising edge of $\overline{WR}$)	t_{DH}		20	-	-	ns

Figure 5.4 Write timing



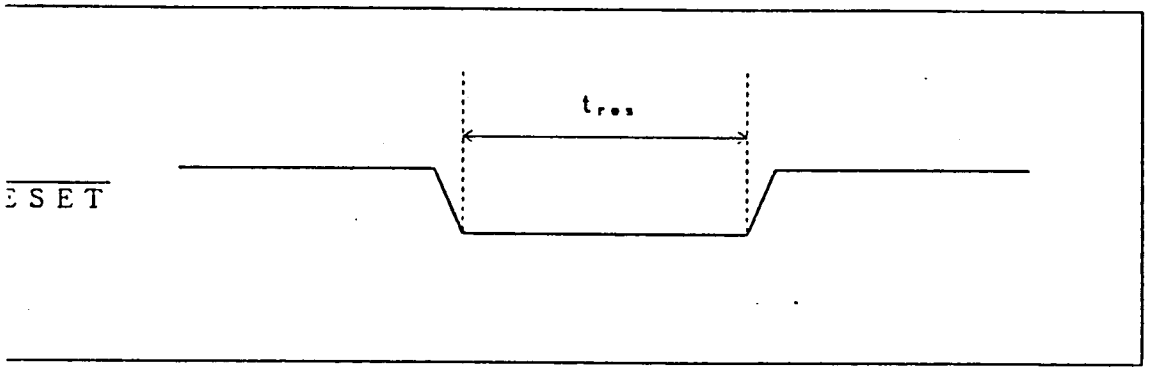
5.5.3 Clock frequency

Item	Symbol	Condition	Standard value			Unit
			Minimum	Standard	Maximum	
Clock frequency	fc	CSEL = "H"	-	4915.2	-	kHz
		CSEL = "L"	-	614.1	-	kHz

5.5.4 Valid pulse width of reset signal

Item	Symbol	Condition	Standard value			Unit
			Minimum	Standard	Maximum	
Reset pulse width	t_{res}		3.2	-	-	μs

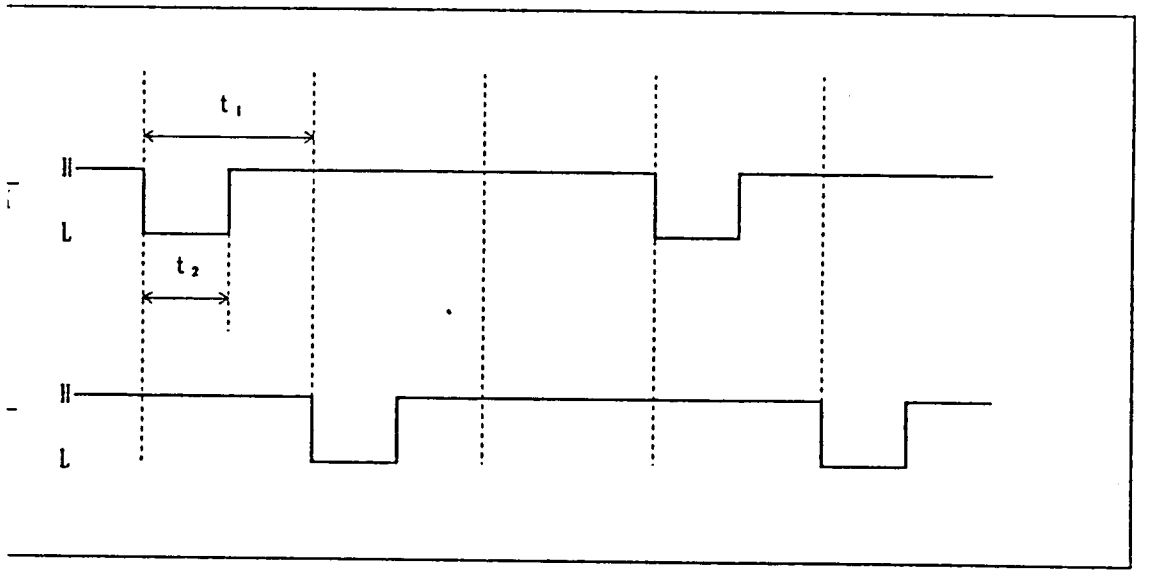
5 Reset signal valid pulse width



ata output timing

tem	Symbol	Condition	Standard value			Unit
			Minimum	Standard	Maximum	
ɔut pitch	t_1		-	104.17	-	μs
ılse width	t_2		-	52.08	-	μs

ɔ Data output timing



5.5.6 Data input timing

Item	Symbol	Condition	Standard value		Unit
			- direction	+ direction	
Input pulse position	t3	Second character and following characters of the packet being received	-13	+26	μs
Input pulse width	t_4		-11.4	+39.1	μs

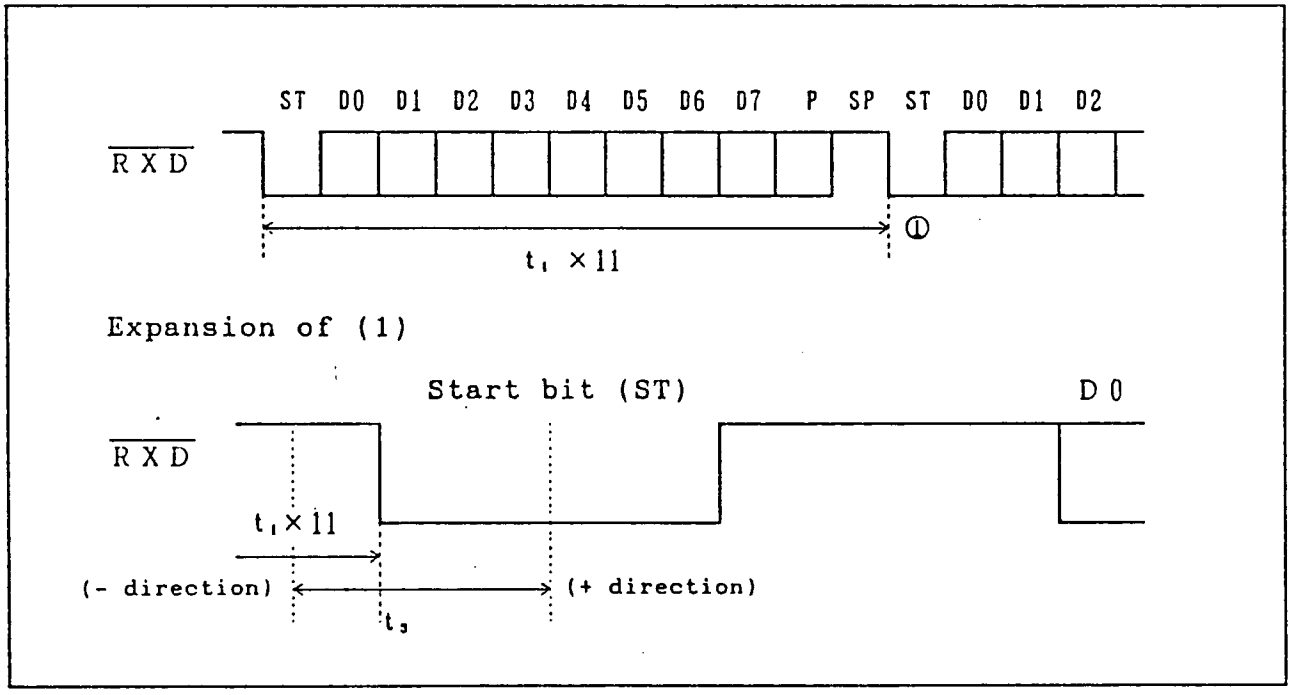


Figure 5.7 Input pulse position

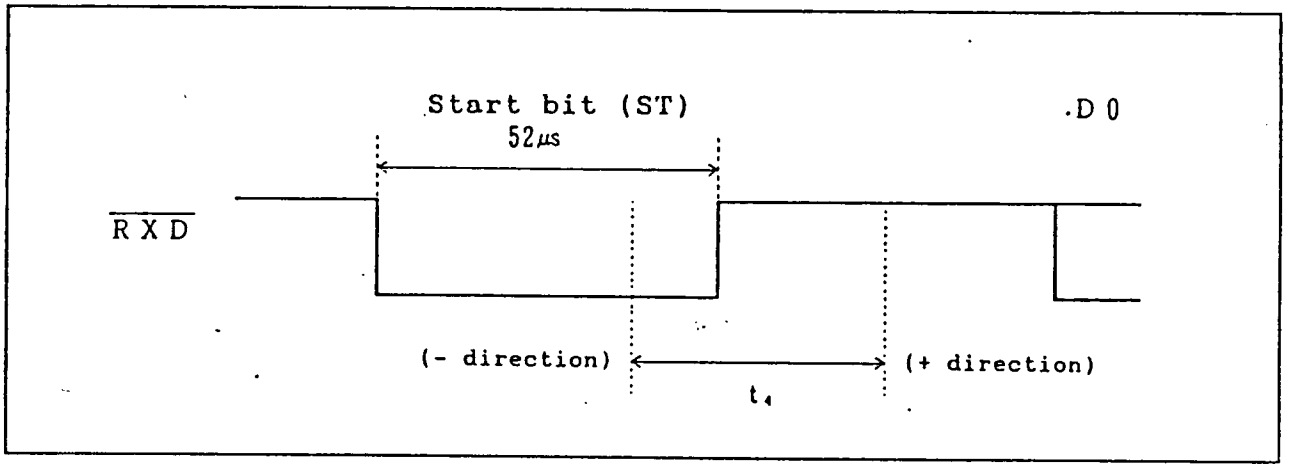


Figure 5.8 Input pulse width

6.1 System Configuration Example

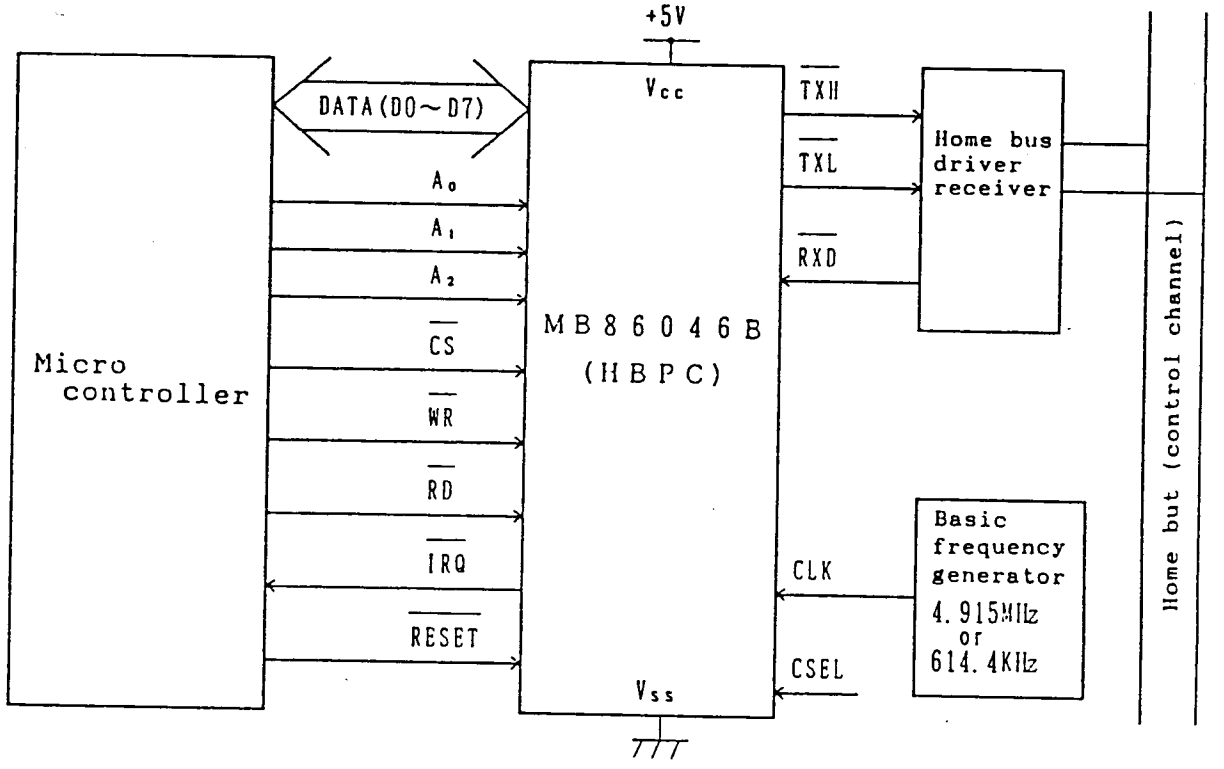


Figure 6.1 System configuration example

6.2 Circuit Configuration Example

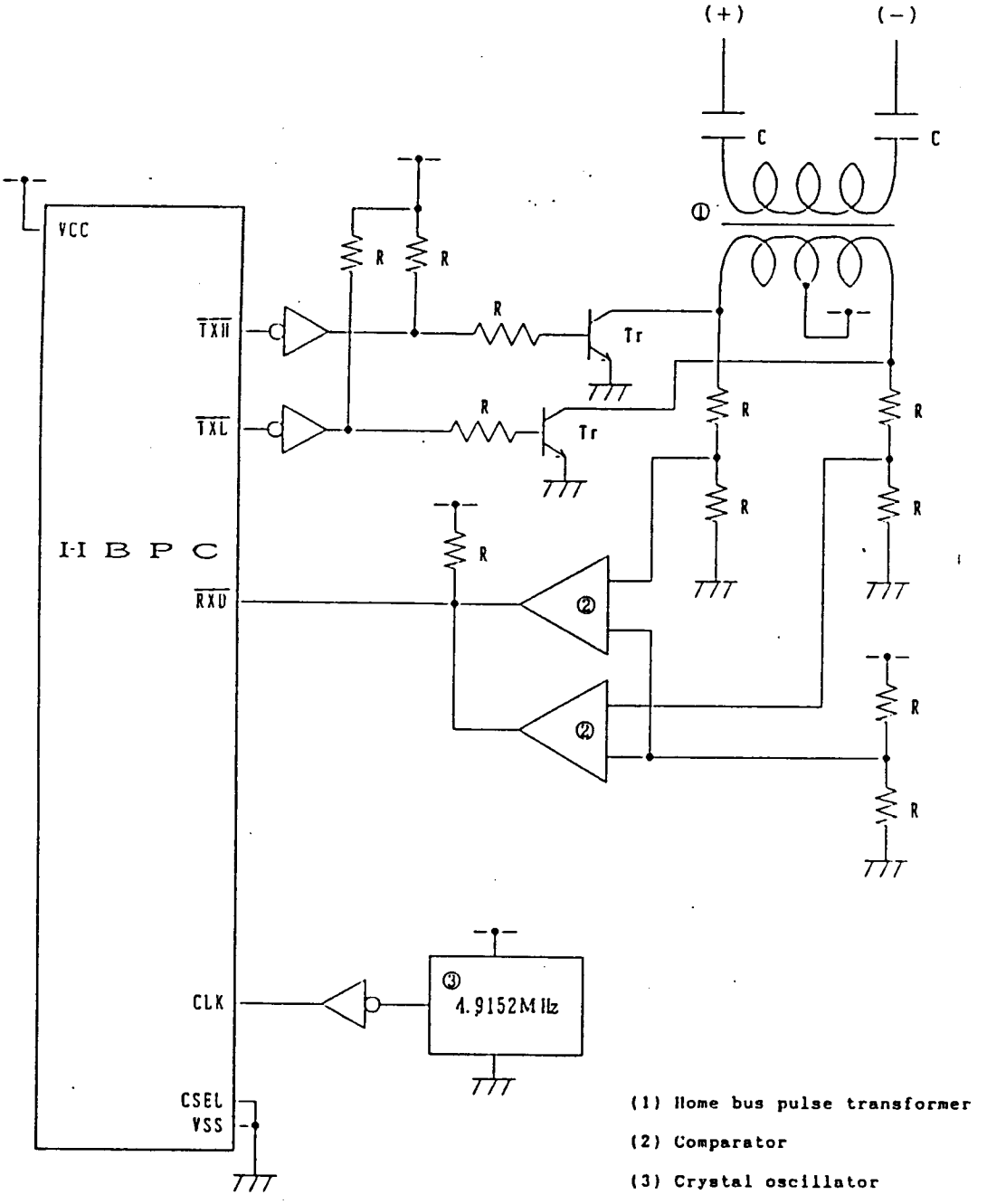


Figure 6.2 Home bus circuit configuration example

Note:

Document by HBS Committee showing an example of pulse transformer.

6.3 Block Diagram Configuration Example