# iC-TW2 8-BIT SIN/COS INTERPOLATION IC WITH INTEGRATED EEPROM



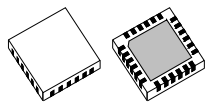
## FEATURES

- Programmable angle resolution from 1 to 256 steps per period
- Interpolation factors from x0.25 to x64
- Input frequency to 115 kHz with x64, to 230 kHz with x32, to 460 kHz with x16
- Latency of less than 1 µs
- Selectable gain permits single-ended and differential input signals from 10 mV to 1.5 V peak-peak
- Index gating input with fine adjustable offset
- Programmable index pulse output position and width
- Four incremental output modes: quadrature encoder with index, up/down clock, increment/direction, 3 phase commutation
- Programmable filter and hysteresis
- Direct sensor connection, minimized count of external components
- Non-volatile setup due to internal EEPROM
- Fully re-programmable via serial 1- and 2-wire interfaces
- Power-on reset circuit and on-chip oscillator
- ESD protection and TTL-/CMOS-compatible outputs

## APPLICATIONS

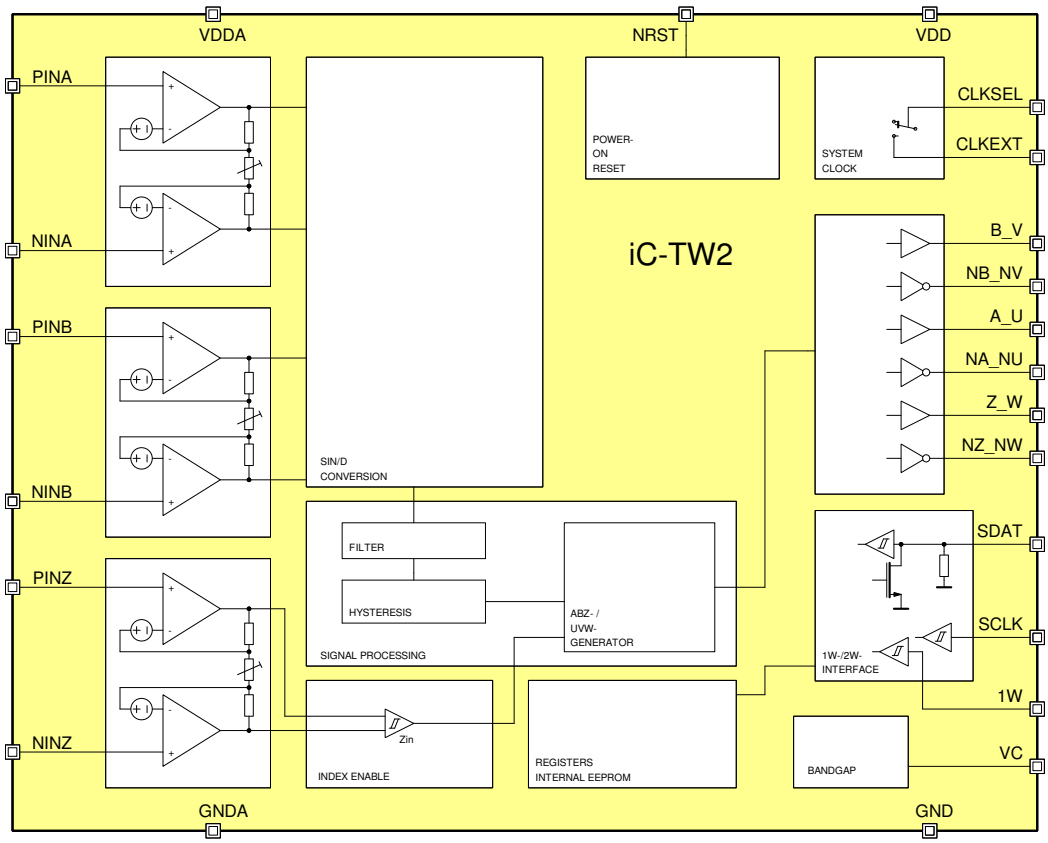
- Interpolation IC for position data acquisition from analog sine/cosine sensors
- Optical linear and rotary encoders
- Magneto resistive sensors and encoders

## PACKAGES



QFN24

## BLOCK DIAGRAM



## DESCRIPTION

iC-TW2's interpolation engine accepts two fully differential sensor bridges delivering sinusoidal input signals (SIN/COS) to produce a highly interpolated output signal. No further external components are required. Single ended sensor signals are supported by tying the negative input terminal to a signal reference, usually VDD/2.

iC-TW2 generates one index pulse for every input period. The position in respect to the start of the period as well as the width of the pulse is fully programmable. Index pulse position can be used in conjunction with the startup mode to guarantee a desired phase relationship between A, B and index output pulse.

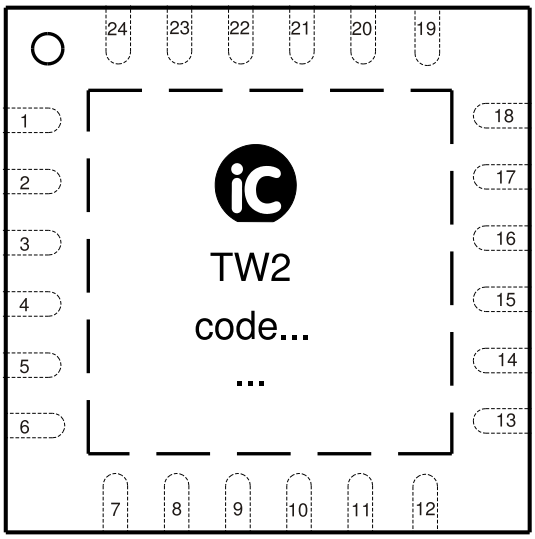
There are four different output modes provided, including 3-phase commutation output for brushless DC motors. It is highly programmable to meet requirements for a wide range of applications. Two serial interfaces have been included to permit configuration of the device, also accessing an internal EEPROM. Both interfaces allow complete configuration of the device including transfer of setup and system data to register and EEPROM for non-volatile configuration.

For an illustration of the interpolation function of the iC-TW2 see Figure 2 on page 10.

## CONTENTS

## PACKAGES

### PIN CONFIGURATION QFN24 4 mm x 4 mm




### PIN FUNCTIONS

| No. | Name | Function |
|---|---|---|
| 1 | VDD | +3 V to +5.5 V Digital Supply Voltage |
| 2 | B_V | B Signal / V Signal Output |
| 3 | NB_NV | Inverted B / Inverted V Signal Output |
| 4 | A_U | A Signal / U Signal Output |
| 5 | NA_NU | Inverted A / Inverted U Signal Output |
| 6 | GND | Digital Ground |
| 7 | NZ_NW | Inverted Z / Inverted W Signal Output |
| 8 | Z_W | Z Signal / W Signal Output |
| 9 | 1W | 1W-Interface, signal input |
| 10 | VDDA | +3 V to +5.5 V Analog Supply Voltage |
| 11 | GNDA | Analog Ground |
| 12 | n.c. | Pin not connected |
| 13 | PINB | Signal Input B+ |
| 14 | NINB | Signal Input B- |
| 15 | CLKSEL | System Clock Selection Input |
| 16 | NRST | External Reset Input (active low) |
| 17 | NINA | Signal Input A- |
| 18 | PINA | Signal Input A+ |
| 19 | VC | 1.2 V Reference Voltage Output |
| 20 | NINZ | Signal Input Z- (Index) |
| 21 | PINZ | Signal Input Z+ (Index) |
| 22 | SCLK | 2-Wire Interface, clock input |
| 23 | CLKEXT | External Clock Input |
| 24 | SDAT | 2-Wire Interface, serial data in/out |
| TP | | *Thermal Pad* (bottom side) |

The *Thermal Pad* of the QFN package (bottom side) is to be connected to a ground plane on the PCB which must have GND potential. GNDA must be wired to GND.

**Only pin 1 marking on top or bottom defines the package orientation (iC-TW2 label and coding is subject to change).**

## ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

| Item No. | Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| G001 | VDD, VDDA | Supply Voltage VDD, VDDA | referenced to GND | -0.3 | 6.0 | V |
| G002 | ΔVDDA | Supply Voltage Difference VDD vs. VDDA | ΔVDDA = VDD - VDDA | 0 | 0.5 | V |
| G003 | V() | Voltage at PINA, NINA, PINB, NINB, PINZ, NINZ, B_V, NB_V, A_U, NA_U, Z_W, NZ_W, 1W, SDAT, SCLK, CLKSEL, CLKEXT | referenced to GND | -0.3 | VDD + 0.5 V | V |
| G004 | I() | Current in PINA, NINA, PINB, NINB, PINZ, NINZ, B_V, NB_V, A_U, NA_U, Z_W, NZ_W, 1W, SDAT, SCLK, CLKSEL, CLKEXT, VC | | -20 | 20 | mA |
| G005 | Vd | ESD Susceptibility Of Signal Outputs | HBM, 100 pF discharged through 1.5 kΩ; pins A_U, NA_U, B_V, NB_V, Z_W, NZ_W | | 1.5 | kV |
| G006 | Vd | ESD Susceptibility (remaining pins) | HBM, 100 pF discharged through 1.5 kΩ | | 1 | kV |
| G007 | Tj | Junction Temperature | | -40 | 125 | °C |
| G008 | Ts | Storage Temperature | | -40 | 125 | °C |

## THERMAL DATA

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| T01 | Ta | Operating Ambient Temperature | | -40 | | 125 | °C |
| T02 | Rthja | Thermal Resistance Chip To Ambient | QFN24 surface mounted to PCB, following JEDEC 51 | | 32 | | K/W |

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

## ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VDDA = 3.0...5.5 V, Tj = -40...125 °C, unless otherwise stated

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Total Device** | | | | | | | |
| 001 | VDD, VDDA | Permissible Supply Voltage VDD, VDDA | | 3.0 | | 5.5 | V |
| 002 | I(VDD, VDDA) | Total Supply Current | VDD = 3.3 V at 0 Hz<br>VDD = 3.3 V at 100 kHz<br>VDD = 5.5 V at 0 Hz<br>VDD = 5.5 V at 100 kHz | | | 5<br>20<br>8<br>40 | mA<br>mA<br>mA<br>mA |
| 003 | Vc()hi | Clamp-Voltage hi at all pins | Vc()hi = V() - VDD; I() = 10 mA | 0.5 | | 1.2 | V |
| 004 | Vc()lo | Clamp-Voltage lo at all pins | I() = -10 mA | -1.1 | | -0.3 | V |
| **Input Amplifier PINA, NINA, PINB, NINB** | | | | | | | |
| 101 | Vin()sig | Permissible Input Voltage Range | | 1.4 | | VDD - 1.2 | V |
| 102 | Step(GC) | Nominal Coarse Gain Step Size | | | 6.0 | | dB |
| 103 | AGabs(GC) | Coarse Gain Absolute Accuracy | | -1.0 | | 3.5 | dB |
| 104 | Step(GF) | Nominal Fine Gain Step Size | | | 0.7 | | dB |
| 105 | AGabs(GF) | Fine Gain Absolute Accuracy | | -0.3 | | 0.3 | dB |
| 106 | CGM | Gain Matching G(CHA)/G(CHB) | | 0.85 | | 1.15 | |
| 107 | Vin()os | Input Referred Offset Voltage | | -15 | | 15 | mV |
| 108 | Vout()ossc | Output Referred Offset Correction Step Accuracy | | -10 | | 10 | mV |
| 109 | Step(OFSx) | Nominal Offset Correction Step Size | | | 13 | | mV |
| 110 | Vout()os | Output Referred Offset Voltage | | -40 | | 40 | mV |
| 111 | FR | Permissible Input Frequency; Frequency Ratio FR = $f_{cal}$ / $f_{in}$ | INTER = 1 . . . 64, FREQ = 0<br>INTER = 1 . . . 64, FREQ = 1<br>INTER = 1 . . . 64, FREQ = 2 . . . 127<br>INTER = 17 . . . 128, FREQ = 0<br>INTER = 17 . . . 128, FREQ = 1 . . . 127<br>INTER = 129 . . . 255<br>INTER = 0 | 64<br>128<br>256<br>128<br>256<br>256<br>256 | | | |
| **Oscillator** | | | | | | | |
| 201 | $f_{osc}$ | Frequency Tuning Range | VDD = 3.0 V, Tj = 25 °C, CLOCK = 0<br>VDD = 3.0 V, Tj = 25 °C, CLOCK = 31<br>VDD = 5.5 V, Tj = 25 °C, CLOCK = 0<br>VDD = 5.5 V, Tj = 25 °C, CLOCK = 31 | <br>35<br><br>40 | | 25<br><br>28<br> | MHz<br>MHz<br>MHz<br>MHz |
| 202 | $f_{cal}$ | User Calibrated Frequency $f_{osc}$ | VDD = 3.6 V, Tj = 25 °C<br>VDD = 5.5 V, Tj = 25 °C | | | 25<br>30 | MHz<br>MHz |
| 203 | $df_{osc}$(T) | Frequency Variation | over temperature range -40 °C to 125 °C | -20 | | 0 | % |
| 204 | $df_{osc}$(V) | Frequency Variation | over supply voltage range 3.0 V to 5.5 V | 0 | | 25 | % |
| **EEPROM** | | | | | | | |
| 301 | Tret | Data Retention Time | Tj = 125 °C<br>Tj = 85 °C | 10<br>100 | | | years<br>years |
| 302 | Ncycles | Number of Erase/Write Cycles | Tj = 25 °C | 1000 | | | |
| 303 | Nread | Number of Read Cycles | | $10^6$ | | | |
| **Reference Voltage Output VC** | | | | | | | |
| 401 | Vref(VC) | Reference Voltage | $C_L$ = 100 nF, I(VC) = 0 mA | 1.15 | 1.21 | 1.27 | V |
| **Digital Inputs NRST** | | | | | | | |
| 501 | Vt()hi | Input Threshold Voltage hi | VDD = 3.3 V +/- 10 %<br>VDD = 5.0 V +/- 10 % | 1.5<br>3.3 | | | V<br>V |
| 502 | Vt()lo | Input Threshold Voltage lo | VDD = 3.3 V +/- 10 %<br>VDD = 5.0 V +/- 10 % | | | 0.8<br>1.0 | V<br>V |
| 503 | Ipu() | Input Pull-up Current | V() = 0...VDD - 1 V | | | -3 | µA |
| 504 | Vpu() | Input Pull-up Voltage | Vpu() = VDD - V(), I() = -3 µA | | | 500 | mV |

## ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VDDA = 3.0...5.5 V, Tj = -40...125 °C, unless otherwise stated

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Digital Inputs CLKSEL, CLKEXT** | | | | | | | |
| 601 | Vt()hi | Input Threshold Voltage hi | VDD = 3.3 V +/- 10 %<br>VDD = 5.0 V +/- 10 % | 1.5<br>3.3 | | | V<br>V |
| 602 | Vt()lo | Input Threshold Voltage lo | VDD = 3.3 V +/- 10 %<br>VDD = 5.0 V +/- 10 % | | | 0.8<br>1.0 | V<br>V |
| 603 | Ipd() | Input Pull-down Current | V() = 1 V...VDD | 4 | | | µA |
| 604 | Vpd() | Input Pull-down Voltage | I() = 3 µA | | | 500 | mV |
| **Digital Outputs A_U, NA_NU, B_V, NB_NV, Z_W, NZ_NW** | | | | | | | |
| 701 | Vs()hi | Output Saturation Voltage hi | Vs()hi = V(VDD) - V(), I() = -6 mA;<br>VDD = 3.3 V +/- 10 %<br>VDD = 5.0 V +/- 10 % | | | <br>0.5<br>0.4 | <br>V<br>V |
| 702 | Isc()hi | Short-circuit Current hi | V() = GND | -100 | | -15 | mA |
| 703 | Vs()lo | Output Saturation Voltage lo | I() = 6 mA;<br>VDD = 3.3 V +/- 10 %<br>VDD = 5.0 V +/- 10 % | | | <br>0.3<br>0.25 | <br>V<br>V |
| 704 | Isc()lo | Short-circuit Current lo | V() = VDD | 20 | | 140 | mA |
| 705 | tr() | Output Rise time | VDD = 3.0 V, CL() = 10 pF | | | 4 | ns |
| 706 | tf() | Output Fall Time | VDD = 3.0 V, CL() = 10 pF | | | 4 | ns |
| 707 | I()max | Permissible Load Current | source and sink | -10 | | 10 | mA |
| 708 | twhi | Duty Cycle at Output A, B | referred to period T, see Fig. 1 | | 50 | | % |
| 709 | tAB | Output Phase A vs. B | referred to period T, see Fig. 1 | | 25 | | % |
| 710 | tMTD | Minimum Transition Distance | see Fig. 1 | | 1/ $f_{core}$ | | |
| **Signal Processing** | | | | | | | |
| 801 | AAabs | Absolute Angular Accuracy | referred to 360° input signal<br>GC(2:0) = 1<br>INTER(7:0) = 0<br>FREQ(6:0) = 127<br>f() < 50 Hz | -6 | | 6 | DEG |
| 802 | AArel | Relative Angular Accuracy | referred to period of A, B<br>GC(2:0) = 1<br>INTER(7:0) = 0<br>FREQ(6:0) = 127<br>f() < 50 Hz | -20 | | 20 | % |
| 803 | ABrel | Relative Angular Accuracy<br>A vs. B | | | 1/2<br>AArel | | % |
| **Index Comparator PINZ, NINZ** | | | | | | | |
| 901 | Vin()sig | Permissible Input Voltage Range | | 0.0 | | VDD | V |
| 902 | Vin()os | Input Referred Offset Voltage | | -15 | | +15 | mV |
| 903 | Vin()step | Comparator Offset Step Size | OFSZ = 0..7<br>OFSZ = 8..15 | | 1.5<br>-1.5 | | mV<br>mV |
| **Power-Down-Reset** | | | | | | | |
| A01 | VDDon | Turn-on Threshold VDD<br>(power on release) | | | 1.8 | | V |
| A02 | tbusy()cfg | Duration of Startup Configuration | | | 20 | | ms |

## ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VDDA = 3.0...5.5 V, Tj = -40...125 °C, unless otherwise stated

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **2-Wire Interface SDAT, SCLK** | | | | | | | |
| B01 | Vt()hi | Input Threshold Voltage hi | VDD = 3.3 V +/- 10 %<br>VDD = 5.0 V +/- 10 % | 1.5<br>3.3 | | | V<br>V |
| B02 | Vt()lo | Input Threshold Voltage lo | VDD = 3.3 V +/- 10 %<br>VDD = 5.0 V +/- 10 % | | | 0.8<br>1.0 | V<br>V |
| B03 | Ipd() | Input Pull-down Current | V() = 1 V...VDD | 4 | | | µA |
| B04 | Vpd() | Input Pull-down Voltage | I() = 3 µA | | | 500 | mV |
| B05 | Vs()lo | Saturation Voltage lo at SDAT | I() = 2 mA | | | 450 | mV |
| B06 | Vs()hi | Saturation Voltage hi at SDAT | Vs()hi = VDD - V(); I() = -2 mA | | | 700 | mV |
| B07 | Isc()lo | Short-circuit Current lo at SDAT | | 3 | | | mA |
| B08 | Isc()hi | Short-circuit Current hi at SDAT | | | | -2.5 | mA |
| B09 | fclk(SCLK) | Permissible Clock Frequency SCLK | scales with oscillator frequency timing, see Table 32 | | | 1.25 | MHz |
| B10 | tbusy()e2p | Max. Duration of EEPROM access | scales with oscillator frequency timing, see Table 32 | | | 20 | ms |
| **1-Wire Interface 1W** | | | | | | | |
| C01 | Vt()hi | Input Threshold Voltage hi | VDD = 3.3 V +/- 10 %<br>VDD = 5.0 V +/- 10 % | 1.5<br>3.3 | | | V<br>V |
| C02 | Vt()lo | Input Threshold Voltage lo | VDD = 3.3 V +/- 10 %<br>VDD = 5.0 V +/- 10 % | | | 0.8<br>1.0 | V<br>V |
| C03 | Ipu() | Input Pull-up Current | V() = 0...VDD - 1 V | | | -3 | µA |
| C04 | Vpu() | Input Pull-up Voltage | Vpu() = VDD - V(), I() = -3 µA | | | 500 | mV |

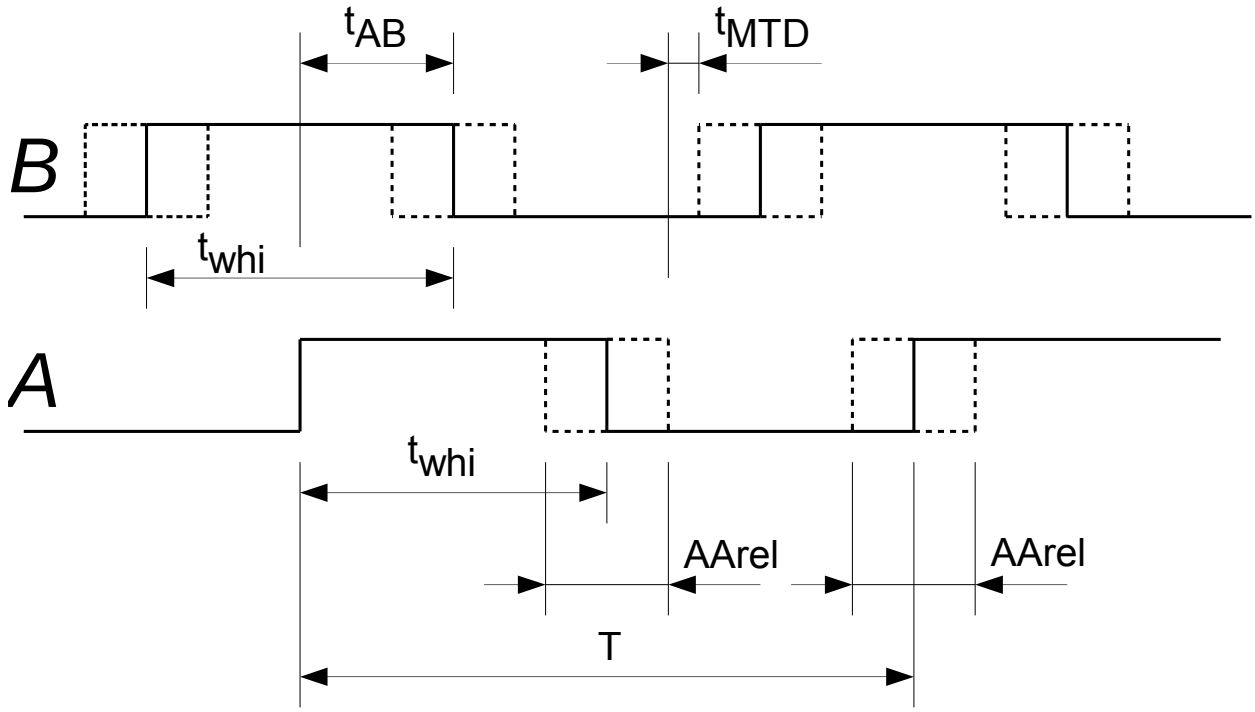



Figure 1: Relative phase distance

## REGISTER MAP

| Register Map | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Adr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| **Device Indentification** | | | | | | | | |
| 0x00 | IDA(3:0) | | | | IDB(3:0) | | | |
| **Operating Modes** | | | | | | | | |
| 0x01 | | RESET (P. 21) | CALIB1 (P. 17) | STARTUP(1:0)(P. 21) | | DIR (P. 12) | MODE(1:0)(P. 12) | |
| **Interpolation Rate** | | | | | | | | |
| 0x02 | INTER(7:0)(P. 12) | | | | | | | |
| **Index Position** | | | | | | | | |
| 0x03 | IPOS(7:0)(P. 13) | | | | | | | |
| **Index Width** | | | | | | | | |
| 0x04 | IWIDTH(7:0)(P. 13) | | | | | | | |
| **Conversion Settings** | | | | | | | | |
| 0x05 | GRANU-LAR(P. 27) | FREQ(6:0)(P. 20) | | | | | | |
| 0x06 | | | | | FILTER(1:0)(P. 20) | | HYST(1:0)(P. 20) | |
| **Gain and Offset** | | | | | | | | |
| 0x07 | | GFB(1:0) (P. 11) | | GFA(1:0) (P. 11) | | GC(2:0) (P. 11) | | |
| 0x08 | | | OFSA(5:0)(P. 11) | | | | | |
| 0x09 | | | OFSB(5:0)(P. 11) | | | | | |
| **Bias and Oscillator Trimming** | | | | | | | | |
| 0x0A | | VC(1:0)(P. 27) | | CLOCK(4:0)(P. 17) | | | | |
| **Index Computation and Miscellaneous** | | | | | | | | |
| 0x0B | OFSZ(3:0)(P. 17) | | | | EN_MON (P. 27) | CLKDLY (P. 27) | CLKDIV (P. 20) | CLKMODE (P. 27) |
| **Reserved and Calibration** | | | | | | | | |
| 0x0C | Reserved(P. 27) | | | | | | | CALIB2 |
| 0x0D | Reserved(P. 27) | | | | | | | |
| **EEPROM Control** | | | | | | | | |
| 0x0E | EE_READ (P. 27) | EE_WRITE (P. 26) | Reserved(P. 27) | | | | | |
| **Test Register** | | | | | | | | |
| 0x0F | MONITOR(7:0)(P. 27) | | | | | | | |

Table 4: Register Map

## PROGRAMMING

## DESCRIPTION OF INTERPOLATION

iC-TW2 is a monolithic A/D converter which converts sine/cosine sensor signals with a selectable resolution and hysteresis into angle position data. The interpolation function is shown in Figure 2.

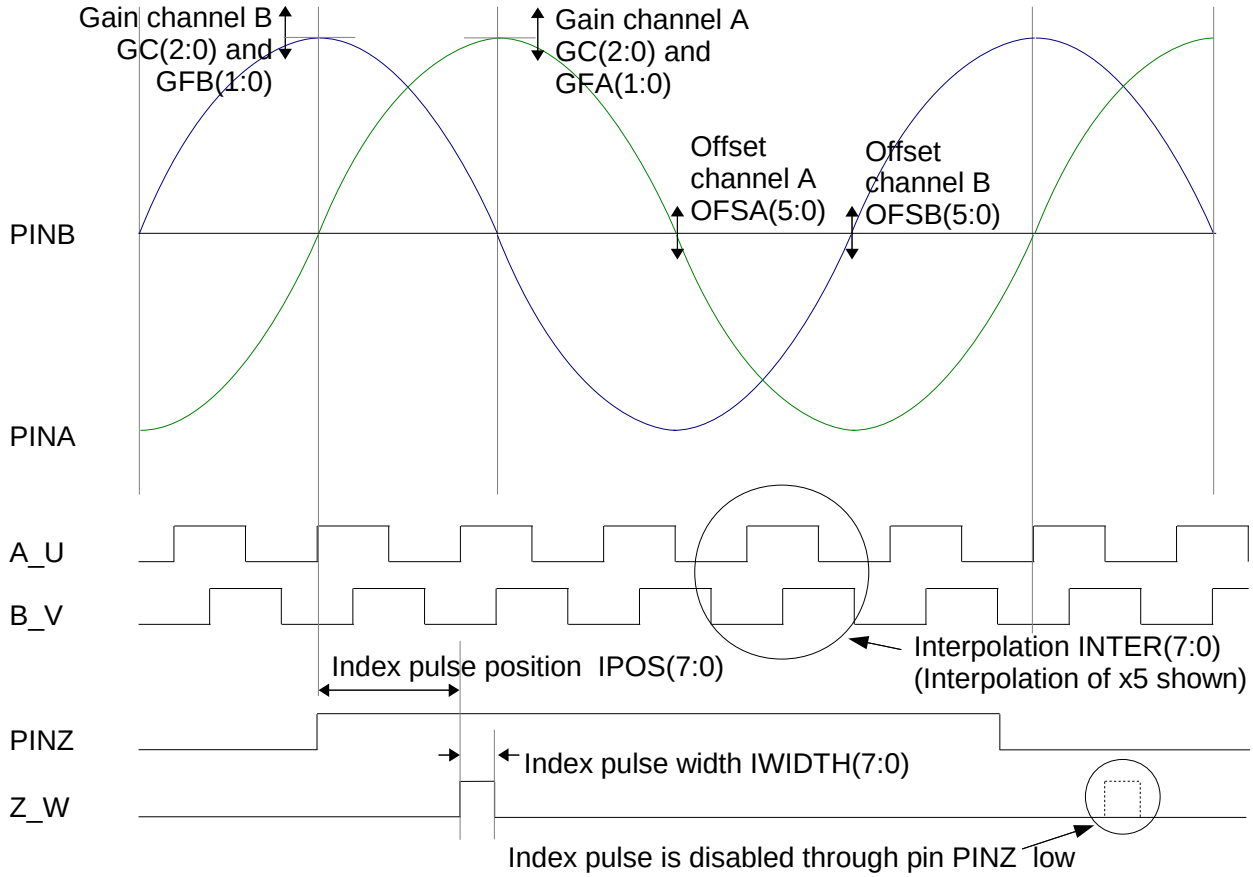



Figure 2: Interpolating function

**Interpolation vs. Resolution**
There is a difference between interpolation factor and resolution. Resolution (interpolation rate) is determined by the sum of edges at the incremental outputs (AB quadrature output) within one input signal period .

Dividing the resolution by the existing edges of the SINE and COSINE signals ( = 4 ) equals to the interpolation factor. The interpolation factor equals to the the resolution divided by 4.

Example:
An interpolation factor of x8 brings a resolution of 32 (edges). To operate with a interpolation factor of 8 configure INTER(7:0) to 32.

## INPUT STAGE

A programmable gain amplifier (PGA) with output referred offset adjustment is used as input stage, shown in Figure 3. The coarse gain is common for both channel A and B and is programmed through register GC(2:0). Table 5 shows the required gain setting for a given input signal amplitude (peak to peak, differential). Fine tuning gain is applied individually to channel A and B by programming registers GFA(1:0) and GFB(1:0) respectively.

| **GC(2:0)** | Addr. 0x07; bit 2:0 | R/W |
|---|---|---|
| Code | Function, *defaults to eeprom setting* | |
| 000 | 1.5 V - 800 mV | |
| 001 | 800 mV - 400 mV | |
| 010 | 400 mV - 200 mV | |
| 011 | 200 mV - 100 mV | |
| 100 | 100 mV - 50 mV | |
| 101 | 50 mV - 25 mV | |
| 110 | 25 mV - 10 mV | |
| 111 | not defined | |

Table 5: Coarse gain control of channel A/B

| **GFA(1:0)** | Addr. 0x07; bit 4:3 | R/W |
|---|---|---|
| **GFB(1:0)** | Addr. 0x07; bit 6:5 | R/W |
| Code | Function, *defaults to eeprom setting* | |
| 00 | 0 dB | |
| 01 | 0.7 dB | |
| 10 | 1.4 dB | |
| 11 | 2.1 dB | |

Table 6: Fine gain control of channel A/B

Offset adjustment is provided at the output of the input amplifier. It is individually programmed through register OFSA(5:0) and OFSB(5:0). Adjustment is made in steps of 13 mV and the corresponding register values are sign magnitude encoded. Input referred offset becomes gain dependent and is defined as follows:

$$OFSA_{\text{input\_referred}} = \frac{13\,mV * OFSA(5:0)}{GC(2:0)}$$

| **OFSA(5:0)** | Addr. 0x08; bit 5:0 | R/W |
|---|---|---|
| **OFSB(5:0)** | Addr. 0x09; bit 5:0 | R/W |
| Code | Function, *defaults to eeprom setting* | |
| 111111 | maximum negative adjust: -403 mV | |
| 111110 | -390 mV | |
| 100001 | -13 mV | |
| 100000 | no correction | |
| 000000 | no correction | |
| 000001 | 13 mV | |
| 011110 | 390 mV | |
| 011111 | maximum positive adjust: 403 mV | |

Table 7: Offset control of channel A/B

Consider Table 8 regarding the relationship between input signal peak-peak differential amplitude, amplifier gain setting and resulting offset correction range.

| Input amplifier gain and offset | | | |
|---|---|---|---|
| Input signal range | Register GC(2:0) | Input referred offset step size | Input referred offset range |
| 800 mV - 1.5 V | 0 | 26 mV | ±806 mV |
| 400 mV - 800 mV | 1 | 13 mV | ±403 mV |
| 200 mV - 400 mV | 2 | 6.5 mV | ±202 mV |
| 100 mV - 200 mV | 3 | 3.25 mV | ±101 mV |
| 50 mV - 100 mV | 4 | 1.63 mV | ±50 mV |
| 25 mV - 50 mV | 5 | 0.81 mV | ±25 mV |
| 10 mV - 25 mV | 6 | 0.41 mV | ±12.6 mV |

Table 8: Input amplifier gain and offset

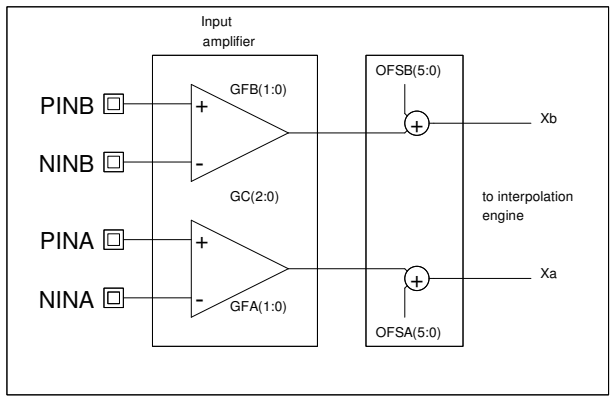



Figure 3: Input stage

## OUTPUT MODES

The iC-TW2 provides four different output modes, which are configured by programming bits MODE(1:0) of register 0x01. Modes 0, 1 and 2 are incremental modes whereas mode 3 is a 3-phase commutation output for brushless DC motors. Consider Figure 4 for a comparison of the 3 incremental output modes.

| **MODE(1:0)** | Addr. 0x01; bit 1:0 | R/W |
|---|---|---|
| Code | Function, *defaults to eeprom setting* | |
| 00 | AB quadrature mode 0 | |
| 01 | up / dn mode 1 | |
| 10 | inc / dir mode 2 | |
| 11 | 3 phase commutation mode 3 | |

Table 9: Output mode selection

In increment / direction mode the count direction can be inverted via control bit DIR of register 0x01.

| **DIR** | Addr. 0x01; bit 2 | R/W |
|---|---|---|
| Code | Function, *defaults to eeprom setting* | |
| 0 | Normal count direction | |
| 1 | Inverted count direction | |

Table 10: Count direction selection

| **INTER (7:0)** | Adr 0x02, Bit 7:0 R/W | | |
|---|---|---|---|
| Code | STEP Angle Steps Per Period | IPF Interpolation Factor | fin()max Maximum Permissible Input Frequency * |
| 0x00 | 256 | 64 | 115 kHz ** |
| 0x01 | 1 | 0.25 | 460 kHz |
| 0x02 | 2 | 0.5 | 460 kHz |
| 0x03 | 3 | 0.75 | 460 kHz |
| 0x04 | 4 | 1 | 460 kHz |
| 0x05 | 5 | 1.25 | 460 kHz |
| ... | ... | ... | 460 kHz |
| 0x3C | 60 | 15 | 460 kHz |
| 0x3D | 61 | 15.25 | 460 kHz |
| 0x3E | 62 | 15.5 | 460 kHz |
| 0x3F | 63 | 15.75 | 460 kHz |
| 0x40 | 64 | 16 | 460 kHz |
| 0x41 | 65 | 16.25 | 230 kHz |
| 0x42 | 66 | 16.5 | 230 kHz |
| 0x43 | 67 | 16.75 | 230 kHz |
| 0x44 | 68 | 17 | 230 kHz |
| 0x45 | 69 | 17.25 | 230 kHz |
| ... | ... | ... | 230 kHz |
| 0x7C | 124 | 31 | 230 kHz |
| 0x7D | 125 | 31.25 | 230 kHz |
| 0x7E | 126 | 31.5 | 230 kHz |
| 0x7F | 127 | 31.75 | 230 kHz |
| 0x80 | 128 | 32 | 230 kHz |
| 0x81 | 129 | 32.25 | 115 kHz |
| 0x82 | 130 | 32.5 | 115 kHz |
| 0x83 | 131 | 32.75 | 115 kHz |
| 0x84 | 132 | 33 | 115 kHz |
| 0x85 | 133 | 33.25 | 115 kHz |
| ... | ... | ... | 115 kHz |
| 0xFA | 250 | 62.5 | 115 kHz |
| 0xFB | 251 | 62.75 | 115 kHz |
| 0xFC | 252 | 63 | 115 kHz |
| 0xFD | 253 | 63.25 | 115 kHz |
| 0xFE | 254 | 63.5 | 115 kHz |
| 0xFF | 255 | 63.75 | 115 kHz |

Table 11: Converter resolution

* Depending on configuration FREQ = 0, CLKDIV = 0 and $f_{cal}$ = 920 kHz.

** Maximum permissible input frequency for commutation operation (mode = 3) .

### AB Quadrature And Up/Down and Incr/Dir Modes

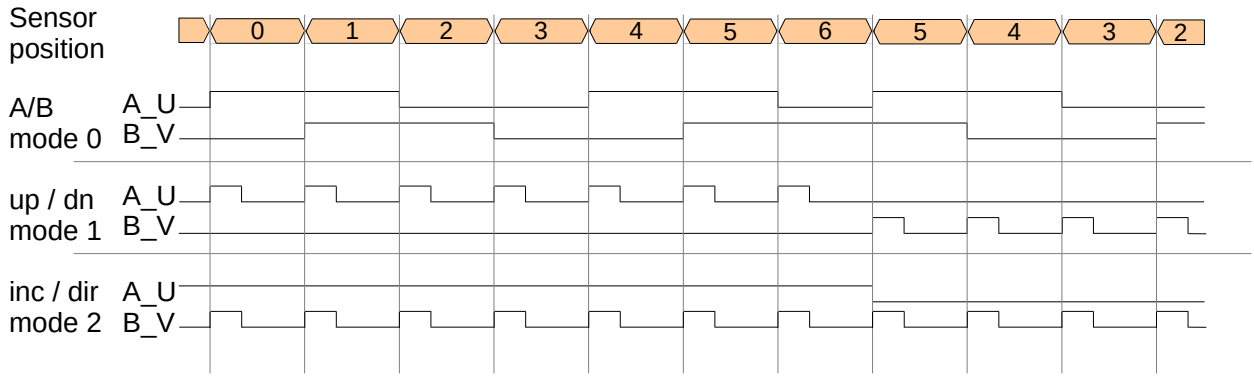



Figure 4: Incremental output modes (mode 0, 1, 2)

| **IPOS(7:0)** | Addr. 0x03; bit 7:0 | R/W |
|---|---|---|
| Code | Function, *defaults to eeprom setting* | |
| 0 | No offset | |
| 1 | 1 increment offset | |
| 2 | 2 increments offset | |
| . . . | . . . | |
| | Index pulse will shifted by IWIDTH(7:0) increments. Programmed value is within the range of 0 to INTER(7:0) - 1. | |
| . . . | . . . | |
| 255 | 255 increments offset | |
| **Note:** | A fixed phase relation to A/B is guaranteed only with STARTUP(1:0) = 0b10 ('ABSOLUTE") or STARTUP(1:0) = 0b11 ('BURST"). | |

Table 12: Index pulse position

| **IWIDTH(7:0)** | Addr. 0x04; bit 7:0 | R/W |
|---|---|---|
| Code | Function, *defaults to eeprom setting* | |
| 0 | disable pulse generation | |
| 1 | 1 increment width | |
| 2 | 2 increments width | |
| . . . | . . . | |
| Any other value n | Index pulse will extend over IWIDTH(7:0) increments. Programmed value is within the range of 0 to INTER(7:0) - 1. | |
| . . . | . . . | |
| 255 | 255 increments width | |

Table 13: Index pulse width selection

### 3 Phase Commutation Mode

The 3 phase commutation output (mode 3) is shown in Figure 5. It is important that register INTER(7:0) is programmed with the value 0x00 in order for the commutation mode to work. The mode = 3 requires an internal interpolation INTER(7:0) of 256. Register IPOS(7:0) is used to accurately position the commutation. IWIDTH(7:4) and IWIDTH(3:0) is subsequently used to fine tune V and W in respect to U. All used offsets within the commutation mode (mode 3) as are IPOS(7:0), IWIDTH(3:0) and IWIDTH(7:4) operate in this step width of 1.4° . There is no other pole count commutation possible to configure as the described 3 phase commutation.

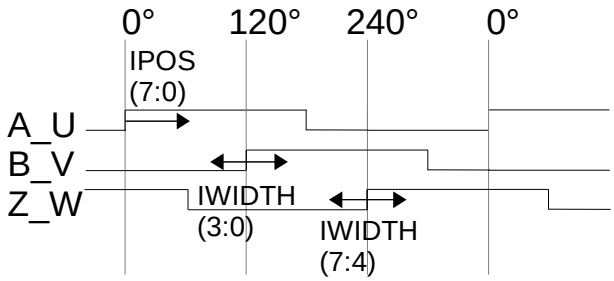



Figure 5: 3-Phase commutation output (mode 3)

| **IPOS(7:0)** | Addr. 0x03; bit 7:0 | R/W |
|---|---|---|
| Code | Function, *defaults to eeprom setting* | |
| 0 | 0° | |
| 1 | 1.40° | |
| 2 | 2.81° | |
| . . . | . . . | |
| | Programmed value is within the range of 0 to INTER(7:0) - 1. | |
| . . . | . . . | |
| 255 | 358,59° | |

Table 14: UVW commutation signal position offset

| **IWIDTH(3:0)** | Addr. 0x04; bit 3:0 | R/W |
|---|---|---|
| Code | V output offset, *defaults to eeprom setting* | |
| 0111 | 9.84° | |
| . . . | . . . | |
| 0010 | 2.81° | |
| 0001 | 1.40° | |
| 0000 | 0° | |
| 1111 | -1.40° | |
| 1110 | -2.81° | |
| . . . | . . . | |
| 1111 | 11.25° | |

Table 15: V commutation signal position offset

| **IWIDTH(7:4)** | Addr. 0x04; bit 7:4 | R/W |
|---|---|---|
| Code | W output offset, *defaults to eeprom setting* | |
| 0111 | 9.84° | |
| . . . | . . . | |
| 0010 | 2.81° | |
| 0001 | 1.40° | |
| 0000 | 0° | |
| 1111 | -1.40° | |
| 1110 | -2.81° | |
| . . . | . . . | |
| 1111 | 11.25° | |

Table 16: W commutation signal position offset

## INDEX GATING

The iC-TW2 can interface to a wide range of index gating sources. Most commonly used are the digital hall sensor and the MR sensor bridge. The digital Hall sensor provides a large swing input signal to the iC-TW2. Depending on the polarity of the Hall it is either connected to pin NINZ or PINZ. Most Hall sensors use an open drain stage pulling the output low in the presence of a magnetic field. The unused terminal PINZ or NINZ should be biased to an adequate mid voltage level to guarantee good noise margin. The iC-TW2 provides a constant 1.21 V at pin VC that can be used for this purpose (refer to Figure 6).

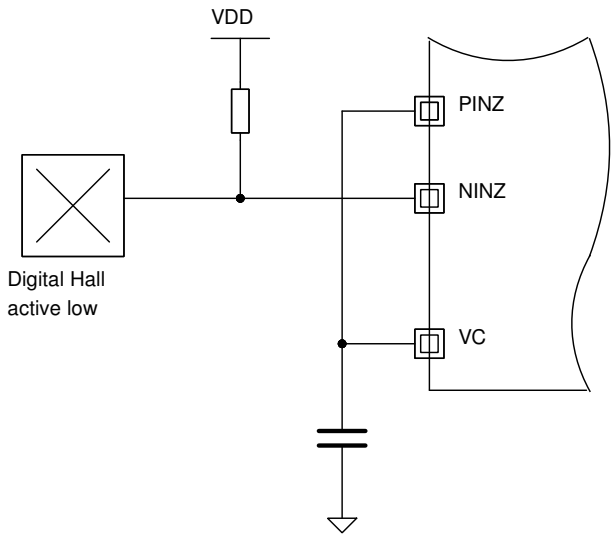



Figure 6: Digital Hall sensor index configuration

An MR sensor differential bridge can also be used to gate the index. Typically, the MR sensor provides a small signal amplitude. In addition, residual side lobes are present that can trigger double indexing. The iC-TW2 provides offset control capability to fine tune the threshold voltage of the index comparator. This greatly simplifies end product calibration as variation in sensor offset can be compensated for. Figure 8 shows a correctly set threshold when using an MR gating sensor. The side lobes are below the threshold line and no parasitic triggering occurs.

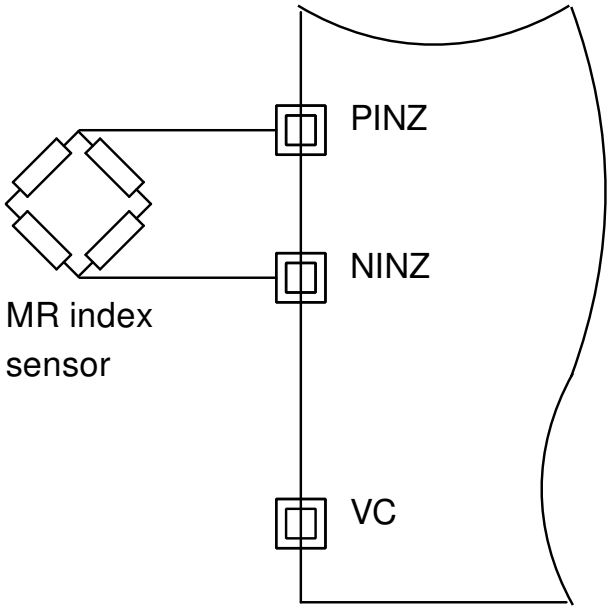



Figure 7: MR sensor index configuration

Index gating should be calibrated at SIN/COS input frequencies below 5 kHz to minimize the effect of latency. Timings shown in Table 17 are valid for input frequencies below 5 kHz and $f_{system}$ of 25 MHz. Once the timings are satisfied according to Table 17, correct operation is guaranteed up to the maximum input frequency as specified in Table 22 on page 19.

| Parameter | Description | Condition * | min |
|---|---|---|---|
| $t_{setup}$ | Index window setup time before rising edge of Z_W | no filter<br>8 average<br>16 average | 0.4 µs<br>0.5 µs<br>0.7 µs |
| $t_{hold}$ | Index window hold time after falling edge of Z_W | no filter<br>8 average<br>16 average | 0.4 µs<br>0.5 µs<br>0.7 µs |
| * Filter register FILTER(1:0)<br>$f_{system}$ = 25 MHz, all timings scale with $f_{system}$<br>Refer to Table 22 for more information | | | |

Table 17: Index gating and timing

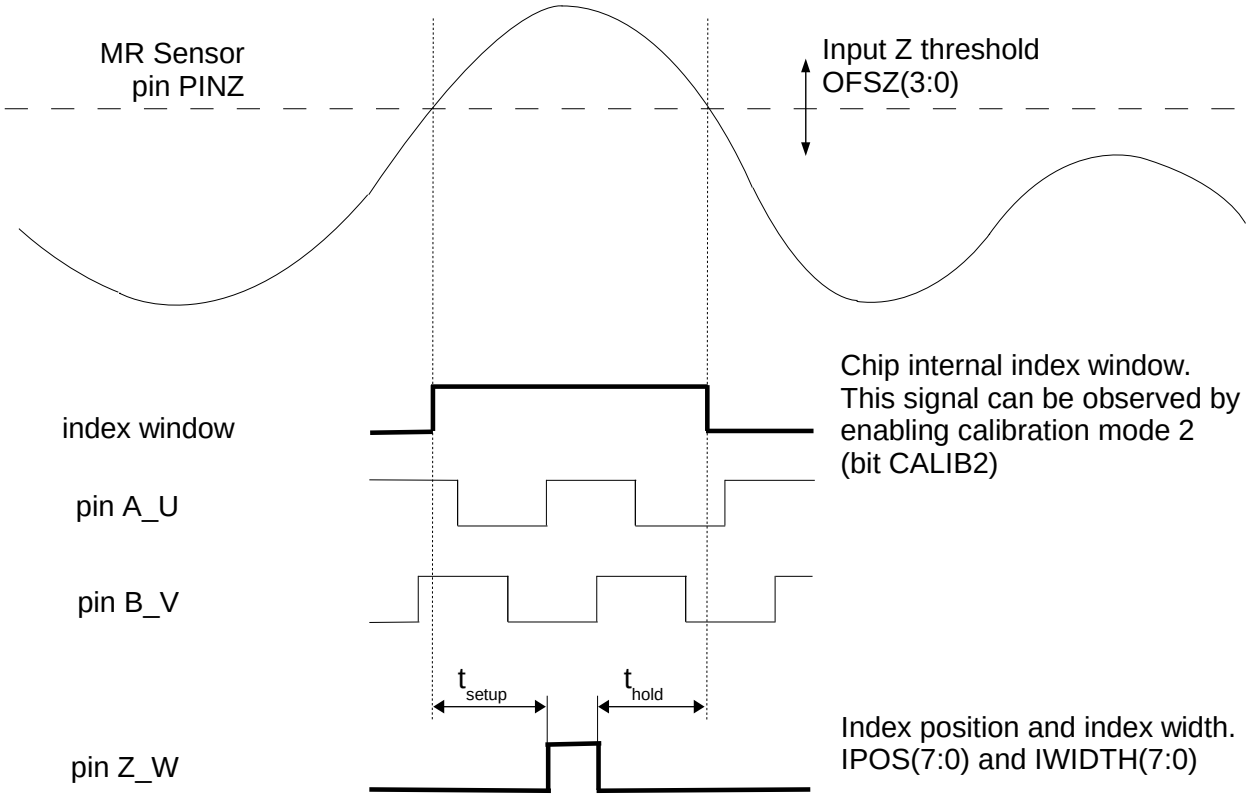



Figure 8: Index gating

## CALIBRATION

In order to facilitate system gain and offset calibration, two calibration modes can be enabled by either setting bit CALIB1 of register 0x01 or CALIB2 of register 0x0C.

| **CALIB2** Addr. 0x0C; bit 0 | | R/W |
|---|---|---|
| **CALIB1** Addr. 0x01; bit 5 | | R/W |
| CALIB2;1 | Function, *defaults to eeprom setting* | |
| 00 | Normal operation, no calibration | |
| 01 | A/B gain and index calbration | |
| 10 | Oscillator and index window calibration | |
| 11 | Not permitted | |

Table 18: Calibration mode

### A/B gain and offset calibration

In calibration mode 1 the SIN/COS input is directly passed through two zero-cross comparators to output pin A and B respectively. In addition, the sum of the input signals

$$\frac{SIN + COS}{\sqrt{2}}$$

is also fed through a comparator and driven on pin Z.

The actual calibration process must be carried out in several steps.

1. Select proper coarse gain by programming register GC(2:0). Set GFA(1:0) and GFB(1:0) to 0.

2. Adjust offset register OFSA(5:0) and OFSB(5:0) until output A and B are 50% duty cycle.

3. Adjust fine gain register GFA(1:0) and GFB(1:0) until output Z is equidistant between output A and B.

4. Repeat step 1 and 2 until no more improvement can be achieved.

### Oscillator and index window calibration

When calibration mode 2 is enabled, the output of the index comparator is driven on pin B_V. In conjunction with the actual index output on pin Z_W, the gating window can be centered around the output pulse. Fine offset adjustment applied to the input of the index comparator is possible through OFSZ(3:0) which is sign magnitude encoded. This is beneficial when using small amplitude index sources such as an MR sensor. Simultaneously, the oscillator frequency $f_{osc}/32$ can be observed on pin A_U. Register CLOCK(4:0) is used to tune the oscillator to its desired frequency.

| **OFSZ(3:0)** Addr. 0x0B; bit 7:4 | | R/W |
|---|---|---|
| Code | Function, *defaults to eeprom setting* | |
| 1111 | maximum negative adjust, -10.5 mV | |
| 1110 | -9 mV | |
| 1001 | -1.5 mV | |
| ... | ... | |
| 1000 | no correction | |
| 0000 | no correction | |
| 0001 | 1.5 mV | |
| ... | ... | |
| 0110 | 9 mV | |
| 0111 | 10.5 mV | |
| 1 | calibration mode 2 activated | |

Table 19: Index comparator offset control

| **CLOCK(4:0)** Addr. 0x0A; bit 4:0 | | R/W |
|---|---|---|
| Code | Function, *defaults to eeprom setting* | |
| 00000 | Slowest clock | |
| ... | ... | |
| 11111 | fastest clock | |

Table 20: Oscillator tuning

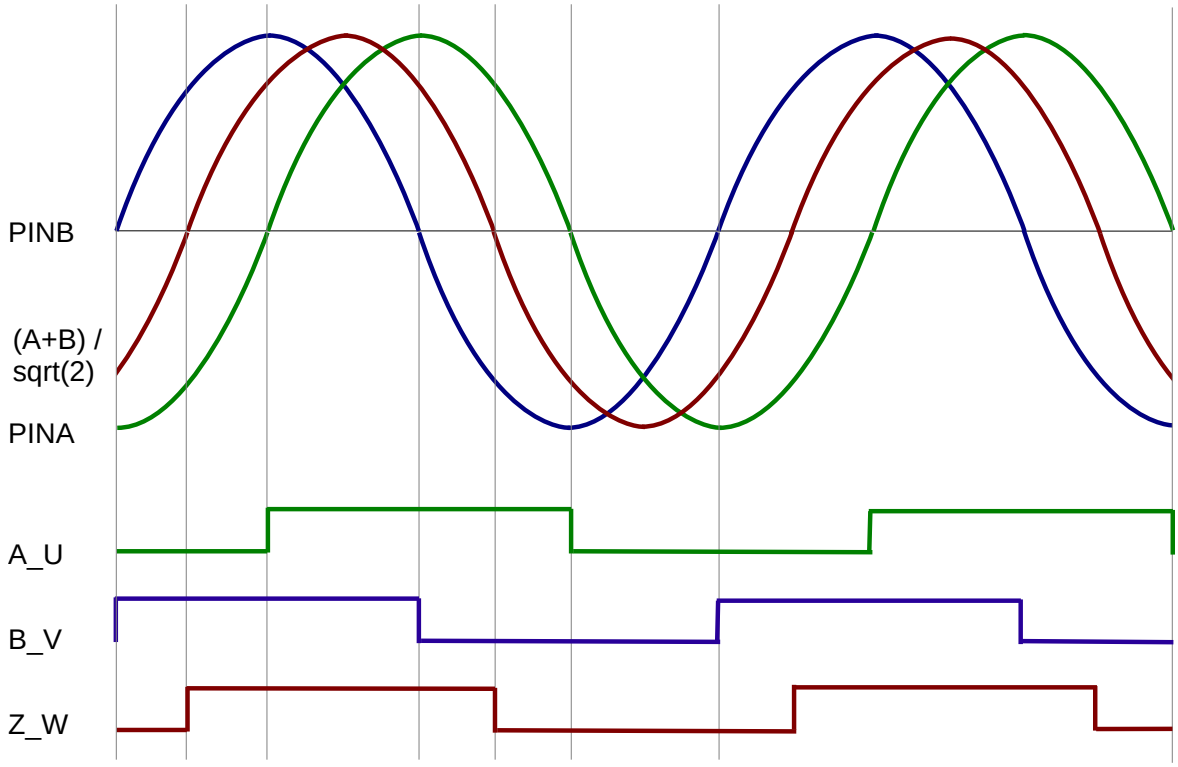



Figure 9: Calibration of A/B gain and offset

## CONFIGURATION DEPENDENCIES

The following paragraph describes dependencies between several chip configuration settings and system performance. It is vital to understand the implication of system parameters to be able to tune the iC-TW2 for full performance. It is especially important to correctly program register FREQ(6:0), since this directly affects accuracy and maximum allowed input frequency.

### Selecting configuration parameters

Follow the outlined procedure below to select the proper configuration. Refer to Table 22 for reference.

1. Determine the maximum input frequency $f_{input}$ as required by the application.

2. Calculate $f_{core}$ based on $f_{input}$ and interpolation rate INTER(7:0).

3. Select $f_{system}$ based on the accuracy requirement. See Table 21. Accuracy is a function of interpolation and frequency (registers INTER(7:0) and FREQ(6:0)). Always use the highest accuracy possible to still satisfy $f_{input}$.

4. Determine $f_{osc}$. Selecting the slowest $f_{osc}$ possible lowers power consumption and improves jitter performance.

### Clock tuning

1. Observe $f_{osc}/32$ on pin A_U during calibration mode 2.

2. Use CLOCK(4:0) to tune the oscillator to the desired $f_{cal}$ frequency. ($f_{pinA} = f_{osc}/32$)

3. Be aware that the oscillator can have as much as 20 % frequency variation over the operating temperature range (-40 °C to 125 °C). The oscillator runs slower at higher temperatures. To guarantee performance at 125 °C it is necessary to tune the oscillator to typ. 12 % higher frequency at room temperature of 25 °C.

| INTER(7:0) | FREQ(6:0) | Accuracy Mode | Theoretical Absolute Accuracy |
|---|---|---|---|
| 129 to 256; 0 | 0 to 127 | High accuracy | ±2.8° |
| 65 to 128 | 0 | Medium accuracy | ±5.6° |
| | 1 to 127 | High accuracy | ±2.8 ° |
| 1 to 64 | 0 | Low accuracy | ±11.2° |
| | 1 | Medium accuracy | ±5.6° |
| | 2 to 127 | High accuracy | ±2.8° |

Table 21: Accuracy modes

| Description | Parameter / Condition | Requirement or relationship | Control bit |
|---|---|---|---|
| Oscillator frequency | $f_{osc}$ [Hz] | <30 MHz, when $V_{DD}$ = 5 V<br><25 MHz, when $V_{DD}$ = 3.3 V | CLOCK(4:0) |
| System Clock | $f_{system}$ [Hz] | $f_{system} = f_{osc}$, if CLKDIV = 0<br>$f_{system} = f_{osc}/2$, if CLKDIV = 1 | CLKDIV |
| Core Clock | $f_{core}$ [Hz] | $f_{core} = f_{system}$ / (1 + FREQ(6:0)) | FREQ(6:0) |
| Max front-end input frequency | $f_{front}$ [Hz] | $f_{front} = f_{system}$ / 256, if High Accuracy<br>$f_{front} = f_{system}$ / 128, if Medium Accuracy<br>$f_{front} = f_{system}$ / 64, if Low Accuracy | FREQ(6:0)<br>INTER(7:0) |
| Max back-end frequency | $f_{back}$ [Hz] | $f_{back} = f_{core}$ / INTER(7:0) | INTER(7:0) |
| Max iC-TW2 input frequency | $f_{input}$ [Hz] | $f_{input} = \min(f_{front}, f_{back})$ | |
| Min A/B edge separation | $t_{edge}$ | $t_{edge} = 1 / f_{core}$ | |
| A/B edge granularity | $t_{gran}$ | $t_{gran} = 1 / f_{system}$ | |
| Hysteresis | | ±(HYST(1:0) x 1.4 °), if High Accuracy<br>±(HYST(1:0) x 2.8 °) if Medium or Low Accuracy | HYST(1:0) |
| SIN/COS to A/B output latency | $t_{latency}$ [µs] | 10 / $f_{system}$ [MHz] + 0.2, if no filter<br>18 / $f_{system}$ [MHz] + 0.2, if 8 sample average<br>26 / $f_{system}$ [MHz] + 0.2, if 16 sample average | FILTER(1:0) |

Table 22: Configuration dependencies

| **FREQ(6:0)** | Addr. 0x05; bit 6:0 | R/W |
|---|---|---|
| Code | Function, *defaults to eeprom setting* | |
| 0x00 | $f_{core} = f_{system}$ | |
| ... | $f_{core} = \frac{f_{system}}{1 + FREQ(6:0)}$ | |
| 0x7F | $f_{core} = \frac{f_{system}}{128}$ | |

Table 23: Maximum input frequency selection

Interpolation setting (register 0x02) in conjunction with the frequency divider (register 0x05) defines the iC-TW2's accuracy mode. Table 21 explains the correlation. Based on the selected accuracy mode other system parameters are defined as shown in Table 22.

It is recommended to use the divider at all times when support for high input frequencies is not required.

| **CLKDIV** | Addr. 0x0B; bit 1 | R/W |
|---|---|---|
| Code | Function, *defaults to eeprom setting* | |
| 0 | fsystem = $f_{osc}$ | |
| 1 | fsystem = $\frac{f_{osc}}{2}$ | |

Table 24: Master clock divider

Hysteresis is dependent upon chosen accuracy. The Table below is valid for *high accuracy* operation.

| **HYST(1:0)** | Addr. 0x06; bit 1:0 | R/W |
|---|---|---|
| Code | Function, *defaults to eeprom setting* | |
| 00 | no hysteresis | |
| 01 | ±1.4 ° | |
| 10 | ±2.81 ° | |
| 11 | ±5.63 ° | |

Table 25: Master clock divider

An averaging filter can be enabled to remove loop instability noise. It is recommended to enable the filter in almost all cases. Enabling the filter increases SIN/COS input to A/B output latency. See Table 22 on page 19 for details.

| **FILTER(1:0)** | Addr. 0x06; bit 3:2 | R/W |
|---|---|---|
| Code | Function, *defaults to eeprom setting* | |
| 00 | filter disabled | |
| 01 | Average of 8 samples | |
| 10 | Average of 16 samples | |
| 11 | undefined | |

Table 26: Datapath filter control

## DEVICE IDENTIFICATION

| **IDA(3:0)** | Addr. 0x00; bit 7:4 | R/W |
|---|---|---|
| Code | Function, Major device identification | |
| | Mask Programmed Value Identifies Major Revision | |

Table 27: Major device revision

| **IDB(3:0)** | Addr. 0x00; bit 3:0 | R/W |
|---|---|---|
| Code | Function, Minor device identification | |
| | Mask Programmed Value Identifies Minor Revision | |

Table 28: Minor device revision

## START UP

### Power-On-Reset

The iC-TW2 contains a built-in Power-On-Reset (POR) circuitry. The POR keeps the iC-TW2 in reset as long as the applied power supply voltage does not allow reliable operation. Once the power supply ramps up above 1.8 V, the POR releases the reset and the iC-TW2 starts the configuration cycle. 20 ms after the device goes out of reset, normal operation begins.

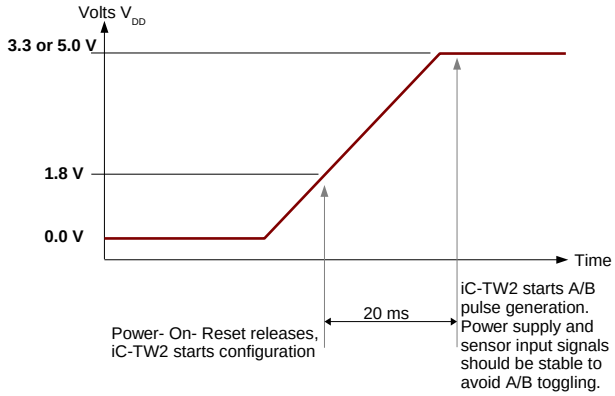



Figure 10: Power supply ramp-up

To avoid A/B output toggling it is important that the power supply and the input signals are stable as soon as normal operation begins. In applications with a slowly rising power supply, it might be necessary to connect an external RC reset to pin NRST to prolong the reset. In applications where startup A/B toggling is acceptable, no precaution must be taken as the iC-TW2 will properly power up on an indefinitely slow supply rise time.

The iC-TW2 startup behaviour is controlled by programming the two control bits STARTUP(1:0) in register 0x01. Three possible startup configurations are allowed, shown in Figure 11. The default behaviour must be specified by the eeprom.

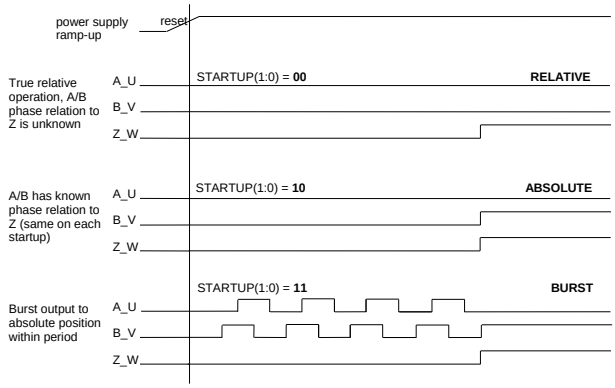



Figure 11: Startup behaviour

| **STARTUP(1:0)** | Addr. 0x01; bit 4:3 | R/W |
|---|---|---|
| Code | Function | |
| 00 | **RELATIVE**<br>A/B output signals are kept low during startup. This resembles true relative operation since there is no relationship between A/B levels and sensor position (and therefore Z output) on startup. | |
| 01 | Reserved | |
| 10 | **ABSOLUTE**<br>A/B output signals are phase-related to Z output. A/B output levels are defined by the absolute sensor position within a period. The register *IPOS* can be used to program the desired A/B to Z phase relationship. | |
| 11 | **BURST**<br>The absolute sensor position within the period is output by an A/B burst. | |

Table 29: Startup sequence selection

### Reset

A control bit RESET is provided to block any burst A/B pulses during chip reconfiguration by a microcontroller. While RESET is set A/B/Z output generation is stopped. Access to the interface and register bank is not affected.

| **RESET** | Addr. 0x01; bit 6 | R/W |
|---|---|---|
| Code | Function | |
| 0 | normal operation *default* | |
| 1 | initiate reset | |

Table 30: Restart interpolation engine

## 1W- / 2W-INTERFACE AND EEPROM ACCESS

**Memory map**
Figure 12 depicts the iC-TW2 memory map and interface diagram. A 2-wire read/write interface and a 1-wire write-only interface allow access to the register bank and the EEPROM bank. The register bank is 8 bits wide and it is used to control all chip functionality. Refer to section "Register Map" on page 8 for an overview of all registers.

The EEPROM bank on the other hand is 32 bits wide. Address 0x05, 0x06 and 0x07 (3 * 4 bytes = 12 bytes) can be used to store user data such as product serial numbers, calibration and manufacturing information.

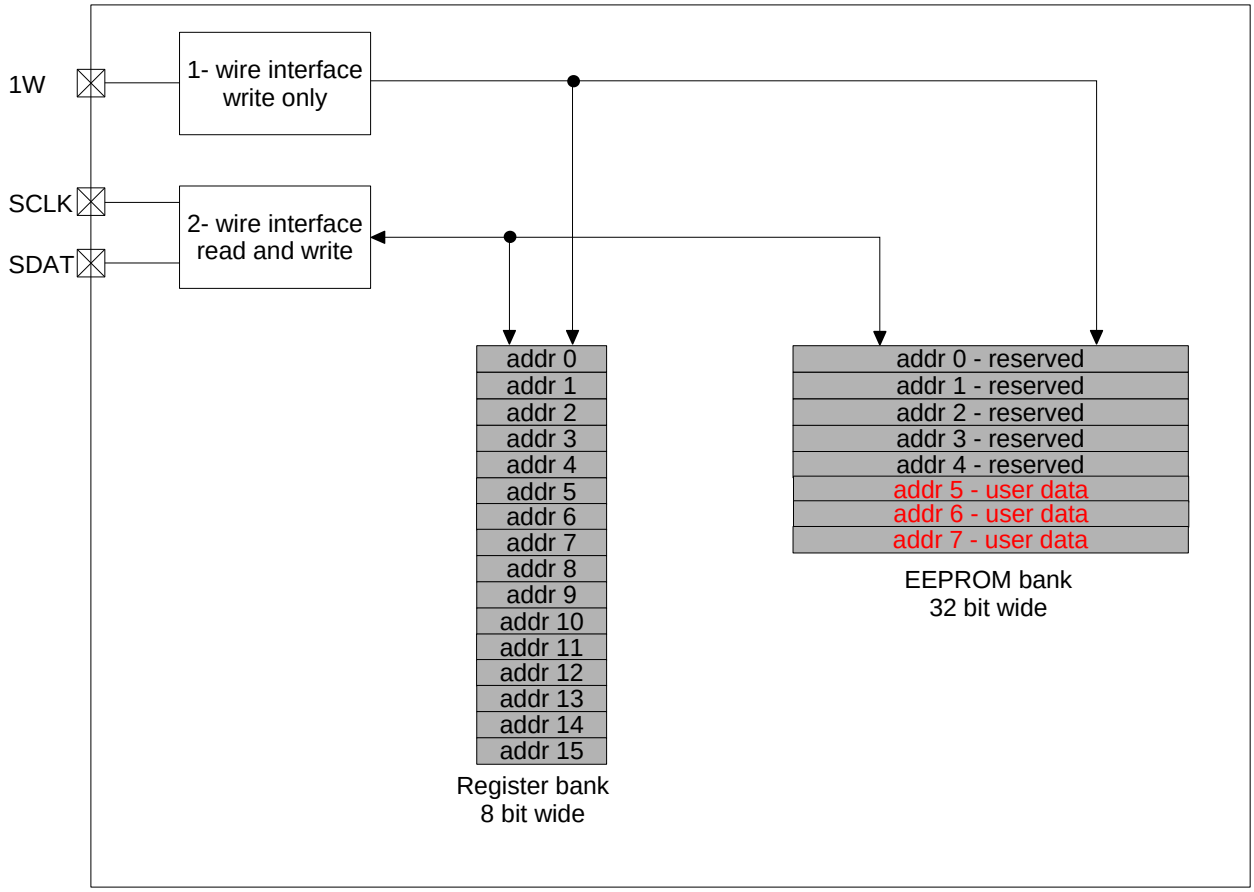



Figure 12: Memory map

**2W-Interface**
The first control interface is a standard 2-wire serial interface. It uses an external clock and bidirectional data line. It allows read and write access to all internal registers as well as access to the user EEPROM. The interface consists of two pins, a dedicated input SCLK, the shifting clock and SDAT for bidirectional serial data.

The interface handles four types of access requests:

1. Write to control register
2. Read from control register
3. Write to EEPROM register (including block access and erase)
4. Read from EEPROM register

Control register access is shown in Figure 13 (write) and Figure 14 (read) respectively. If SDAT is **00** after the start bit a write access is requested. The data word d(7:0) will be written into register a(4:0). Please note that a(4) is always 0 since the iC-TW2 only has 16 addressable registers.

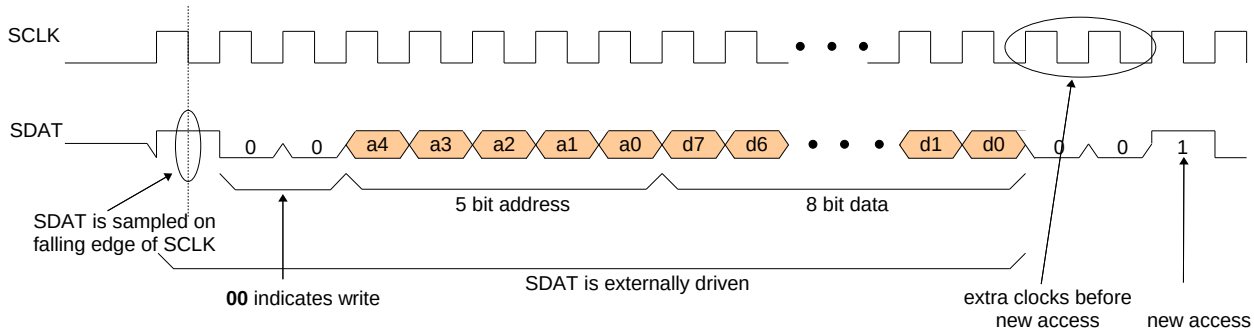



Figure 13: Register bank write access on 2W-Interface

On a register read access the register content is shifted out on SDAT. A read access is indicated by SDAT 10 after the start bit. There is an idle clock required between the last address bit a(0) and the first data bit d(7) returned on SDAT. This clock cycle is used to avoid any bus contention while turning around the bus driver.

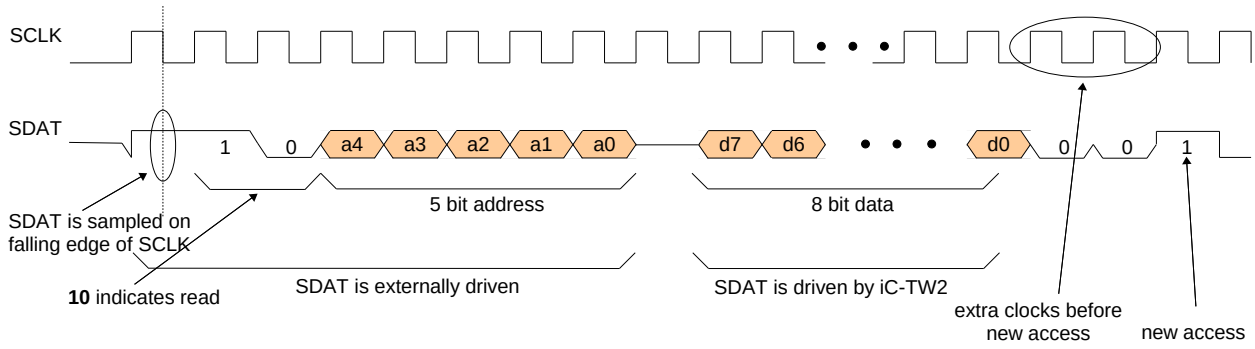



Figure 14: Register bank read access on 2-wire interface

Write access to the EEPROM follows the procedure depicted in Figure 15. A start bit is followed by four command bits c-1-e-b. The encoding of the command bits is shown in Table 31. The most useful command is **0100** which performs an erase followed by a write therefore allowing the user to write a new value to the EEPROM with only one interface access.

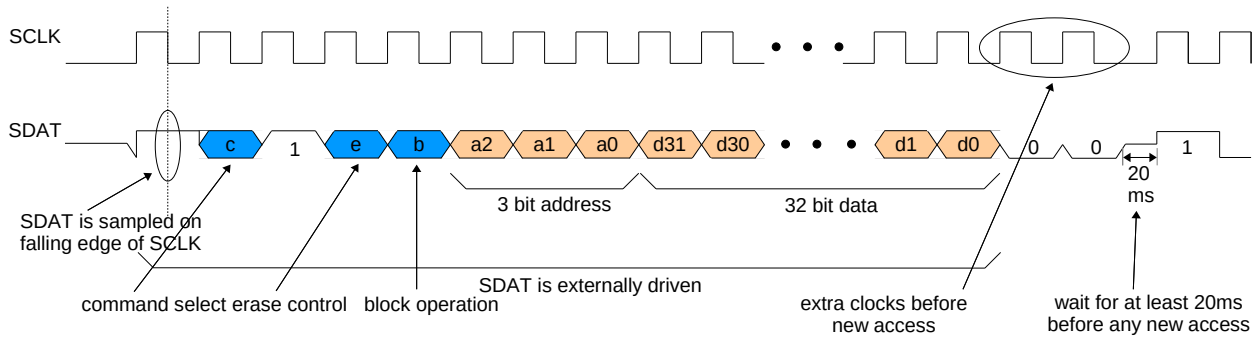



Figure 15: EEPROM write access on 2-wire interface

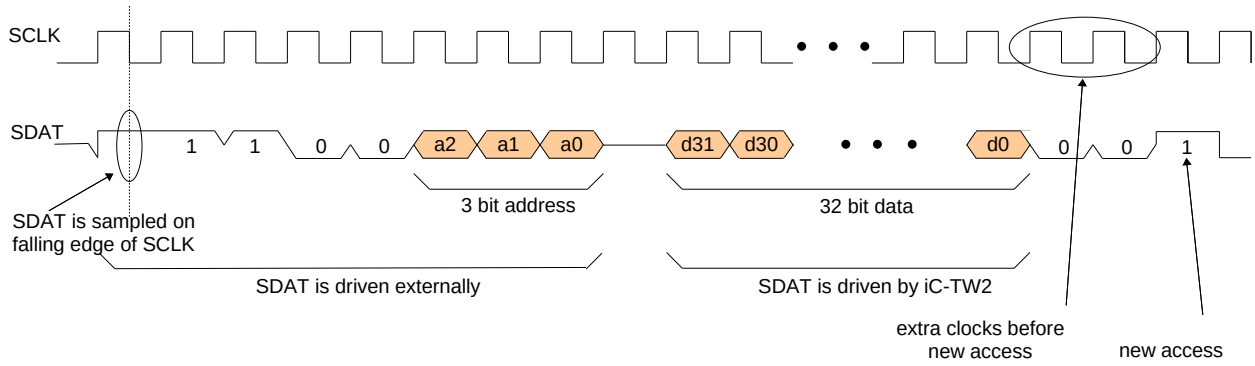



Figure 16: EEPROM read access on 2-wire interface

The 3 bit address a(2:0) selects the EEPROM register to write to (Figure 12). Each EEPROM register is 32 bits wide, therefore 32 data bits d(31:0) are sent across the interface. At least 20 ms delay is required after every transaction before any new access can start.

EEPROM read access is shown in Figure 16. The start bit is followed with the 4 bit read command **1100** and the 3 bit address a(2:0). An idle clock cycle is used to avoid any contention on SDAT while reversing data flow direction. Finally d(31:0) is shifted out on SDAT. EEPROM read access is slow. Please take notice of the timings in Table 32.

At least one extra clock with SDAT low is required after every transaction on the 2-wire interface before a new access is started. The interface will not work correctly if this clock cycle is omitted.

| **EEPROM Commands** | | | | | |
|---|---|---|---|---|---|
| c | 1 | e | b | Description | Purpose |
| 0 | 1 | 0 | 0 | Erase followed by write | Normal EEPROM programming |
| 0 | 1 | 0 | 1 | Block erase followed by block write | |
| 0 | 1 | 1 | 0 | Block write | Test only |
| 0 | 1 | 1 | 1 | Read. Please refer to Figure 16 for more details | |
| 1 | 1 | 0 | 1 | Reserved. Do not use this command | |
| 1 | 1 | 1 | 0 | Erase | Test only |
| 1 | 1 | 1 | 1 | Block erase | Special production environment |

Table 31: EEPROM Commands

**2W-Interface timing**

The timing of the 2W-Interface is dependent on the type of access performed. Register bank access and EEPROM write access can be performed at full speed. EEPROM read access requires a slow SCLK. Also a 20 ms delay is required after every EEPROM write access before a new transaction of any kind is started (this includes read and write to the register bank).

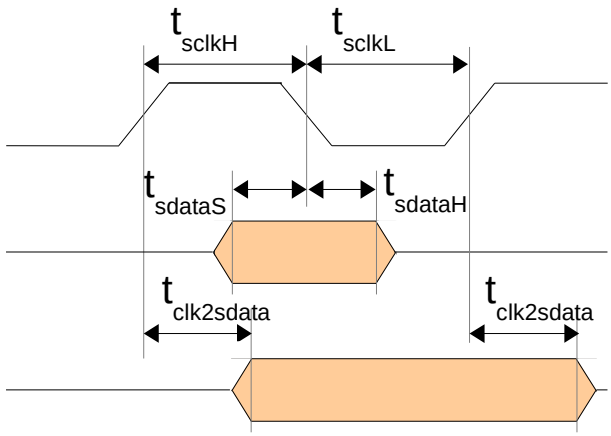



Figure 17: 2W-Interface timing diagram

| **2W-Interface timing** | | | | |
|---|---|---|---|---|
| **Parameter** | **Description** | **Condition** | **min** | **max** |
| $t_{sclkH}$ | SCLK high | EEPROM read access<br>Any other access | 2 µs<br>400 ns | 0 |
| $t_{sclkL}$ | SCLK low | EEPROM read access<br>Any other access | 2 µs<br>400 ns | |
| $t_{sdataS}$ | SDAT setup before falling edge of SCLK | | 100 ns<br>100 ns | |
| $t_{sdataH}$<br>$t_{sdataH}$ | SDAT setup hold after falling edge of SCLK | | 100 ns<br>100 ns | |
| $t_{clk2sdata}$ | SDAT setup hold after falling edge of SCLK | 5 ns | 105 ns | |

Table 32: 2W-Interface timing

### 1W-Interface

The 1W-Interface provides a write-only access port to the register bank. It is intended as a minimal configuration interface to program the internal EEPROM during in-field service or production. An infrared phototransistor can directly connect to the pin to build a cost effective wireless write port. The input bit stream is pulse-width modulated (or duty-cycle modulated) as shown in Figure 18. A zero-bit is encoded as a short low followed by a long high. A one-bit is encoded as a long low followed by a short high. The modulated signal is independent of the receiver or transmitter clock frequency. Since the iC-TW2 uses a free-running oscillator, it is important to implement a robust, frequency-insensitive protocol.

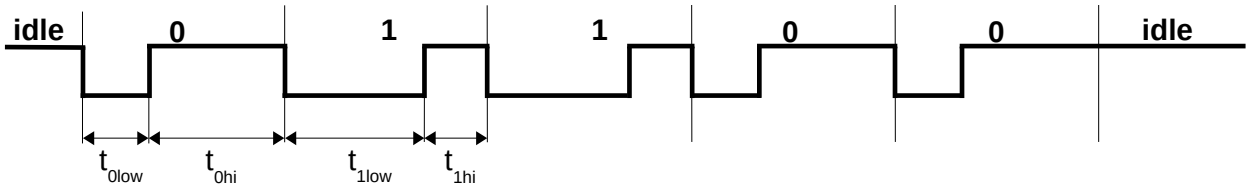



Figure 18: Pulse width modulated bit stream

The interface timing is specified in the following Table.

| Parameter | Description | min | max |
|---|---|---|---|
| $t_{0low}$ | Low time bit 0 | 40 µs | 100 µs |
| $t_{0hi}$ | High time bit 0 | 120 µs | 200 µs |
| $t_{1low}$ | Low time bit 1 | 120 µs | 200 µs |
| $t_{1high}$ | High time bit 1 | 40 µs | 100 µs |

Table 33: 1W-Interface timing

### 1W-Interface write sequence

Figure 19 describes the write sequence to the register bank, which uses the same protocol as the 2W-Interface. On an idle wire, a write sequence is initiated by writing a start bit **(1)** followed by the write command **(00)** followed by the address and register data. At the end of the sequence, a stop-bit **(0)** is required.

1W-Interface write access to the EEPROM bank is shown in Figure 20. The 4 bit EEPROM command after the start bit is decoded in Table 31.

### Writing the register bank to the EEPROM

To permanently store a configuration in the internal EEPROM the following procedure should be followed.

1. The 1W-/2W-Interface is used to fully write the desired configuration into the register bank.

2. A logic one is written to bit EE_WRITE of register 0x0E. This will initiate a write sequence which copies all registers into the internal EEPROM. A complete write takes 100 ms. During this time, no access to the register bank through either the 1W-/2W-Interface is allowed or data corruption might occur.

3. Finally the register content, after a device reset and configuration, should be verified to ensure a successfull EEPROM write sequence.

Writing the registers to the EEPROM using EE_WRITE takes up to 100 msec. During this access to the register bank either through the 1W- or 2W-Interface is prohibited. Any access will corrupt data written to the EEPROM.

| **EE_WRITE** | Addr. 0x0E; bit 6 | W |
|---|---|---|
| Code | Function, bit is automatically reset upon completion of operation | |
| 0 | Normal operation (default) | |
| 1 | Store registers into EEPROM | |

Table 34: EEPROM store command

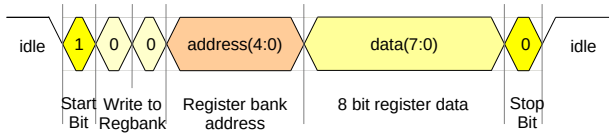



Figure 19: 1W-Interface register bank write sequence

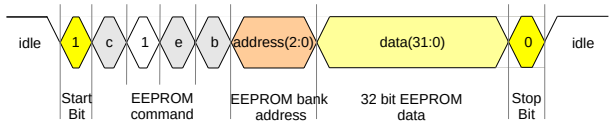



Figure 20: 1W-Interface EEPROM write sequence

## TEST MODES

The iC-TW2 provides various control bits located in different registers to enable or disable certain test modes. The majority of these is only required for extended chip testing capability, others are required for production test.

| **GRANULAR** | Addr. 0x05; bit 7 | R/W |
|---|---|---|
| Code | Function, test mode only | |
| 0 | normal operation | |
| 1 | test mode only | |

Table 35: A/B output edge granularity control

| **VC(1:0)** | Addr. 0x0A; bit 6:5 | R/W |
|---|---|---|
| Code | Function, test mode only | |
| | register must be set to 0 for correct device functionality | |

Table 36: Reference voltage fine tuning

| **CLKMODE** | Addr. 0x0B; bit 0 | R/W |
|---|---|---|
| Code | Function, test mode only | |
| 0 | Select comparator clock *default* | |
| 1 | Select direct oscillator clock | |

Table 37: Clock source select

| **CLKDLY** | Addr. 0x0B; bit 2 | R/W |
|---|---|---|
| Code | Function | |
| 0 | Normal operation | |
| 1 | Add clock delay | |

Table 38: Clock distribution delay line selection

Enabling the position monitor will allow access to the internal absolute period position. The position can be read through register 0x0F. This is considered a test mode and should not be used during normal operation.

| **EN_MON** | Addr. 0x0B; bit 3 | R/W |
|---|---|---|
| Code | Function | |
| 0 | Position monitor disabled *default* | |
| 1 | Monitor enabled | |

Table 39: Position monitor control

| **MONITOR(7:0)** | Addr. 0x0F; bit 7:0 | R/W |
|---|---|---|
| Code | Function | |
| | Access to the internal absolute period position. RT only! | |

Table 40: Monitor register

| **EE_READ** | Addr. 0x0E; bit 7 | W |
|---|---|---|
| Code | Function | |
| 0 | Normal operation | |
| 1 | Read all iC-TW2 registers from the EEPROM. Bit is automatically reset upon completion. Not required during normal operation since this is done automatically on start-up. | |

Table 41: EEPROM read command register

**Production test control bits**

Production test control bits are reserved bits. Do not use the production test control bits during normal operation. Keep reserved bits ”0”.

| **Reserved** | Addr. 0xC; bit 7:1 | R/W |
|---|---|---|
| **Reserved** | Addr. 0xD; bit 7:0 | R/W |
| **Reserved** | Addr. 0xE; bit 2:0 | R/W |
| Code | Function | |
| 0 | Normal operation | |
| 1 . . . | Do not use or alter to | |

Table 42: Test modes

## TYPICAL APPLICATIONS

The circuit in Figure 21 depicts a typical application. Differential sensor signals (or differential SIN / COS encoder signals) are directly connected to the iC-TW2. Index gating is single ended active low as is frequently the case when using a HALL switch. The VC signal of 1.21 V is used to bias the positive input PINZ. It is recommended to decouple VC with a small capacitor when it is used as a reference. When VC is left unconnected, no capacitor is required.

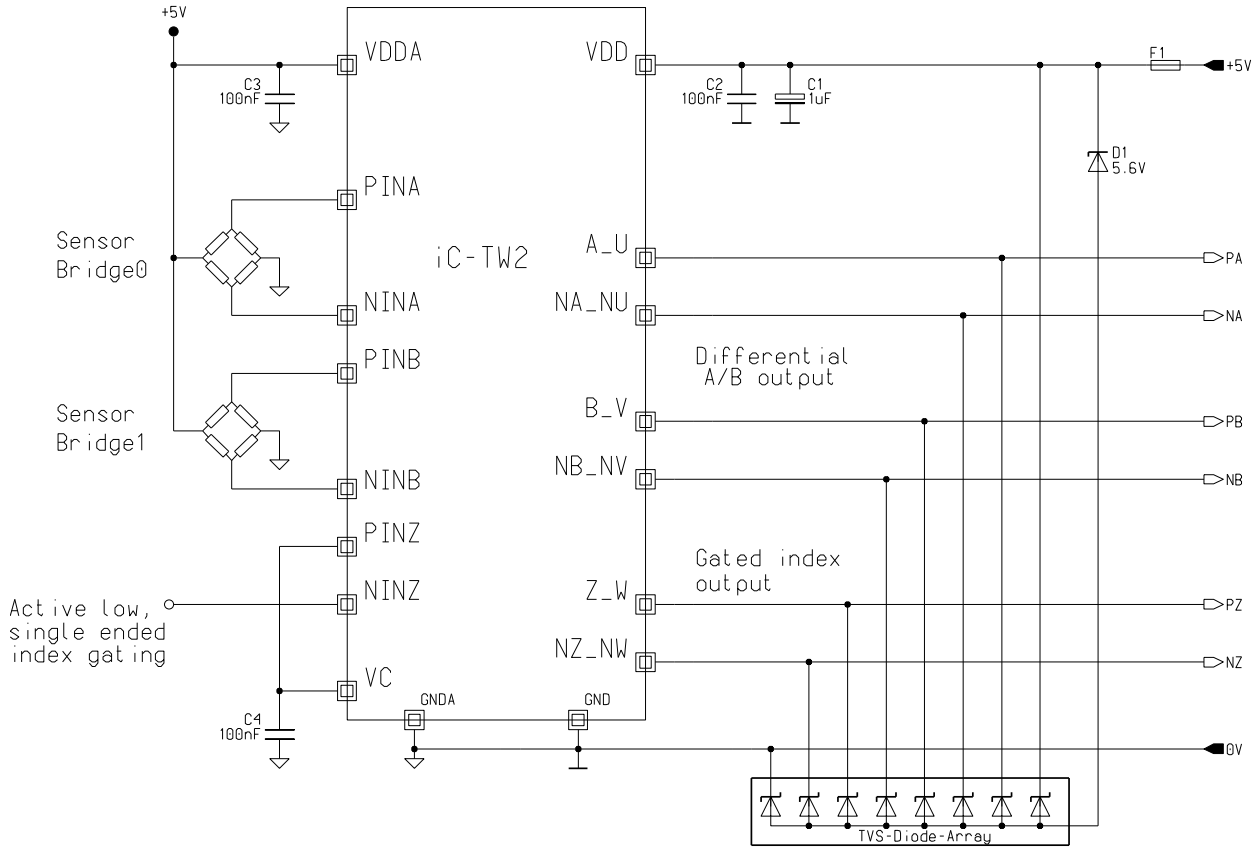



Figure 21: Example of application circuit with differential sensor and single ended index gating

## PCB LAYOUT GUIDELINES

The iC-TW2 is a noise sensitive mixed signal device, which requires careful PCB layout considerations. Violating the layout guidelines can result in poor performance. Please consider Figure 22 .

Power pins VDDA (pin 10) and VDD (pin 1) must be decoupled with 1 µF.

Trace length to VDD pins must be no longer than 3 mm.

The decoupling caps can be placed on the bottom side of the PCB directly connecting it to the iC-TW2 pads using vias.

Ground pins GND (pin 6) and GNDA (pin 11) must be tied to the center exposed pad.

The exposed pad is then directly connected to the PCB ground plane using several vias.

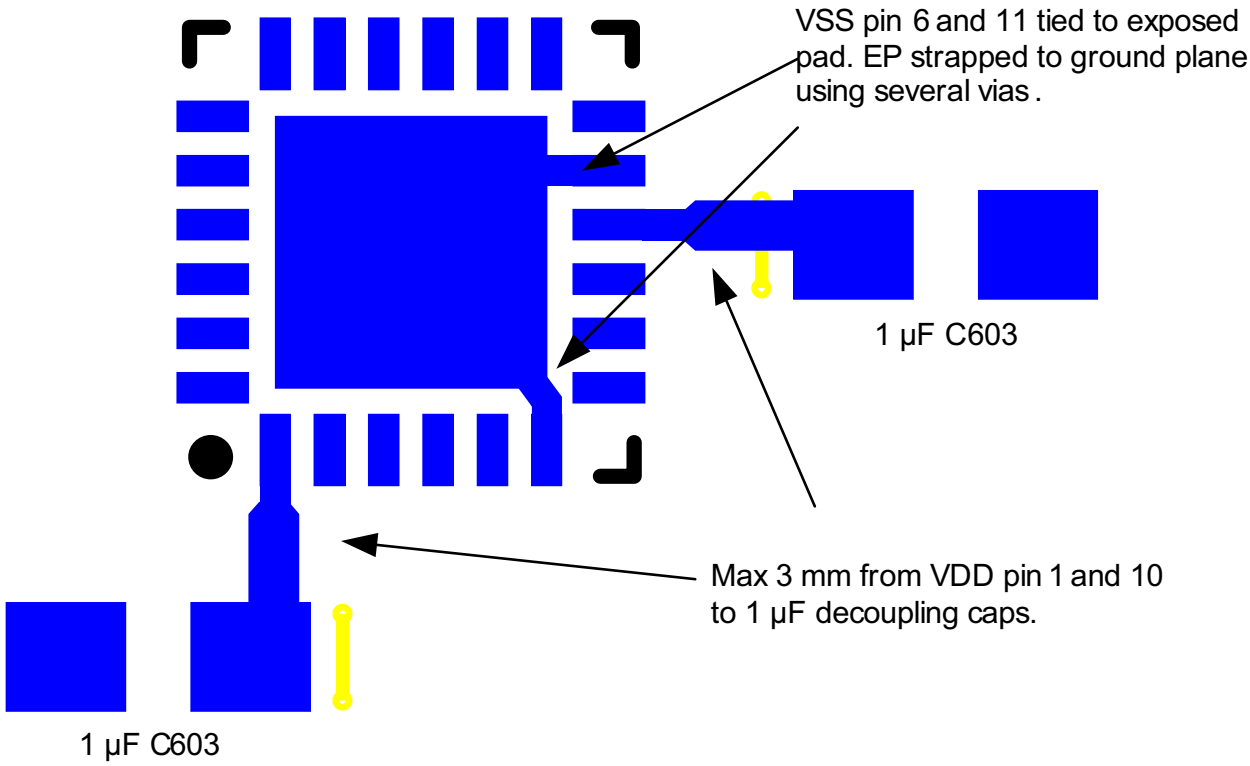



Figure 22: PCB layout guidelines

## ORDERING INFORMATION

| Type | Package | Order Designation |
|---|---|---|
| iC-TW2 | 24 pin QFN, 4 mm x 4 mm | iC-TW2 QFN24 |
| Evaluation Board | PCB 100 mm x 80 mm | iC-TW2 EVAL TW2_2D |

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