

# iC-NV

## 6-BIT Sin/D FLASH CONVERTER

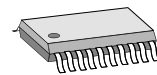
### FEATURES

- Fast flash converter
- Integrated glitch filter; minimum transition distance can be set using the optional resistor
- Selectable resolution of up to 64 steps per cycle and up to 16-fold interpolation
- Integrated instrumentation amplifiers with adjustable gain
- Direct connection of sensor bridges, no external components required
- 200kHz input frequency with the highest resolution
- Incremental A QUAD B output of up to 3.2MHz
- Reversed A/B phase selectable
- Index signal processing
- Sensor bridge calibration supportable by analog/digital test signals
- Low power consumption from single 5V supply
- TTL- /CMOS-compatible outputs
- Inputs and outputs protected against destruction by ESD

### APPLICATIONS

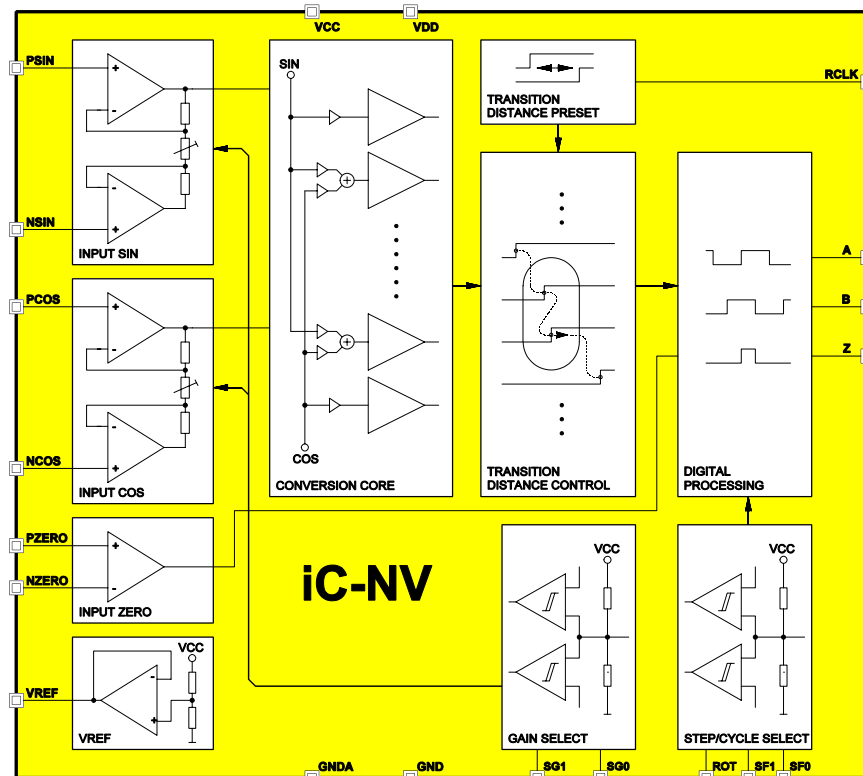
- Angle interpolation from orthogonal sinusoidal input signals
- Linear and rotary encoders
- MR sensor systems

### PACKAGES



TSSOP20

### BLOCK DIAGRAM



# iC-NV

## 6-BIT Sin/D FLASH CONVERTER



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### DESCRIPTION

iC-NV is a monolithic A/D converter which produces two digital A/B incremental signals phase-shifted at 90° from two sinusoidal input signals, also phase-shifted at 90°.

The converter operates on the flash principle with fast single comparators. The back-end signal processing circuit includes a no-delay glitch filter which can be set so that only clearly countable incremental signals are generated. The minimum transition distance for outputs A and B can be set via an external resistor and adapted to suit the application on hand. For static input signals hysteresis prevents the switching of the outputs.

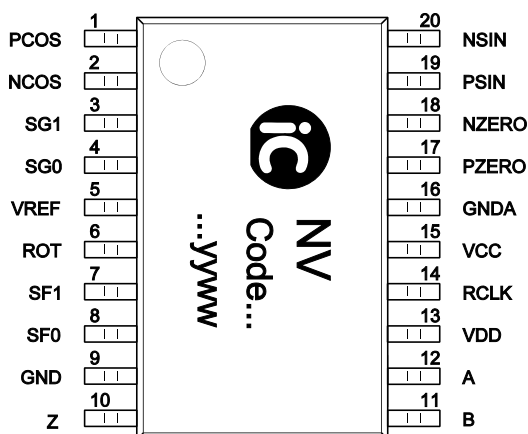
By programming the pins the interpolator can be set to nine different resolutions between 4 and 64 angle steps per cycle; multiplication values of between 1 and 16 are possible for the frequency. The phase relation between the sine/cosine input signals and the A/B incremental signals generated can be selected here.

The device also incorporates an index signal processing circuit which generates a digital zero pulse at Z dependent on the analog sine/cosine input signals and the enable input ZERO. Alternatively, the converter MSB can also be output at Z for synchronization purposes in an absolute measuring system.

The input amplifiers are configured as instrumentation amplifiers and permit sensor bridges to be directly connected without the need for external resistors. The input amplification has nine selectable settings which have been graded to suit standard sensor signals of between ca. 10mVpk and 1Vpk. If external calibration of the sensor bridge is required, eg. with regard to offset, various test functions can be activated. By this the amplified analog input signals come available at the outputs, for instance.

### PACKAGES TSSOP20 to JEDEC Standard

#### PIN CONFIGURATION TSSOP20 4.4mm (top view)



#### PIN FUNCTIONS

| No. | Name    | Function   |
|-----|---------|--|
| 1   | PCOS    | Input Cosine %   |
| 2   | NCOS    | Input Cosine &   |
| 3   | SG1     | Gain Select Input  |
| 4   | SG0     | Gain Select Input  |
| 5   | VREF    | Reference Voltage Output   |
| 6   | ROT     | S6 A/B Phase Selection Input / Test Signal Output                            |
| 7   | SF1     | S5 Resolution Selection Input / Test Signal Output                           |
| 8   | SF0     | S4 Resolution Selection Input / Test Signal Output                           |
| 9   | GND     | Ground (digital)   |
| 10  | Z (MSB) | S3 Index Signal Output Z (MSB Output when ROT= open) / Test Signal Output    |
| 11  | B       | S2 Incremental Output B / Test Signal Output                                 |
| 12  | A       | S1 Incremental Output A / Test Signal Output                                 |
| 13  | VDD     | +5 V Supply Voltage (digital)  |
| 14  | RCLK    | Min. Transition Distance Preset Input (use is optional; can be wired to VCC) |
| 15  | VCC     | +5 V Supply Voltage (analog)   |
| 16  | GNDA    | Ground (analog)  |
| 17  | PZERO   | Index Signal Enable Input %  |
| 18  | NZERO   | Index Signal Enable Input &  |
| 19  | PSIN    | Input Sine %   |
| 20  | NSIN    | Input Sine &   |

External connections linking VCC to VDD and GND to GNDA are required.

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### ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

| Item | Symbol                 | Parameter  | Conditions                       | Fig. |      |      | Unit |
|------|------------------------|--|----------------------------------|------|------|------|------|
|      |                        |  |                                  |      | Min. | Max. |      |
| G001 | VCC                    | Supply Voltage analog  |                                  |      | -0.3 | 6    | V    |
| G002 | VDD                    | Supply Voltage digital   |                                  |      | -0.3 | 6    | V    |
| G003 | V()                    | Voltage at<br>NSIN, PSIN, NCOS, PCOS, NZERO,<br>PZERO, SG1, SG0, RCLK<br>SF1, SF0, ROT, A, B, Z        | V() < VCC+0.3V<br>V() < VDD+0.3V |      | -0.3 | 6    | V    |
| G004 | I <sub>mx</sub> (VCC)  | Current in VCC   |                                  |      | -50  | 50   | mA   |
| G005 | I <sub>mx</sub> (GNDA) | Current in GNDA  |                                  |      | -50  | 50   | mA   |
| G006 | I <sub>mx</sub> (VDD)  | Current in VDD   |                                  |      | -50  | 50   | mA   |
| G007 | I <sub>mx</sub> (GND)  | Current in GND   |                                  |      | -50  | 50   | mA   |
| G008 | I <sub>mx</sub> ()     | Current in<br>NSIN, PSIN, NCOS, PCOS,<br>NZERO, PZERO, SG1, SG0, VREF,<br>RCLK, SF1, SF0, ROT, A, B, Z |                                  |      | -10  | 10   | mA   |
| G009 | I <sub>lu</sub> ()     | Pulse Current in all pins<br>(Latch-up strength)   | pulse duration < 10μs            |      | -100 | 100  | mA   |
| EG1  | V <sub>d</sub> ()      | ESD Susceptibility at all pins   | 100pF discharged through 1.5kΩ   |      |      | 2    | kV   |
| TG1  | T <sub>j</sub>         | Operating Junction Temperature   |                                  |      | -40  | 150  | °C   |
| TG2  | T <sub>s</sub>         | Storage Temperature Range  |                                  |      | -40  | 165  | °C   |

### THERMAL DATA

Operating Conditions: VCC= VDD= 5V ±10%

| Item | Symbol         | Parameter   | Conditions | Fig. |      |      |      | Unit |
|------|----------------|---|------------|------|------|------|------|------|
|      |                |   |            |      | Min. | Typ. | Max. |      |
| T1   | T <sub>a</sub> | Operating Ambient Temperature<br>Range<br><br>(extended temperature range of<br>-40 to 125 °C available on request) |            |      | -25  |      | 85   | °C   |

All voltages are referenced to ground unless otherwise noted.  
All currents into the device pins are positive; all currents out of the device pins are negative.

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## 6-BIT Sin/D FLASH CONVERTER



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### ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC= VDD= 5V ±10%, Tj= -40..125°C, unless otherwise noted

| Item  | Symbol      | Parameter  | Conditions  | Tj<br>°C | Fig.   |                          |      |                                 | Unit                       |
|---|-------------|--|---|----------|--------|--------------------------|------|---------------------------------|----------------------------|
|   |             |  |   |          |        | Min.                     | Typ. | Max.                            |                            |
| <b>Total Device</b>                                   |             |  |   |          |        |                          |      |                                 |                            |
| 001   | VCC,<br>VDD | Permissible Supply Voltage   |   |          |        | 4.5                      |      | 5.5                             | V                          |
| 002   | I(VCC)      | Supply Current in VCC  | fin()= 200kHz; A, B, Z open   |          |        |                          |      | 15                              | mA                         |
| 003   | I(VDD)      | Supply Current in VDD  | fin()= 200kHz; A, B, Z open   |          |        |                          |      | 5                               | mA                         |
| 004   | Von         | Power-On Reset Threshold   |   |          |        | 2                        |      | 3.8                             | V                          |
| 005   | Voff        | Power-Down Reset Threshold   |   |          |        | 1                        |      | 2.2                             | V                          |
| 006   | Vhys        | Power-On Reset Hysteresis  |   |          |        | 0.4                      |      | 1.8                             | V                          |
| 007   | Vc(hi)      | Clamp Voltage hi at<br>NSIN, PSIN, NCOS, PCOS,<br>NZERO, PZERO, SG1, SG0,<br>ROT, SF1, SF0, VREF, RCLK             | Vc(hi)= V()-VCC;<br>I()= 1mA, other pins open   |          |        | 0.3                      |      | 1.6                             | V                          |
| 008   | Vc(lo)      | Clamp Voltage lo at<br>NSIN, PSIN, NCOS, PCOS,<br>NZERO, PZERO, SG1, SG0,<br>ROT, SF1, SF0, VREF, RCLK, A,<br>B, Z | I()= -1mA, other pins open  |          |        | -1.5                     |      | -0.3                            |                            |
| 009   | Vc(hi)      | Clamp Voltage hi at<br>A, B, Z   | Vc(hi)= V()-VDD;<br>I()= 1mA, other pins open   |          |        | 0.3                      |      | 1.6                             | V                          |
| <b>Input Amplifiers NSIN, PSIN, NCOS, PCOS</b>        |             |  |   |          |        |                          |      |                                 |                            |
| 101   | Vos()       | Input Offset Voltage   | Vin() see table gain select<br>GAIN= 10..66<br>GAIN= 3..7.1   |          |        | -7<br>-10                |      | 7<br>10                         | mV<br>mV                   |
| 102   | Iin()       | Input Current  | V()= 0V.. VCC   |          |        | -50                      |      | 50                              | nA                         |
| 103   | G()         | Gain   | GAIN following table gain select  |          |        | 95                       |      | 101                             | %                          |
| 104   | Grel        | Gain Ration SIN/COS  | GAIN following table gain select  |          |        | 98                       |      | 102                             | %                          |
| 105   | fhc         | Cut-off Frequency  | GAIN= 66.667<br>GAIN= 3.03  |          |        | 500<br>2.3               |      |                                 | kHz<br>MHz                 |
| 106   | SR          | Slew Rate  | GAIN= 66.667<br>GAIN= 3.03  |          |        | 10<br>15                 |      |                                 | V/μs<br>V/μs               |
| <b>Signal Processing: Converter Accuracy</b>          |             |  |   |          |        |                          |      |                                 |                            |
| 201   | AAabs       | Absolute Angle Accuracy  | referred to 360° input signal,<br>GAIN= 3.03;<br>VPin= 2...2.6 Vpp, VNin= 2.5 Vdc<br>VPin= 1...1.3 Vpp, VNin= 2.5 Vdc |          |        | -1<br>-2                 |      | 1<br>2                          | DEG<br>DEG                 |
| 202   | AArel       | Relative Angle Accuracy  | referred to period of A, B<br>GAIN= 3.03  |          | 7      | -10                      |      | 10                              | %                          |
| <b>VREF</b>   |             |  |   |          |        |                          |      |                                 |                            |
| 401   | V(VREF)     | Reference Voltage at VREF  | I(VREF)= -1mA..+1mA   |          |        | 48                       |      | 52                              | %VCC                       |
| <b>Signal Processing: Transition Distance Control</b> |             |  |   |          |        |                          |      |                                 |                            |
| 501   | RCLK        | Permissible Resistor at<br>RCLK vs. GNDA   | DIV= 1 (IPF= 10, 12, 16)<br>DIV= 2 (IPF= 5, 8)<br>DIV= 4 (IPF= 3, 4)<br>DIV= 8 (IPF=2)<br>DIV= 16 (IPF= 1)            |          |        | 47<br>23<br>12<br>6<br>3 |      | 500<br>500<br>500<br>500<br>500 | kΩ<br>kΩ<br>kΩ<br>kΩ<br>kΩ |
| 502   | DT()        | Minimum Transition Distance  | R(RCLK, GNDA)= 47KΩ 1%;<br>DIV= 1<br>DIV= 16  |          | 4<br>2 | 45<br>490                |      | 78<br>1000                      | ns<br>ns                   |
| 503   | DT()        | Minimum Transition Distance  | V(RCLK)= VCC;<br>DIV= 1<br>DIV= 16  |          |        | 30<br>420                |      | 78<br>1000                      | ns<br>ns                   |

### ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC= VDD= 5V ±10%, Tj= -40..125°C, unless otherwise noted

| Item   | Symbol             | Parameter                        | Conditions  | Tj<br>°C | Fig. |      |      |         | Unit |      |
|--|--------------------|----------------------------------|---|----------|------|------|------|---------|------|------|
|  |                    |                                  |   |          |      | Min. | Typ. | Max.    |      |      |
| <b>Zero Comparator</b>                                   |                    |                                  |   |          |      |      |      |         |      |      |
| 701  | Vos()              | Input Offset Voltage             | V() <sub>i</sub> = Vcm()                              |          |      | -20  |      | 20      |      | mV   |
| 702  | Iin()              | Input Current                    | V() <sub>i</sub> = 0V.. VCC                           |          |      | -50  |      | 50      |      | nA   |
| 703  | Vcm()              | Common-Mode Input Volt. Range    |   |          |      | 1.4  |      | VCC-1.5 |      | V    |
| 704  | Vdm()              | Differential Input Voltage Range |   |          |      | 0    |      | VCC     |      | V    |
| <b>Signal Processing: Inputs SG1, SG0, ROT, SF1, SF0</b> |                    |                                  |   |          |      |      |      |         |      |      |
| 801  | Vt() <sub>hi</sub> | Input Threshold Voltage hi       |   |          |      | 60   |      | 78      |      | %VCC |
| 802  | Vt() <sub>lo</sub> | Input Threshold Voltage lo       |   |          |      | 25   |      | 40      |      | %VCC |
| 803  | V0()               | Mid Level Voltage                |   |          |      | 43   |      | 57      |      | %VCC |
| 804  | Ri()               | Input Resistance                 |   |          |      | 45   | 150  | 220     |      | kΩ   |
| <b>Signal Processing: Outputs A, B, Z</b>                |                    |                                  |   |          |      |      |      |         |      |      |
| D01  | Vs() <sub>hi</sub> | Saturation Voltage hi            | Vs() <sub>hi</sub> = VDD-V(); I() <sub>i</sub> = -4mA |          |      |      |      | 0.4     |      | V    |
| D02  | Vs() <sub>lo</sub> | Saturation Voltage lo            | I() <sub>i</sub> = 4mA                                |          |      |      |      | 0.4     |      | V    |
| D05  | tr()               | Rise Time                        | CL() <sub>i</sub> = 50pF                              |          |      |      |      | 60      |      | ns   |
| D06  | tf()               | Fall Time                        | CL() <sub>i</sub> = 50pF                              |          |      |      |      | 60      |      | ns   |

### ELECTRICAL CHARACTERISTICS: Diagrams

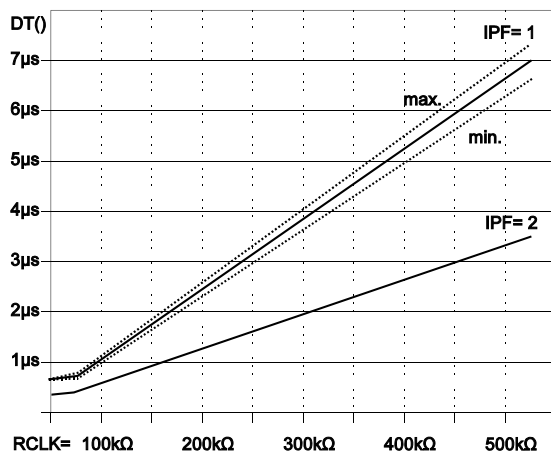


Fig. 1: Adjusting the minimum transition distance via resistor RCLK (given typical at 5V, 27°C; for IPF= 1 within 5V ±10% and -40..+125°C ranges).

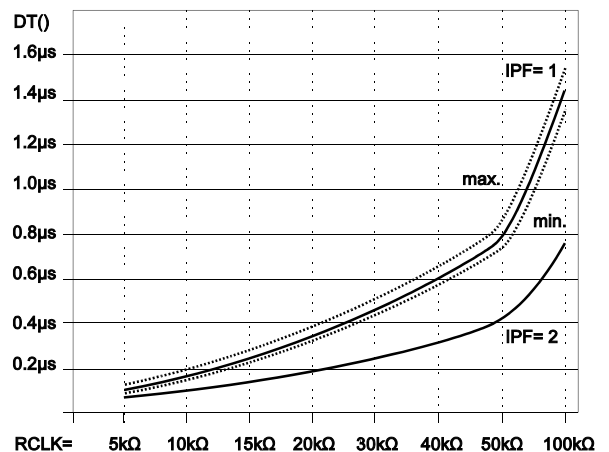


Fig. 2: Similar to Figure 1; the minimum transition distance can be reduced by smaller resistors RCLK.

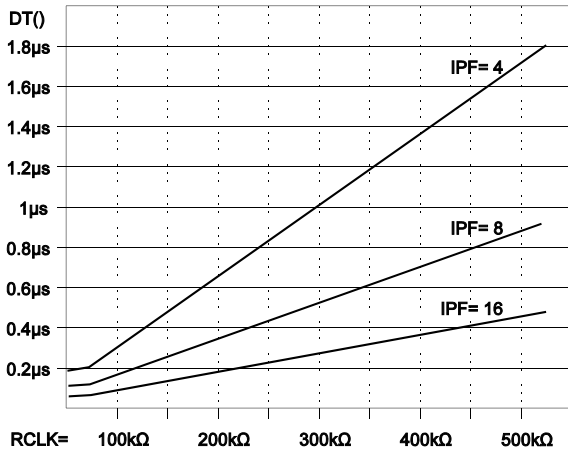


Fig. 3: Adjusting the minimum transition distance via resistor RCLK.

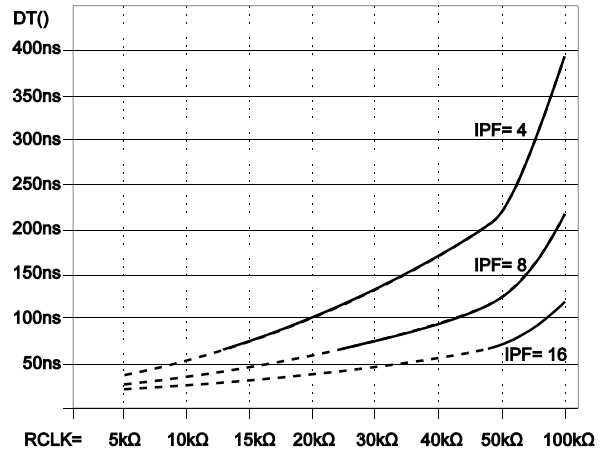


Fig. 4: Similar to Figure 3; minimum transition distance for smaller RCLK resistor values.

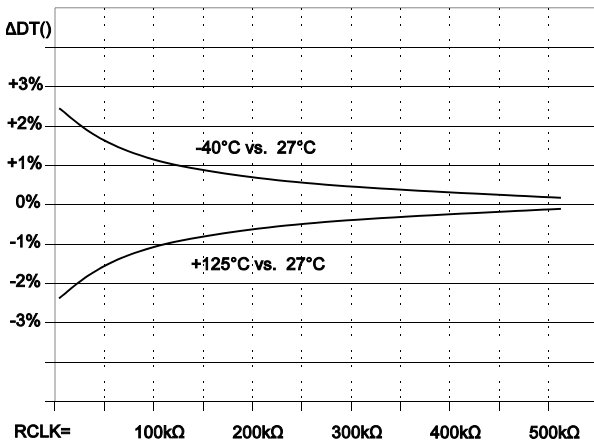


Fig. 5: Temperature drift of the minimum transition distance versus 27°C (VDD= 5V).

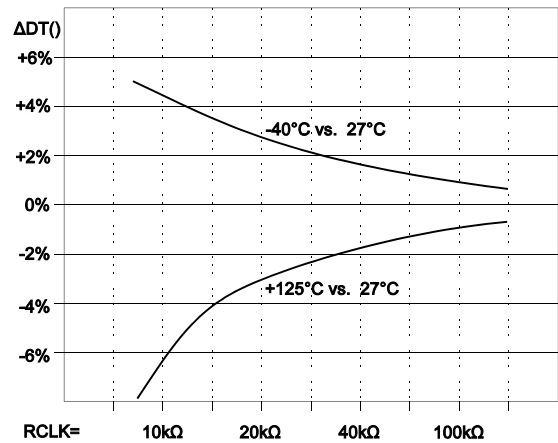


Fig. 6: Temperature drift of the reduced minimum transition distance versus 27°C (VDD= 5V).

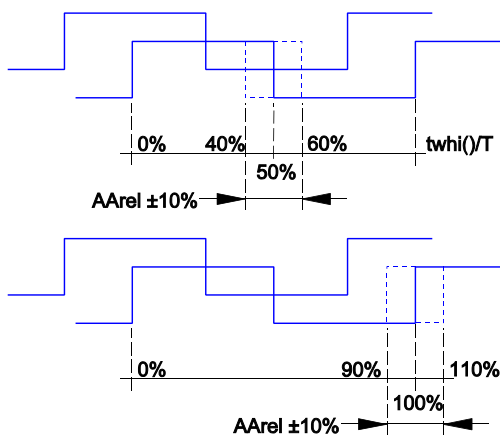


Fig. 7: Definition of the relative angle accuracy.

**DESCRIPTION OF FUNCTIONS**

**Input Amplifiers**

Input stages SIN and COS are configured as instrumentation amplifiers. The gain is dependent on the amplitude of the input signal and set via pins SG0 and SG1 according to the following table. So that the DC level to be adjusted half of the supply voltage is available at VREF.

| GAIN SELECT |      |        |                                       |               |                    |                  |
|-------------|------|--------|---------------------------------------|---------------|--------------------|------------------|
| SG1         | SG0  | Gain   | Sine/Cosine Input Signal Levels Vin() |               |                    |                  |
|             |      |        | Amplitude                             |               | Average value (DC) |                  |
|             |      |        | differential                          | single ended  | differential       | single ended     |
| hi          | hi   | 66.667 | up to 60mVpp                          | up to 120mVpp | 0.7V .. VCC-1.2V   | 0.7V .. VCC-1.2V |
| hi          | open | 50.000 | up to 80mVpp                          | up to 160mVpp | 0.7V .. VCC-1.2V   | 0.7V .. VCC-1.2V |
| hi          | lo   | 33.333 | up to 120mVpp                         | up to 240mVpp | 1.2V .. VCC-1.2V   | 1.2V .. VCC-1.3V |
| open        | hi   | 20.000 | up to 0.2Vpp                          | up to 0.4Vpp  | 1.2V .. VCC-1.2V   | 1.2V .. VCC-1.3V |
| open        | open | 14.300 | up to 0.28Vpp                         | up to 0.56Vpp | 0.7V .. VCC-1.3V   | 0.8V .. VCC-1.4V |
| open        | lo   | 10.000 | up to 0.4Vpp                          | up to 0.8Vpp  | 1.2V .. VCC-1.3V   | 1.3V .. VCC-1.5V |
| lo          | hi   | 7.125  | up to 0.56Vpp                         | up to 1.1Vpp  | 1.2V .. VCC-1.4V   | 1.4V .. VCC-1.7V |
| lo          | open | 4.000  | up to 1Vpp                            | up to 2Vpp    | 1.2V .. VCC-1.6V   | 1.6V .. VCC-2.1V |
| lo          | lo   | 3.030  | up to 1.3Vpp                          | up to 2.6Vpp  | 1.2V .. VCC-1.7V   | 1.8V .. VCC-2.4V |

**Converter Core, Transition Distance Control**

For each of the 64 comparator levels the sine/cosine input signals are calculated according to the theorem of addition and are fed into single comparators. This procedure guarantees a very high converter frequency yet also means that consecutive comparators can switch in a very short space of time in the event of input signal disturbances.

The comparator outputs are thus fed into a transition distance control unit. This monitors the temporal sequence of the switching operations in such a way that each event is delayed by the length of the settable minimum gap to the previous event. If no errors arise the transitions pass the control unit without a time delay. Synchronization with a fixed clock pulse does not occur.

The minimum transition distance is set via an external resistor positioned between RCLK and GNDA. Alternatively, pin RCLK can be shorted to VCC. Depending on the resolution maximum input frequencies of at least 200kHz are then guaranteed (see table of resolution).

**Digital Processing Unit**

The transition distance control unit is followed by the digital processing unit. This is where the transition events are converted into a pulse sequence for the incremental outputs A and B. The square-wave signals generated have a phase shift of +90° or -90°, depending on the direction of rotation. The phase relation between the sine/cosine input signals and the A/B output signals can be set using programming pin ROT.

Alternatively, the MSB of the converter can be output to Z when ROT is high. With the zero signal this changes to high and has the pulse length of half a cycle. This signal can be used to synchronize the high-order tracks of an absolute-value encoder device.

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| A/B OUTPUT PHASE SELECTION |                           |                        |
|----------------------------|---------------------------|------------------------|
| ROT                        | Input signals             | Output signals A, B; Z |
| lo                         | positive; COS leading SIN | B leading A; Z         |
| lo                         | negative; SIN leading COS | A leading B; Z         |
| open                       | positive; COS leading SIN | B leading A; MSB       |
| open                       | negative; SIN leading COS | A leading B; MSB       |
| hi                         | positive; COS leading SIN | A leading B; Z         |
| hi                         | negative; SIN leading COS | B leading A; Z         |

### Resolution, frequency ranges

Nine different resolutions or interpolation factors (IPF) can be programmed via inputs SF0 and SF1. Resolutions 16, 12 and 10 are generated at the core of the converter itself. Resolutions of less than 10 are produced by division DIV in the digital processing unit. The minimum transition distance at outputs A and B corresponds to that of the transition distance control multiplied by the divisor of the digital processing unit.

The minimum output transition distance (maximum output frequency) should be adjusted to carry with the overall system (bandwidth of the transfer medium, sampling rate of the counter). The maximum input frequency is determined by the transition distance control and the resolution of the converter core (16, 12 or 10). This frequency can be increased for resolutions of less than 10 with an external resistor at RCLK. The following table gives possible settings.

| RESOLUTION |      |     |                             |                       |  |
|------------|------|-----|-----------------------------|-----------------------|--|
| SF1        | SF0  | IPF | DIV<br>internal<br>division | $f_{in\_MAX}$         | $f_{in\_MAX}$<br>for RCLK= VCC<br>or RCLK= 47 kΩ |
| hi         | hi   | 16  | 1                           | 200 kHz, RCLK= 47 kΩ  | 200 kHz  |
| hi         | open | 12  | 1                           | 260 kHz, RCLK= 47 kΩ  | 260 kHz  |
| hi         | lo   | 10  | 1                           | 320 kHz, RCLK= 47 kΩ  | 320 kHz  |
| open       | hi   | 8   | 2                           | 400 kHz, RCLK= 23 kΩ  | 200 kHz  |
| open       | open | 5   | 2                           | 640 kHz, RCLK= 23 kΩ  | 320 kHz  |
| open       | lo   | 4   | 4                           | 800 kHz, RCLK= 12 kΩ  | 200 kHz  |
| lo         | hi   | 3   | 4                           | 1.04 MHz, RCLK= 12 kΩ | 260 kHz  |
| lo         | open | 2   | 8                           | 1.6 MHz, RCLK= 6 kΩ   | 200 kHz  |
| lo         | lo   | 1   | 16                          | (3.2 MHz), RCLK= 3 kΩ | 200 kHz  |



### Hysteresis

iC-NV has an angular hysteresis which is independent of the input amplitude and phase. It prevents the outputs from switching when the inputs are static. The following diagram shows the effect this has with an interpolation factor of 8..

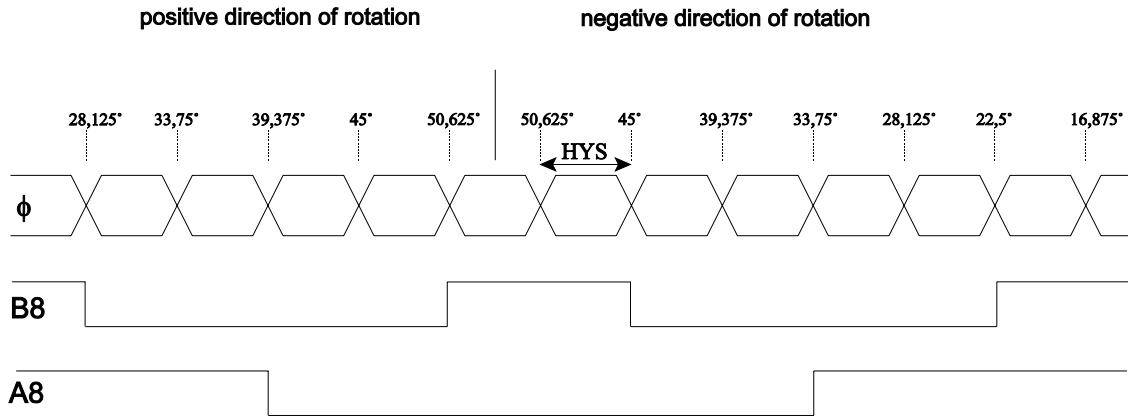


Fig. 8: Effect of angle hysteresis

When the direction of rotation is reversed the integrated hysteresis circuit prompts the change in direction to be signaled at the outputs; the hysteresis causes a delay here. According to the resolution the hysteresis is set to one of the following fixed values.

| ANGLE HYSTERESIS       |        |        |      |        |     |        |     |      |        |
|------------------------|--------|--------|------|--------|-----|--------|-----|------|--------|
| Interpolation factor   | 1      | 2      | 3    | 4      | 5   | 8      | 10  | 12   | 16     |
| Hysteresis DEG         | 5,625° | 5,625° | 7,5° | 5,625° | 9°  | 5,625° | 9°  | 7,5° | 5,625° |
| referred to A/B period | 1/64   | 1/32   | 1/16 | 1/16   | 1/8 | 1/8    | 1/4 | 1/4  | 1/4    |

### Zero pulse

One zero pulse (index) is generated per cycle from the sine/cosine inputs. To be output to Z it must be enabled by the comparator at differential inputs PZERO and NZERO. The width of the zero pulse is a quarter of the length of the A and/or B signal output cycle. When Z is high, simultaneously A&B are high. The position of the zero pulse dependent on the interpolation factor and the direction of rotation is given in the following table.

| INDEX POSITION |                                |                                |
|----------------|--------------------------------|--------------------------------|
| IPF            | positive direction of rotation | negative direction of rotation |
| 16             | 45° .. 50,625°                 | 39,375° .. 45°                 |
| 12             | 45° .. 52,5°                   | 37,5° .. 45°                   |
| 10             | 45° .. 54°                     | 36° .. 45°                     |
| 8              | 39,375° .. 50,625°             | 33,75° .. 45°                  |
| 5              | 36° .. 54°                     | 27° .. 45°                     |
| 4              | 33,75° .. 56,25°               | 28,125° .. 50,625°             |
| 3              | 30° .. 60°                     | 22,5° .. 52,5°                 |
| 2              | 22,5° .. 67,5°                 | 16,875° .. 61,875°             |
| 1              | 0° .. 90°                      | 354,375° .. 84,625°            |

**Oscilloscope diagrams**

The following diagrams give the input and output signals for various directions of rotation and ROT settings for interpolation factors 1 and 16.

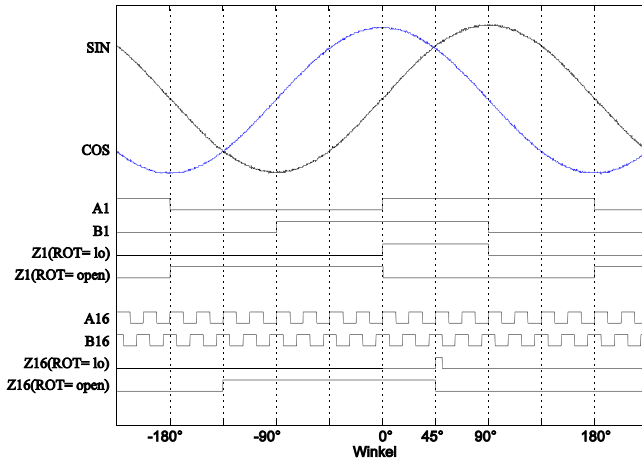


Fig. 9: ROT= lo/open, COS leading SIN

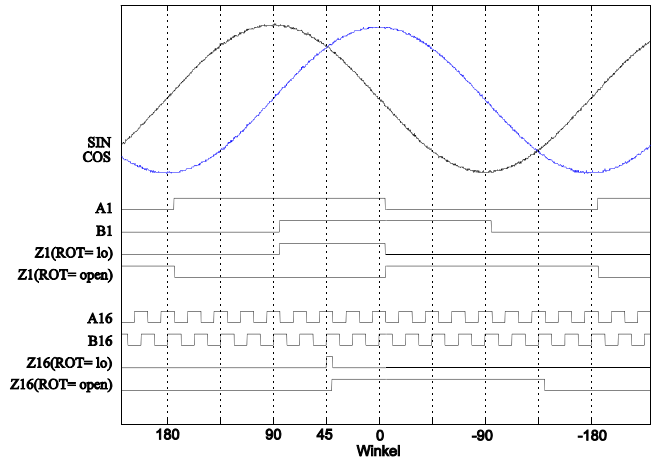


Fig. 10: ROT= lo/open, SIN leading COS

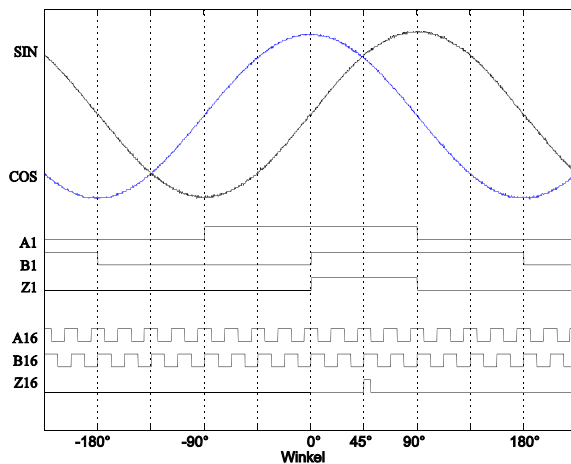


Fig. 11: ROT= hi, COS leading SIN

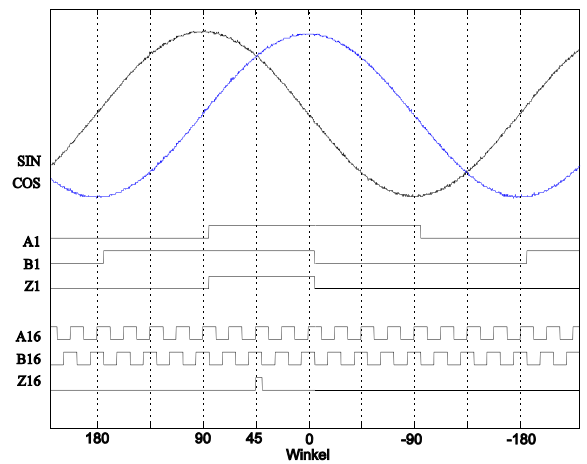


Fig. 12: ROT= hi, SIN leading COS

# iC-NV

## 6-BIT Sin/D FLASH CONVERTER

### Test functions

Device iC-NV features internal test functions which can be used to ease sensor bridge calibration procedures if such are required. To enable test operation, a threshold current of approx. 1mA present at pin RCLK must be exceeded during power up. Subsequently, four different test modes are selectable starting with mode 3 set initially.

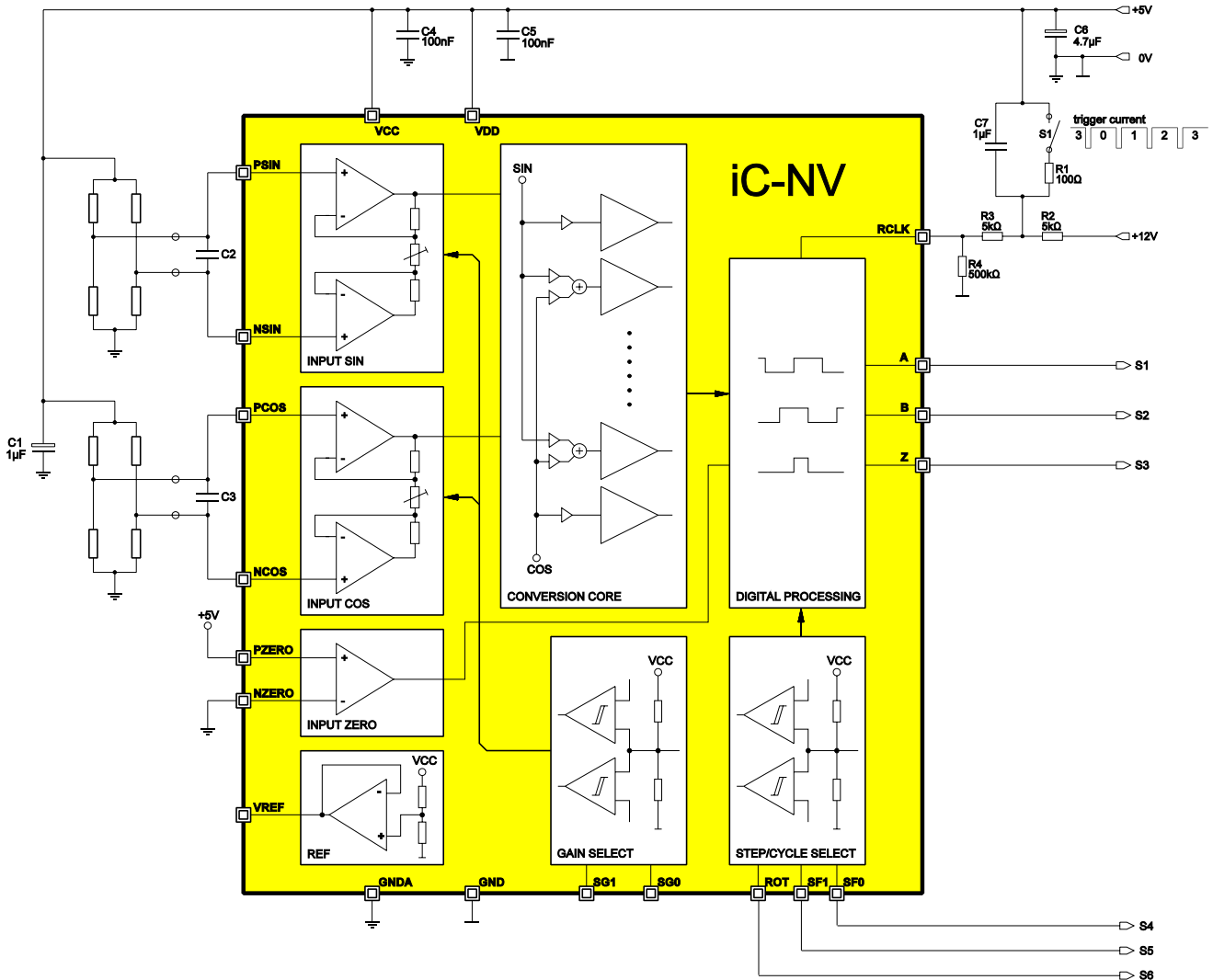


Fig. 13: Activating test functions via pin RCLK.

# iC-NV

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### Description of test signals

#### MODE 3

**ZK** un-gated index/zero comparator output  
**EXKA** all comparators EXOR-gated  
**SIN, NSIN, COS, NCOS**  
 amplifier outputs (signal valid with no load only)

#### MODE 1
















**CLK, UP, DN**  
 Control signals for external counters.

#### MODE 2

**NENOS, CLK, DALL**  
 Test signals for iC-Haus device test.

#### MODE 0

**KA(0)** Comparator 0°-180°  
 Duty cycle indicates offset of sine signal.  
**KA(16)** Comparator 90°-270°  
 Duty cycle indicates offset of cosine signal.  
**KA(X): KA(8) EXOR KA(24)**  
 Comparator 45°-225°  
 Duty cycle indicates amplitude ratio of sine/cosine signal. Offset calibration must be performed first.

| Test Mode | S1 (A)  | S2 (B)   | S3 (Z)  | S4 (SF0)   | S5 (SF1)  | S6 (ROT)   |
|-----------|---|--|---|--|---|--|
| 3         | ZK     | EXKA    | SIN    | NSIN  | COS  | NCOS  |
| 0         | KA(0)  | KA(16)  | KA(X)  |  |   |  |
| 1         | CLK    | UP      | DN     |  |   |  |
| 2         | NENOS  | CLK     | DALL   |  |   |  |

### APPLICATIONS INFORMATION

#### Principal Input Circuits

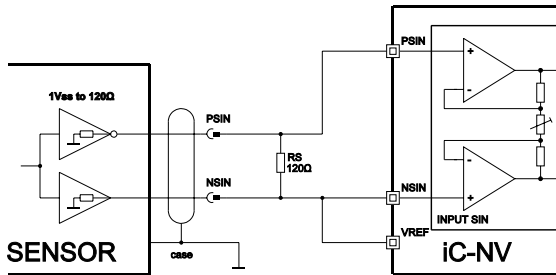


Fig. 14: Input circuit for voltage signals of 1Vpp with no ground reference. When grounds are not separated the connection NSIN to VREF must be omitted.

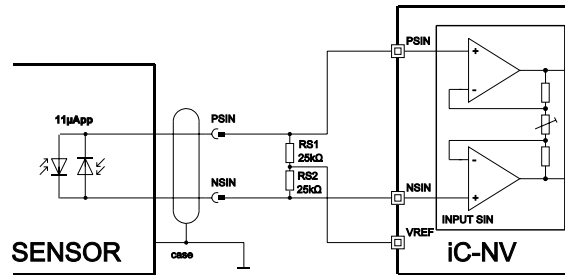


Fig. 15: Input circuit for current signals of 11μA. In this circuit offset adjustment is not possible.

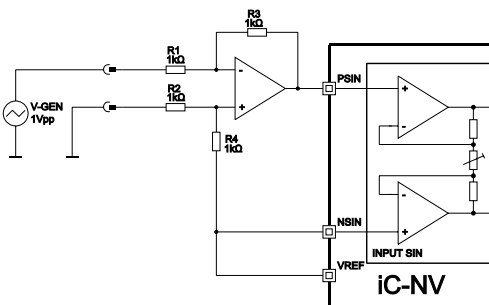


Fig. 16: Input circuit for single-side voltage or current source signals with ground reference (adaptation via resistors R3, R4).

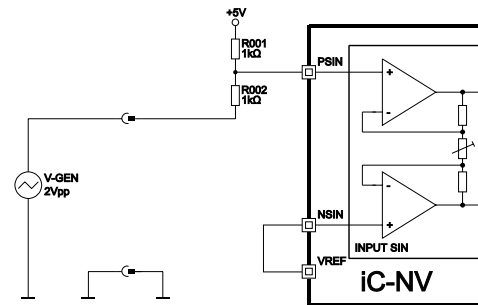


Fig. 17: Simplified input wiring for single-side voltage signals with ground reference.

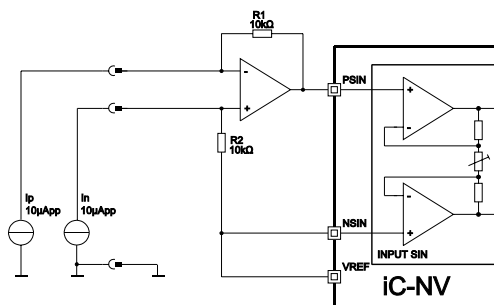


Fig. 18: Input circuit for differential current sink sensor outputs, eg. using Opto Encoder iC-WG.

### Wiring photodiode arrays with common cathodes

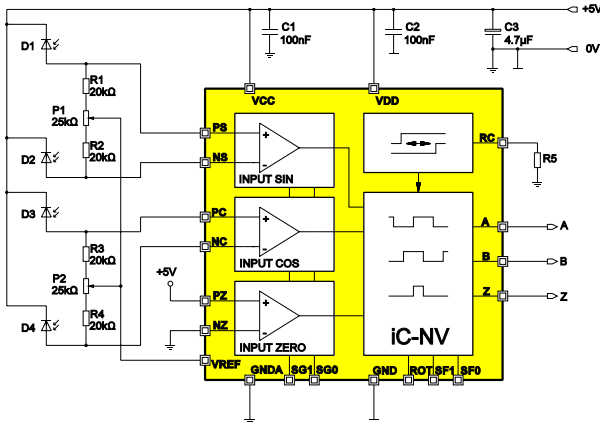


Fig. 19: Wiring scheme with offset adjustment possibility; the resistor values must be selected with respect to the photo currents available (eg. 65kΩ for max. 16μApk at GAIN= 3, or 1μA at GAIN= 50 respectively).

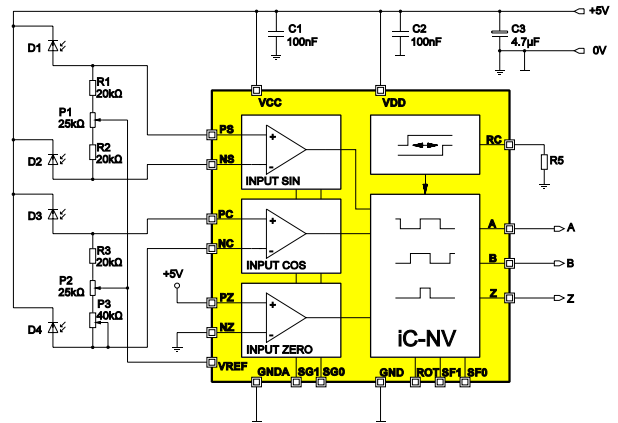


Fig. 20: Additional adjustment possibility for amplitude differences; settings at P3 must be done first.

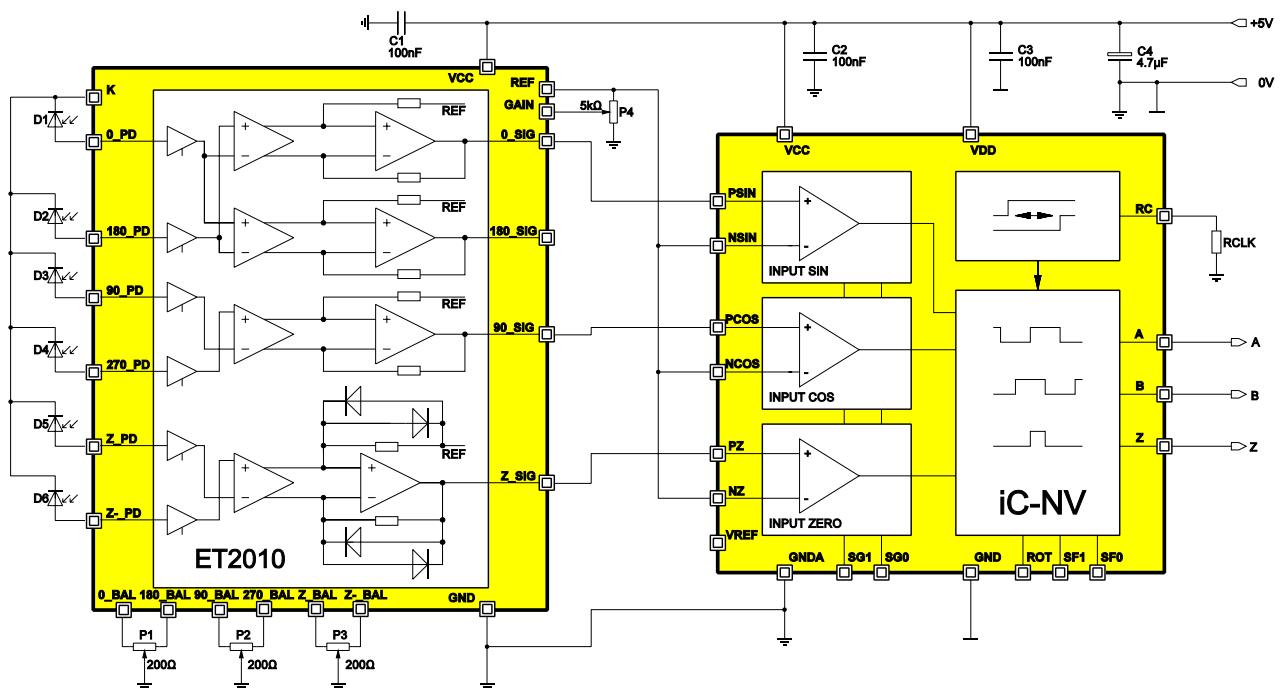


Fig. 21: Photodiode scanning circuit using ET2010 pre-amp and adjustment device.

### Wiring photodiode arrays with common anodes

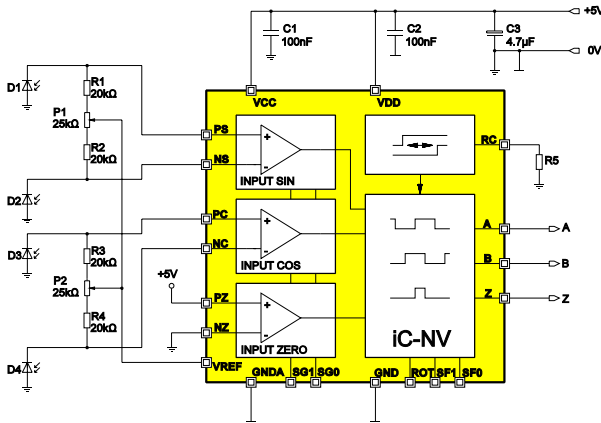


Fig. 22: Wiring scheme with offset adjustment possibility; the resistor values must be selected with respect to the photo currents available (eg. 65kΩ for max. 16µA pk at GAIN= 3, or 1µA at GAIN= 50 respectively).

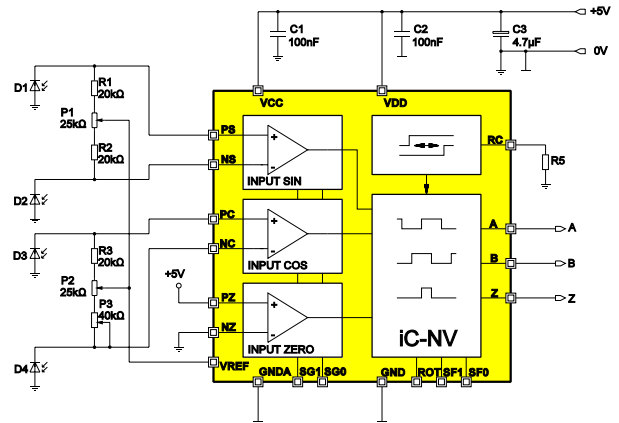


Fig. 23: Additional adjustment possibility for amplitude differences; settings at P3 must be done first.

### Wiring magneto-resistor bridge sensors

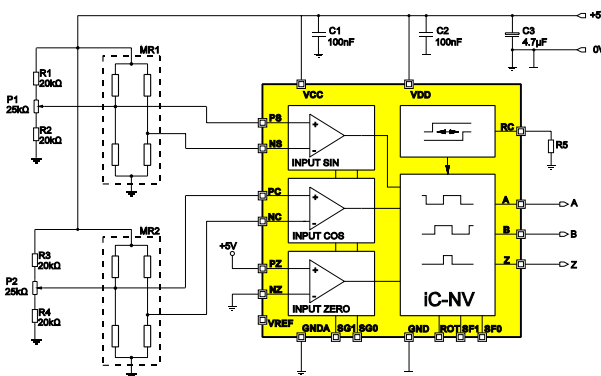


Fig. 24: Wiring MR sensor bridges with offset adjustment possibility; setup pins remaining open can be linked to VREF to enhance interference immunity.

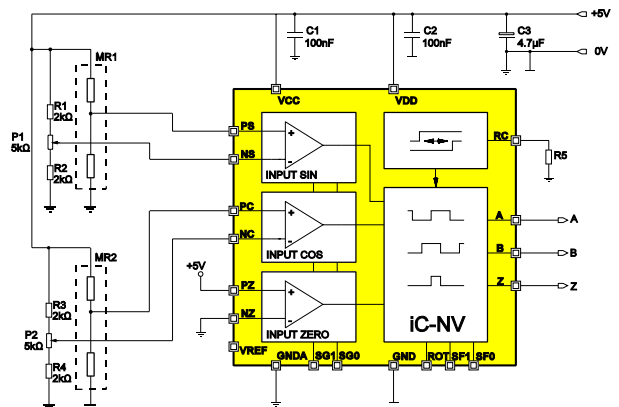


Fig. 25: Wiring MR half-bridge sensors with offset adjustment possibility.

### MR Sensor System Application Example

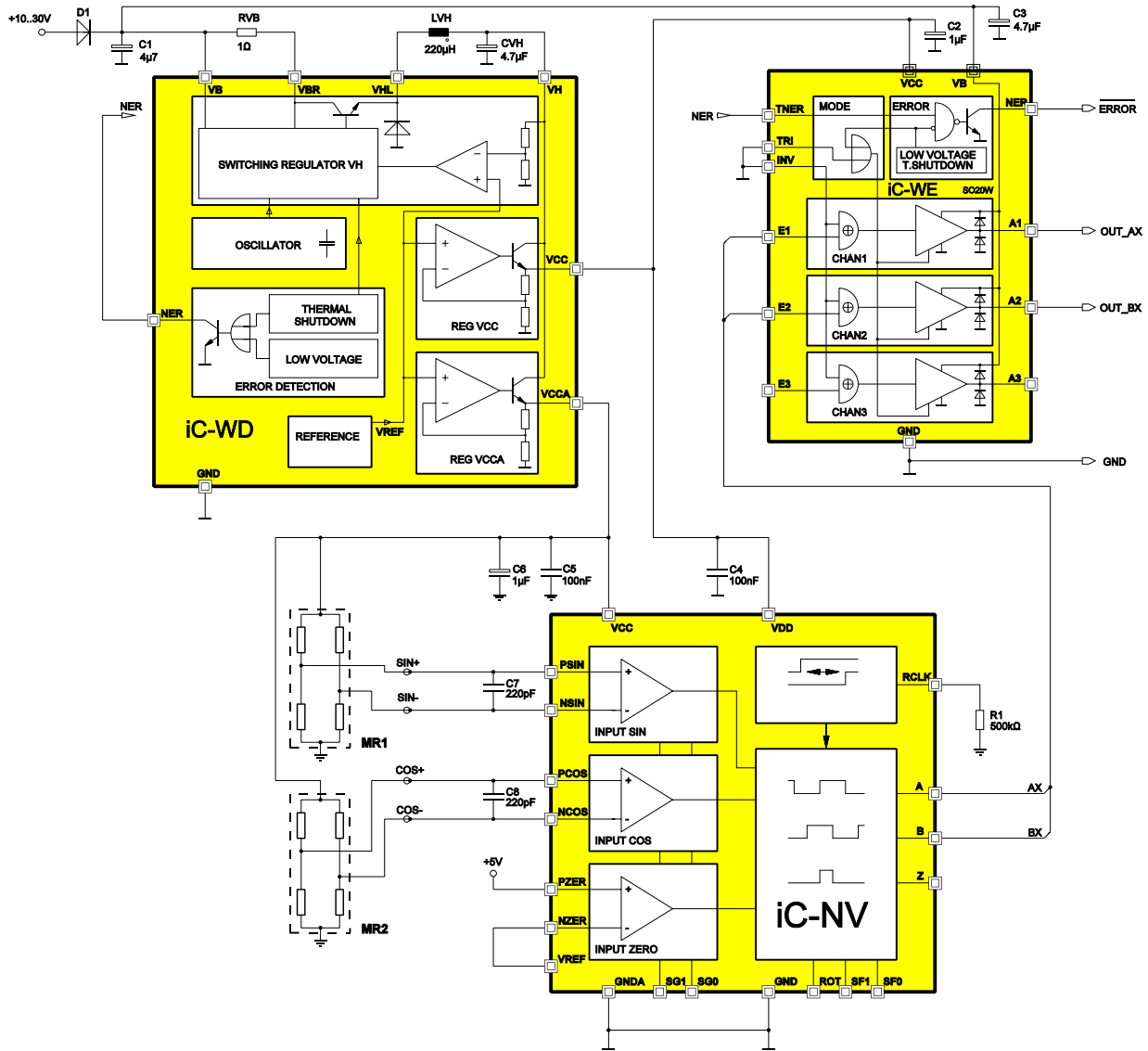


Fig. 26: Complete MR sensor system for 24V environment featuring low-noise switch-mode power supply linear regulator combo iC-WD and line driver iC-WE, enabling data transmission via 100m cable length. The maximum output frequency is limited to approx. 280kHz by  $R1 = 500k\Omega$  to comply with speed-limited external counters (pins SF1 and SF0 are open and select  $IPF = 5$ ). C7/C8 can help to improve noise immunity additionally, for instance with motor applications.



# iC-NV

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### DEMO BOARD

The iC-NV device is equipped with a Demo Board for test purposes. Figures 10 to 12 show the wiring as well as the top and bottom layout of the test PCB.

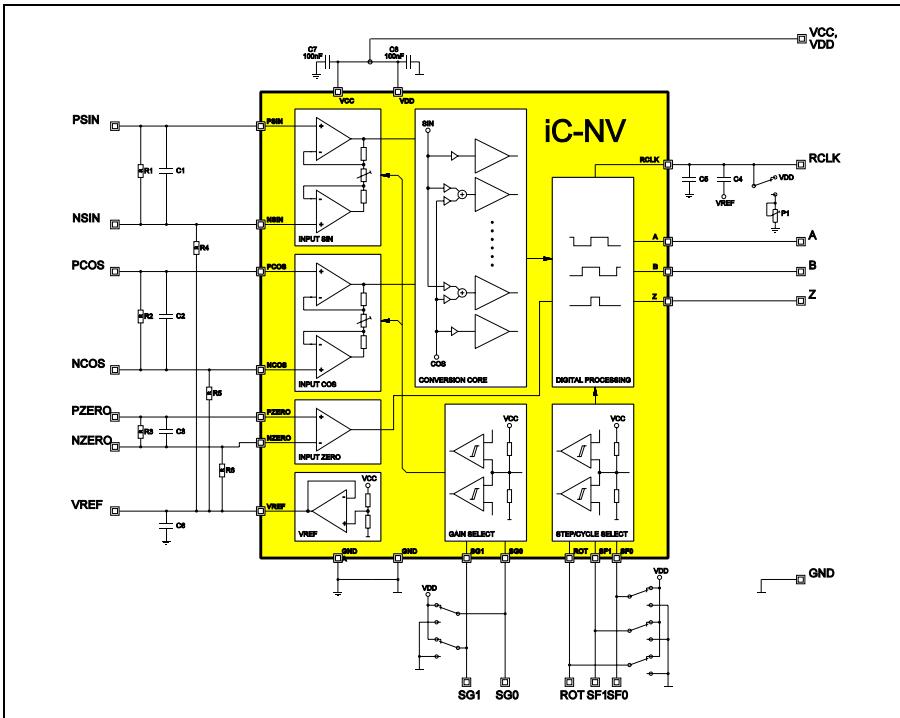


Fig. 27: Circuit diagram of the demo board (delivery comes without pot assembly; the corresponding switch must remain set to high).

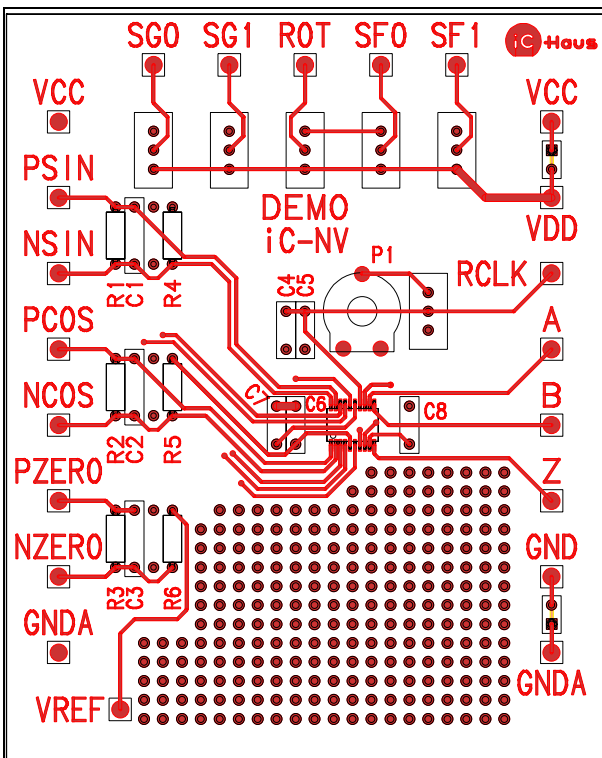


Fig. 28: Demo Board (components side)

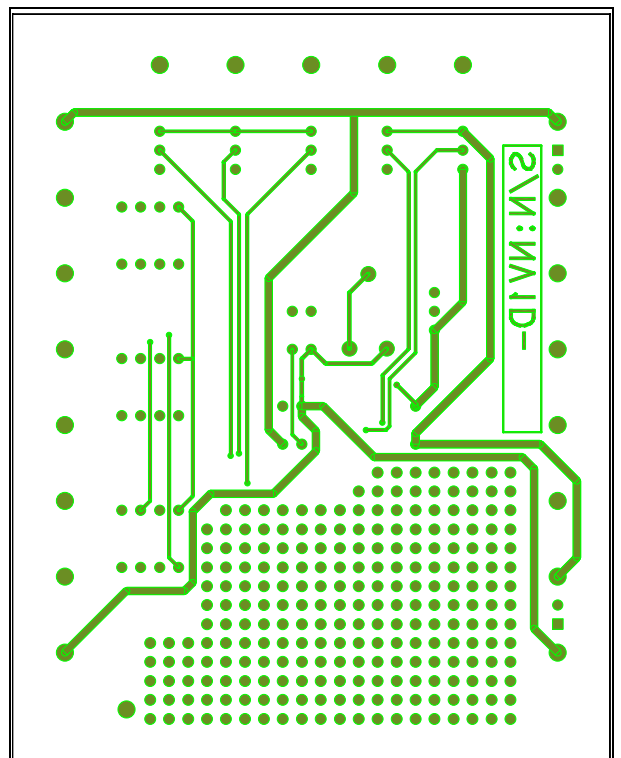


Fig. 29: Demo Board (bottom side)

# iC-NV

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**ORDERING INFORMATION**

| Type       | Package       | Order designation |
|------------|---------------|-------------------|
| iC-NV      | TSSOP20 4.4mm | iC-NV TSSOP20     |
| Demo Board |               | EVAL NV1D         |

For technical support, information about prices and terms of delivery please contact:

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