# 14 Pin DIP 10 Tap TTL Compatible Active Delay Lines with Leading And Trailing Edge Precision

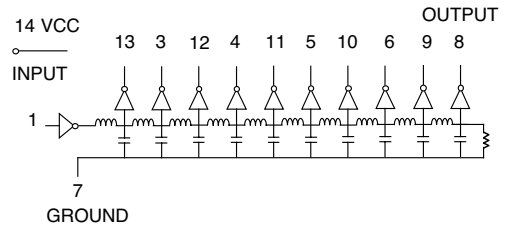
| TAP DELAYS ±5% or ±2 nS† | TOTAL DELAYS ±5% or ±2 nS† | PART NUMBER | TAP DELAYS ±5% or ±2 nS† | TOTAL DELAYS ±5% or ±2 nS† | PART NUMBER |
|---|---|---|---|---|---|
| 5 | 50 | EPA460-50 | 44 | 440 | EPA460-440 |
| 6 | 60 | EPA460-60 | 45 | 450 | EPA460-450 |
| 7.5 | 75 | EPA460-75 | 47 | 470 | EPA460-470 |
| 10 | 100 | EPA460-100 | 50 | 500 | EPA460-500 |
| 12.5 | 125 | EPA460-125 | 55 | 550 | EPA460-550 |
| 15 | 150 | EPA460-150 | 60 | 600 | EPA460-600 |
| 17.5 | 175 | EPA460-175 | 65 | 650 | EPA460-650 |
| 20 | 200 | EPA460-200 | 70 | 700 | EPA460-700 |
| 22.5 | 225 | EPA460-225 | 75 | 750 | EPA460-750 |
| 25 | 250 | EPA460-250 | 80 | 800 | EPA460-800 |
| 30 | 300 | EPA460-300 | 85 | 850 | EPA460-850 |
| 35 | 350 | EPA460-350 | 90 | 900 | EPA460-900 |
| 40 | 400 | EPA460-400 | 95 | 950 | EPA460-950 |
| 42 | 420 | EPA460-420 | 100 | 1000 | EPA460-1000 |

*†Whichever is greater. Delay times referenced from input to leading edges at 25°C, 5.0V, with no load.*

## DC Electrical Characteristics

| | Parameter | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | High-Level Output Voltage | $V_{CC}$ = min. $V_{IL}$ = max. $I_{OH}$ = max | 2.7 | | V |
| $V_{OL}$ | Low-Level Output Voltage | $V_{CC}$ = min. $V_{IH}$ = min. $I_{OL}$ = max | | 0.5 | V |
| $V_{IK}$ | Input Clamp Voltage | $V_{CC}$ = min. $I_I$ = $II_K$ | | -1.2V | V |
| $I_{IH}$ | High-Level Input Current | $V_{CC}$ = max. $V_{IN}$ = 2.7V | | 50 | µA |
| | | $V_{CC}$ = max. $V_{IN}$ = 5.25V | | 1.0 | mA |
| $I_{IL}$ | Low-Level Input Current | $V_{CC}$ = max. $V_{IN}$ = 0.5V | | -2 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = max. $V_{OUT}$ = 0. (One output at a time) | -40 | -100 | mA |
| $I_{CCH}$ | High-Level Supply Current | $V_{CC}$ = max. $V_{IN}$ = OPEN | | 150 | mA |
| $I_{CCL}$ | Low-Level Supply Current | $V_{CC}$ = max. $V_{IN}$ = 0 | | 150 | mA |
| $T_{RO}$ | Output Rise Time | Td ≤ 500 nS (0.75 to 2.4 Volts) | | 4 | nS |
| | | Td > 500 nS | | 5 | nS |
| $N_H$ | Fanout High-Level Output | $V_{CC}$ = max. $V_{OH}$ = 2.7V | | 20 TTL LOAD | |
| $N_L$ | Fanout Low-Level Output | $V_{CC}$ = max. $V_{OL}$ = 0.5V | | 10 TTL LOAD | |

## Schematic




## Recommended Operating Conditions

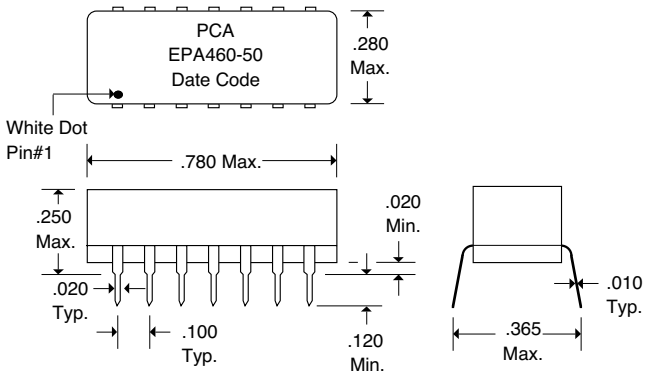
| | | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.75 | 5.25 | V |
| $V_{IH}$ | High-Level Input Voltage | 2.0 | | V |
| $V_{IL}$ | Low-Level Input Voltage | | 0.8 | V |
| $I_{IK}$ | Input Clamp Current | | -18 | mA |
| $I_{OH}$ | High-Level Output Current | | -1.0 | mA |
| $I_{OL}$ | Low-Level Output Current | | 20 | mA |
| $P_W$* | Pulse Width of Total Delay | 40 | | % |
| d* | Duty Cycle | | 40 | % |
| $T_A$ | Operating Free-Air Temperature | 0 | +70 | °C |

**These two values are inter-dependent.*

## Input Pulse Test Conditions @ 25° C

| | | | Unit |
|---|---|---|---|
| $E_{IN}$ | Pulse Input Voltage | 3.2 | Volts |
| $P_W$ | Pulse Width % of Total Delay | 110 | % |
| $T_{RI}$ | Pulse Rise Time (0.75 - 2.4 Volts) | 2.0 | nS |
| $P_{RR}$ | Pulse Repetition Rate @ Td ≤ 200 nS | 1.0 | MHz |
| | Pulse Repetition Rate @ Td > 200 nS | 100 | KHz |
| $V_{CC}$ | Supply Voltage | 5.0 | Volts |

## Package Dimensions




DSA460 Rev. A 2/5/96

QAF-CSO1 Rev. B 8/25/94

Unless Otherwise Noted Dimensions in Inches
Tolerances:
Fractional = ± 1/32
.XX = ± .030 .XXX = ± .010



PCA ELECTRONICS INC.

16799 SCHOENBORN ST.
NORTH HILLS, CA 91343
TEL: (818) 892-0761
FAX: (818) 894-5791