INTEGRATED COMPLEMENTARY BUFFERED-GATE SCRS FOR DUAL POLARITY SLIC OVERVOLTAGE PROTECTION

TISP9110LDM Overvoltage Protector

High Performance Protection for SLICs with +ve and -ve Battery Supplies
- **Wide -110 V to +110 V Programming Range**
- **Low 5 mA max. Gate Triggering Current**
- **Dynamic Protection Performance Specified for International Surge Waveshapes**

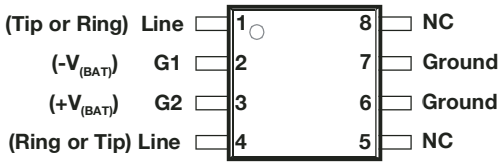
Applications include:
- **Wireless Local Loop**
- **Access Equipment**
- **Regenerated POTS**
- **VOIP Applications**

Rated for International Surge Wave Shapes

Wave Shape	Standard	I_{PPSM} A
2/10	GR-1089-CORE	100
10/700	ITU-T K.20/21/45	45
10/1000	GR-1089-CORE	30

..... UL Recognized Component

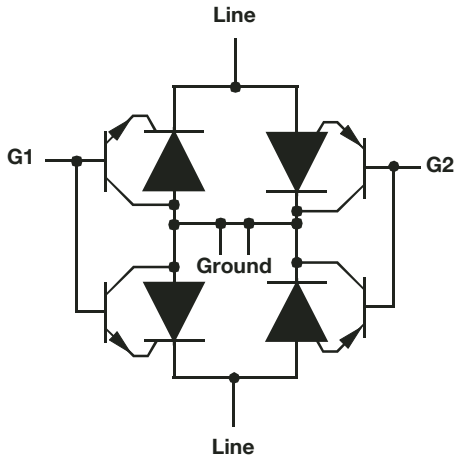
8-SOIC (210 mil) Package (Top View)



NC - No internal connection
Terminal typical application names shown in parenthesis

MD-8SOIC(210)-003-a

Device Symbol



SD-TISP9-001-a

Description

The TISP9110LDM is a programmable overvoltage protection device designed to protect modern dual polarity supply rail ringing SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line. Overvoltages can be caused by lightning, a.c. power contact and induction. Four separate protection structures are used; two positive and two negative to provide optimum protection during Metallic (Differential) and Longitudinal (Common Mode) protection conditions in both polarities. Dynamic protection performance is specified under typical international surge waveforms from Telcordia GR-1089-CORE, ITU-T K.44 and YD/T 950.

The TISP9110LDM is programmed by connecting the G1 and G2 gate terminals to the negative ($-V_{(BAT)}$) and positive ($+V_{(BAT)}$) SLIC Battery supplies respectively. This creates a protector operating at typically +1.4 V above $+V_{(BAT)}$ and -1.4 V below $-V_{(BAT)}$ under a.c. power induction and power contact conditions. The protector gate circuitry incorporates 4 separate buffer transistors designed to provide independent control for each protection element. The gate buffer transistors minimize supply regulation issues by reducing the gate current drawn to around 5 mA, while the high voltage base emitter structures eliminate the need for expensive reverse bias protection gate diodes.

The TISP9110LDM is rated for common surges contained in regulatory requirements such as ITU-T K.20, K.45, Telcordia GR-1089-CORE, YD/T 950. By the use of appropriate overcurrent protection devices such as the Bourns® Multifuse® and Telefuse™ devices, circuits can be designed to comply with modern telecom standards.

How To Order

Device	Package	Carrier	Order As	Marking Code	Standard Quantity
TISP9110LDM	8-SOIC (210 mil)	Embossed Tape Reeled	TISP9110LDMR-S	9110L	2000

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex

AUGUST 2004 – REVISED JANUARY 2007

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage $V_{G1(Line)}$ = 0, V_{G2} ≥ +5 V $V_{G2(Line)}$ = 0, V_{G1} ≥ -5 V	V_{DRM}	-120 +120	V
Non-repetitive peak impulse current (see Notes 1, 2, 3 and 4) 2/10 µs (Telcordia GR-1089-CORE) 5/310 µs (ITU-T K.20, K.21 & K.45, K.44 open-circuit voltage wave shape 10/700 µs) 10/1000 µs (Telcordia GR-1089-CORE)	I_{PPSM}	 ±100 ±45 ±30	A
Non-repetitive peak on-state current, 50 Hz / 60 Hz (see Notes 1, 2, 3 and 5) 0.2 s 1 s 900 s	I_{TSM}	 9.0 5.0 1.7	A
Maximum negative battery supply voltage	V_{G1M}	-110	V
Maximum positive battery supply voltage	V_{G2M}	+110	V
Maximum differential battery supply voltage	$\Delta V_{(BAT)M}$	220	V
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. Initially the device must be in thermal equilibrium with T_J = 25 °C. The surge may be repeated after the device returns to its initial conditions.
2. The rated current values may be applied to either of the Line to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of a single terminal pair).
3. Rated currents only apply if pins 6 & 7 (Ground) are connected together.
4. Applies for the following bias conditions: V_{G1} = -20 V to -110 V, V_{G2} = 0 V to +110 V.
5. EIA/JESD51-2 environment and EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.

Electrical Characteristics for any Section, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_D	Off-state current	$V_D = V_{DRM}$, $V_{G1(Line)}$ = 0, V_{G2} ≥ +5 V	T_A = 25 °C			-5	µA
			T_A = 85 °C			-50	
		$V_D = V_{DRM}$, $V_{G2(Line)}$ = 0, V_{G1} ≥ -5 V	T_A = 25 °C			+5	
			T_A = 85 °C			+50	
$I_{G1(Line)}$	Negative-gate leakage current	$V_{G1(Line)}$ = -220 V				-5	µA
$I_{G2(Line)}$	Positive-gate leakage current	$V_{G2(Line)}$ = +220 V				+5	µA
$V_{G1L(BO)}$	Gate - Line impulse breakover voltage	V_{G1} = -100 V, I_T = -100 A (see Note 6)	2/10 µs			-15	V
		V_{G1} = -100 V, I_T = -30 A	10/1000 µs			-11	
$V_{G2L(BO)}$	Gate - Line impulse breakover voltage	V_{G2} = +100 V, I_T = +100 A (see Note 6)	2/10 µs			+15	V
		V_{G2} = +100 V, I_T = +30 A	10/1000 µs			+11	
I_H-	Negative holding current	V_{G1} = -60 V, I_T = -1 A, di/dt = 1 A/ms		-150			mA
I_{G1T}	Negative-gate trigger current	I_T = -5 A, $t_{p(g)}$ ≥ 20 µs, V_{G1} = -60 V				+5	mA
I_{G2T}	Positive-gate trigger current	I_T = 5 A, $t_{p(g)}$ ≥ 20 µs, V_{G2} = 60 V				-5	mA
C_O	Line - Ground off-state capacitance	f = 1 MHz, V_D = -3 V, G1 & G2 open circuit			32		pF

NOTE: 6. Voltage measurements should be made with an oscilloscope with limited bandwidth (20 MHz) to avoid high frequency noise.

Thermal Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	EIA/JESD51-7 PCB, EIA/JESD51-2 Environment, P_{TOT} = 4 W (See Note 7)		55		°C/W

NOTE 7. EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.

Parameter Measurement Information

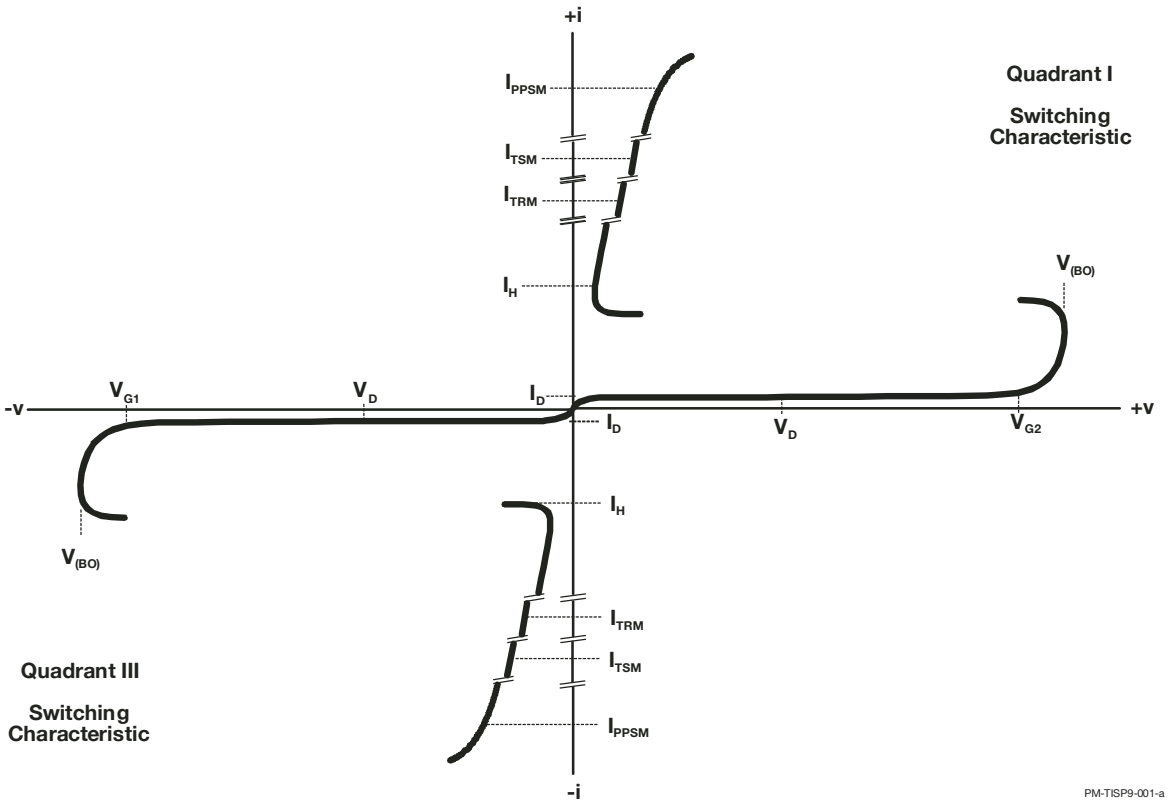


Figure 1. Voltage-Current Characteristic
Unless Otherwise Noted, All Voltages are Referenced to the Ground Terminal

Typical Characteristics

OFF-STATE CAPACITANCE
vs
OFF-STATE VOLTAGE

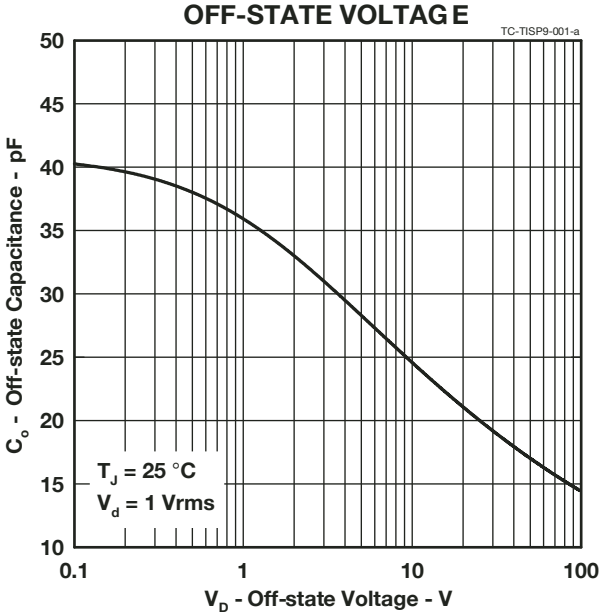


Figure 2.

Thermal Information

NON-REPETITIVE PEAK ON-STATE CURRENT
vs
CURRENT DURATION

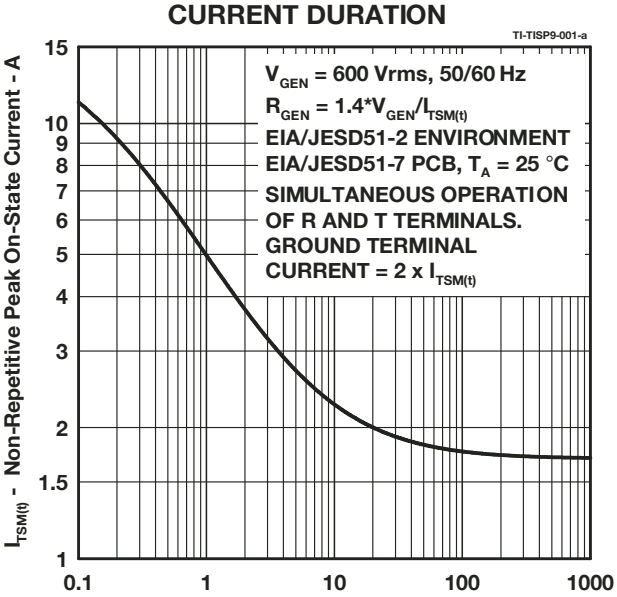


Figure 3.

APPLICATIONS INFORMATION

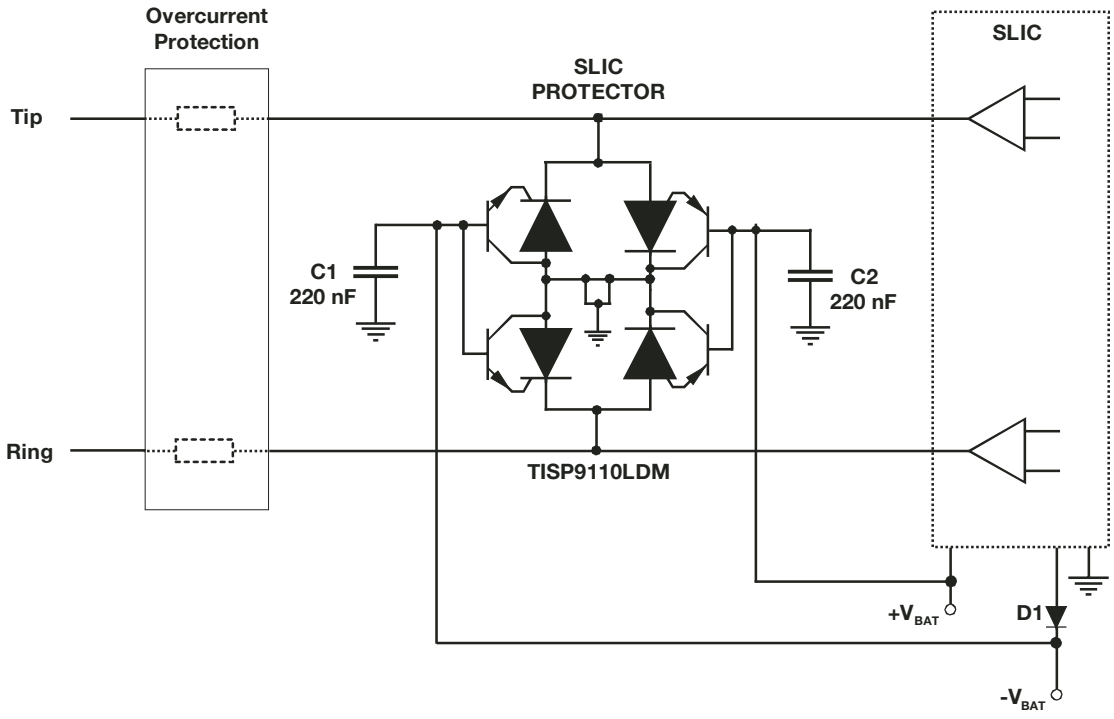


Figure 4. Typical Application Diagram

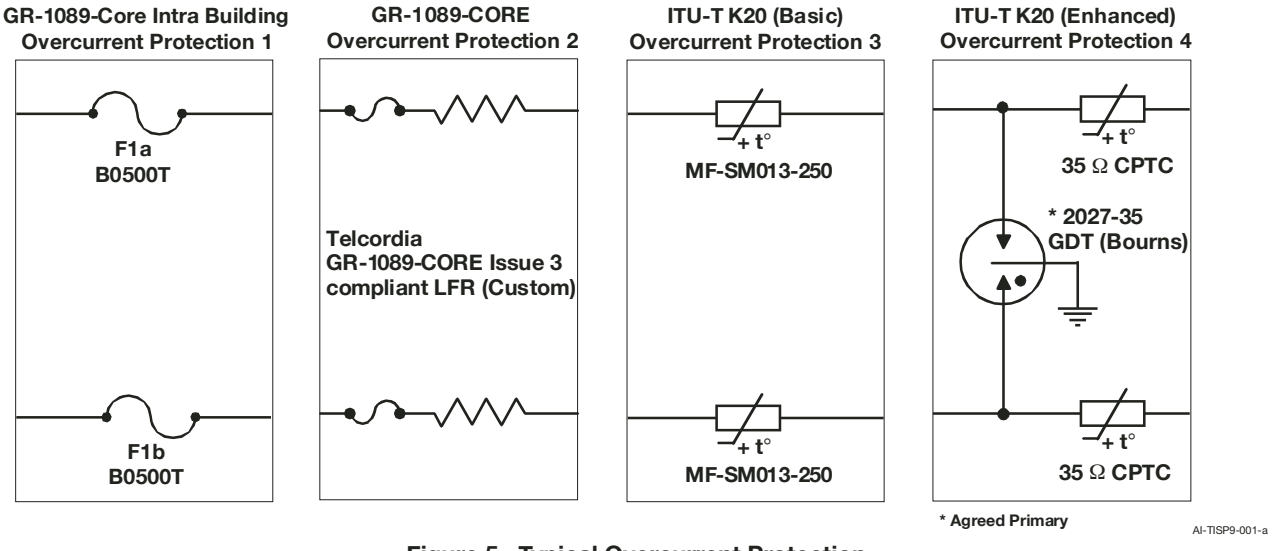


Figure 5. Typical Overcurrent Protection