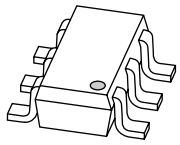


PRTR5V0U2D

Ultra low capacitance double rail-to-rail ESD protection

Rev. 01 — 28 April 2009 Product data sheet

1. Product profile

1.1 General description

Ultra low capacitance double rail-to-rail ElectroStatic Discharge (ESD) protection device in a SOT457 (SC-74) small Surface-Mounted Device (SMD) plastic package.

The device is designed to protect two Hi-Speed data lines or high-frequency signal lines from the damage caused by ESD and other transients.

PRTR5V0U2D integrates two ultra low capacitance rail-to-rail ESD protection channels and one additional ESD protection diode to ensure signal line protection even if no supply voltage is available.

1.2 Features

- ESD protection of two Hi-Speed data lines or high-frequency signal lines
- Ultra low input/output to ground capacitance: $C_{(I/O-GND)}$ = 1 pF
- ESD protection up to 8 kV
- IEC 61000-4-2, level 4 (ESD)
- Very low clamping voltage due to an integrated additional ESD protection diode
- Very low reverse current
- AEC-Q101 qualified (85 °C)
- Small SMD plastic package

1.3 Applications

- USB 2.0 interfaces
- Digital Video Interface (DVI)
- High Definition Multimedia Interface (HDMI)
- Mobile and cordless phones
- Personal Digital Assistants (PDA)
- Digital cameras
- Wide Area Network (WAN) / Local Area Network (LAN) systems
- PCs, notebooks, printers and other PC peripherals

1.4 Quick reference data

Table 1. Quick reference data

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per channel							
$C_{(I/O-GND)}$	input/output to ground capacitance	f = 1 MHz; $V_{(I/O-GND)}$ = 0 V	[1]	-	1.0	1.5	pF
$C_{(I/O-I/O)}$	input/output to input/output capacitance	f = 1 MHz; $V_{(I/O-I/O)}$ = 0 V	[2]	-	0.6	-	pF
Zener diode							
V_{RWM}	reverse standoff voltage		[3]	-	-	5.5	V
C_{sup}	supply pin to ground capacitance	f = 1 MHz; V_{CC} = 0 V	[3]	-	16	-	pF

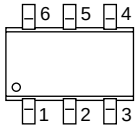
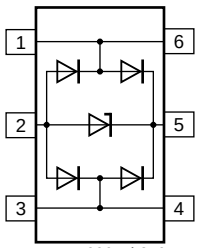
[1] Measured from pin 1, 3, 4 or 6 to ground.

[2] Measured from pin 1 or 6 to pin 3 or 4.

[3] Measured from pin 5 to ground.

2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I/O1	input/output 1		
2	GND	ground		
3	I/O2	input/output 2		
4	I/O2	input/output 2		
5	V_{CC}	supply voltage		
6	I/O1	input/output 1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PRTR5V0U2D	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PRTR5V0U2D	ZB

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per device					
T_{amb}	ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

Table 6. ESD maximum ratings

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
Per channel						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1][2]	-	8	kV
		MIL-STD-883 (human body model)	[2]	-	10	kV

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1, 3, 4 or 6 to pin 2 or 5.

Table 7. ESD standards compliance

Standard	Conditions
Per channel	
IEC 61000-4-2; level 4 (ESD)	> 8 kV (contact)
MIL-STD-883; class 3 (human body model)	> 4 kV

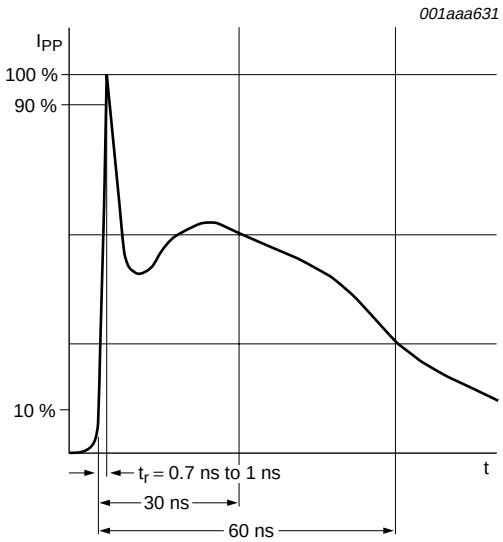


Fig 1. ESD pulse waveform according to IEC 61000-4-2

6. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

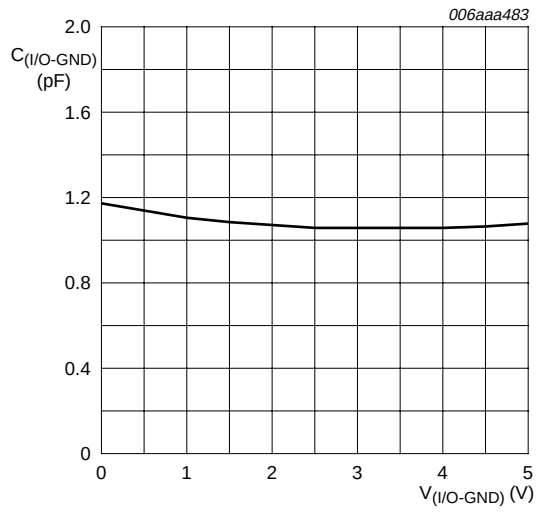
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per channel							
I_R	reverse current	V_R = 5 V	[1]	-	< 1	100	nA
$C_{(I/O-GND)}$	input/output to ground capacitance	f = 1 MHz; $V_{(I/O-GND)}$ = 0 V	[1]	-	1.0	1.5	pF
$C_{(I/O-I/O)}$	input/output to input/output capacitance	f = 1 MHz; $V_{(I/O-I/O)}$ = 0 V	[2]	-	0.6	-	pF
V_F	forward voltage	I_F = 1 mA	[3]	-	0.7	-	V
Zener diode							
V_{RWM}	reverse standoff voltage		[4]	-	-	5.5	V
V_{BR}	breakdown voltage		[4]	6	-	9	V
C_{sup}	supply pin to ground capacitance	f = 1 MHz; V_{CC} = 0 V	[4]	-	16	-	pF

[1] Measured from pin 1, 3, 4 or 6 to ground.

[2] Measured from pin 1 or 6 to pin 3 or 4.

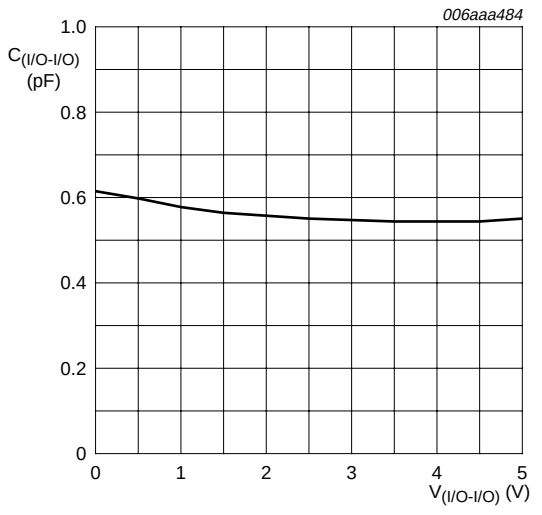
[3] Measured from pin 1, 3, 4 or 6 to pin 5.

[4] Measured from pin 5 to ground.



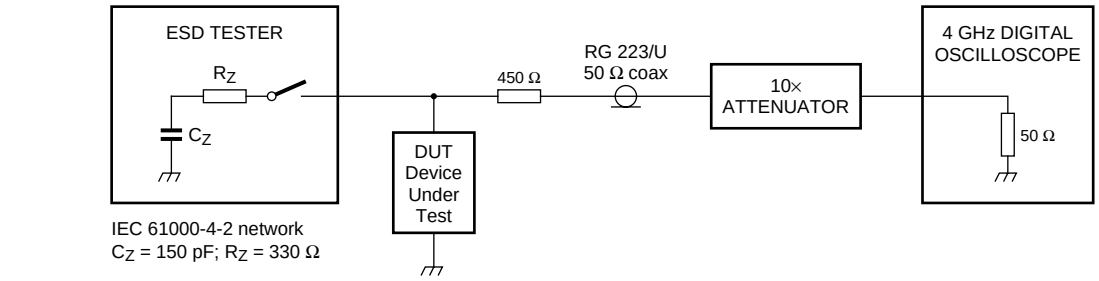
f = 1 MHz; T_{amb} = 25 °C

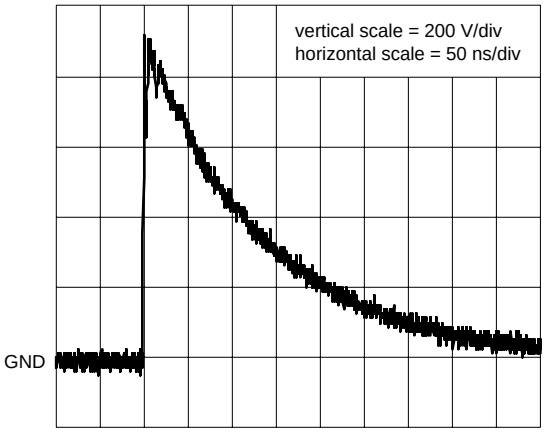
Fig 2. Input/output to ground capacitance as a function of input/output to ground voltage; typical values



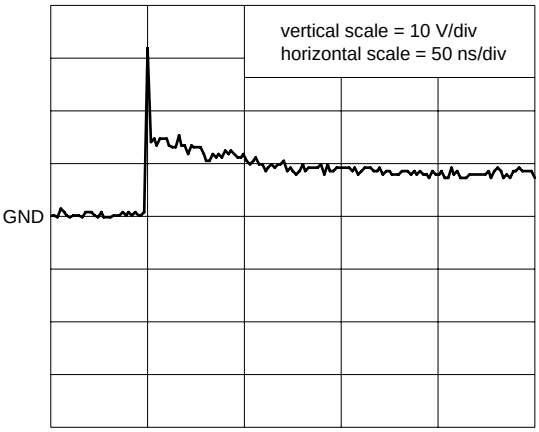
f = 1 MHz; T_{amb} = 25 °C

Fig 3. Input/output to ground capacitance as a function of input/output to input/output voltage; typical values

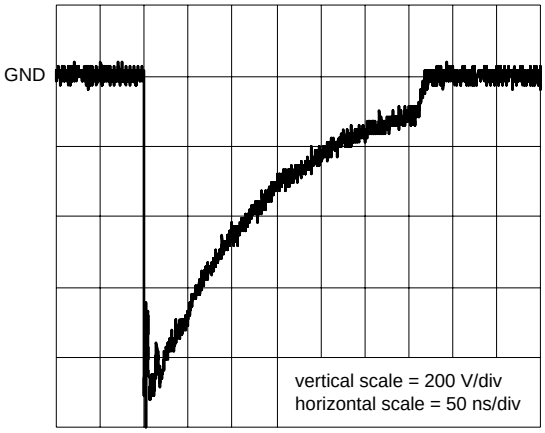




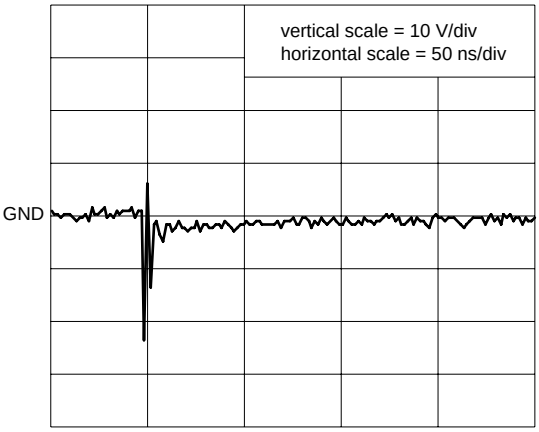
unclamped +1 kV ESD voltage waveform
(IEC 61000-4-2 network)



clamped +1 kV ESD voltage waveform
(IEC 61000-4-2 network)



unclamped −1 kV ESD voltage waveform
(IEC 61000-4-2 network)



clamped −1 kV ESD voltage waveform
(IEC 61000-4-2 network)

006aab112

Fig 4. ESD clamping test setup and waveforms

7. Application information

Handling data rates up to 480 Mbit/s, USB 2.0 interfaces require ESD protection devices with an extremely low line capacitance in order to avoid signal distortion.

With a capacitance of only 1 pF, the PRTR5V0U2D offers IEC 61000-4-2, level 4 compliant ESD protection.

The PRTR5V0U2D integrates two ultra low capacitance rail-to-rail ESD protection channels and one additional ESD protection diode.

The additional ESD protection diode connected between ground and V_{CC} prevents charging of the supply.

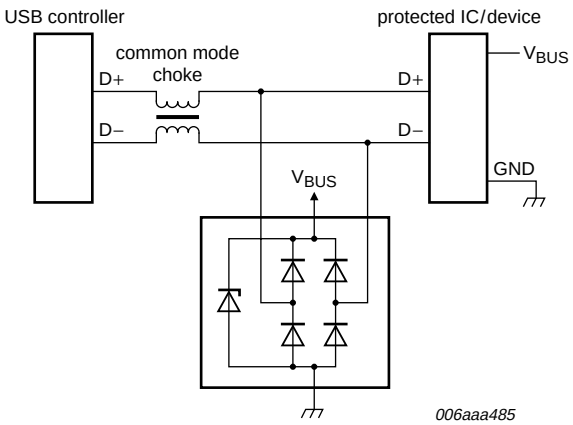


Fig 5. Application diagram: USB 2.0

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the PRTR5V0U2D as close to the input terminal or connector as possible.
2. The path length between the PRTR5V0U2D and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

8. Package outline

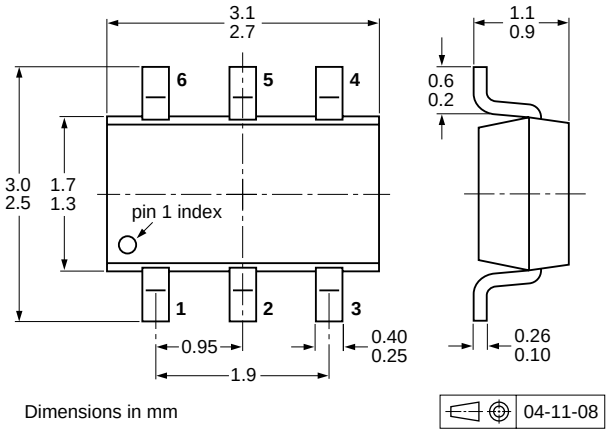


Fig 6. Package outline SOT457 (SC-74)

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description		Packing quantity	
				3000	10000
PRTR5V0U2D	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-165

[1] For further information and the availability of packing methods, see Section 13.

[2] T1: normal taping

[3] T2: reverse taping

10. Soldering

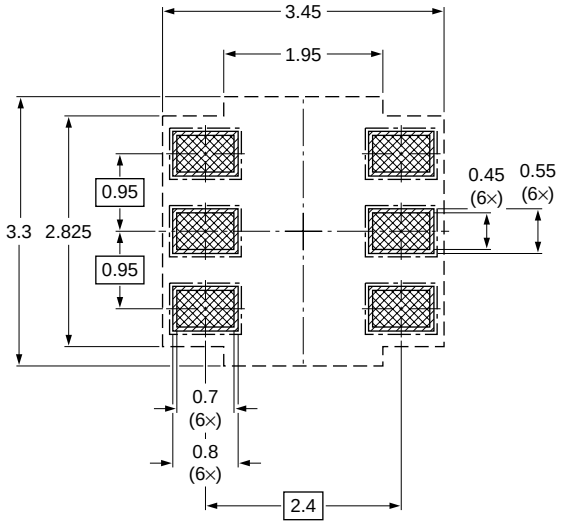


Fig 7. Reflow soldering footprint SOT457 (SC-74)

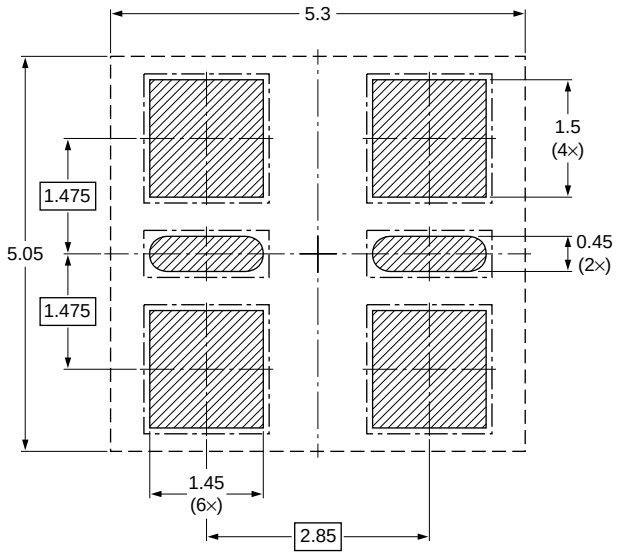


Fig 8. Wave soldering footprint SOT457 (SC-74)

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PRTR5V0U2D_1	20090428	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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