



## K10 Sub-Family Data Sheet

Supports the following:

MK10N512VLK100, MK10N512VMB100

### Features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105°C
- Performance
  - Up to 100 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz
- Memories and memory interfaces
  - Up to 512 KB program flash memory on non-FlexMemory devices
  - Up to 128 KB RAM
  - Serial programming interface (EzPort)
  - FlexBus external bus interface
- Clocks
  - 1 to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator
- System peripherals
  - 10 low-power modes to provide power optimization based on application requirements
  - Memory protection unit with multi-master protection
  - 16-channel DMA controller, supporting up to 64 request sources
  - External watchdog monitor
  - Software watchdog
  - Low-leakage wakeup unit
- Security and integrity modules
  - Hardware CRC module to support fast cyclic redundancy checks
  - Hardware random-number generator
  - 128-bit unique identification (ID) number per chip
- Human-machine interface
  - Low-power hardware touch sensor interface (TSI)
  - General-purpose input/output
- Analog modules
  - 16-bit SAR ADC with PGA (x64)
  - 12-bit DAC
  - Analog comparator (CMP) containing a 6-bit DAC and programmable reference input
  - Voltage reference
- Timers
  - Programmable delay block
  - Eight-channel motor control/general purpose/PWM timers
  - Two-channel quadrature decoder/general purpose timers
  - Periodic interrupt timers
  - 16-bit low-power timer
  - Carrier modulator transmitter
  - Real-time clock
- Communication interfaces
  - Controller Area Network (CAN) module
  - SPI modules
  - I2C modules
  - UART modules
  - Secure Digital host controller (SDHC)
  - I2S



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Preliminary

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Preliminary

# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [www.freescale.com](http://www.freescale.com) and perform a part number search for the following device numbers: PK10 and MK10.

## 2 Part identification

### 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

### 2.2 Format

Part numbers for this device have the following format:

Q K## M FFF T PP CCC N

### 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
K##	Kinetis family	<ul style="list-style-type: none"> <li>K10</li> </ul>
M	Flash memory type	<ul style="list-style-type: none"> <li>N = Program flash only</li> <li>X = Program flash and FlexMemory</li> </ul>

*Table continues on the next page...*

Field	Description	Values
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>• 32 = 32 KB</li> <li>• 64 = 64 KB</li> <li>• 128 = 128 KB</li> <li>• 256 = 256 KB</li> <li>• 512 = 512 KB</li> <li>• 1M0 = 1 MB</li> </ul>
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>• V = -40 to 105</li> </ul>
PP	Package identifier	<ul style="list-style-type: none"> <li>• FM = 32 QFN (5 mm x 5 mm)</li> <li>• FT = 48 QFN (7 mm x 7 mm)</li> <li>• LF = 48 LQFP (7 mm x 7 mm)</li> <li>• FX = 64 QFN (9 mm x 9 mm)</li> <li>• LH = 64 LQFP (10 mm x 10 mm)</li> <li>• LK = 80 LQFP (12 mm x 12 mm)</li> <li>• MB = 81 MAPBGA (8 mm x 8 mm)</li> <li>• LL = 100 LQFP (14 mm x 14 mm)</li> <li>• ML = 104 MAPBGA (8 mm x 8 mm)</li> <li>• LQ = 144 LQFP (20 mm x 20 mm)</li> <li>• MD = 144 MAPBGA (13 mm x 13 mm)</li> <li>• MF = 196 MAPBGA (15 mm x 15 mm)</li> <li>• MJ = 256 MAPBGA (17 mm x 17 mm)</li> </ul>
CCC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> <li>• 50 = 50 MHz</li> <li>• 72 = 72 MHz</li> <li>• 100 = 100 MHz</li> <li>• 120 = 120 MHz</li> <li>• 150 = 150 MHz</li> </ul>
N	Packaging type	<ul style="list-style-type: none"> <li>• R = Tape and reel</li> <li>• (Blank) = Trays</li> </ul>

## 2.4 Example

This is an example part number:

MK10N512VMD100

## 3 Terminology and guidelines

### 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

### 3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	0.9	1.1	V

### 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

#### 3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/pulldown current	10	130	μA

### 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

#### 3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

### 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

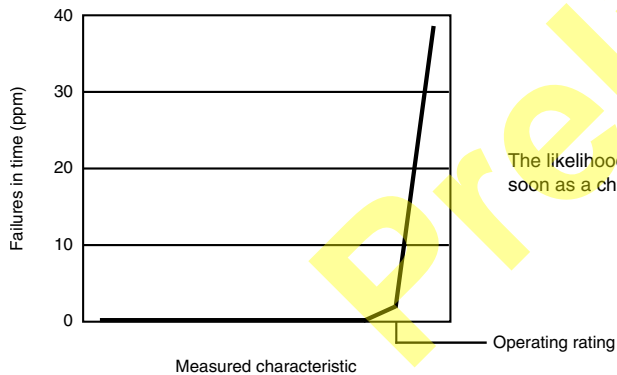
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

#### 3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	-0.3	1.2	V

### 3.5 Result of exceeding a rating



### 3.6 Relationship between ratings and operating requirements

Operating or handling rating (min.)		Operating requirement (min.)		Operating requirement (max.)		Operating or handling rating (max.)	
<b>Fatal range</b>  - Probable permanent failure	<b>Limited operating range</b>  - No permanent failure - Possible decreased life - Possible incorrect operation	<b>Normal operating range</b>  - No permanent failure - Correct operation	<b>Limited operating range</b>  - No permanent failure - Possible decreased life - Possible incorrect operation	<b>Fatal range</b>  - Probable permanent failure			
<b>Handling range</b> - No permanent failure							

### 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

### 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

#### 3.8.1 Example 1

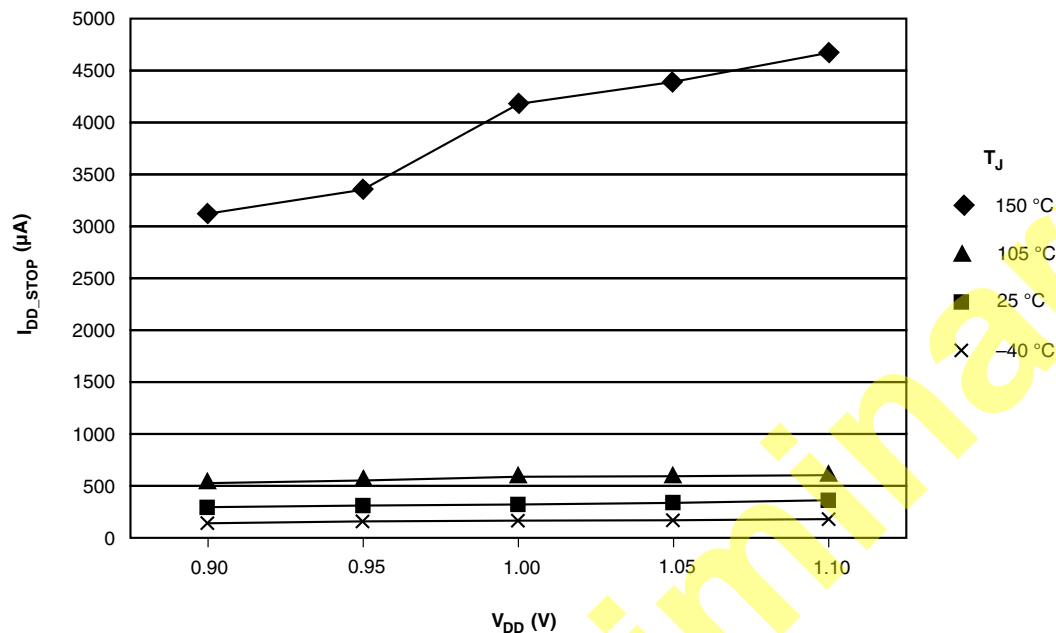
This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/pulldown current	10	70	130	μA



### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



### 3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
$T_A$	Ambient temperature	25	$^{\circ}C$
$V_{DD}$	3.3 V supply voltage	3.3	V

## 4 Ratings

## 4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 85°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

## 4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	Digital supply voltage	-0.3	3.8	V
I <sub>DD</sub>	Digital supply current	—	185	mA
V <sub>DIO</sub>	Digital input voltage (except $\overline{\text{RESET}}$ , EXTAL, and XTAL)	-0.3	5.5	V
V <sub>AIO</sub>	Analog, $\overline{\text{RESET}}$ , EXTAL, and XTAL input voltage	-0.3	V <sub>DD</sub> + 0.3	V

Table continues on the next page...

Symbol	Description	Min.	Max.	Unit
$I_D$	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
$I_{DDA}$	Analog supply current <sup>1</sup>	TBD	TBD	mA
$V_{BAT}$	RTC battery supply voltage	-0.3	3.8	V
$V_{RAM}$	$V_{DD}$ voltage required to retain RAM	1.2	—	V
$V_{RFVBAT}$	$V_{BAT}$ voltage required to retain the VBAT register file	TBD	—	V

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.

## 5 General

### 5.1 Nonswitching electrical specifications

#### 5.1.1 Voltage and Current Operating Requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	3.6	V	
$V_{DDA}$	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	$V_{DD}$ -to- $V_{DDA}$ differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	$V_{SS}$ -to- $V_{SSA}$ differential voltage	-0.1	0.1	V	
$V_{IH}$	Input high voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
$V_{IL}$	Input low voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	
$V_{HYS}$	Input hysteresis	$0.06 \times V_{DD}$	—	V	

Table continues on the next page...

**Table 1. Voltage and current operating requirements (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
$I_{IC}$	DC injection current — single pin				1
	<ul style="list-style-type: none"> <li><math>V_{IN} &gt; V_{DD}</math></li> <li><math>V_{IN} &lt; V_{SS}</math></li> </ul>	0	2	mA	
		0	-0.2	mA	
	DC injection current — total MCU limit, includes sum of all stressed pins				1
	<ul style="list-style-type: none"> <li><math>V_{IN} &gt; V_{DD}</math></li> <li><math>V_{IN} &lt; V_{SS}</math></li> </ul>	0	25	mA	
		0	-5	mA	

1. All functional non-supply pins are internally clamped to VSS and VDD. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values. Power supply must maintain regulation within operating VDD range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{IN} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of VDD and could result in external power supply going out of regulation. Ensure external VDD load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

## 5.1.2 LVD and POR operating requirements

**Table 2. LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{POR}$	Falling VDD POR detect voltage	TBD	1.1	TBD	V	
$V_{LVDH}$	Falling low-voltage detect threshold — high range (LVDV=01)	TBD	2.56	TBD	V	
	Low-voltage warning thresholds — high range					1
$V_{LVW1}$	<ul style="list-style-type: none"> <li>Level 1 falling (LVWV=00)</li> </ul>	TBD	2.70	TBD	V	
$V_{LVW2}$	<ul style="list-style-type: none"> <li>Level 2 falling (LVWV=01)</li> </ul>	TBD	2.80	TBD	V	
$V_{LVW3}$	<ul style="list-style-type: none"> <li>Level 3 falling (LVWV=10)</li> </ul>	TBD	2.90	TBD	V	
$V_{LVW4}$	<ul style="list-style-type: none"> <li>Level 4 falling (LVWV=11)</li> </ul>	TBD	3.00	TBD	V	
$V_{HYS}$	Low-voltage inhibit reset/recover hysteresis — high range		60		mV	
$V_{LVDL}$	Falling low-voltage detect threshold — low range (LVDV=00)	TBD	TBD	TBD	V	
	Low-voltage warning thresholds — low range					1
$V_{LVW1}$	<ul style="list-style-type: none"> <li>Level 1 falling (LVWV=00)</li> </ul>	TBD	1.80	TBD	V	
$V_{LVW2}$	<ul style="list-style-type: none"> <li>Level 2 falling (LVWV=01)</li> </ul>	TBD	1.90	TBD	V	
$V_{LVW3}$	<ul style="list-style-type: none"> <li>Level 3 falling (LVWV=10)</li> </ul>	TBD	2.00	TBD	V	
$V_{LVW4}$	<ul style="list-style-type: none"> <li>Level 4 falling (LVWV=11)</li> </ul>	TBD	2.10	TBD	V	

Table continues on the next page...

**Table 2. LVD and POR operating requirements (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{HYS}$	Low-voltage inhibit reset/recover hysteresis — low range		40		mV	
$V_{BG}$	Bandgap voltage reference	TBD	1.00	TBD	V	
$t_{LPO}$	Internal low power oscillator period factory trimmed	TBD	1000	TBD	$\mu$ s	

1. Rising thresholds are falling threshold +  $V_{HYS}$

### 5.1.3 Voltage and current operating behaviors

**Table 3. Voltage and current operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{OH}$	Output high voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OH} = -10\text{mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OH} = -3\text{mA}$	$V_{DD} - 0.5$	—	V	
	Output high voltage — low drive strength				
• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OH} = -2\text{mA}$	$V_{DD} - 0.5$	—	V		
• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OH} = -0.6\text{mA}$	$V_{DD} - 0.5$	—	V		
$I_{OHT}$	Output high current total for all ports	—	100	mA	
$V_{OL}$	Output low voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OL} = 10\text{mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OL} = 3\text{mA}$	—	0.5	V	
	Output low voltage — low drive strength				
• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , $I_{OL} = 2\text{mA}$	—	0.5	V		
• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ , $I_{OL} = 0.6\text{mA}$	—	0.5	V		
$I_{OLT}$	Output low current total for all ports	—	100	mA	
$I_{IN}$	Input leakage current (per pin)	—	1	$\mu$ A	
$I_{OZ}$	Hi-Z (off-state) leakage current (per pin)	—	1	$\mu$ A	
$R_{PU}$ and $R_{PD}$	Internal weak pullup and pulldown resistors	30	50	k $\Omega$	1

1. Measured at  $V_{IL}$  max and  $V_{DD}$  min

## 5.1.4 Power mode transition operating behaviors

In the table below, all specifications except  $t_{POR}$ , assume the following clock configuration:

- CPU and system clocks = 100MHz
- Bus and FlexBus clocks = 50 MHz
- Flash clock = 25 MHz

**Table 4. Power mode transition operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$t_{POR}$	After a POR event, amount of time from the point $V_{DD}$ reaches 1.8V to execution of the first instruction across the operating temperature range of the chip.	—	300	$\mu s$	1
	RUN → VLLS1 → RUN				
	• RUN → VLLS1	—	4.1	$\mu s$	
	• VLLS1 → RUN	—	123.8	$\mu s$	
	RUN → VLLS2 → RUN				
	• RUN → VLLS2	—	4.1	$\mu s$	
	• VLLS2 → RUN	—	49.3	$\mu s$	
	RUN → VLLS3 → RUN				
	• RUN → VLLS3	—	4.1	$\mu s$	
	• VLLS3 → RUN	—	49.2	$\mu s$	
	RUN → LLS → RUN				
	• RUN → LLS	—	4.1	$\mu s$	
	• LLS → RUN	—	5.9	$\mu s$	
	RUN → STOP → RUN				
	• RUN → STOP	—	4.1	$\mu s$	
	• STOP → RUN	—	4.2	$\mu s$	
	RUN → VLPS → RUN				
	• RUN → VLPS	—	4.1	$\mu s$	
	• VLPS → RUN	—	5.8	$\mu s$	

1. Normal boot (FTFL\_OPT[LPBOOT]=1)

## 5.1.5 Power consumption operating behaviors

**Table 5. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DD\_RUN}$	Run mode current — all peripheral clocks disabled, code executing from flash <ul style="list-style-type: none"> <li>@ 1.8V</li> <li>@ 3.0V</li> </ul>	— —	40 42	TBD TBD	mA mA	1
$I_{DD\_RUN}$	Run mode current — all peripheral clocks enabled, code executing from flash <ul style="list-style-type: none"> <li>@ 1.8V</li> <li>@ 3.0V</li> </ul>	— —	55 56	TBD TBD	mA mA	2
$I_{DD\_RUN\_MAX}$	Run mode current — all peripheral clocks enabled and peripherals active, code executing from flash <ul style="list-style-type: none"> <li>@ 1.8V</li> <li>@ 3.0V</li> </ul>	— —	85 85	TBD TBD	mA mA	3
$I_{DD\_WAIT}$	Wait mode current at 3.0 V — all peripheral clocks disabled	—	15	TBD	mA	4
$I_{DD\_STOP}$	Stop mode current at 3.0 V	—	1.4	TBD	mA	
$I_{DD\_VLPR}$	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.25	TBD	mA	5
$I_{DD\_VLPR}$	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	TBD	TBD	mA	6
$I_{DD\_VLPW}$	Very-low-power wait mode current at 3.0 V	—	1.05	TBD	mA	7
$I_{DD\_VLPS}$	Very-low-power stop mode current at 3.0 V	—	30	TBD	$\mu$ A	
$I_{DD\_LLS}$	Low leakage stop mode current at 3.0 V	—	12	TBD	$\mu$ A	
$I_{DD\_VLLS3}$	Very low-leakage stop mode 3 current at 3.0 V <ul style="list-style-type: none"> <li>128KB RAM devices</li> </ul>	—	8	TBD	$\mu$ A	
$I_{DD\_VLLS2}$	Very low-leakage stop mode 2 current at 3.0 V	—	4	TBD	$\mu$ A	
$I_{DD\_VLLS1}$	Very low-leakage stop mode 1 current at 3.0 V	—	2	TBD	$\mu$ A	
$I_{DD\_VBAT}$	Average current when CPU is not accessing RTC registers at 3.0 V	—	550	TBD	nA	

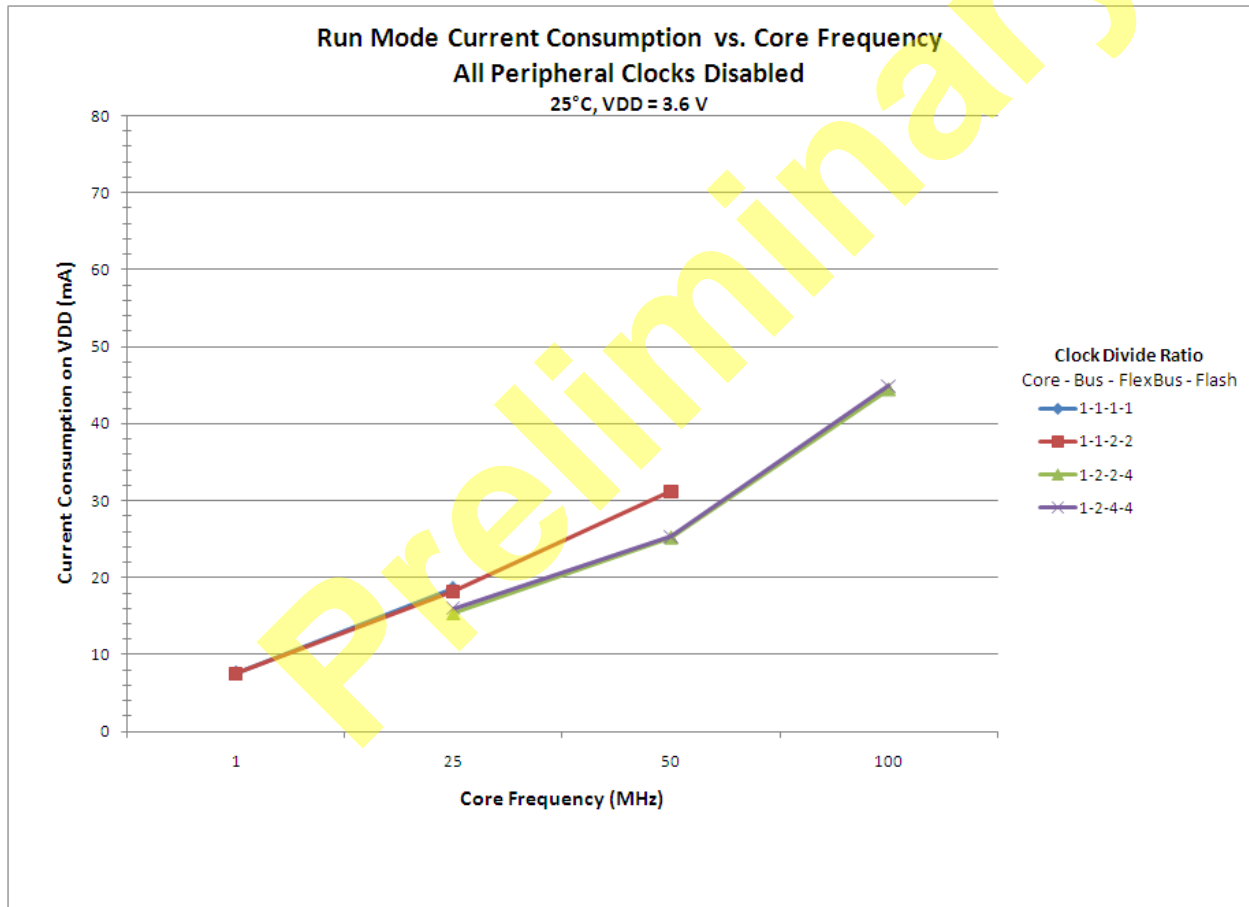
- 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
- 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, but peripherals are not in active operation.
- 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
- 25MHz core and system clock, 25MHz bus clock, and 12.5MHz FlexBus and flash clock. MCG configured for FEI mode.
- 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for fast IRCLK mode. All peripheral clocks disabled. Code executing from flash.
- 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for fast IRCLK mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.

- 7. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for fast IRCLK mode. All peripheral clocks disabled.

### 5.1.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG in FEI mode (39.0625 kHz IRC), except for 1 MHz core (FBE)
- All peripheral clocks disabled except FTFL
- LVD disabled
- No GPIOs toggled
- Code execution from flash



**Figure 1. Run mode supply current vs. core frequency — all peripheral clocks disabled**

The following data was measured under these conditions:

- MCG in FEI mode (39.0625 kHz IRC), except for 1 MHz core (FBE)
- All peripheral clocks enabled but peripherals are not in active operation
- LVD disabled
- No GPIOs toggled
- Code execution from flash



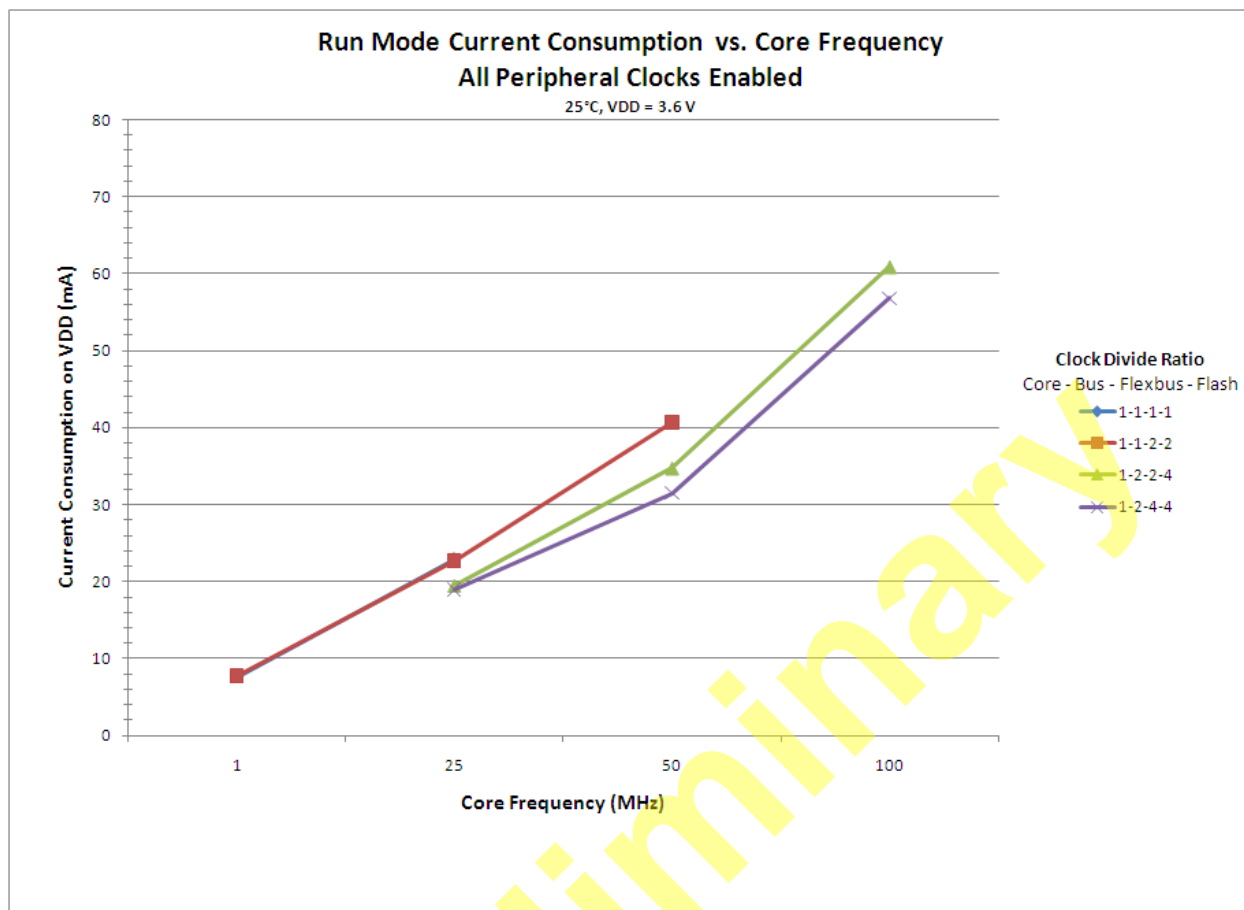


Figure 2. Run mode supply current vs. core frequency — all peripheral clocks enabled

## 5.1.6 EMC radiated emissions operating behaviors

Table 6. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	TBD	dBμV	1, 2
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	TBD		
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	TBD		
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	TBD		
V <sub>RE_IEC_SAE</sub>	IEC and SAE level	0.15–1000	TBD	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions*, IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*, and SAE Standard J1752-3, *Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method*.
2. V<sub>DD</sub> = 3 V, T<sub>A</sub> = 25 °C, f<sub>OSC</sub> = 16 MHz (crystal), f<sub>BUS</sub> = 20 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*, and Appendix D of SAE Standard J1752-3, *Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method*.

### 5.1.7 Designing with radiated emissions in mind

1. To find application notes that provide guidance on designing your system to minimize interference from radiated emissions, go to [www.freescale.com](http://www.freescale.com) and perform a keyword search for “EMC design.”

### 5.1.8 Capacitance attributes

Table 7. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
$C_{IN\_A}$	Input capacitance: analog pins	—	7	pF
$C_{IN\_D}$	Input capacitance: digital pins	—	7	pF

## 5.2 Switching electrical specifications

Table 8. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
$f_{SYS}$	System and core clock	—	100	MHz	
$f_{BUS}$	Bus clock	—	50	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
$f_{FLASH}$	Flash clock	—	25	MHz	
VLPR mode					
$f_{SYS}$	System and core clock	—	2	MHz	
$f_{BUS}$	Bus clock	—	2	MHz	
FB_CLK	FlexBus clock	—	2	MHz	
$f_{FLASH}$	Flash clock	—	1	MHz	

## 5.3 Thermal specifications

### 5.3.1 Thermal operating requirements

Table 9. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
$T_J$	Die junction temperature	-40	125	°C
$T_A$	Ambient temperature	-40	105	°C

### 5.3.2 Thermal attributes

Board type	Symbol	Description	81 MAPBGA	80 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	TBD	TBD	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	TBD	TBD	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	TBD	TBD	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	TBD	TBD	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	TBD	TBD	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	TBD	TBD	°C/W	3
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	TBD	TBD	°C/W	4

## 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

## 6.1.1 Debug trace timing specifications

Table 10. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
$T_{cyc}$	Clock period	Frequency dependent		MHz
$T_{wl}$	Low pulse width	2	—	ns
$T_{wh}$	High pulse width	2	—	ns
$T_r$	Clock and data rise time	—	3	ns
$T_f$	Clock and data fall time	—	3	ns
$T_s$	Data setup	3	—	ns
$T_h$	Data hold	2	—	ns

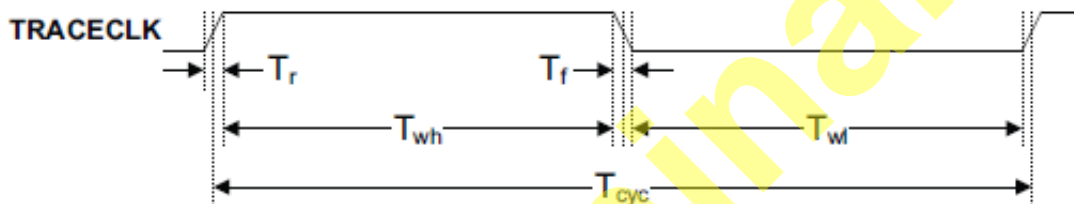


Figure 3. TRACE\_CLKOUT specifications

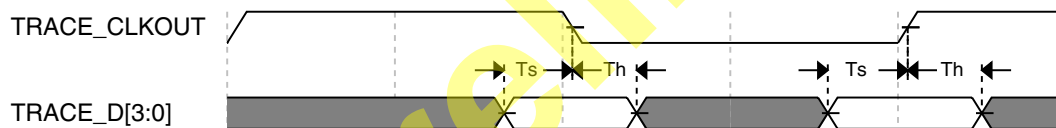


Figure 4. Trace data specifications

## 6.1.2 JTAG electricals

Table 11. JTAG electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>JTAG and CJTAG</li> <li>Serial Wire Debug</li> </ul>	0	25	MHz
J2	TCLK cycle period	1/J1	—	ns

Table continues on the next page...

Table 11. JTAG electricals (continued)

Symbol	Description	Min.	Max.	Unit
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	20 10	— —	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	30	ns
J8	TCLK low to boundary scan output high-Z	—	30	ns
J9	TMS, TDI input data setup time to TCLK rise	16	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	4	ns
J12	TCLK low to TDO high-Z	—	4	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

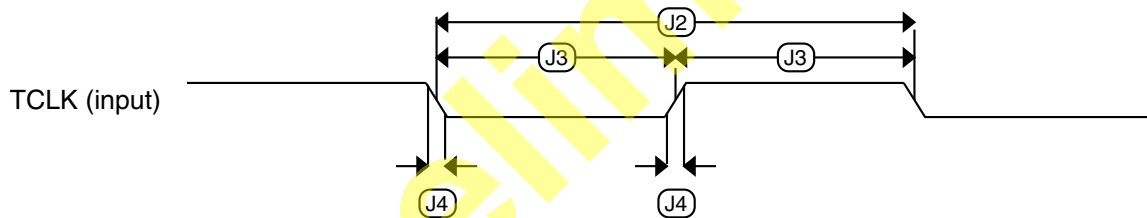


Figure 5. Test clock input timing

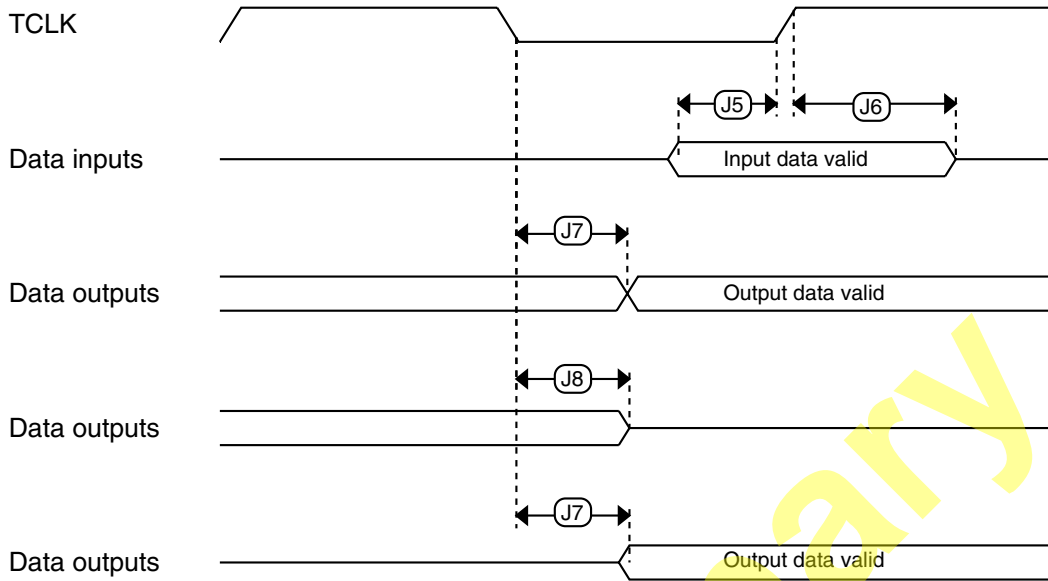


Figure 6. Boundary scan (JTAG) timing

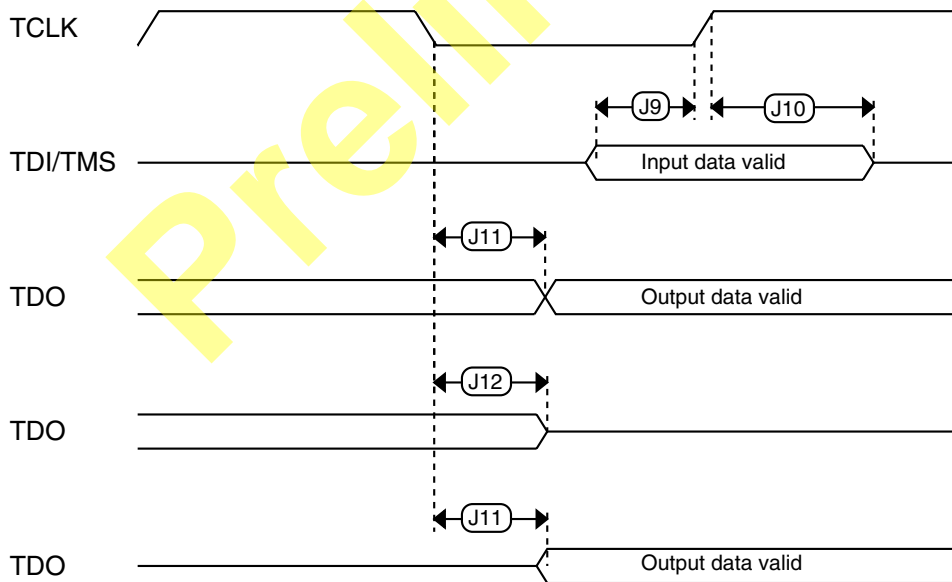


Figure 7. Test Access Port timing

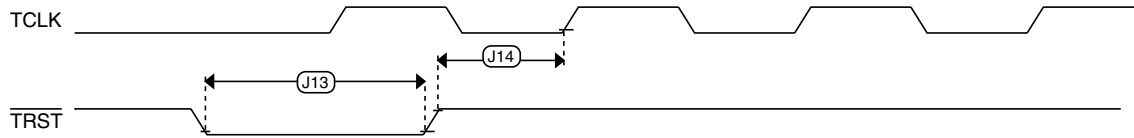


Figure 8. TRST timing

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

### 6.3.1 MCG Specifications

Table 12. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ints\_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25°C	—	32.768	—	kHz	
$f_{\text{ints\_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$t_{\text{refsts}}$	Internal reference (slow clock) startup time	—	TBD	4	μs	
$\Delta f_{\text{dco\_res\_t}}$	Resolution of trimmed DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.1	± 0.3	% $f_{\text{dco}}$	
$\Delta f_{\text{dco\_res\_t}}$	Resolution of trimmed DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	% $f_{\text{dco}}$	
$\Delta f_{\text{dco\_t}}$	Total deviation of trimmed DCO output frequency over voltage and temperature	—	+ 0.5 - 1.0	± 3.5	% $f_{\text{dco}}$	
$\Delta f_{\text{dco\_t}}$	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.5	± TBD	% $f_{\text{dco}}$	
$f_{\text{intf\_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	3.875	4	4.125	MHz	
$f_{\text{intf\_t}}$	Internal reference frequency (fast clock) — user trimmed	3	—	5	MHz	

Table continues on the next page...

Table 12. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$t_{\text{refstf}}$	Internal reference startup time (fast clock)	—	TBD	TBD	$\mu\text{s}$		
$f_{\text{loc\_low}}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{\text{ints\_t}}$	—	—	kHz		
$f_{\text{loc\_high}}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{\text{ints\_t}}$	—	—	kHz		
FLL							
$f_{\text{dco\_t}}$	DCO output frequency range — user trimmed and DMX32=0	Low range (DRS=00) $640 \times f_{\text{ints\_t}}$	20	20.97	25	MHz	1, 2
		Mid range (DRS=01) $1280 \times f_{\text{ints\_t}}$	40	41.94	50	MHz	
		Mid-high range (DRS=10) $1920 \times f_{\text{ints\_t}}$	60	62.91	75	MHz	
		High range (DRS=11) $2560 \times f_{\text{ints\_t}}$	80	83.89	100	MHz	
$f_{\text{dco\_t\_DMX32}}^2$	DCO output frequency range — reference = 32,768Hz and DMX32=1	Low range (DRS=00) $732 \times f_{\text{ints\_t}}$	—	23.99	—	MHz	3
		Mid range (DRS=01) $1464 \times f_{\text{ints\_t}}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{\text{ints\_t}}$	—	71.99	—	MHz	
		High range (DRS=11) $2929 \times f_{\text{ints\_t}}$	—	95.98	—	MHz	
$J_{\text{cyc\_fll}}$	FLL period jitter	—	TBD	TBD	ps	4	
$J_{\text{acc\_fll}}$	FLL accumulated jitter of DCO output over a 1 $\mu\text{s}$ time window	—	TBD	TBD	ps		
$t_{\text{fll\_acquire}}$	FLL target frequency acquisition time	—	—	1	ms	5	
PLL							
$f_{\text{vco}}$	VCO operating frequency	48.0	—	100	MHz		
$f_{\text{pll\_ref}}$	PLL reference frequency range	2.0	—	4.0	MHz		
$J_{\text{cyc\_pll}}$	PLL period jitter	—	400	—	ps	6, 7	
$J_{\text{acc\_pll}}$	PLL accumulated jitter over 1 $\mu\text{s}$ window	—	TBD	—	ps	6, 7	
$D_{\text{lock}}$	Lock entry frequency tolerance	$\pm 1.49$	—	$\pm 2.98$	%		
$D_{\text{unl}}$	Lock exit frequency tolerance	$\pm 4.47$	—	$\pm 5.97$	%		
$t_{\text{pll\_lock}}$	Lock detector detection time	—	—	$0.15 + 1075(1/f_{\text{pll\_ref}})$	ms	8	

1. The resulting system clock frequencies should not exceed their maximum specified values.



2. This specification includes the 2% precision of the internal reference frequency (slow clock).
3. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
4. This specification was obtained at TBD frequency.
5. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
6. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
7. This specification was obtained at internal frequency of TBD.
8. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator Electrical Characteristics

This section provides the electrical characteristics of the module.

### 6.3.2.1 Oscillator DC Electrical Specifications

**Table 13. Oscillator DC electrical specifications, ( $V_{SSOSC} = 0 V_{DC}$ ) ( $T_A = T_L$  to  $T_H$ )**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DD33OSC}$	3.3 V supply voltage	1.71	—	3.6	V	
$I_{DDOSC}$	Supply current — low-power mode <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 1 MHz</li> <li>• 4 MHz</li> <li>• 8 MHz</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	500	—	nA	1
		—	100	—	$\mu$ A	
		—	200	—	$\mu$ A	
		—	300	—	$\mu$ A	
		—	700	—	$\mu$ A	
		—	1.2	—	mA	
		—	1.5	—	mA	
$I_{DDOSC}$	Supply current — high gain mode <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 1 MHz</li> <li>• 4 MHz</li> <li>• 8 MHz</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	25	—	$\mu$ A	1
		—	200	—	$\mu$ A	
		—	400	—	$\mu$ A	
		—	800	—	$\mu$ A	
		—	1.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
$C_x$	EXTAL load capacitance	—	—	—		2, 3
$C_y$	XTAL load capacitance	—	—	—		2, 3

Table continues on the next page...

**Table 13. Oscillator DC electrical specifications, ( $V_{SSOSC} = 0 V_{DC}$ ) ( $T_A = T_L$  to  $T_H$ ) (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$R_F$	Feedback resistor — low-frequency, low-power mode	—	—	—	M $\Omega$	2, 3
	Feedback resistor — low-frequency, high-gain mode	—	10	—	M $\Omega$	
	Feedback resistor — high-frequency, low-power mode (1 – 8 MHz, 8 – 32 MHz)	—	—	—	M $\Omega$	
	Feedback resistor — high-frequency, high-gain mode (1 – 8 MHz, 8 – 32 MHz)	—	1	—	M $\Omega$	
$R_S$	Series resistor — low-frequency, low-power mode	—	—	—	k $\Omega$	
	Series resistor — low-frequency, high-gain mode	—	200	—	k $\Omega$	
	Series resistor — high-frequency, low-power mode	—	—	—	k $\Omega$	
	Series resistor — high-frequency, high-gain mode					
	• 1 MHz resonator	—	6.6	—	k $\Omega$	
	• 2 MHz resonator	—	3.3	—	k $\Omega$	
	• 4 MHz resonator	—	0	—	k $\Omega$	
	• 8 MHz resonator	—	0	—	k $\Omega$	
• 16 MHz resonator	—	0	—	k $\Omega$		
• 20 MHz resonator	—	0	—	k $\Omega$		
• 32 MHz resonator	—	0	—	k $\Omega$		
$V_{pp}$	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode	$0.75 \times V_{DD33OSC}$	$V_{DD33OSC}$	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode	$0.75 \times V_{DD33OSC}$	$V_{DD33OSC}$	—	V	

- $V_{DD33OSC} = 3.3$  V, Temperature = 27 °C,  $C_x/C_y = 20$  pF
- See crystal or resonator manufacturer's recommendation
- $R_F$  and  $C_x, C_y$  are integrated in low-frequency, low-power mode and must not be attached externally

### 6.3.2.2 Oscillator frequency specifications

**Table 14. Oscillator frequency specifications, ( $V_{DD33OSC} = V_{DD33OSC}(\min)$  to  $V_{DD33OSC}(\max)$ ,  $T_A = T_L$  to  $T_H$ )**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal or resonator frequency — low frequency mode	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range)	1	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range)	8	—	32	MHz	
$t_{dc\_extal}$	Input clock duty cycle (external clock mode)	40	50	60	%	
$t_{cst}$	Crystal start-up time — 32 kHz low-frequency, low-power mode	—	TBD	—	ms	1, 2, 3
	Crystal start-up time — 32 kHz low-frequency, high-gain mode	—	800	—	ms	
	Crystal start-up time — 8 MHz high-frequency, low-power mode	—	4	—	ms	
	Crystal start-up time — 8 MHz high-frequency, high-gain mode	—	3	—	ms	

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.
3. Crystal start up time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG\_S register being set.

### 6.3.3 32kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

#### 6.3.3.1 32kHz Oscillator DC Electrical Specifications

**Table 15. 32kHz Oscillator Module DC Electrical Specifications ( $V_{SSOSC} = 0 V_{DC}$ ) ( $T_A = T_L$  to  $T_H$ )**

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{BAT}$	Supply voltage	1.71	—	3.6	V
$R_F$	Internal feedback resistor	—	100	—	M $\Omega$
$C_{para}$	Parasitical capacitance of EXTAL32 and XTAL32	—	2.5	—	pF
$C_{load}$	Internal load capacitance (programmable)	—	15	—	pF
$V_{pp}$	Peak-to-peak amplitude of oscillation	—	0.6	—	V

### 6.3.3.2 32kHz Oscillator Frequency Specifications

**Table 16. 32kHz oscillator frequency specifications ( $V_{DD33OSC} = V_{DD33OSC}(\min)$  to  $V_{DD33OSC}(\max)$ ,  $T_A = T_L$  to  $T_H$ )**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal	—	32	—	kHz	
$t_{start}$	Crystal start-up time	—	1000	—	ms	1, 2

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

## 6.4 Memories and memory interfaces

### 6.4.1 Flash (FTFL) Electrical Characteristics

This section describes the electrical characteristics of the FTFL module.

#### 6.4.1.1 Flash Timing Parameters — Program and Erase

The following characteristics represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 17. NVM program/erase timing characteristics**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvpgm4}$	Longword Program high-voltage time	—	20	TBD	$\mu$ s	
$t_{hversscr}$	Sector Erase high-voltage time	—	20	100	ms	1
$t_{hversblk}$	Erase Block high-voltage time	—	160	800	ms	1

1. Maximum time based on expectations at cycling end-of-life.

#### 6.4.1.2 Flash Timing Parameters — Commands

**Table 18. Flash command timing characteristics**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk}$	Read 1s Block execution time	—	—	1.4	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (2 KB flash sector)	—	—	40	$\mu$ s	
$t_{pgmchk}$	Program Check execution time	—	—	35	$\mu$ s	

Table continues on the next page...

**Table 18. Flash command timing characteristics (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rdsrc}$	Read Resource execution time	—	—	35	$\mu$ s	1
$t_{pgm4}$	Program Longword execution time	—	50	TBD	$\mu$ s	
$t_{ersblk}$	Erase Flash Block execution time	—	160	800	ms	2
$t_{ersscr}$	Erase Flash Sector execution time	—	20	100	ms	2
$t_{pgmsec2k}$	Program Section execution time (2 KB flash sector)	—	TBD	TBD	ms	
$t_{rd1all}$	Read 1s All Blocks execution time	—	—	2.8	ms	
$t_{rdonce}$	Read Once execution time	—	—	35	$\mu$ s	1
$t_{pgmonce}$	Program Once execution time	—	50	TBD	$\mu$ s	
$t_{ersall}$	Erase All Blocks execution time	—	320	1600	ms	2
$t_{vfykey}$	Verify Backdoor Access Key execution time	—	—	35	$\mu$ s	1

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

### 6.4.1.3 Flash (FTFL) Current and Power Parameters

**Table 19. Flash (FTFL) current and power parameters**

Symbol	Description	Typ.	Unit
$I_{DD\_PGM}$	Worst case programming current in program flash	10	mA

### 6.4.1.4 Reliability Characteristics

**Table 20. NVM reliability characteristics**

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	TBD	—	years	2
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	10	TBD	—	years	2
$t_{nvmretp100}$	Data retention after up to 100 cycles	15	TBD	—	years	2
$n_{nvmcycp}$	Cycling endurance	10 K	TBD	—	cycles	3

1. Typical data retention values are based on intrinsic capability of the technology measured at high temperature derated to 25°C. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618.
2. Data retention is based on  $T_{javg} = 55^{\circ}\text{C}$  (temperature profile over the lifetime of the application).
3. Cycling endurance represents number of program/erase cycles at  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$

## 6.4.2 EzPort Switching Specifications

Table 21. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{EZP\_CS}$ negation to next $\overline{EZP\_CS}$ assertion	$2 \times t_{EZP\_CK}$	—	ns
EP3	$\overline{EZP\_CS}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{EZP\_CS}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid (setup)	—	12	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{EZP\_CS}$ negation to EZP_Q tri-state	—	12	ns

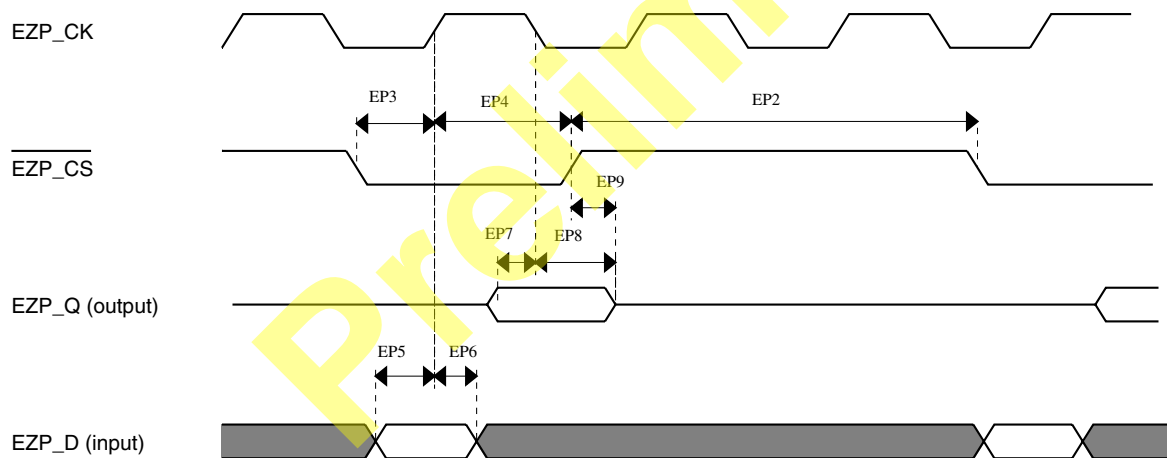


Figure 9. EzPort Timing Diagram

## 6.4.3 Flexbus Switching Specifications

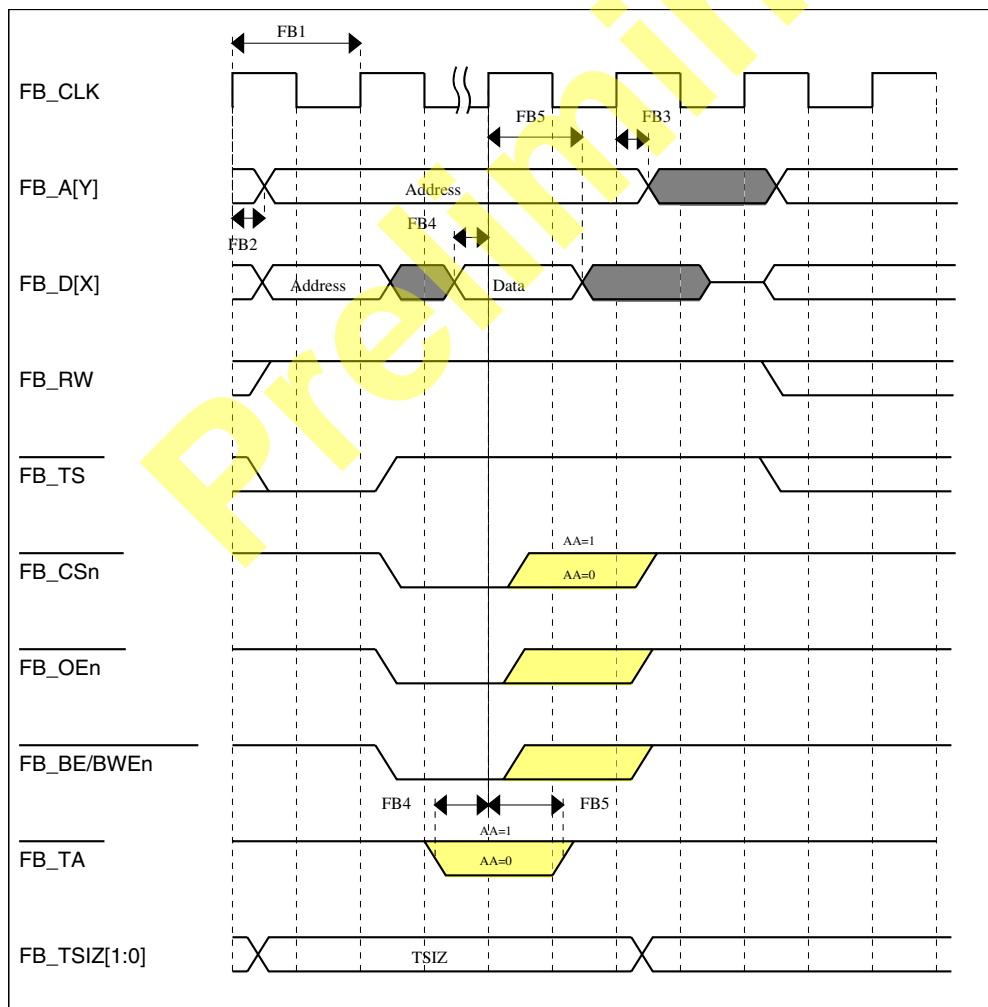
All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB\_CLK. The FB\_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB\_CLK). All other timing relationships can be derived from these values.

**Table 22. Flexbus switching specifications**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	50	Mhz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	TBD	11.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	8.5	—	ns	2
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB\_AD[31:0],  $\overline{\text{FB\_BE/BWE}n}$ ,  $\overline{\text{FB\_CS}n}$ ,  $\overline{\text{FB\_OE}}$ ,  $\overline{\text{FB\_R/W}}$ ,  $\overline{\text{FB\_TBST}}$ ,  $\overline{\text{FB\_TSIZ}}[1:0]$ , and  $\overline{\text{FB\_TS}}$ .
2. Specification is valid for all FB\_AD[31:0] and  $\overline{\text{FB\_TA}}$ .



**Figure 10. FlexBus read timing diagram**

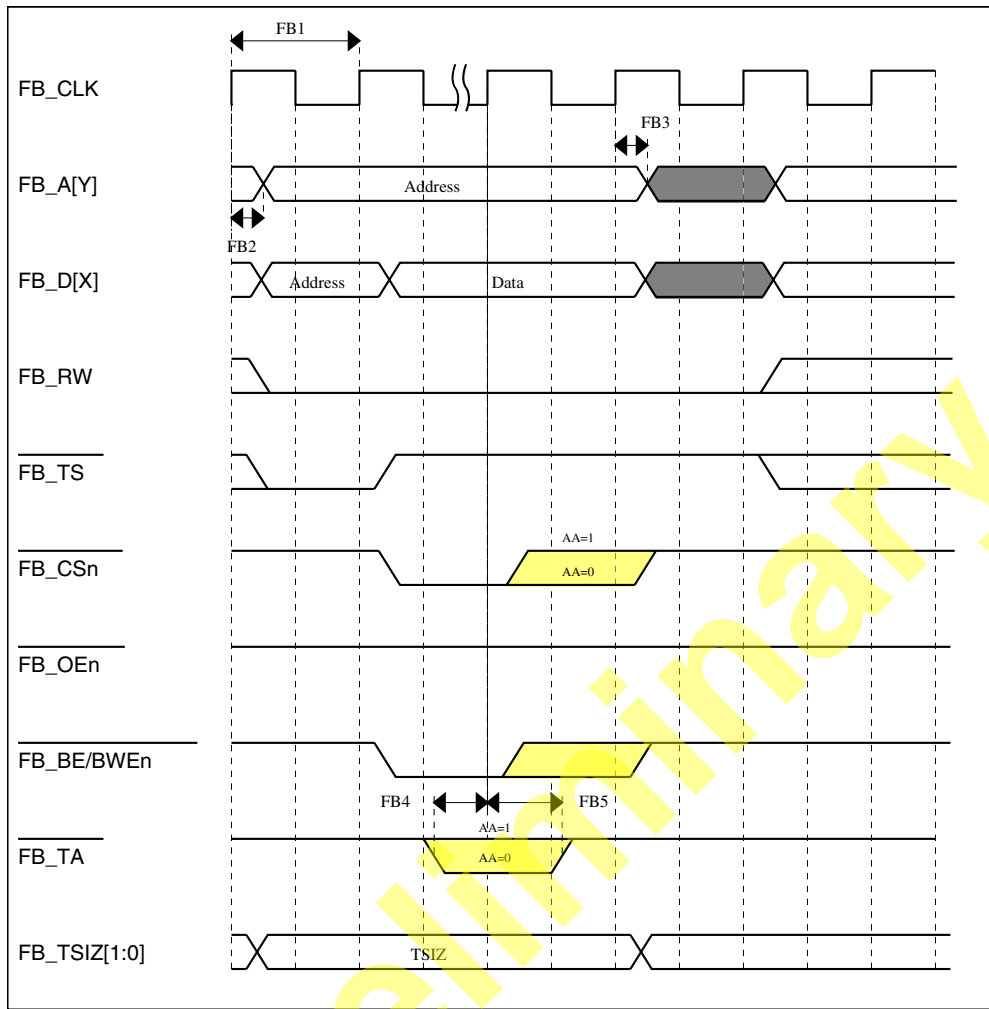


Figure 11. FlexBus write timing diagram

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 6.6 Analog

### 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 23](#) and [Table 24](#) are achievable on the differential pins (ADCx\_DP0, ADCx\_DM0, ADC, ADCx\_DP1, ADCx\_DM1, ADCx\_DP3, and ADCx\_DM3). The ADCx\_DP2 and ADCx\_DM2 ADC inputs are used



as the PGA inputs and are not direct device pins. Accuracy specifications for these pins are defined in [Table 25](#) and [Table 26](#). All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

### 6.6.1.1 16-bit ADC operating conditions

**Table 23. 16-bit ADC operating conditions**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	Absolute	1.71	—	3.6	V	
$\Delta V_{DDA}$	Supply voltage	Delta to $V_{DD}$ ( $V_{DD} - V_{DDA}$ )	-100	0	+100	mV	2
$\Delta V_{SSA}$	Ground voltage	Delta to $V_{SS}$ ( $V_{SS} - V_{SSA}$ )	-100	0	+100	mV	2
$V_{REFH}$	ADC reference voltage high		1.13	$V_{DDA}$	$V_{DDA}$	V	
$V_{REFL}$	Reference voltage low		$V_{SSA}$	$V_{SSA}$	$V_{SSA}$	V	
$V_{ADIN}$	Input voltage		$V_{REFL}$	—	$V_{REFH}$	V	
$C_{ADIN}$	Input capacitance	<ul style="list-style-type: none"> <li>• 16 bit modes</li> <li>• 8/10/12 bit modes</li> </ul>	—	8 4	10 5	pF	
$R_{ADIN}$	Input resistance		—	2	5	k $\Omega$	

*Table continues on the next page...*

**Table 23. 16-bit ADC operating conditions (continued)**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes	
R <sub>AS</sub>	Analog source resistance	16 bit modes					External to MCU Assumes ADLSMP=0	
		• f <sub>ADCK</sub> > 8MHz	—	—	0.5	kΩ		
		• f <sub>ADCK</sub> = 4–8MHz	—	—	1	kΩ		
		• f <sub>ADCK</sub> < 4MHz	—	—	2	kΩ		
		13/12 bit modes						
		• f <sub>ADCK</sub> > 16MHz	—	—	0.5	kΩ		
		• f <sub>ADCK</sub> > 8MHz	—	—	1	kΩ		
		• f <sub>ADCK</sub> = 4–8MHz	—	—	2	kΩ		
		• f <sub>ADCK</sub> < 4MHz	—	—	5	kΩ		
		11/10 bit modes						
		• f <sub>ADCK</sub> > 8MHz	—	—	2	kΩ		
		• f <sub>ADCK</sub> = 4–8MHz	—	—	5	kΩ		
• f <sub>ADCK</sub> < 4MHz	—	—	10	kΩ				
9/8 bit modes								
• f <sub>ADCK</sub> > 8MHz	—	—	5	kΩ				
• f <sub>ADCK</sub> < 8MHz	—	—	10	kΩ				
f <sub>ADCK</sub>	ADC conversion clock frequency	ADLPC=0, ADHSC=1						
		• 16 bit modes	1.0	—	TBD	MHz		
		• ≤13 bit modes	1.0	—	TBD	MHz		
		ADLPC=0, ADHSC=0						
		• 16 bit modes	1.0	—	8.0	MHz		
		• ≤13 bit modes	1.0	—	12.0	MHz		
		ADLPC=1, ADHSC=1						
		• 16 bit modes	1.0	—	5.0	MHz		
		• ≤13 bit modes	1.0	—	8.0	MHz		
		ADLPC=1, ADHSC=0						
		• 16 bit modes	1.0	—	2.5	MHz		
		• ≤13 bit modes	1.0	—	5.0	MHz		

1. Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25°C, f<sub>ADCK</sub> = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2. DC potential difference.

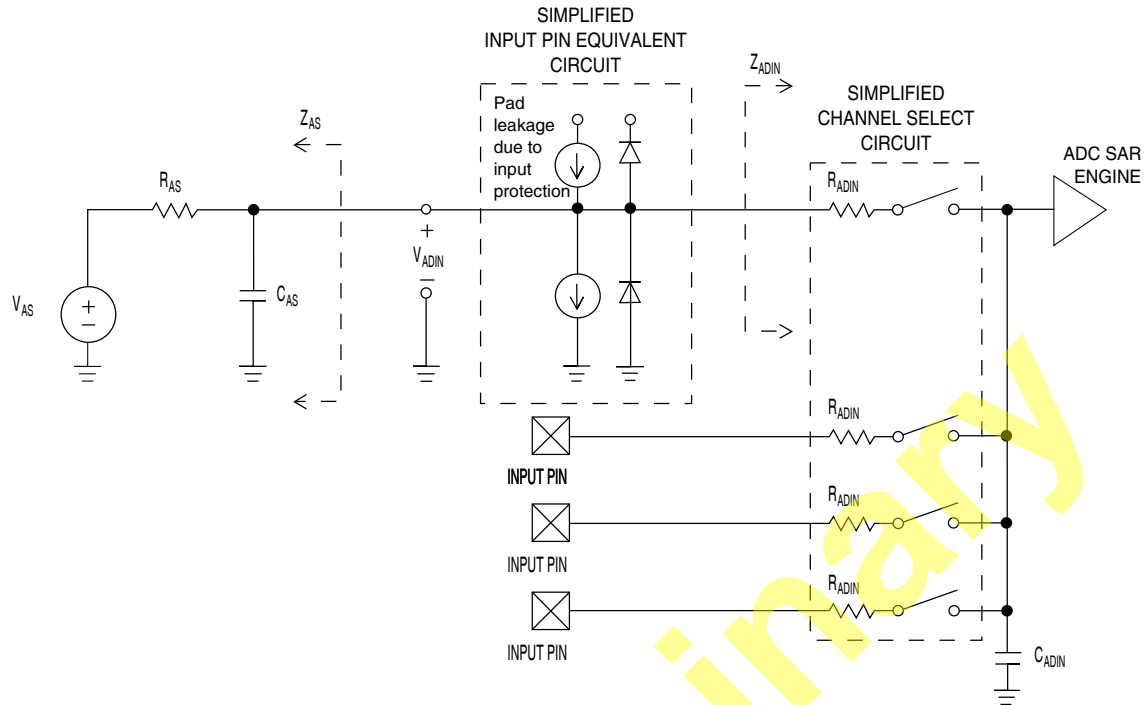


Figure 12. ADC input impedance equivalency diagram

### 6.6.1.2 16-bit ADC electrical characteristics

Table 24. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$I_{DDA}$	Supply current	<ul style="list-style-type: none"> <li>• ADLPC=1, ADHSC=0</li> <li>• ADLPC=1, ADHSC=1</li> <li>• ADLPC=0, ADHSC=0</li> <li>• ADLPC=0, ADHSC=1</li> </ul>	—	215	—	$\mu\text{A}$	ADLSMP=0 ADCO=1
	Supply current	• Stop, reset, module off	—	0.01	0.8	$\mu\text{A}$	
$f_{ADACK}$	ADC asynchronous clock source	• ADLPC=1, ADHSC=0	TBD	2.4	TBD	MHz	$t_{ADACK} = 1/f_{ADACK}$
		• ADLPC=1, ADHSC=1	TBD	4.0	TBD	MHz	
		• ADLPC=0, ADHSC=0	TBD	5.2	TBD	MHz	
		• ADLPC=0, ADHSC=1	TBD	6.2	TBD	MHz	
	Sample Time	See Reference Manual chapter for sample times					
	Conversion Time	See Reference Manual chapter for conversion times					

Table continues on the next page...

**Table 24. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
TUE	Total unadjusted error	<ul style="list-style-type: none"> <li>16 bit differential</li> <li>16 bit single-ended</li> <li>13 bit differential</li> <li>12 bit single-ended</li> <li>11 bit differential</li> <li>10 bit single-ended</li> <li>9 bit differential</li> <li>8 bit single-ended</li> </ul>	—	±14.0	±TBD	LSB <sup>3</sup>	Max hardware averaging (AVGE = %1, AVGS = %11)
DNL	Differential non-linearity	<ul style="list-style-type: none"> <li>16 bit differential</li> <li>16 bit single-ended</li> <li>13 bit differential</li> <li>12 bit single-ended</li> <li>11 bit differential</li> <li>10 bit single-ended</li> <li>9 bit differential</li> <li>8 bit single-ended</li> </ul>	—	±2.5	±TBD	LSB <sup>3</sup>	Max hardware averaging (AVGE = %1, AVGS = %11)
INL	Integral non-linearity	<ul style="list-style-type: none"> <li>16 bit differential</li> <li>16 bit single-ended</li> <li>13 bit differential</li> <li>12 bit single-ended</li> <li>11 bit differential</li> <li>10 bit single-ended</li> <li>9 bit differential</li> <li>8 bit single-ended</li> </ul>	—	-6 to +2.5	—	LSB <sup>3</sup>	Max averaging
E <sub>ZS</sub>	Zero-scale error	<ul style="list-style-type: none"> <li>16 bit differential</li> <li>16 bit single-ended</li> <li>13 bit differential</li> <li>12 bit single-ended</li> <li>11 bit differential</li> <li>10 bit single-ended</li> <li>9 bit differential</li> <li>8 bit single-ended</li> </ul>	—	±4.0	—	LSB <sup>3</sup>	$V_{ADIN} = V_{SSA}$

Table continues on the next page...

Table 24. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$E_{FS}$	Full-scale error	<ul style="list-style-type: none"> <li>16 bit differential</li> <li>16 bit single-ended</li> <li>13 bit differential</li> <li>12 bit single-ended</li> <li>11 bit differential</li> <li>10 bit single-ended</li> <li>9 bit differential</li> <li>8 bit single-ended</li> </ul>	—	0 to +10	—	LSB <sup>3</sup>	$V_{ADIN} = V_{DDA}$
$E_Q$	Quantization error	<ul style="list-style-type: none"> <li>16 bit modes</li> <li>≤13 bit modes</li> </ul>	—	-1 to 0	—	LSB <sup>3</sup>	
ENOB	Effective number of bits	16 bit differential mode <ul style="list-style-type: none"> <li>Avg=32</li> <li>Avg=16</li> <li>Avg=8</li> <li>Avg=4</li> <li>Avg=1</li> </ul> 16 bit single-ended mode <ul style="list-style-type: none"> <li>Avg=32</li> <li>Avg=16</li> <li>Avg=8</li> <li>Avg=4</li> <li>Avg=1</li> </ul>	TBD	13.6	TBD	bits	4
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16 bit differential mode <ul style="list-style-type: none"> <li>Avg=32</li> </ul> 16 bit single-ended mode <ul style="list-style-type: none"> <li>Avg=32</li> </ul>	—	-94	TBD	dB	4
SFDR	Spurious free dynamic range	16 bit differential mode <ul style="list-style-type: none"> <li>Avg=32</li> </ul> 16 bit single-ended mode <ul style="list-style-type: none"> <li>Avg=32</li> </ul>	TBD	95	—	dB	4

Table continues on the next page...

**Table 24. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$E_{IL}$	Input leakage error		$I_{in} \times R_{AS}$			mV	$I_{in}$ = leakage current  (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	<ul style="list-style-type: none"> <li>-40°C to 25°C</li> <li>25°C to 105°C</li> </ul>	—	TBD	—	mV/°C	
$V_{TEMP25}$	Temp sensor voltage	25°C	—	TBD	—	mV	

1. All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
2. Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25°C,  $f_{ADCK} = 2.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$
4. Input data is 1 kHz sine wave.

### 6.6.1.3 16-bit ADC with PGA operating conditions

**Table 25. 16-bit ADC with PGA operating conditions**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	Absolute	1.71	—	3.6	V	
$V_{REFPGA}$	PGA ref voltage		VREFOUT	VREFOUT	VREFOUT	V	2, 3
$V_{ADIN}$	Input voltage		$V_{SSA}$	—	$V_{DDA}$	V	
$R_{PGA}$	Input impedance	Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64	TBD TBD TBD	64 32 16	TBD TBD TBD	kΩ	
$R_{PGAD}$	Differential input impedance	Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64	TBD TBD TBD	128 64 32	TBD TBD TBD	kΩ	IN+ to IN-
$R_{AS}$	Analog source resistance	Gain = 16, 32	—	100	—	Ω	4
$T_S$	ADC sampling time	Gain = 64	1.25	—	—	μs	5

1. Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25°C,  $f_{ADCK} = 6$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREFOUT)
3. PGA reference connected to the VREFOUT pin. If the user wishes to drive VREFOUT with a voltage other than the output of the VREF module, the VREF module must be disabled.

- The analog source resistance ( $R_{AS}$ ), external to MCU, should be kept as minimum as possible. Increased  $R_{AS}$  causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
- The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of  $1.25\mu s$  time should be allowed for  $F_{in}=4$  kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock. The ADLSTS bits can be adjusted for different ADC clock frequency

### 6.6.1.4 16-bit ADC with PGA characteristics

Table 26. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$I_{DDA\_PGA}$	Supply current		TBD	590	TBD	$\mu A$	
$I_{LKG}$	Leakage current	PGA disabled	—	< 1	TBD	$\mu A$	
G	Gain <sup>2</sup>	<ul style="list-style-type: none"> <li>PGAG=0</li> <li>PGAG=1</li> <li>PGAG=2</li> <li>PGAG=3</li> <li>PGAG=4</li> <li>PGAG=5</li> <li>PGAG=6</li> </ul>	TBD	1	TBD	dB	$R_{AS} < 100\Omega$
			TBD	2	TBD	dB	
			TBD	3.9	TBD	dB	
			TBD	TBD	TBD	dB	
			TBD	TBD	TBD	dB	
			TBD	29.9	TBD	dB	
			TBD	TBD	TBD	dB	
$G_A$	Gain error		—	—	$\pm 0.5$	dB	$R_{AS} < 100\Omega$
BW	Input signal bandwidth	<ul style="list-style-type: none"> <li>16-bit modes</li> <li>&lt; 16-bit modes</li> </ul>	—	—	4	kHz	
			—	—	40	kHz	
PSRR	Power supply rejection ration	Gain=1	TBD	TBD	—	dB	$V_{DDA} = 3V \pm 100mV$ , $f_{VDDA} = 50Hz, 60Hz$
CMRR	Common mode rejection ratio	<ul style="list-style-type: none"> <li>Gain=1</li> <li>Gain=64</li> </ul>	TBD	TBD	—	dB	$V_{CM} = 500mV_{pp}$ , $f_{VCM} = 50Hz, 100Hz$
			TBD	TBD	—	dB	
$V_{OFS}$	Input offset voltage		—	0.2	TBD	mV	Gain=1, ADC Averaging=32
$T_{GSW}$	Gain switching settling time		—	TBD	10	$\mu s$	3
dG/dT	Gain drift over temperature	<ul style="list-style-type: none"> <li>Gain=1</li> <li>Gain=64</li> </ul>	—	TBD	TBD	ppm/ $^{\circ}C$	0 to $50^{\circ}C$
			—	TBD	TBD	ppm/ $^{\circ}C$	
d $V_{OFS}$ /dT	Offset drift over temperature	Gain=1	—	TBD	TBD	ppm/ $^{\circ}C$	0 to $50^{\circ}C$ , ADC Averaging=32
dG/d $V_{DDA}$	Gain drift over supply voltage	<ul style="list-style-type: none"> <li>Gain=1</li> <li>Gain=64</li> </ul>	—	TBD	TBD	%/V	$V_{DDA}$ from 1.71 to 3.6V
			—	TBD	TBD	%/V	

Table continues on the next page...

**Table 26. 16-bit ADC with PGA characteristics (continued)**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$E_{IL}$	Input leakage error	All modes	$I_{in} \times R_{AS}$			mV	$I_{in}$ = leakage current (refer to the MCU's voltage and current operating ratings)
$V_{PP,DIFF}$	Maximum differential input signal swing		$[(V_{REFPGA} \times 2.33) - 0.2] / (2 \times \text{Gain})$			V	4
SNR	Signal-to-noise ratio	<ul style="list-style-type: none"> <li>Gain=1</li> <li>Gain=64</li> </ul>	TBD	8.3	—	dB	Average=32
			TBD	57.7	—	dB	
THD	Total harmonic distortion	<ul style="list-style-type: none"> <li>Gain=1</li> <li>Gain=64</li> </ul>	TBD	87.3	—	dB	Average=32, $f_{in}=100\text{Hz}$
			TBD	85.3	—	dB	
SFDR	Spurious free dynamic range	<ul style="list-style-type: none"> <li>Gain=1</li> <li>Gain=64</li> </ul>	TBD	92.42	—	dB	Average=32, $f_{in}=100\text{Hz}$
			TBD	92.54	—	dB	
ENOB	Effective number of bits	Gain=1, Average=4	TBD	12.3	—	bits	
		Gain=1, Average=8	TBD	12.7	—	bits	
		Gain=64, Average=4	TBD	8.4	—	bits	
		Gain=64, Average=8	TBD	8.7	—	bits	
		Gain=1, Average=32	TBD	13.4	—	bits	
		Gain=2, Average=32	TBD	13.1	—	bits	
		Gain=4, Average=32	TBD	12.6	—	bits	
		Gain=8, Average=32	TBD	11.8	—	bits	
		Gain=16, Average=32	TBD	11.1	—	bits	
		Gain=32, Average=32	TBD	10.2	—	bits	
Gain=64, Average=32	TBD	9.3	—	bits			
SINAD	Signal-to-noise plus distortion ratio	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	

1. Typical values assume  $V_{DDA} = 3.0\text{V}$ ,  $\text{Temp} = 25^\circ\text{C}$ ,  $f_{ADCK} = 6\text{MHz}$  unless otherwise stated.
2.  $\text{Gain} = 2^{\text{PGAGx}}$
3. When the PGA gain is changed, it takes some time to settle the output for the ADC to work properly. During a gain switching, a few ADC outputs should be discarded (minimum two data samples, may be more depending on ADC sampling rate and time of the switching).
4. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.



## 6.6.2 CMP and 6-bit DAC electrical specifications

**Table 27. Comparator and 6-bit DAC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply voltage	1.71	—	3.6	V
I <sub>DDHS</sub>	Supply current, High-speed mode (EN=1, PMODE=1, VDDA >= V <sub>LVI_trip</sub> )	—	—	200	μA
I <sub>DDL</sub>	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
I <sub>DDOFF</sub>	Supply current, OFF Mode (EN=0,)	—	—	100	nA
V <sub>AIN</sub>	Analog input voltage	V <sub>SS</sub> – 0.3	—	V <sub>DD</sub>	V
V <sub>AIO</sub>	Analog input offset voltage	—	—	20	mV
V <sub>H</sub>	Analog comparator hysteresis	—	5	—	mV
		—	10	—	mV
		—	20	—	mV
		—	30	—	mV
V <sub>CMPOH</sub>	Output high	V <sub>DD</sub> – 0.5	—	—	V
V <sub>CMPOI</sub>	Output low	—	—	0.5	V
t <sub>DHS</sub>	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	120	ns
t <sub>DLS</sub>	Propagation delay, low-speed mode (EN=1, PMODE=1)	120	250	420	ns
	Analog comparator initialization delay	—	—	TBD	ns
I <sub>DAC6b</sub>	6-bit DAC current adder (enabled)	—	—	8	μA
INL	6-bit DAC integral non-Linearity	–0.5	—	0.5	LSB <sup>1</sup>
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. 1 LSB = V<sub>reference</sub>/64

## 6.6.3 12-bit DAC electrical characteristics

### 6.6.3.1 12-bit DAC operating requirements

**Table 28. 12-bit DAC operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	1.71	3.6	V	
V <sub>DACR</sub>	Reference voltage	1.15	3.6	V	1
T <sub>A</sub>	Temperature	–40	105	°C	

Table continues on the next page...

**Table 28. 12-bit DAC operating requirements (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
$C_L$	Output load capacitance	—	100	pF	2
$I_L$	Output load current	—	1	mA	

1. The DAC reference can be selected to be VDDA or the voltage output of the VREF module (VREFO)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

### 6.6.3.2 12-bit DAC operating behaviors

**Table 29. 12-bit DAC operating behaviors**

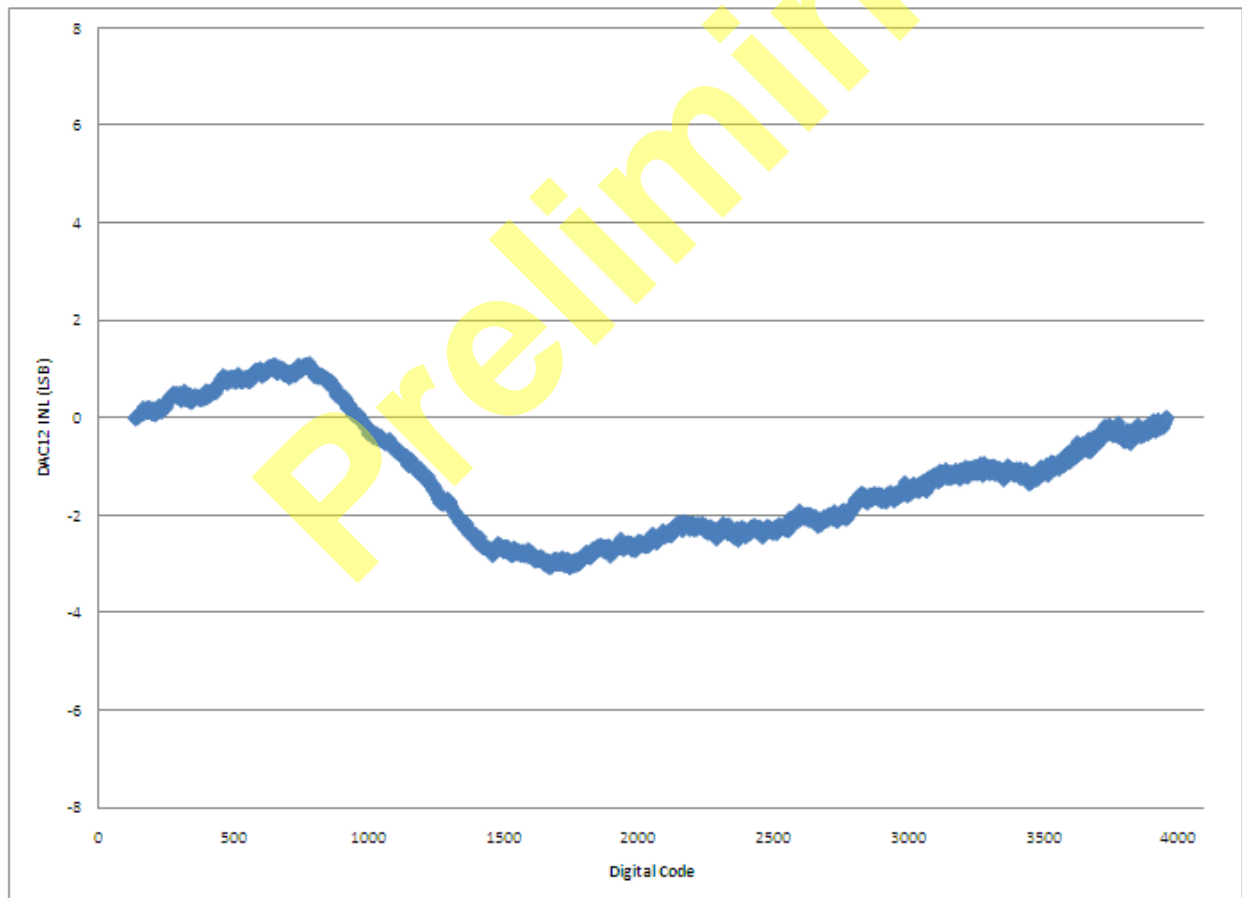
Symbol	Description	Min.	Typ.	Max.	Unit	Notes
n	Resolution	12	—	12	b	
$I_{DDA\_DACLP}$	Supply current — low-power mode	—	—	150	$\mu$ A	
$I_{DDA\_DACHP}$	Supply current — high-speed mode	—	—	700	$\mu$ A	
$t_{DACLP}$	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	$\mu$ s	1
$t_{DACHP}$	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	$\mu$ s	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode	—	—	5	$\mu$ s	1
$t_{CCDACHP}$	Code-to-code settling time (0xBF8 to 0xC08) — high-speed mode	1	TBD	—	$\mu$ s	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	0	100	—	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF	$V_{DACR}$ -100	—	$V_{DACR}$	mV	
INL	Integral non-linearity error — high speed mode	$\pm 3$	—	$\pm 8$	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2$ V	$\pm 0.5$	—	$\pm 1$	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = VREFO$ (1.15 V)	$\pm 0.5$	—	$\pm 1$	LSB	4
$V_{OFFSET}$	Offset error	$\pm 0.4$	—	$\pm 0.8$	%FSR	5
$E_G$	Gain error	$\pm 0.1$	—	$\pm 0.6$	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4$ V	60	—	90	dB	
$T_{CO}$	Temperature coefficient offset voltage	—	TBD	—	$\mu$ V/C	
$T_{GE}$	Temperature coefficient gain error	—	TBD	—	ppm of FSR/C	
$A_C$	Offset aging coefficient	—	—	TBD	$\mu$ V/yr	
$R_{op}$	Output resistance load = 3 k $\Omega$	—	—	250	$\Omega$	

Table continues on the next page...

**Table 29. 12-bit DAC operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
SR	Slew rate -80h→ F7Fh→ 80h <ul style="list-style-type: none"> <li>High power (SP<sub>HP</sub>)</li> <li>Low power (SP<sub>LP</sub>)</li> </ul>	1.2 0.05	1.7 0.12	— —	V/μs	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth <ul style="list-style-type: none"> <li>High power (SP<sub>HP</sub>)</li> <li>Low power (SP<sub>LP</sub>)</li> </ul>	550 40	— —	— —	kHz	

1. Settling within  $\pm 1$  LSB
2. The INL is measured for 0+100mV to VD<sub>ACR</sub>-100 mV
3. The DNL is measured for 0+100 mV to V<sub>D<sub>ACR</sub></sub>-100 mV
4. The DNL is measured for 0+100mV to V<sub>D<sub>ACR</sub></sub>-100 mV with V<sub>D<sub>DDA</sub></sub> > 2.4V
5. Calculated by a best fit curve from V<sub>SS</sub>+100 mV to V<sub>REF</sub>-100 mV

**Figure 13. Typical INL error vs. digital code**

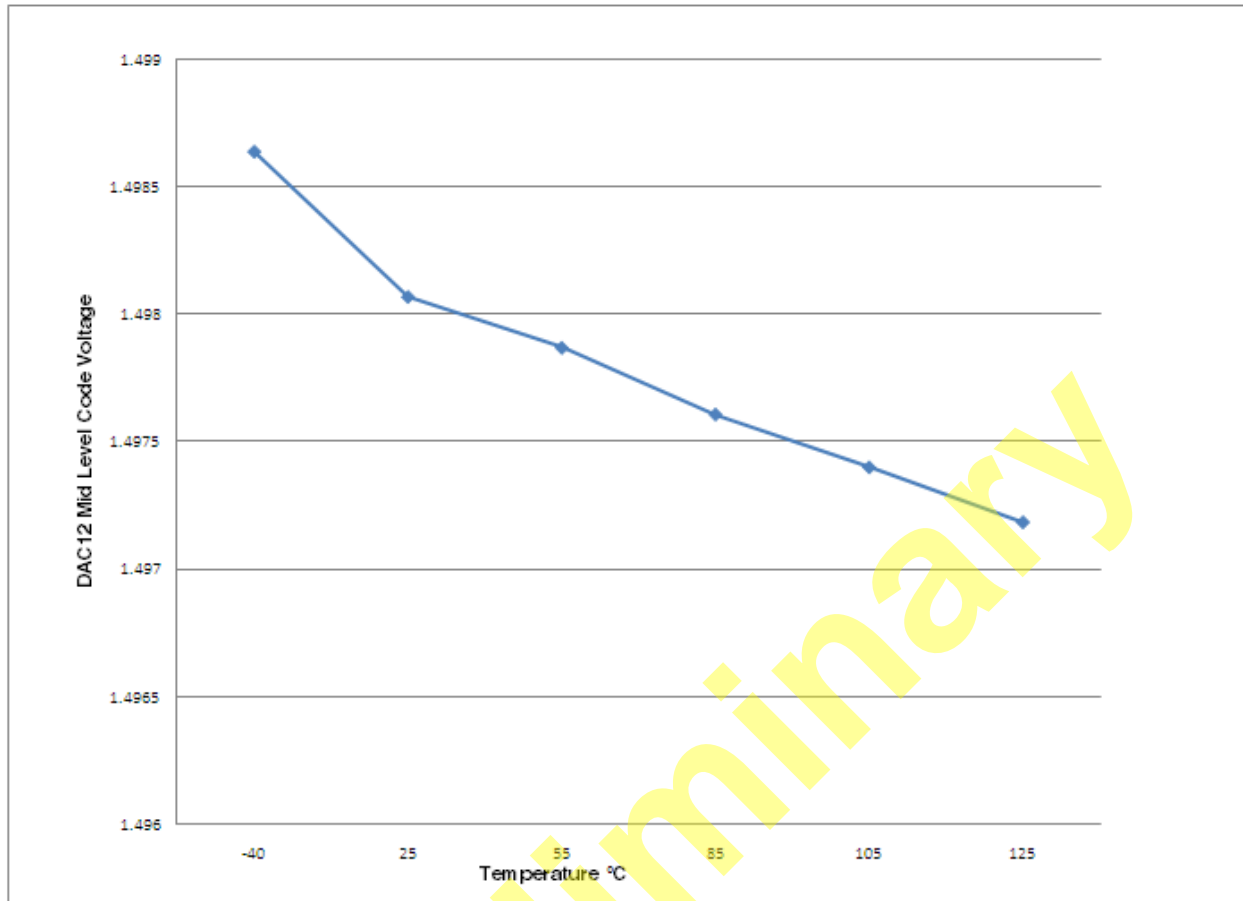


Figure 14. Offset at half scale vs. temperature

## 6.6.4 Voltage Reference Electrical Specifications

Table 30. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	
$T_A$	Temperature	-40	105	°C	
$C_L$	Output load capacitance	—	100	nF	

Table 31. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim	TBD	1.2	TBD	V	
$V_{out}$	Voltage reference output without factory trim	1.15	—	1.24	V	
$V_{drift}$	Temperature drift ( $V_{max} - V_{min}$ across the full temperature range)	—	—	7	mV	See <a href="#">Figure 15</a>

Table continues on the next page...

**Table 31. VREF full-range operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$T_c$	Temperature coefficient	—	—	TBD	ppm/°C	
$A_c$	Aging coefficient	—	—	TBD	ppm/year	
$I_{off}$	Powered down current (off mode, VREFEN = 0, VRSTEN = 0)	—	—	0.10	μA	
$I_{bg}$	Bandgap only (MODE_LV = 00) current	—	TBD	75	μA	
$I_{tr}$	Tight-regulation buffer (MODE_LV = 10) current	—	—	1.1	mA	
	Load regulation (MODE_LV = 10) current	—	—	100	μV/mA	
$T_{stup}$	Buffer startup time	100	—	TBD	μs	
DC	Line regulation (power supply rejection)	—	—	TBD	mV	
		-60	—	TBD	dB	

**Table 32. VREF limited-range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$T_A$	Temperature	0	50	°C	

**Table 33. VREF limited-range operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim	TBD	TBD	μA	

TBD

**Figure 15. Typical output vs. temperature**

TBD

**Figure 16. Typical output vs. VDD**

## 6.7 Timers

See [General Switching Specifications](#).

## 6.8 Communication interfaces

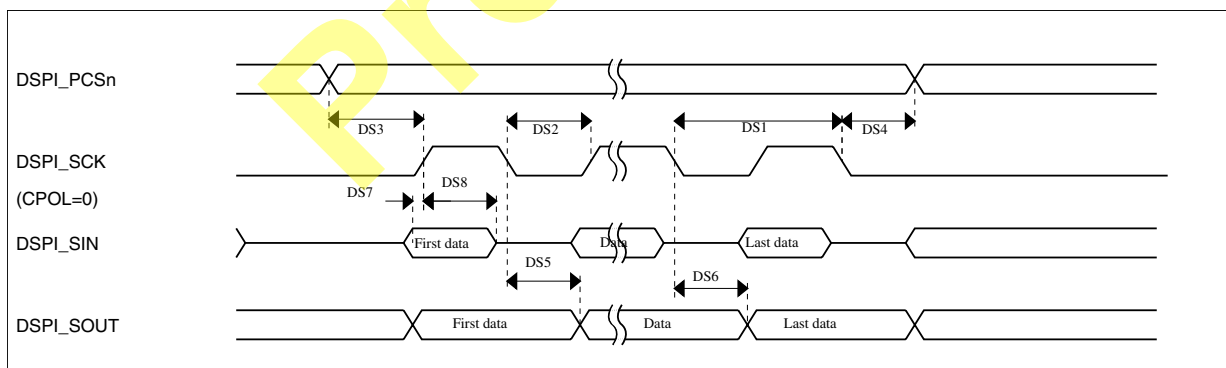
### 6.8.1 DSPI Switching Specifications for Low-speed Operation

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 34. Master Mode DSPI Timing (Low-speed mode)**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t <sub>BCLK</sub>	—	ns	
DS2	DSPI_SCK output high/low time	(t <sub>SCK/2</sub> ) - 4	(t <sub>SCK/2</sub> ) + 4	ns	
DS3	DSPI_PCS <sub>n</sub> to DSPI_SCK output valid	(t <sub>SCK/2</sub> ) - 4	—	ns	
DS4	DSPI_SCK to DSPI_PCS <sub>n</sub> output hold	(t <sub>SCK/2</sub> ) - 4	—	ns	
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

- The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.



**Figure 17. DSPI Classic SPI Timing — Master Mode**

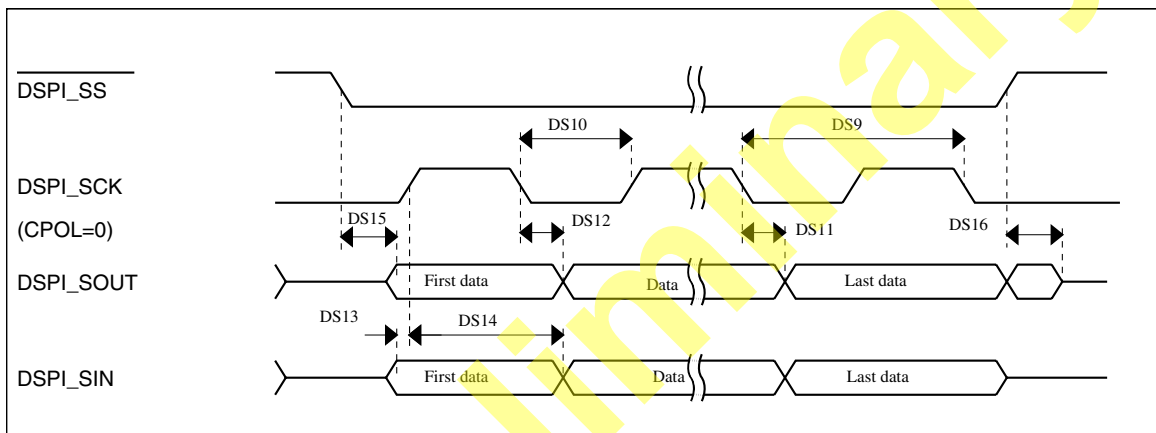
**Table 35. Slave Mode DSPI Timing (Low-speed Mode)**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz

Table continues on the next page...

**Table 35. Slave Mode DSPI Timing (Low-speed Mode) (continued)**

Num	Description	Min.	Max.	Unit
DS9	DSPI_SCK input cycle time	$8 \times t_{BCLK}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK/2}) - 4$	$(t_{SCK/2}) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	15	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	15	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	15	ns

**Figure 18. DSPI Classic SPI Timing — Slave Mode**

## 6.8.2 DSPI Switching Specifications (High-speed mode)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

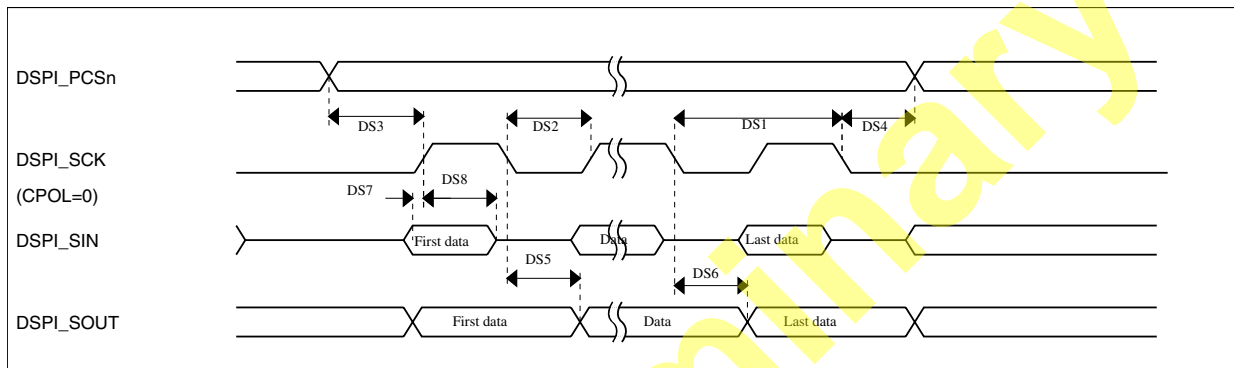
**Table 36. Master Mode DSPI Timing (High-speed mode)**

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation	—	25	MHz
DS1	DSPI_SCK output cycle time	$2 \times t_{BCLK}$	—	ns
DS2	DSPI_SCK output high/low time	$(t_{SCK/2}) - 2$	$(t_{SCK/2}) + 2$	ns

Table continues on the next page...

**Table 36. Master Mode DSPI Timing (High-speed mode) (continued)**

Num	Description	Min.	Max.	Unit
DS3	DSPI_PCSn to DSPI_SCK output valid	$(t_{SCK}/2) - 2$	—	ns
DS4	DSPI_SCK to DSPI_PCSn output hold	$(t_{SCK}/2) - 2$	—	ns
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns
DS7	DSPI_SIN to DSPI_SCK input setup	TBD	—	ns
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns



**Figure 19. DSPI Classic SPI Timing — Master Mode**

**Table 37. Slave Mode DSPI Timing (High-speed mode)**

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BCLK}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	TBD	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{DSPI\_SS}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{DSPI\_SS}$ inactive to DSPI_SOUT not driven	—	14	ns



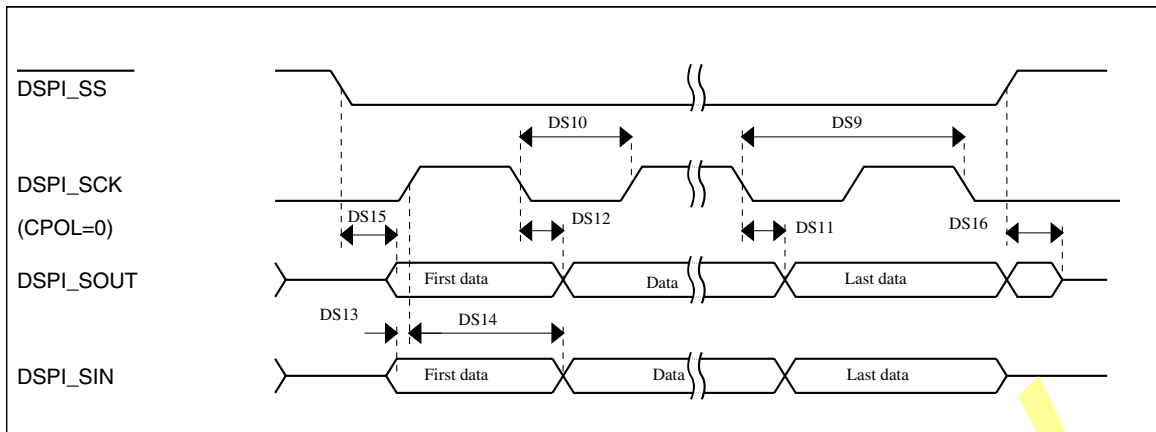


Figure 20. DSPI Classic SPI Timing — Slave Mode

### 6.8.3 SDHC Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 38. SDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
<b>Card input clock</b>					
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed)	0	25	MHz
	fpp	Clock frequency (MMC full speed)	0	20	MHz
	f <sub>OD</sub>	Clock frequency (identification mode)	0	400	kHz
SD2	t <sub>WL</sub>	Clock low time	7	—	ns
SD3	t <sub>WH</sub>	Clock high time	7	—	ns
SD4	t <sub>TLH</sub>	Clock rise time	—	3	ns
SD5	t <sub>THL</sub>	Clock fall time	—	3	ns
<b>SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)</b>					
SD6	t <sub>OD</sub>	SDHC output delay (output valid)	-5	6.5	ns
<b>SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)</b>					
SD7	t <sub>THL</sub>	SDHC input setup time	5	—	ns
SD8	t <sub>THL</sub>	SDHC input hold time	0	—	ns

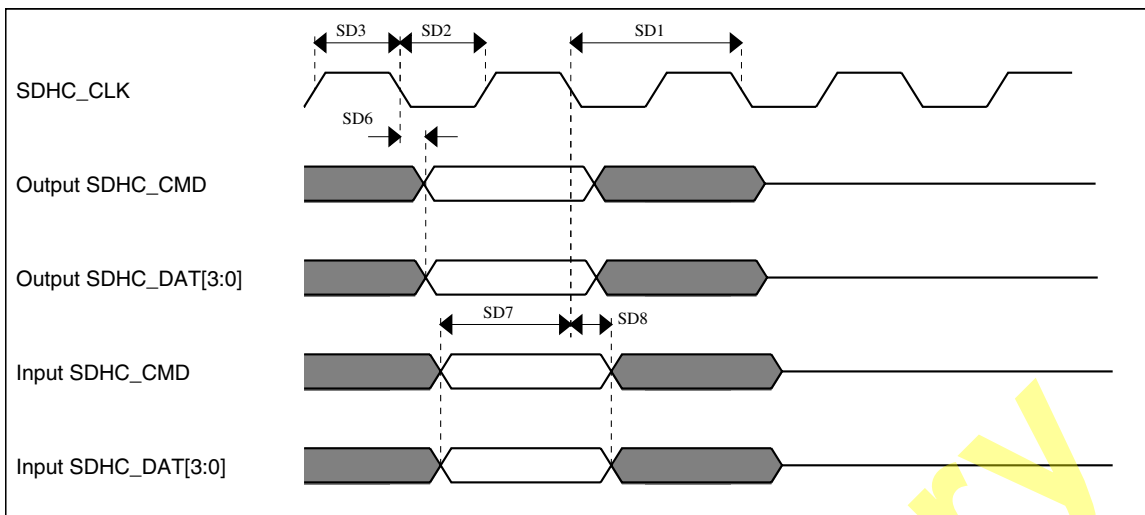


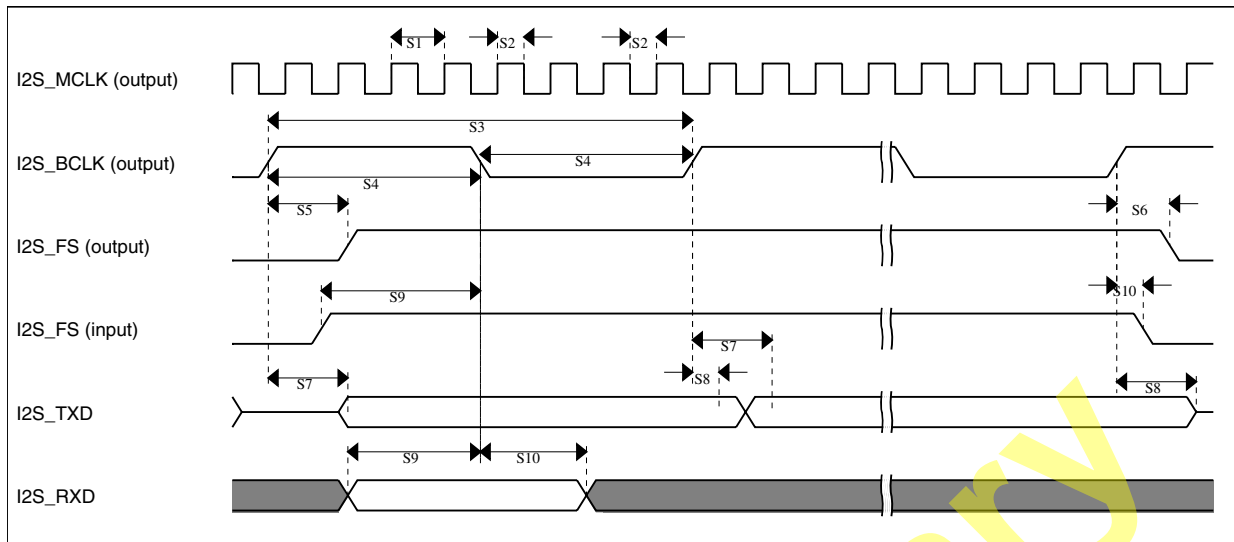
Figure 21. SDHC timing

## 6.8.4 I<sup>2</sup>S Switching Specifications

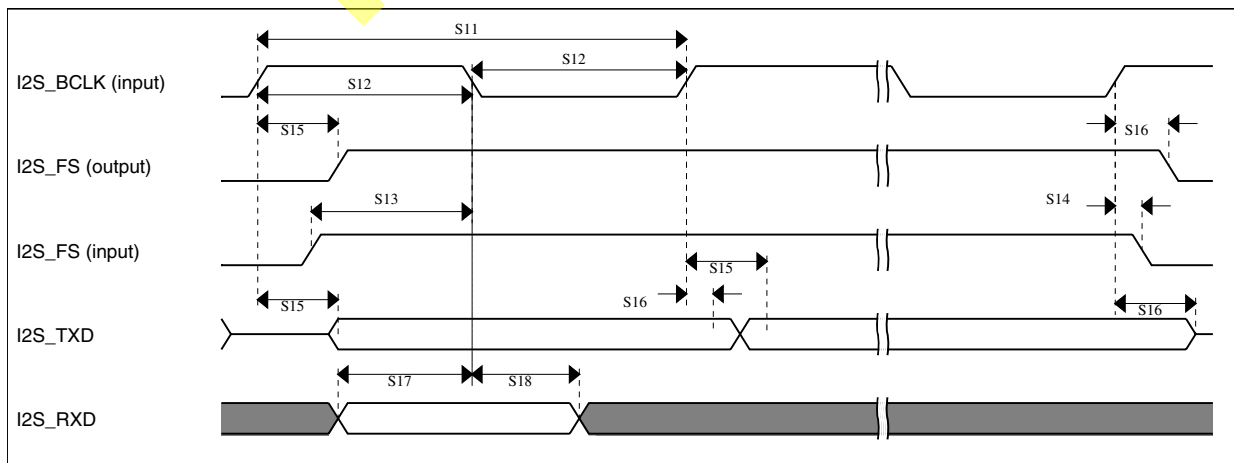
This section provides the AC timings for the I<sup>2</sup>S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S\_BCLK) and/or the frame sync (I2S\_FS) shown in the figures below.

Table 39. I<sup>2</sup>S master mode timing

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	2 x t <sub>sys</sub>		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	5 x t <sub>sys</sub>	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	-2.5	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	-3	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	20	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

Figure 22. I<sup>2</sup>S timing — master modeTable 40. I<sup>2</sup>S slave mode timing

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_BCLK cycle time (input)	$8 \times t_{SYS}$	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	10	—	ns
S14	I2S_FS input hold after I2S_BCLK	3	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	20	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns

Figure 23. I<sup>2</sup>S timing — slave modes

## 6.9 Human-machine interfaces (HMI)

### 6.9.1 General Switching Specifications

These general purpose specifications apply to all signals configured for GPIO, SCI, FlexCAN, CMT, and I<sup>2</sup>C signals.

**Table 41. General switching specifications**

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	2
	External reset pulse width (digital glitch filter disabled)	TBD	—		
	Mode select ( $\overline{\text{EZP\_CS}}$ ) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength)				3
	• Slew disabled	—	12	ns	
	• Slew enabled	—	36	ns	
	Port rise and fall time (low drive strength)				4
	• Slew disabled	—	32	ns	
	• Slew enabled	—	36	ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75pF load
4. 15pF load

### 6.9.2 TSI Electrical Specifications

**Table 42. Touch Sensing Input module specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>DDTSI</sub>	Operating voltage	1.71	—	3.6	V	
C <sub>ELE</sub>	Target electrode capacitance range	1	20	500	pF	1
f <sub>REFmax</sub>	Reference oscillator frequency	—	5.5	TBD	MHz	

Table continues on the next page...

**Table 42. Touch Sensing Input module specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ELEmax}}$	Electrode oscillator frequency	—	0.5	TBD	MHz	
$C_{\text{REF}}$	Internal reference capacitor	TBD	1	TBD	pF	
$V_{\text{DELTA}}$	Oscillator delta voltage	TBD	600	TBD	mV	
$I_{\text{REF}}$	Reference oscillator current source base current	TBD	1	TBD	$\mu\text{A}$	2
$I_{\text{ELE}}$	Electrode oscillator current source base current	TBD	1	TBD	$\mu\text{A}$	3
Pres5	Electrode capacitance measurement precision	—	TBD	TBD	%	4
Pres20	Electrode capacitance measurement precision	—	TBD	TBD	%	5
Pres100	Electrode capacitance measurement precision	—	TBD	TBD	%	6
Max-Sens20	Max sensitivity @ 20pF electrode	0.15	0.326	600	fF	7
MaxSens	Maximum sensitivity	0.006	0.326	24	fF	8
Res	Resolution	—	—	16	bits	
$T_{\text{Con20}}$	Response time @ 20pF	—	30	—	$\mu\text{s}$	9
$I_{\text{TSL\_RUN}}$	Current added in run mode	—	TBD	—	$\mu\text{A}$	
$I_{\text{TSL\_LP}}$	Low power mode current adder	—	1	TBD	$\mu\text{A}$	

1. The TSI module is functional with capacitance values outside of this range. However, optimal performance is not guaranteed.
2. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current
3. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current
4. Measured with a 5pF electrode, reference oscillator frequency of 10MHz, PS = 128, NCSC = 8; Iext = 16
5. Measured with a 20pF electrode, reference oscillator frequency of 10MHz, PS = 128, NCSC = 2; Iext = 16
6. Measured with a 20pF electrode, reference oscillator frequency of 10MHz, PS = 16, NCSC = 3; Iext = 16
7. 6.2ms scan time
8. 1pF electrode capacitance with 4.96ms scan time
9. Time that takes to do one complete measurement of the electrode. Sensitivity resolution of 0.0133pF

## 7 Dimensions

### 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [www.freescale.com](http://www.freescale.com) and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
80-pin LQFP	98ASS23174W
81-pin MAPBGA	98ASH98051A

## 8 Pinout

### 8.1 K10 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

80 QFP	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C1_SDA		
2	ADC1_SE5a	ADC1_SE5a	PTE1	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL		
3	ADC1_SE6a	ADC1_SE6a	PTE2	SPI1_SCK	UART1_CTS_b	SDHC0_DCLK				
4	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_b	SDHC0_CMD				
5	DISABLED		PTE4	SPI1_PCS0	UART3_TX	SDHC0_D3				
6	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2				
7	VDD	VDD								
8	VSS	VSS								
9	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
10	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPT00_ALT3		
11	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_b	I2C0_SDA				
12	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_b	I2C0_SCL				
13	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
14	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								
15	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
16	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
17	VDDA	VDDA								
18	VREFH	VREFH								
19	VREFL	VREFL								
20	VSSA	VSSA								
21	VREF_OUT	VREF_OUT								
22	DAC0_OUT	DAC0_OUT								

80 QFP	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
23	XTAL32	XTAL32								
24	EXTAL32	EXTAL32								
25	VBAT	VBAT								
26	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_ b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
27	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
28	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
29	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
30	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4		FTM0_CH1				NMI_b	EZP_CS_b
31	JTAG_TRST		PTA5		FTM0_CH2		CMP2_OUT	I2S0_RX_BCL K	JTAG_TRST	
32	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0			I2S0_TXD	FTM1_QD_PH A	
33	CMP2_IN1	CMP2_IN1	PTA13	CAN0_RX	FTM1_CH1			I2S0_TX_FS	FTM1_QD_PH B	
34	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_TX_BCL K		
35	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD		
36	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_ b			I2S0_RX_FS		
37	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_ b			I2S0_MCLK	I2S0_CLKIN	
38	VDD	VDD								
39	VSS	VSS								
40	EXTAL	EXTAL	PTA18		FTM0_FLT2	FTM_CLKIN0				
41	XTAL	XTAL	PTA19		FTM1_FLT0	FTM_CLKIN1		LPT0_ALT1		
42	RESET_b	RESET_b								
43	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	PTB0	I2C0_SCL	FTM1_CH0				FTM1_QD_PH A	
44	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1				FTM1_QD_PH B	
45	ADC0_SE12/ TSI0_CH7	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UART0_RTS_ b				FTM0_FLT3	
46	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS_ b				FTM0_FLT0	
47	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX		FB_AD19	FTM0_FLT1		
48	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX		FB_AD18	FTM0_FLT2		
49	VSS	VSS								
50	VDD	VDD								

## Pinout

80 QFP	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
51	TSI0_CH9	TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX		FB_AD17	EWM_IN		
52	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	UART0_TX		FB_AD16	EWM_OUT_b		
53	TSI0_CH11	TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_BCLK	FB_AD15	FTM2_QD_PHA		
54	TSI0_CH12	TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_PHB		
55	ADC0_SE14/ TSI0_CH13	ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG	I2S0_TXD	FB_AD14			
56	ADC0_SE15/ TSI0_CH14	ADC0_SE15/ TSI0_CH14	PTC1	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13			
57	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12			
58	CMP1_IN1	CMP1_IN1	PTC3	SPI0_PCS1	UART1_RX	FTM0_CH2	FB_CLKOUT			
59	VSS	VSS								
60	VDD	VDD								
61	DISABLED		PTC4	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT		
62	DISABLED		PTC5	SPI0_SCK		LPT0_ALT2	FB_AD10	CMP0_OUT		
63	CMP0_IN0	CMP0_IN0	PTC6	SPI0_SOUT	PDB0_EXTRG		FB_AD9			
64	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN			FB_AD8			
65	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8		I2S0_MCLK	I2S0_CLKIN	FB_AD7			
66	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_BCLK	FB_AD6	FTM2_FLT0		
67	ADC1_SE6b/ CMP0_IN4	ADC1_SE6b/ CMP0_IN4	PTC10	I2C1_SCL		I2S0_RX_FS	FB_AD5			
68	ADC1_SE7b	ADC1_SE7b	PTC11	I2C1_SDA		I2S0_RXD	FB_RW_b			
69	VSS	VSS								
70	VDD	VDD								
71	DISABLED		PTC16	CAN1_RX	UART3_RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_	BLS15_8_b		
72	DISABLED		PTC17	CAN1_TX	UART3_TX		FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_	BLS7_0_b		
73	DISABLED		PTD0	SPI0_PCS0	UART2_RTS_b		FB_ALE/ FB_CS1_b/ FB_TS_b			
74	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b		FB_CS0_b			
75	DISABLED		PTD2	SPI0_SOUT	UART2_RX		FB_AD4			
76	DISABLED		PTD3	SPI0_SIN	UART2_TX		FB_AD3			
77	DISABLED		PTD4	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FB_AD2	EWM_IN		



80 QFP	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
78	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b	FTM0_CH5	FB_AD1	EWM_OUT_b		
79	ADC0_SE7b	ADC0_SE7b	PTD6	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		
80	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		

## 8.2 K10 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

Preliminary



**Table 43. Revision History**

Rev. No.	Date	Substantial Changes
1	11/2010	Initial public revision

Preliminary

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