

Silicon PNP Power Transistors

2SB946

DESCRIPTION

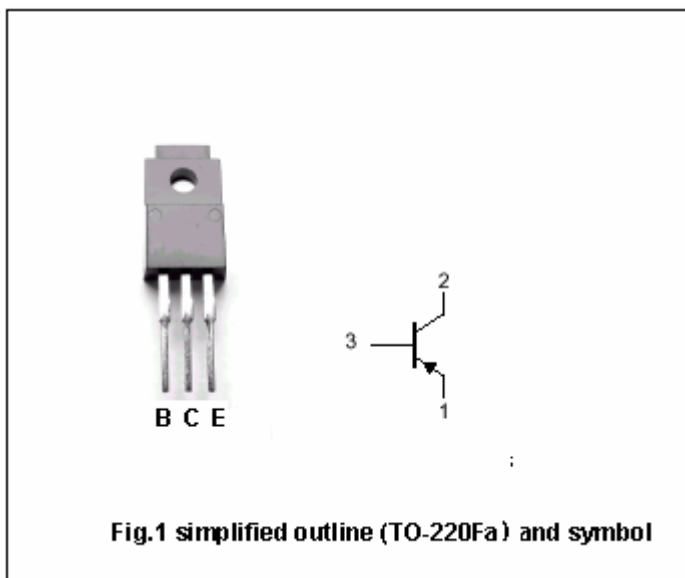
- With TO-220Fa package
- Complement to type 2SD1271
- Low saturation voltage
- Good linearity of h_{FE}
- High current

APPLICATIONS

- For power switching applications

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector
3	Base



Absolute maximum ratings($T_a=25^\circ C$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-130	V
V_{CEO}	Collector-emitter voltage	Open base	-80	
V_{EBO}	Emitter-base voltage	Open collector	-7	V
I_C	Collector current (DC)		-7	A
I_{CM}	Collector current-Peak		-15	A
P_C	Collector power dissipation	$T_C=25^\circ C$	40	W
		$T_a=25^\circ C$	2	
T_j	Junction temperature		150	$^\circ C$
T_{stg}	Storage temperature		-55~150	$^\circ C$

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-10mA, I _B =0	-80			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-5A; I _B =-0.25A			-0.5	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-5A; I _B =-0.25A			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-100V; I _E =0			-10	μA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-50	μA
h _{FE-1}	DC current gain	I _C =-0.1A; V _{CE} =-2V	45			
h _{FE-2}	DC current gain	I _C =-3A; V _{CE} =-2V	60		260	
f _T	Transition frequency	I _C =-0.5A; V _{CE} =-10V		30		MHz

Switching times

t _{on}	Turn-on time	I _C =-3A; I _{B1} =-0.3A I _{B2} =0.3A		0.5		μs
t _s	Storage time			1.5		μs
t _f	Fall time			0.1		μs

◆ h_{FE-2} Classifications

R	Q	P
60-120	90-180	130-260

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PACKAGE OUTLINE

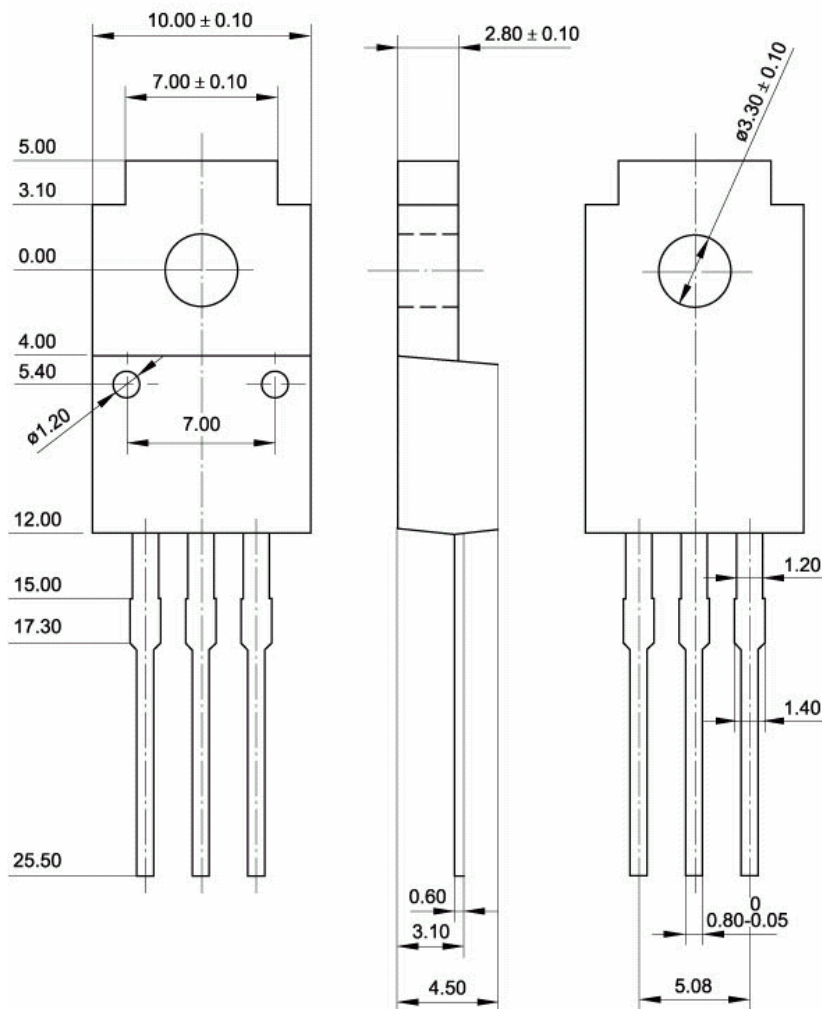


Fig.2 Outline dimensions (unindicated tolerance: ± 0.15 mm)

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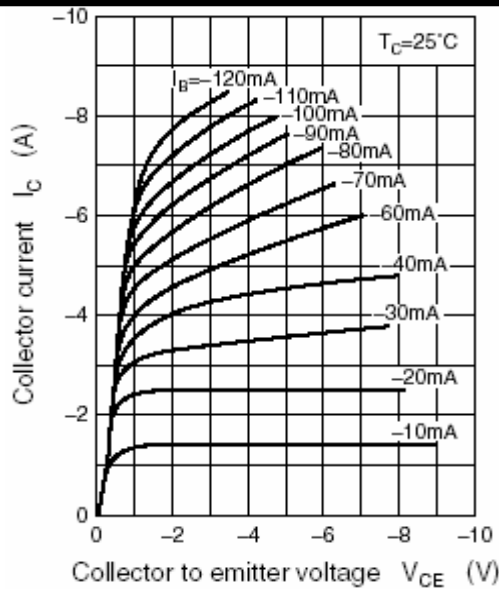


Fig.3 Static Characteristic

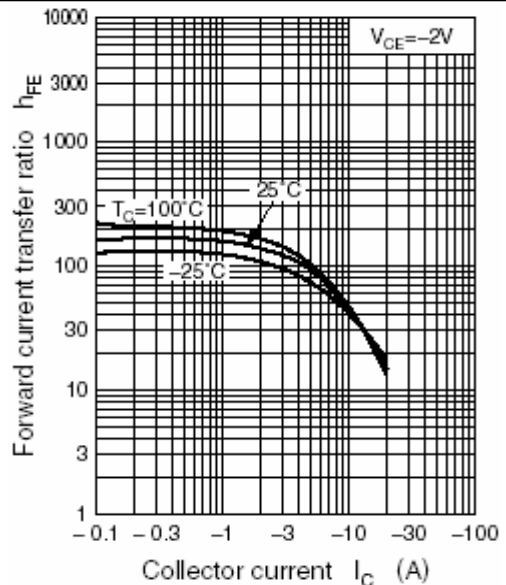


Fig.4 DC current Gain

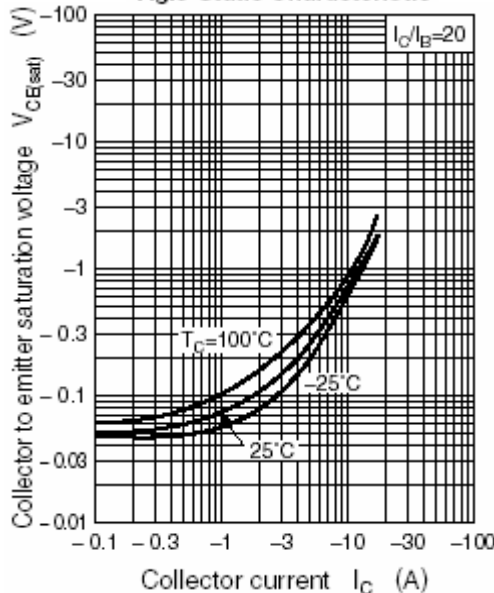


Fig.5 Collector-Emitter Saturation Voltage

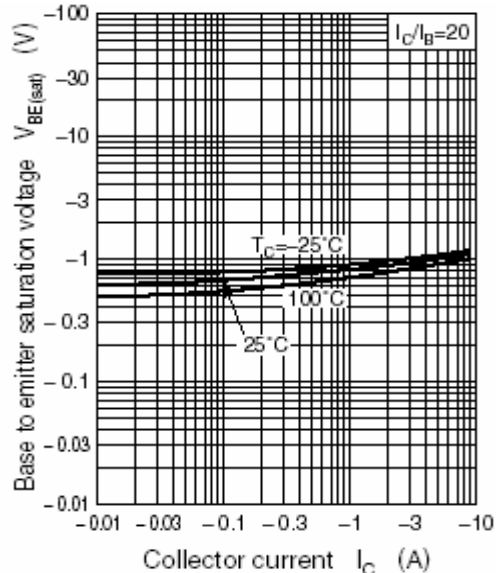


Fig.6 Base-Emitter Saturation Voltage

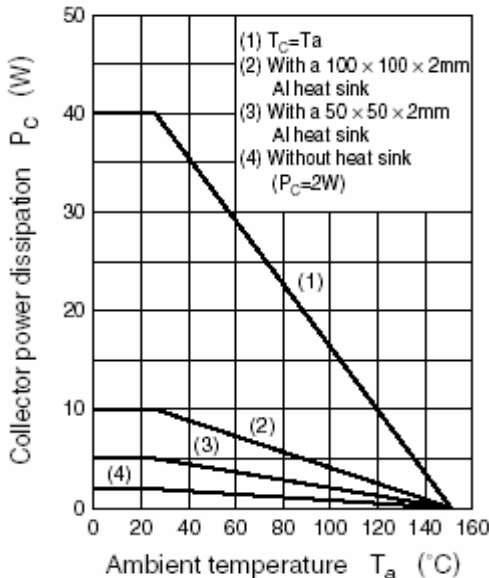


Fig.7 Power Derating

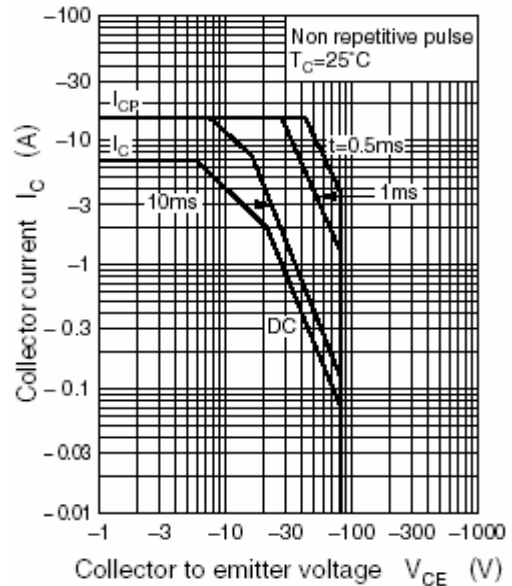


Fig.8 Safe Operating Area