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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## 1. Overview

### 1.1 Features

The R8C/L35A Group, R8C/L36A Group, R8C/L38A Group, R8C/L3AA Group, R8C/L35B Group, R8C/L36B Group, R8C/L38B Group, and R8C/L3AB Group of single-chip MCUs incorporate the R8C CPU core, which implements a powerful instruction set for a high level of efficiency and supports a 1 Mbyte address space, allowing execution of instructions at high speed. In addition, the CPU core integrates a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.

Integration of many peripheral functions, including multifunction timer and serial interface, helps reduce the number of system components.

The R8C/L35A Group, R8C/L36A Group, R8C/L38A Group, and R8C/L3AA Group have data flash (1 KB × 4 blocks) with the background operation (BGO) function.

#### 1.1.1 Applications

Household appliances, office equipment, audio equipment, consumer products, etc.

## 1.1.2 Differences between Groups

Tables 1.1 and 1.2 list the differences between the groups, Table 1.3 lists the I/O ports provided for each group, and Table 1.4 lists the LCD Display Function Pins Provided for Each Group. Figures 1.13 to 1.17 show the pin assignment for each group, and Tables 1.8 to 1.15 list product information.

The explanations in the chapters which follow apply to the R8C/L3AA Group only. Note the differences shown below.

**Table 1.1 Differences between Groups (1)**

| Item       | Function   | R8C/L35A Group, R8C/L36A Group<br>R8C/L38A Group, R8C/L3AA Group | R8C/L35B Group, R8C/L36B Group<br>R8C/L38B Group, R8C/L3AB Group |
|------------|--|--|--|
| Data flash | 1 KB × 4 blocks with BGO (background operation) function | Provided   | Not provided   |

**Table 1.2 Differences between Groups (2)**

| Item                      | Function                               | R8C/L35A Group<br>R8C/L35B Group | R8C/L36A Group<br>R8C/L36B Group | R8C/L38A Group<br>R8C/L38B Group | R8C/L3AA Group<br>R8C/L3AB Group |
|---------------------------|--|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| I/O Ports                 | Programmable I/O ports                 | 41 pins                          | 52 pins                          | 68 pins                          | 88 pins                          |
|                           | High current drive ports               | 5 pins                           | 8 pins                           | 8 pins                           | 16 pins                          |
| Interrupts                | $\overline{\text{INT}}$ interrupt pins | 5 pins                           | 8 pins                           | 8 pins                           | 8 pins                           |
|                           | Key input interrupt pins               | 4 pins                           | 4 pins                           | 8 pins                           | 8 pins                           |
| Timers                    | Timer RA pins (I/O: 1, output: 1)      | 1 pin (I/O pin only)             | 2 pins                           | 2 pins                           | 2 pins                           |
|                           | Timer RB pin (output: 1)               | None                             | 1 pin                            | 1 pin                            | 1 pin                            |
|                           | Timer RD pin (I/O: 8)                  | None                             | None                             | 8 pins                           | 8 pins                           |
|                           | Timer RE pin (output: 1)               | None                             | 1 pin                            | 1 pin                            | 1 pin                            |
|                           | Timer RG pin (I/O: 2, output: 2)       | None                             | None                             | None                             | 4 pins                           |
| A/D Converter             | Analog input pin                       | 10 pins                          | 10 pins                          | 16 pins                          | 20 pins                          |
| LCD Drive Control Circuit | LCD power supply                       | 3 pins (VL1, VL2, VL4)           | 4 pins (VL1 to VL4)              | 4 pins (VL1 to VL4)              | 4 pins (VL1 to VL4)              |
|                           | Common output pins                     | Max. 4 pins                      | Max. 8 pins                      | Max. 8 pins                      | Max. 8 pins                      |
|                           | Segment output pins                    | Max. 24 pins                     | Max. 32 pins                     | Max. 48 pins                     | Max. 56 pins                     |
| Other Pin Function        | $\overline{\text{WKUP1}}$              | Not supported                    | Not supported                    | Supported                        | Supported                        |
| Packages                  |  | 52-pin LQFP                      | 64-pin LQFP                      | 80-pin LQFP                      | 100-pin LQFP/<br>100-pin QFP     |

Note:

- I/O ports are shared with I/O functions, such as interrupts or timers. Refer to Tables 1.16 to 1.18, Pin Name Information by Pin Number, for details.

**Table 1.3 Programmable I/O Ports Provided for Each Group**

| Programmable I/O Port | R8C/L35A Group<br>R8C/L35B Group<br>Total: 41 I/O pins |       |       |       |       |       |       |       | R8C/L36A Group<br>R8C/L36B Group<br>Total: 52 I/O pins |       |       |       |       |       |       |       | R8C/L38A Group<br>R8C/L38B Group<br>Total: 68 I/O pins |       |       |       |       |       |       |       | R8C/L3AA Group<br>R8C/L3AB Group<br>Total: 88 I/O pins |       |       |       |       |       |       |       |
|-----------------------|--|-------|-------|-------|-------|-------|-------|-------|--|-------|-------|-------|-------|-------|-------|-------|--|-------|-------|-------|-------|-------|-------|-------|--|-------|-------|-------|-------|-------|-------|-------|
|                       | bit 7  | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | bit 7  | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | bit 7  | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | bit 7  | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| P0                    | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     |       |       |
| P1                    | -  | -     | -     | -     | -     | -     | -     | -     | -  | -     | -     | -     | -     | -     | -     | -     | -  | -     | -     | -     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     |       |       |       |
| P2                    | ✓  | ✓     | ✓     | ✓     | -     | -     | -     | -     | ✓  | ✓     | ✓     | ✓     | -     | -     | -     | -     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     |       |       |       |
| P3                    | -  | -     | -     | -     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     |       |       |       |
| P4                    | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     |       |       |       |
| P5                    | -  | -     | -     | -     | -     | -     | -     | -     | -  | -     | -     | -     | -     | -     | -     | -     | -  | -     | -     | -     | -     | -     | -     | -     | -  | -     | -     | -     | ✓     |       |       |       |
| P6                    | -  | -     | -     | -     | -     | -     | -     | -     | -  | -     | -     | -     | -     | -     | -     | -     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     |       |       |       |
| P7                    | ✓  | ✓     | ✓     | ✓     | -     | -     | -     | -     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     |       |       |       |
| P10                   | -  | -     | -     | -     | -     | -     | -     | -     | -  | -     | -     | -     | -     | -     | -     | -     | -  | -     | -     | -     | -     | -     | -     | -     | -  | -     | -     | -     | ✓     |       |       |       |
| P11                   | -  | -     | -     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     |       |       |       |
| P12                   | -  | -     | -     | -     | ✓     | ✓     | ✓     | ✓     | -  | -     | -     | -     | ✓     | ✓     | ✓     | ✓     | -  | -     | -     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     |       |       |       |
| P13                   | -  | -     | -     | -     | ✓     | ✓     | ✓     | ✓     | -  | -     | -     | -     | ✓     | ✓     | ✓     | ✓     | -  | -     | -     | ✓     | ✓     | ✓     | ✓     | ✓     | ✓  | ✓     | ✓     | ✓     | ✓     |       |       |       |

Notes:

- The symbol “✓” indicates a programmable I/O port.
- The symbol “-” indicates the settings should be made as follows:
  - Set 1 to the corresponding PDi (i = 0 to 7 and 10 to 13) register. When read, the content is 1.
  - Set 0 to the corresponding Pi (i = 0 to 7 and 10 to 13) register. When read, the content is 0.
  - Set 0 to the corresponding P10DRR or P11DRR register. When read, the content is 0.

**Table 1.4 LCD Display Function Pins Provided for Each Group**

| Shared I/O Port | L35A, L35B Group<br>Common output: Max. 4<br>Segment output: Max. 24 |        |        |        |        |        |        |        | L36A, L36B Group<br>Common output: Max. 8<br>Segment output: Max. 32 |        |        |        |        |        |        |        | L38A, L38B Group<br>Common output: Max. 8<br>Segment output: Max. 48 |        |        |        |        |        |        |        | L3AA, L3AB Group<br>Common output: Max. 8<br>Segment output: Max. 56 |        |        |        |        |        |        |        |        |        |   |
|-----------------|--|--------|--------|--------|--------|--------|--------|--------|--|--------|--------|--------|--------|--------|--------|--------|--|--------|--------|--------|--------|--------|--------|--------|--|--------|--------|--------|--------|--------|--------|--------|--------|--------|---|
|                 | SEG 7  | SEG 6  | SEG 5  | SEG 4  | SEG 3  | SEG 2  | SEG 1  | SEG 0  | SEG 7  | SEG 6  | SEG 5  | SEG 4  | SEG 3  | SEG 2  | SEG 1  | SEG 0  | SEG 7  | SEG 6  | SEG 5  | SEG 4  | SEG 3  | SEG 2  | SEG 1  | SEG 0  | SEG 7  | SEG 6  | SEG 5  | SEG 4  | SEG 3  | SEG 2  | SEG 1  | SEG 0  |        |        |   |
| P0              | -  | -      | -      | -      | -      | -      | -      | -      | -  | -      | -      | -      | -      | -      | -      | -      | -  | -      | -      | -      | -      | -      | -      | -      | -  | -      | -      | -      | -      | -      |        |        |        |        |   |
| P1              | -  | -      | -      | -      | -      | -      | -      | -      | -  | -      | -      | -      | -      | -      | -      | -      | -  | -      | -      | -      | SEG 11 | SEG 10 | SEG 9  | SEG 8  | SEG 15   | SEG 14 | SEG 13 | SEG 12 | SEG 11 | SEG 10 | SEG 9  | SEG 8  |        |        |   |
| P2              | SEG 23   | SEG 22 | SEG 21 | SEG 20 | -      | -      | -      | -      | SEG 23   | SEG 22 | SEG 21 | SEG 20 | -      | -      | -      | -      | SEG 23   | SEG 22 | SEG 21 | SEG 20 | SEG 19 | SEG 18 | SEG 17 | SEG 16 | SEG 23   | SEG 22 | SEG 21 | SEG 20 | SEG 19 | SEG 18 | SEG 17 | SEG 16 |        |        |   |
| P3              | -  | -      | -      | -      | SEG 27 | SEG 26 | SEG 25 | SEG 24 | SEG 31   | SEG 30 | SEG 29 | SEG 28 | SEG 27 | SEG 26 | SEG 25 | SEG 24 | SEG 31   | SEG 30 | SEG 29 | SEG 28 | SEG 27 | SEG 26 | SEG 25 | SEG 24 | SEG 31   | SEG 30 | SEG 29 | SEG 28 | SEG 27 | SEG 26 | SEG 25 | SEG 24 |        |        |   |
| P4              | SEG 39   | SEG 38 | SEG 37 | SEG 36 | SEG 35 | SEG 34 | SEG 33 | SEG 32 | SEG 39   | SEG 38 | SEG 37 | SEG 36 | SEG 35 | SEG 34 | SEG 33 | SEG 32 | SEG 39   | SEG 38 | SEG 37 | SEG 36 | SEG 35 | SEG 34 | SEG 33 | SEG 32 | SEG 39   | SEG 38 | SEG 37 | SEG 36 | SEG 35 | SEG 34 | SEG 33 | SEG 32 |        |        |   |
| P5              | -  | -      | -      | -      | -      | -      | -      | -      | -  | -      | -      | -      | -      | -      | -      | -      | -  | -      | -      | -      | -      | -      | -      | -      | -  | -      | -      | -      | -      | -      | SEG 43 | SEG 42 | SEG 41 | SEG 40 |   |
| P6              | -  | -      | -      | -      | -      | -      | -      | -      | -  | -      | -      | -      | -      | -      | -      | -      | SEG 51   | SEG 50 | SEG 49 | SEG 48 | SEG 47 | SEG 46 | SEG 45 | SEG 44 | SEG 51   | SEG 50 | SEG 49 | SEG 48 | SEG 47 | SEG 46 | SEG 45 | SEG 44 |        |        |   |
| P7              | COM 0  | COM 1  | COM 2  | COM 3  | -      | -      | -      | -      | COM 0  | COM 1  | COM 2  | COM 3  | SEG 55 | SEG 54 | SEG 53 | SEG 52 | COM 0  | COM 1  | COM 2  | COM 3  | SEG 55 | SEG 54 | SEG 53 | SEG 52 | COM 0  | COM 1  | COM 2  | COM 3  | SEG 55 | SEG 54 | SEG 53 | SEG 52 |        |        |   |
| P12             | -  | -      | -      | -      | CL2    | CL1    | -      | -      | -  | -      | -      | -      | CL2    | CL1    | -      | -      | -  | -      | -      | -      | -      | -      | -      | -      | -  | -      | -      | -      | -      | -      | -      | CL2    | CL1    | -      | - |
| -               | VL1  |        |        |        |        |        |        |        | VL1  |        |        |        |        |        |        |        | VL1  |        |        |        |        |        |        |        | VL1  |        |        |        |        |        |        |        |        |        |   |
| -               | VL2  |        |        |        |        |        |        |        | VL2  |        |        |        |        |        |        |        | VL2  |        |        |        |        |        |        |        | VL2  |        |        |        |        |        |        |        |        |        |   |
| -               | -  |        |        |        |        |        |        |        | VL3  |        |        |        |        |        |        |        | VL3  |        |        |        |        |        |        |        | VL3  |        |        |        |        |        |        |        |        |        |   |
| -               | VL4  |        |        |        |        |        |        |        | VL4  |        |        |        |        |        |        |        | VL4  |        |        |        |        |        |        |        | VL4  |        |        |        |        |        |        |        |        |        |   |

Notes:

- The symbol “-” indicates there is no LCD display function. Select the I/O port function with registers LSE1 to LSE7 for these pins.
- SEG52 to SEG55 can be used as COM7 to COM4.
- The R8C/L35A Group and R8C/L35B Group do not have the VL3 pin.  
 The available bias settings are 1/3 bias, 1/2 bias, or static.

### 1.1.3 Specifications

Tables 1.5 to 1.7 list the specifications.

**Table 1.5 Specifications (1)**

| Item                           | Function  | Specification   |   |
|--------------------------------|---|---|---|
| CPU                            | Central processing unit   | R8C CPU core <ul style="list-style-type: none"> <li>• Number of fundamental instructions: 89</li> <li>• Minimum instruction execution time:                             <ul style="list-style-type: none"> <li>50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)</li> <li>200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V)</li> </ul> </li> <li>• Multiplier: 16 bits × 16 bits → 32 bits</li> <li>• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits</li> <li>• Operating mode: Single-chip mode (address space: 1 Mbyte)</li> </ul>  |   |
| Memory                         | ROM/RAM<br>Data flash   | Refer to Tables 1.8 to 1.15 Product Lists.  |   |
| Power Supply Voltage Detection | Voltage detection circuit   | <ul style="list-style-type: none"> <li>• Power-on reset</li> <li>• Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)</li> </ul>   |   |
| I/O Ports                      | Programmable I/O ports  | R8C/L35A Group  | <ul style="list-style-type: none"> <li>• CMOS I/O ports: 41, selectable pull-up resistor</li> <li>• High current drive ports: 5</li> </ul>  |
|                                |   | R8C/L35B Group  |   |
|                                |   | R8C/L36A Group  | <ul style="list-style-type: none"> <li>• CMOS I/O ports: 52, selectable pull-up resistor</li> <li>• High current drive ports: 8</li> </ul>  |
|                                |   | R8C/L36B Group  |   |
|                                |   | R8C/L38A Group  | <ul style="list-style-type: none"> <li>• CMOS I/O ports: 68, selectable pull-up resistor</li> <li>• High current drive ports: 8</li> </ul>  |
| R8C/L38B Group                 |   |   |   |
| R8C/L3AA Group                 | <ul style="list-style-type: none"> <li>• CMOS I/O ports: 88, selectable pull-up resistor</li> <li>• High current drive ports: 16</li> </ul>   |   |   |
| R8C/L3AB Group                 |   |   |   |
| Clock                          | Clock generation circuits   | 4 circuits: XIN clock oscillation circuit<br>XCIN clock oscillation circuit (32 kHz)<br>High-speed on-chip oscillator (with frequency adjustment function)<br>Low-speed on-chip oscillator  |   |
|                                |   | <ul style="list-style-type: none"> <li>• Oscillation stop detection:                             <ul style="list-style-type: none"> <li>XIN clock oscillation stop detection function</li> </ul> </li> <li>• Frequency divider circuit:                             <ul style="list-style-type: none"> <li>Division ratio selectable from 1, 2, 4, 8, and 16</li> </ul> </li> <li>• Low-power-consumption modes:                             <ul style="list-style-type: none"> <li>Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode, power-off mode</li> </ul> </li> </ul> |   |
| Interrupts                     |   | Real-time clock (timer RE)  |   |
|                                |   | R8C/L35A Group  | <ul style="list-style-type: none"> <li>• Number of interrupt vectors: 69</li> <li>• External Interrupt: 9 (<math>\overline{\text{INT}} \times 5</math>, key input × 4)</li> <li>• Priority levels: 7 levels</li> </ul>  |
|                                |   | R8C/L35B Group  |   |
|                                |   | R8C/L36A Group  | <ul style="list-style-type: none"> <li>• Number of interrupt vectors: 69</li> <li>• External Interrupt: 12 (<math>\overline{\text{INT}} \times 8</math>, key input × 4)</li> <li>• Priority levels: 7 levels</li> </ul> |
| R8C/L36B Group                 |   |   |   |
| R8C/L38A Group                 | <ul style="list-style-type: none"> <li>• Number of interrupt vectors: 69</li> <li>• External Interrupt: 16 (<math>\overline{\text{INT}} \times 8</math>, key input × 8)</li> <li>• Priority levels: 7 levels</li> </ul> |   |   |
| R8C/L38B Group                 |   |   |   |
| R8C/L3AA Group                 | <ul style="list-style-type: none"> <li>• Number of interrupt vectors: 69</li> <li>• External Interrupt: 16 (<math>\overline{\text{INT}} \times 8</math>, key input × 8)</li> <li>• Priority levels: 7 levels</li> </ul> |   |   |
| R8C/L3AB Group                 |   |   |   |
| Watchdog Timer                 |   | <ul style="list-style-type: none"> <li>• 14 bits × 1 (with prescaler)</li> <li>• Selectable reset start function</li> <li>• Selectable low-speed on-chip oscillator for watchdog timer</li> </ul>   |   |
| DTC (Data Transfer Controller) |   | <ul style="list-style-type: none"> <li>• 1 channel</li> <li>• Activation sources: 38</li> <li>• Transfer modes: 2 (normal mode, repeat mode)</li> </ul>   |   |

**Table 1.6 Specifications (2)**

| Item  | Function  | Specification   |   |
|---|---|---|---|
| Timer                                       | Timer RA  | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode   |   |
|   | Timer RB  | 8 bits × 1 (with 8-bit prescaler)<br>Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode   |   |
|   | Timer RC  | 16 bits × 1 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)  |   |
|   | Timer RD  | 16 bits × 2 (with 4 capture/compare registers)<br>Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output: 6 pins, sawtooth wave modulation), complementary PWM mode (three-phase waveform output: 6 pins, triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins) |   |
|   | Timer RE  | 8 bits × 1<br>Real-time clock mode (counting of seconds, minutes, hours, days of week), output compare mode   |   |
|   | Timer RG  | 16 bits × 1<br>Phase-counting mode, timer mode (output compare function, input capture function), PWM mode (output: 1 pin)  |   |
| Serial Interface                            | UART0, UART1  | Clock synchronous serial I/O/UART × 2 channels  |   |
|   | UART2   | Clock synchronous serial I/O/UART, I <sup>2</sup> C mode (I <sup>2</sup> C-bus), multiprocessor communication function  |   |
| Synchronous Serial Communication Unit (SSU) |   | 1 (shared with I <sup>2</sup> C-bus)  |   |
| I <sup>2</sup> C bus                        |   | 1 (shared with SSU)   |   |
| LIN Module                                  |   | Hardware LIN: 1 channel (timer RA, UART0 used)  |   |
| A/D Converter                               | R8C/L35A Group<br>R8C/L35B Group                      | 10-bit resolution × 10 channels, including sample and hold function, with sweep mode  |   |
|   | R8C/L36A Group<br>R8C/L36B Group                      | 10-bit resolution × 10 channels, including sample and hold function, with sweep mode  |   |
|   | R8C/L38A Group<br>R8C/L38B Group                      | 10-bit resolution × 16 channels, including sample and hold function, with sweep mode  |   |
|   | R8C/L3AA Group<br>R8C/L3AB Group                      | 10-bit resolution × 20 channels, including sample and hold function, with sweep mode  |   |
|   | D/A Converter   |   | 8-bit resolution × 2 circuits                           |
| Comparator A                                |   | <ul style="list-style-type: none"> <li>• 2 circuits (shared with voltage monitor 1 and voltage monitor 2)</li> <li>• External reference voltage input available</li> </ul>  |   |
| Comparator B                                |   | 2 circuits  |   |
| LCD Drive Control Circuit                   | R8C/L35A Group<br>R8C/L35B Group                      | Common output: Max. 4 pins<br>Segment output: Max. 24 pins  | Bias: 1/2, 1/3<br>Duty: static, 1/2, 1/3, 1/4           |
|   | R8C/L36A Group<br>R8C/L36B Group                      | Common output: Max. 8 pins<br>Segment output: Max. 32 pins <sup>(1)</sup>   |   |
|   | R8C/L38A Group<br>R8C/L38B Group                      | Common output: Max. 8 pins<br>Segment output: Max. 48 pins <sup>(1)</sup>   | Bias: 1/2, 1/3, 1/4<br>Duty: static, 1/2, 1/3, 1/4, 1/8 |
|   | R8C/L3AA Group<br>R8C/L3AB Group                      | Common output: Max. 8 pins<br>Segment output: Max. 56 pins <sup>(1)</sup>   |   |
|   | Voltage multiplier and dedicated regulator integrated |   |   |

Note:

1. This applies when four pins are selected for common output.

**Table 1.7 Specifications (2)**

| Item                                   | Function   | Specification  |
|--|--|--|
| Flash Memory                           | R8C/L35A Group<br>R8C/L36A Group<br>R8C/L38A Group<br>R8C/L3AA Group | <ul style="list-style-type: none"> <li>• Programming and erasure voltage: VCC = 2.7 to 5.5 V</li> <li>• Programming and erasure endurance: 10,000 times (data flash)<br/>1,000 times (program ROM)</li> <li>• Program security: ROM code protect, ID code check</li> <li>• Debug functions: On-chip debug, on-board flash rewrite function</li> <li>• Background operation (BGO) function</li> </ul> |
|  | R8C/L35B Group<br>R8C/L36B Group<br>R8C/L38B Group<br>R8C/L3AB Group | <ul style="list-style-type: none"> <li>• Programming and erasure voltage: VCC = 2.7 to 5.5 V</li> <li>• Programming and erasure endurance: 1,000 times</li> <li>• Program security: ROM code protect, ID code check</li> <li>• Debug functions: On-chip debug, on-board flash rewrite function</li> </ul>  |
| Operating Frequency/<br>Supply Voltage |  | f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)<br>f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)  |
| Current Consumption                    |  | Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)<br>Typ. 3.6 mA (VCC = 3.0 V, f(XIN) = 10 MHz)<br>Typ. 3.5 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz))<br>Typ. 2 μA (VCC = 3.0 V, stop mode)<br>Typ. 1 μA (VCC = 3.0 V, power-off mode, timer RE enabled)<br>Typ. 0.02 μA (VCC = 3.0 V, power-off mode, timer RE disabled)  |
| Operating Ambient Temperature          |  | -20 to 85°C (N version)<br>-40 to 85°C (D version) <sup>(1)</sup>  |

Note:

1. Specify the D version if D version functions are to be used.



## 1.2 Product Lists

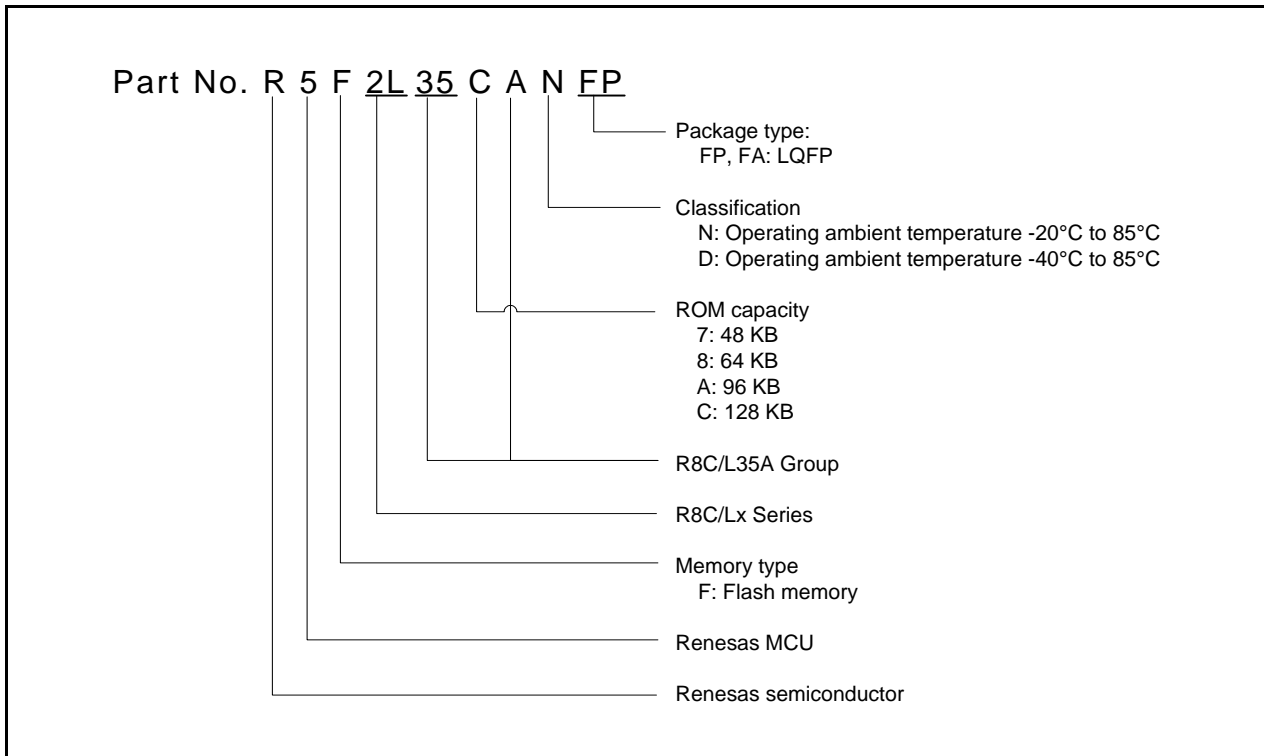
Tables 1.8 to 1.15 list product information for each group. Figure 1.1 to 1.8 show the Correspondence of Part No., with Memory Size and Package of R8C/Lx Group.

**Table 1.8 Product List for R8C/L35A Group**

**Current of Jan 2009**

| Part No.         | Internal ROM Capacity |             | Internal RAM Capacity | Package Type | Remarks   |
|------------------|-----------------------|-------------|-----------------------|--------------|-----------|
|                  | Program ROM           | Data Flash  |                       |              |           |
| R5F2L357ANFP (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PLQP0052JA-A | N Version |
| R5F2L358ANFP (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PLQP0052JA-A |           |
| R5F2L35AANFP (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PLQP0052JA-A |           |
| R5F2L35CANFP (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PLQP0052JA-A |           |
| R5F2L357ADFP (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PLQP0052JA-A | D Version |
| R5F2L358ADFP (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PLQP0052JA-A |           |
| R5F2L35AADFP (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PLQP0052JA-A |           |
| R5F2L35CADFP (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PLQP0052JA-A |           |

(D): Under development



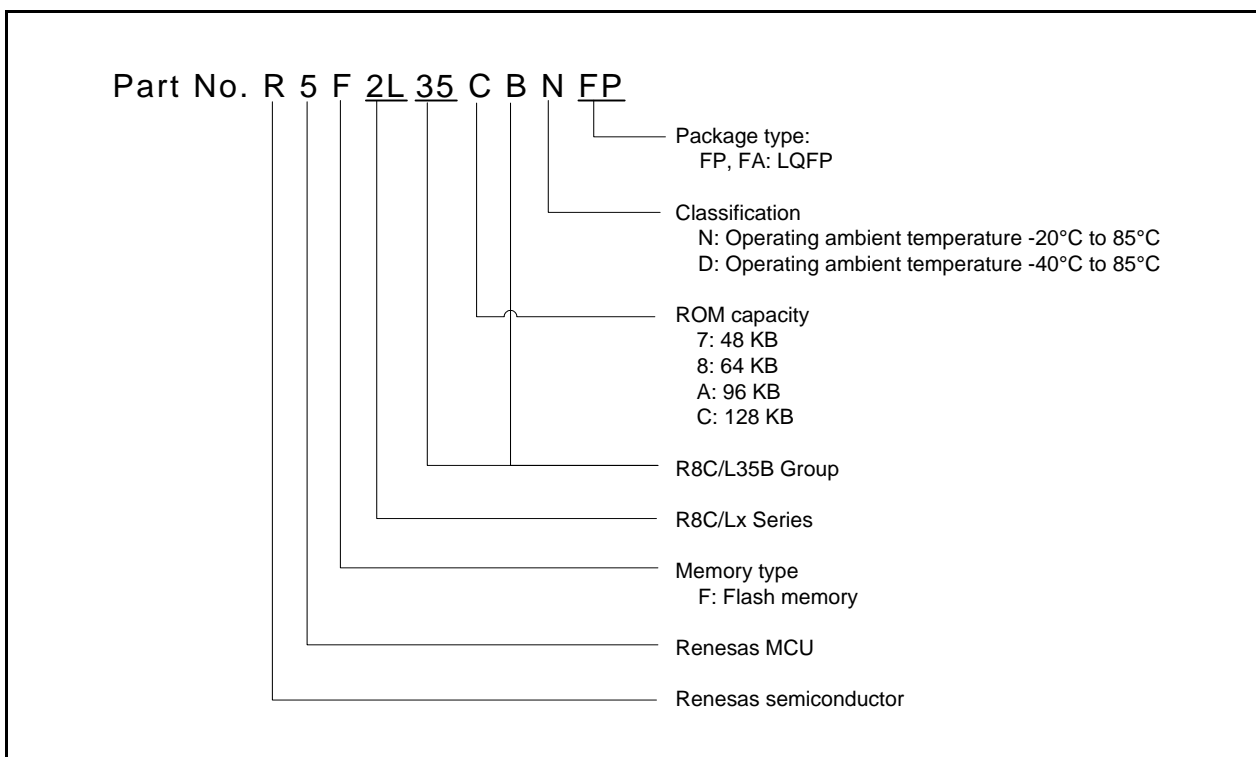
**Figure 1.1 Correspondence of Part No., with Memory Size and Package of R8C/L35A Group**

**Table 1.9 Product List for R8C/L35B Group**

**Current of Jan 2009**

| Part No.         | Internal ROM Capacity | Internal RAM Capacity | Package Type | Remarks   |
|------------------|-----------------------|-----------------------|--------------|-----------|
| R5F2L357BNFP (D) | 48 Kbytes             | 6 Kbytes              | PLQP0052JA-A | N Version |
| R5F2L358BNFP (D) | 64 Kbytes             | 8 Kbytes              | PLQP0052JA-A |           |
| R5F2L35ABNFP (D) | 96 Kbytes             | 10 Kbytes             | PLQP0052JA-A |           |
| R5F2L35CBNFP (D) | 128 Kbytes            | 10 Kbytes             | PLQP0052JA-A |           |
| R5F2L357BDFP (D) | 48 Kbytes             | 6 Kbytes              | PLQP0052JA-A | D Version |
| R5F2L358BDFP (D) | 64 Kbytes             | 8 Kbytes              | PLQP0052JA-A |           |
| R5F2L35ABDFP (D) | 96 Kbytes             | 10 Kbytes             | PLQP0052JA-A |           |
| R5F2L35CBDFP (D) | 128 Kbytes            | 10 Kbytes             | PLQP0052JA-A |           |

(D): Under development



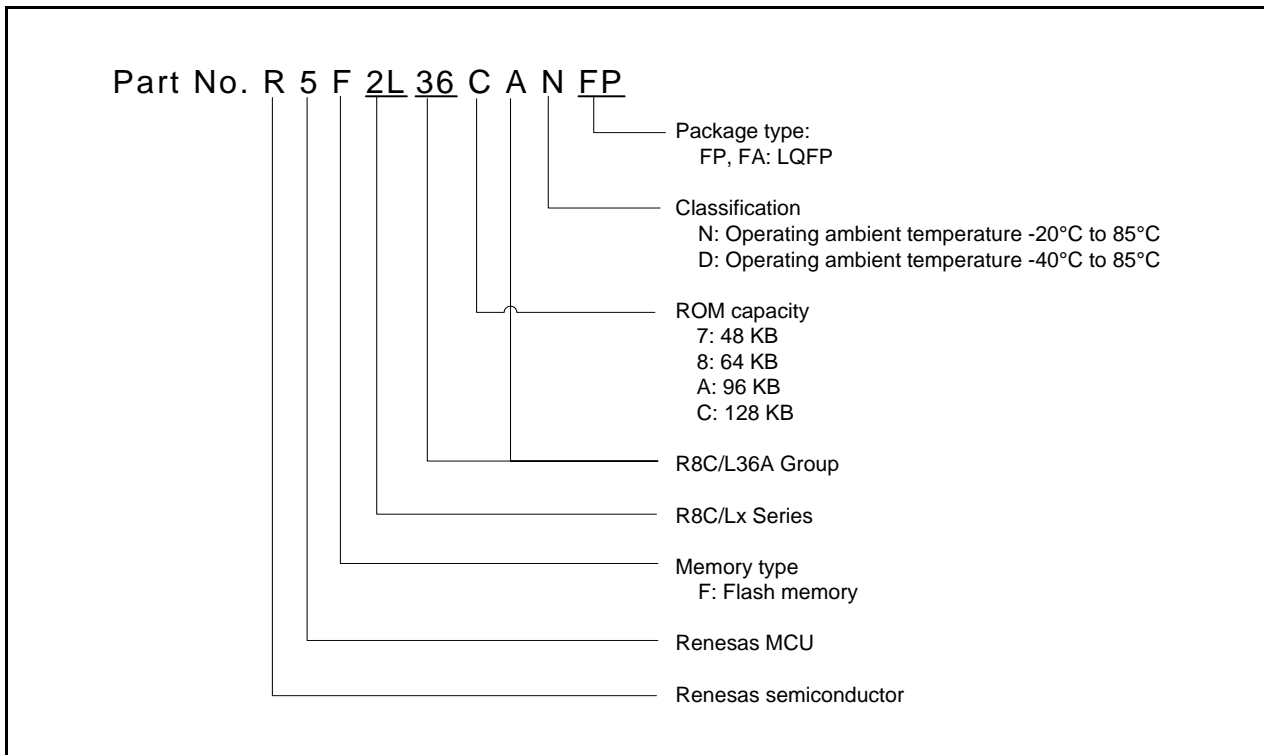
**Figure 1.2 Correspondence of Part No., with Memory Size and Package of R8C/L35B Group**

**Table 1.10 Product List for R8C/L36A Group**

**Current of Jan 2009**

| Part No.         | Internal ROM Capacity |             | Internal RAM Capacity | Package Type | Remarks   |
|------------------|-----------------------|-------------|-----------------------|--------------|-----------|
|                  | Program ROM           | Data Flash  |                       |              |           |
| R5F2L367ANFP (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PLQP0064KB-A | N Version |
| R5F2L367ANFA (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PLQP0064GA-A |           |
| R5F2L368ANFP (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PLQP0064KB-A |           |
| R5F2L368ANFA (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PLQP0064GA-A |           |
| R5F2L36AANFP (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PLQP0064KB-A |           |
| R5F2L36AANFA (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PLQP0064GA-A |           |
| R5F2L36CANFP (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PLQP0064KB-A |           |
| R5F2L36CANFA (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PLQP0064GA-A |           |
| R5F2L367ADFP (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PLQP0064KB-A | D Version |
| R5F2L367ADFA (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PLQP0064GA-A |           |
| R5F2L368ADFP (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PLQP0064KB-A |           |
| R5F2L368ADFA (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PLQP0064GA-A |           |
| R5F2L36AADFP (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PLQP0064KB-A |           |
| R5F2L36AADFA (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PLQP0064GA-A |           |
| R5F2L36CADFP (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PLQP0064KB-A |           |
| R5F2L36CADFA (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PLQP0064GA-A |           |

(D): Under development



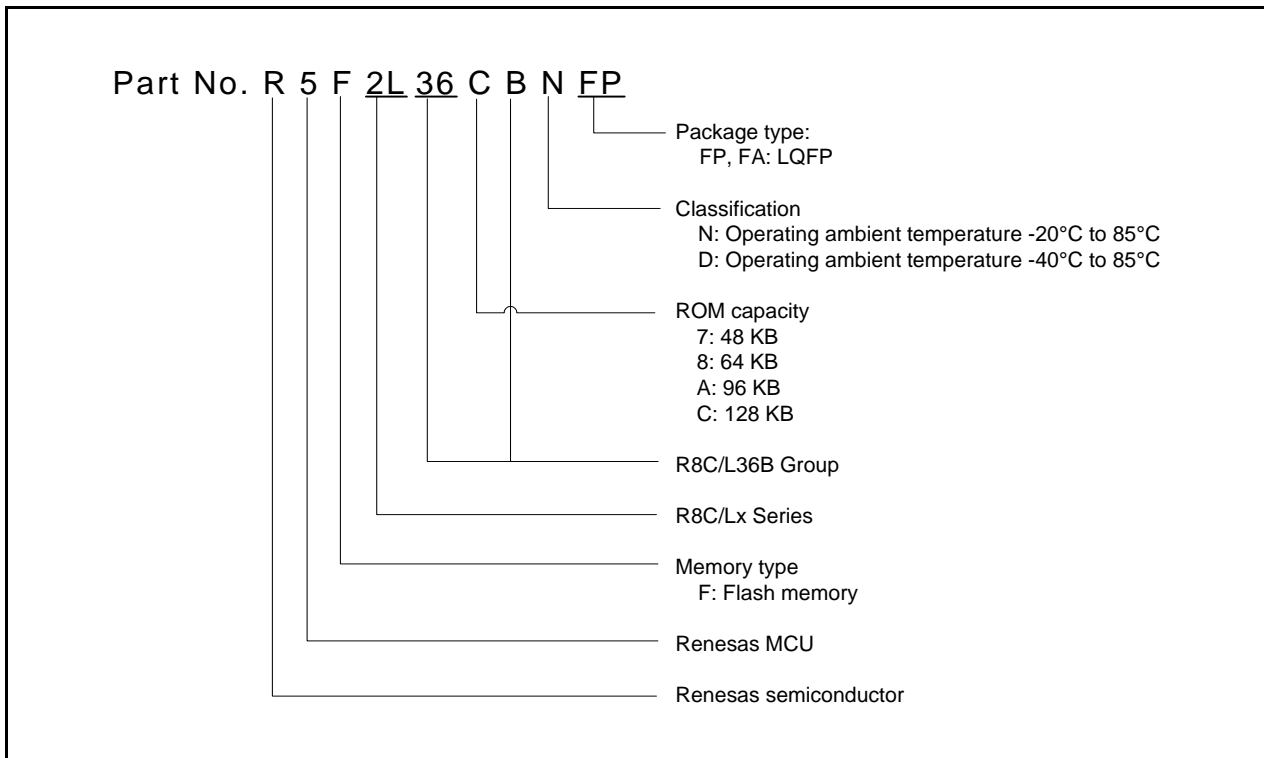
**Figure 1.3 Correspondence of Part No., with Memory Size and Package of R8C/L36A Group**

**Table 1.11 Product List for R8C/L36B Group**

**Current of Jan 2009**

| Part No.         | Internal ROM Capacity | Internal RAM Capacity | Package Type | Remarks   |
|------------------|-----------------------|-----------------------|--------------|-----------|
| R5F2L367BNFP (D) | 48 Kbytes             | 6 Kbytes              | PLQP0064KB-A | N Version |
| R5F2L367BNFA (D) | 48 Kbytes             | 6 Kbytes              | PLQP0064GA-A |           |
| R5F2L368BNFP (D) | 64 Kbytes             | 8 Kbytes              | PLQP0064KB-A |           |
| R5F2L368BNFA (D) | 64 Kbytes             | 8 Kbytes              | PLQP0064GA-A |           |
| R5F2L36ABNFP (D) | 96 Kbytes             | 10 Kbytes             | PLQP0064KB-A |           |
| R5F2L36ABNFA (D) | 96 Kbytes             | 10 Kbytes             | PLQP0064GA-A |           |
| R5F2L36CBNFP (D) | 128 Kbytes            | 10 Kbytes             | PLQP0064KB-A |           |
| R5F2L36CBNFA (D) | 128 Kbytes            | 10 Kbytes             | PLQP0064GA-A |           |
| R5F2L367BDFP (D) | 48 Kbytes             | 6 Kbytes              | PLQP0064KB-A | D Version |
| R5F2L367BDFA (D) | 48 Kbytes             | 6 Kbytes              | PLQP0064GA-A |           |
| R5F2L368BDFP (D) | 64 Kbytes             | 8 Kbytes              | PLQP0064KB-A |           |
| R5F2L368BDFA (D) | 64 Kbytes             | 8 Kbytes              | PLQP0064GA-A |           |
| R5F2L36ABDFP (D) | 96 Kbytes             | 10 Kbytes             | PLQP0064KB-A |           |
| R5F2L36ABDFA (D) | 96 Kbytes             | 10 Kbytes             | PLQP0064GA-A |           |
| R5F2L36CBDFP (D) | 128 Kbytes            | 10 Kbytes             | PLQP0064KB-A |           |
| R5F2L36CBDFA (D) | 128 Kbytes            | 10 Kbytes             | PLQP0064GA-A |           |

(D): Under development



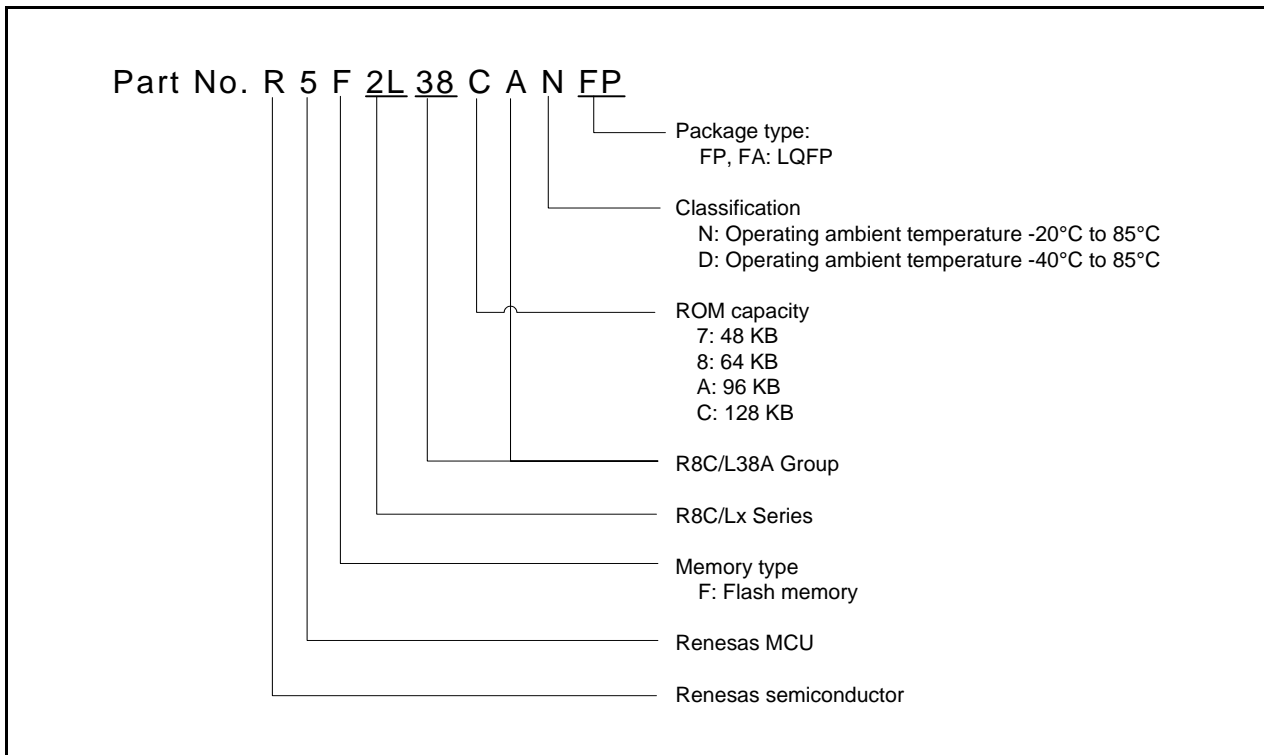
**Figure 1.4 Correspondence of Part No., with Memory Size and Package of R8C/L36B Group**

**Table 1.12 Product List for R8C/L38A Group**

**Current of Jan 2009**

| Part No.         | Internal ROM Capacity |             | Internal RAM Capacity | Package Type | Remarks   |
|------------------|-----------------------|-------------|-----------------------|--------------|-----------|
|                  | Program ROM           | Data Flash  |                       |              |           |
| R5F2L387ANFP (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PLQP0080KB-A | N Version |
| R5F2L387ANFA (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PLQP0080JA-A |           |
| R5F2L388ANFP (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PLQP0080KB-A |           |
| R5F2L388ANFA (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PLQP0080JA-A |           |
| R5F2L38AANFP (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PLQP0080KB-A |           |
| R5F2L38AANFA (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PLQP0080JA-A |           |
| R5F2L38CANFP (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PLQP0080KB-A |           |
| R5F2L38CANFA (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PLQP0080JA-A |           |
| R5F2L387ADFP (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PLQP0080KB-A | D Version |
| R5F2L387ADFA (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PLQP0080JA-A |           |
| R5F2L388ADFP (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PLQP0080KB-A |           |
| R5F2L388ADFA (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PLQP0080JA-A |           |
| R5F2L38AADFP (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PLQP0080KB-A |           |
| R5F2L38AADFA (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PLQP0080JA-A |           |
| R5F2L38CADFP (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PLQP0080KB-A |           |
| R5F2L38CADFA (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PLQP0080JA-A |           |

(D): Under development



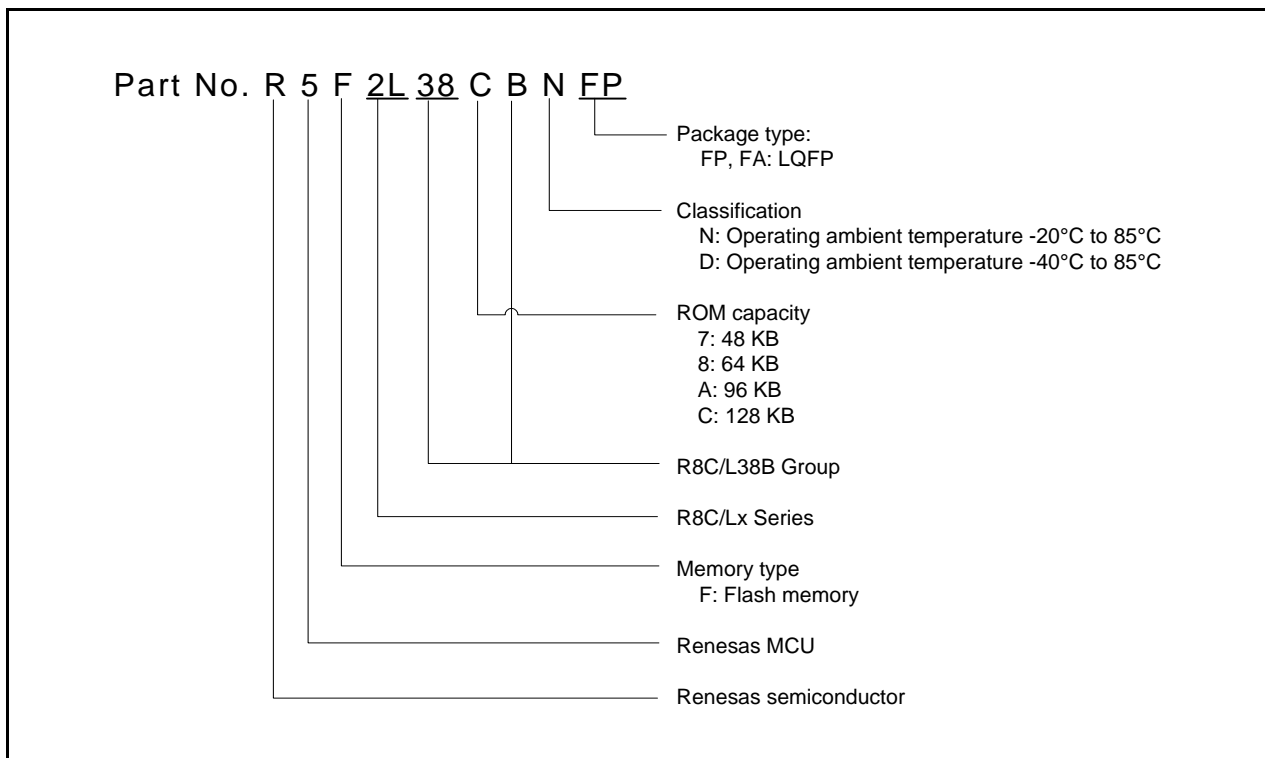
**Figure 1.5 Correspondence of Part No., with Memory Size and Package of R8C/L38A Group**

**Table 1.13 Product List for R8C/L38B Group**

**Current of Jan 2009**

| Part No.         | Internal ROM Capacity | Internal RAM Capacity | Package Type | Remarks   |
|------------------|-----------------------|-----------------------|--------------|-----------|
| R5F2L387BNFP (D) | 48 Kbytes             | 6 Kbytes              | PLQP0080KB-A | N Version |
| R5F2L387BNFA (D) | 48 Kbytes             | 6 Kbytes              | PLQP0080JA-A |           |
| R5F2L388BNFP (D) | 64 Kbytes             | 8 Kbytes              | PLQP0080KB-A |           |
| R5F2L388BNFA (D) | 64 Kbytes             | 8 Kbytes              | PLQP0080JA-A |           |
| R5F2L38ABNFP (D) | 96 Kbytes             | 10 Kbytes             | PLQP0080KB-A |           |
| R5F2L38ABNFA (D) | 96 Kbytes             | 10 Kbytes             | PLQP0080JA-A |           |
| R5F2L38CBNFP (D) | 128 Kbytes            | 10 Kbytes             | PLQP0080KB-A |           |
| R5F2L38CBNFA (D) | 128 Kbytes            | 10 Kbytes             | PLQP0080JA-A |           |
| R5F2L387BDFP (D) | 48 Kbytes             | 6 Kbytes              | PLQP0080KB-A | D Version |
| R5F2L387BDFA (D) | 48 Kbytes             | 6 Kbytes              | PLQP0080JA-A |           |
| R5F2L388BDFP (D) | 64 Kbytes             | 8 Kbytes              | PLQP0080KB-A |           |
| R5F2L388BDFA (D) | 64 Kbytes             | 8 Kbytes              | PLQP0080JA-A |           |
| R5F2L38ABDFP (D) | 96 Kbytes             | 10 Kbytes             | PLQP0080KB-A |           |
| R5F2L38ABDFA (D) | 96 Kbytes             | 10 Kbytes             | PLQP0080JA-A |           |
| R5F2L38CBDFP (D) | 128 Kbytes            | 10 Kbytes             | PLQP0080KB-A |           |
| R5F2L38CBDFA (D) | 128 Kbytes            | 10 Kbytes             | PLQP0080JA-A |           |

(D): Under development

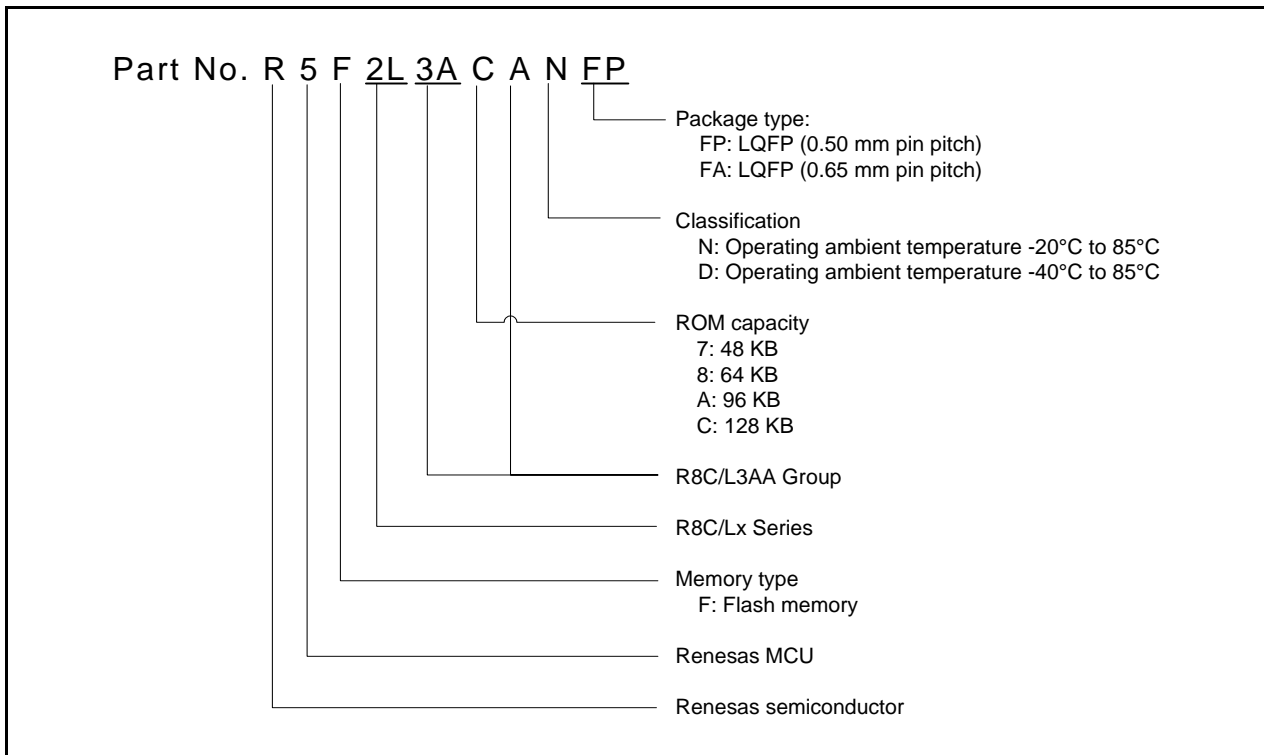


**Figure 1.6 Correspondence of Part No., with Memory Size and Package of R8C/L38B Group**

**Table 1.14 Product List for R8C/L3AA Group** **Current of Jan 2009**

| Part No.         | Internal ROM Capacity |             | Internal RAM Capacity | Package Type | Remarks   |
|------------------|-----------------------|-------------|-----------------------|--------------|-----------|
|                  | Program ROM           | Data Flash  |                       |              |           |
| R5F2L3A7ANFP (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PLQP0100KB-A | N Version |
| R5F2L3A7ANFA (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PRQP0100JD-B |           |
| R5F2L3A8ANFP (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PLQP0100KB-A |           |
| R5F2L3A8ANFA (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PRQP0100JD-B |           |
| R5F2L3AAANFP (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PLQP0100KB-A |           |
| R5F2L3AAANFA (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PRQP0100JD-B |           |
| R5F2L3ACANFP (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PLQP0100KB-A |           |
| R5F2L3ACANFA (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PRQP0100JD-B |           |
| R5F2L3A7ADFP (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PLQP0100KB-A | D Version |
| R5F2L3A7ADFA (D) | 48 Kbytes             | 1 Kbyte × 4 | 6 Kbytes              | PRQP0100JD-B |           |
| R5F2L3A8ADFP (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PLQP0100KB-A |           |
| R5F2L3A8ADFA (D) | 64 Kbytes             | 1 Kbyte × 4 | 8 Kbytes              | PRQP0100JD-B |           |
| R5F2L3AAADFP (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PLQP0100KB-A |           |
| R5F2L3AAADFA (D) | 96 Kbytes             | 1 Kbyte × 4 | 10 Kbytes             | PRQP0100JD-B |           |
| R5F2L3ACADFP (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PLQP0100KB-A |           |
| R5F2L3ACADFA (D) | 128 Kbytes            | 1 Kbyte × 4 | 10 Kbytes             | PRQP0100JD-B |           |

(D): Under development



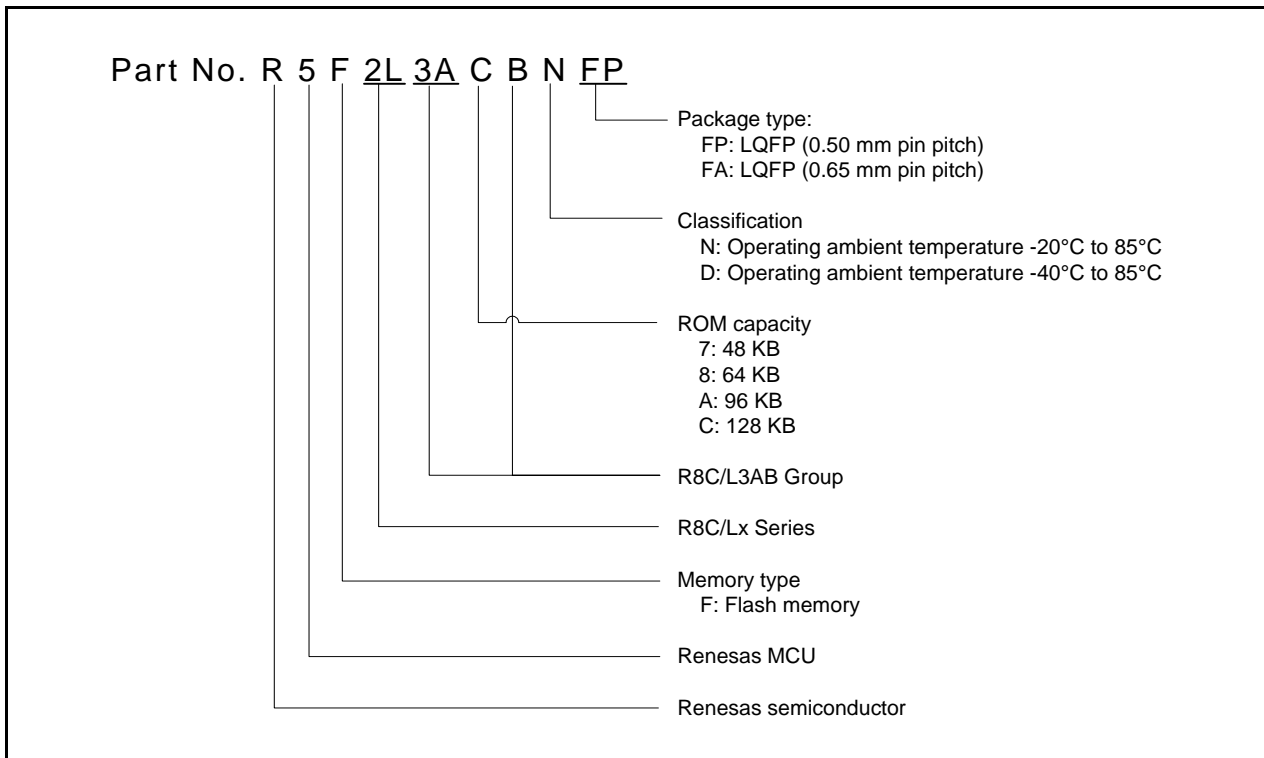
**Figure 1.7 Correspondence of Part No., with Memory Size and Package of R8C/L3AA Group**

**Table 1.15 Product List for R8C/L3AB Group**

**Current of Jan 2009**

| Part No.         | Internal ROM Capacity | Internal RAM Capacity | Package Type | Remarks   |
|------------------|-----------------------|-----------------------|--------------|-----------|
| R5F2L3A7BNFP (D) | 48 Kbytes             | 6 Kbytes              | PLQP0100KB-A | N Version |
| R5F2L3A7BNFA (D) | 48 Kbytes             | 6 Kbytes              | PRQP0100JD-B |           |
| R5F2L3A8BNFP (D) | 64 Kbytes             | 8 Kbytes              | PLQP0100KB-A |           |
| R5F2L3A8BNFA (D) | 64 Kbytes             | 8 Kbytes              | PRQP0100JD-B |           |
| R5F2L3AABNFP (D) | 96 Kbytes             | 10 Kbytes             | PLQP0100KB-A |           |
| R5F2L3AABNFA (D) | 96 Kbytes             | 10 Kbytes             | PRQP0100JD-B |           |
| R5F2L3ACBNFP (D) | 128 Kbytes            | 10 Kbytes             | PLQP0100KB-A |           |
| R5F2L3ACBNFA (D) | 128 Kbytes            | 10 Kbytes             | PRQP0100JD-B |           |
| R5F2L3A7BDFP (D) | 48 Kbytes             | 6 Kbytes              | PLQP0100KB-A | D Version |
| R5F2L3A7BDFA (D) | 48 Kbytes             | 6 Kbytes              | PRQP0100JD-B |           |
| R5F2L3A8BDFP (D) | 64 Kbytes             | 8 Kbytes              | PLQP0100KB-A |           |
| R5F2L3A8BDFA (D) | 64 Kbytes             | 8 Kbytes              | PRQP0100JD-B |           |
| R5F2L3AABDFP (D) | 96 Kbytes             | 10 Kbytes             | PLQP0100KB-A |           |
| R5F2L3AABDFA (D) | 96 Kbytes             | 10 Kbytes             | PRQP0100JD-B |           |
| R5F2L3ACBDFP (D) | 128 Kbytes            | 10 Kbytes             | PLQP0100KB-A |           |
| R5F2L3ACBDFA (D) | 128 Kbytes            | 10 Kbytes             | PRQP0100JD-B |           |

(D): Under development



**Figure 1.8 Correspondence of Part No., with Memory Size and Package of R8C/L3AB Group**



### 1.3 Block Diagrams

Figure 1.9 shows a Block Diagram of R8C/L35A and R8C/L35B Groups. Figure 1.10 shows a Block Diagram of R8C/L36A and R8C/L36B Groups. Figure 1.11 shows a Block Diagram of R8C/L38A and R8C/L38B Groups. Figure 1.12 shows a Block Diagram of R8C/L3AA and R8C/L3AB Groups.

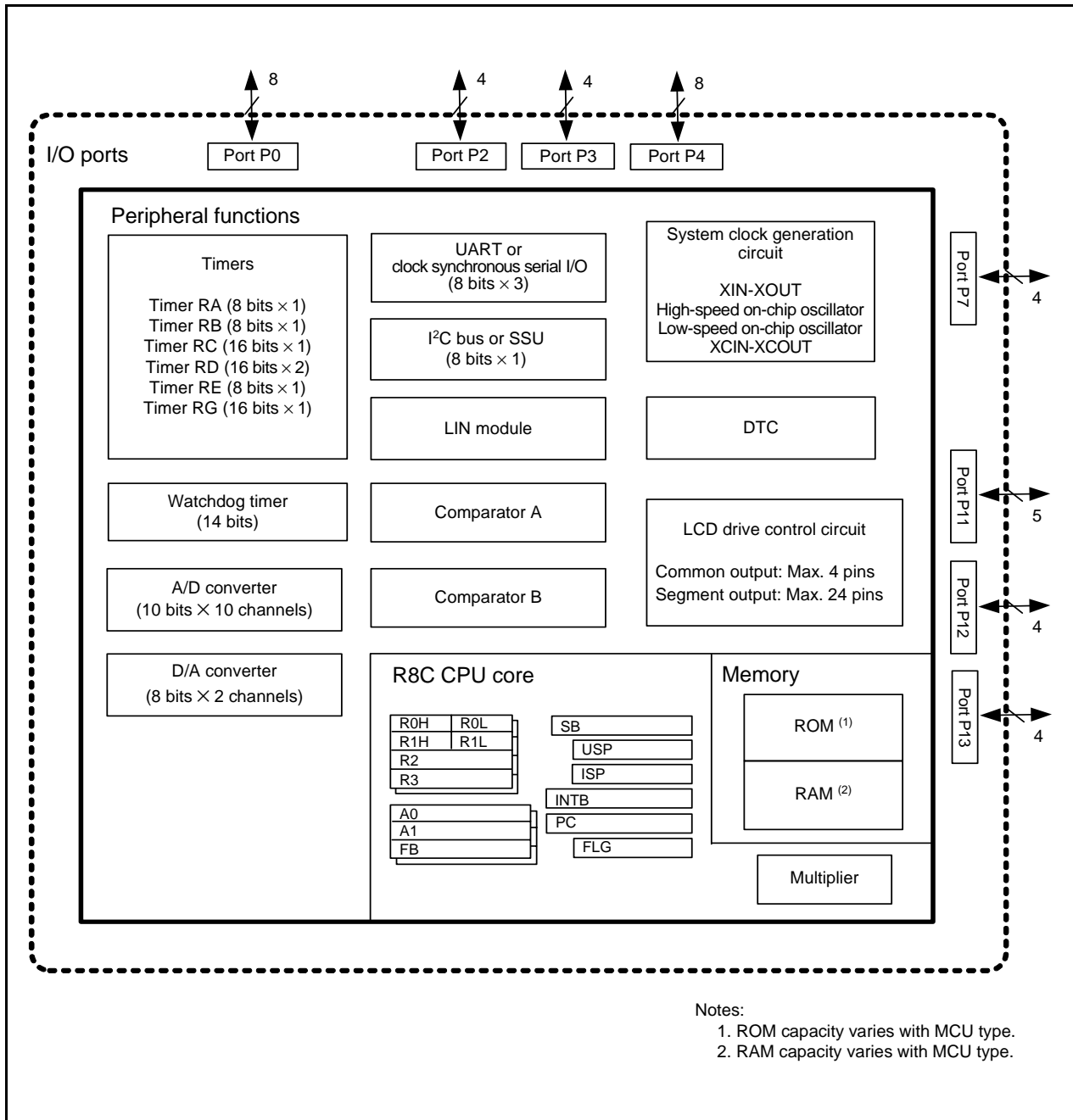
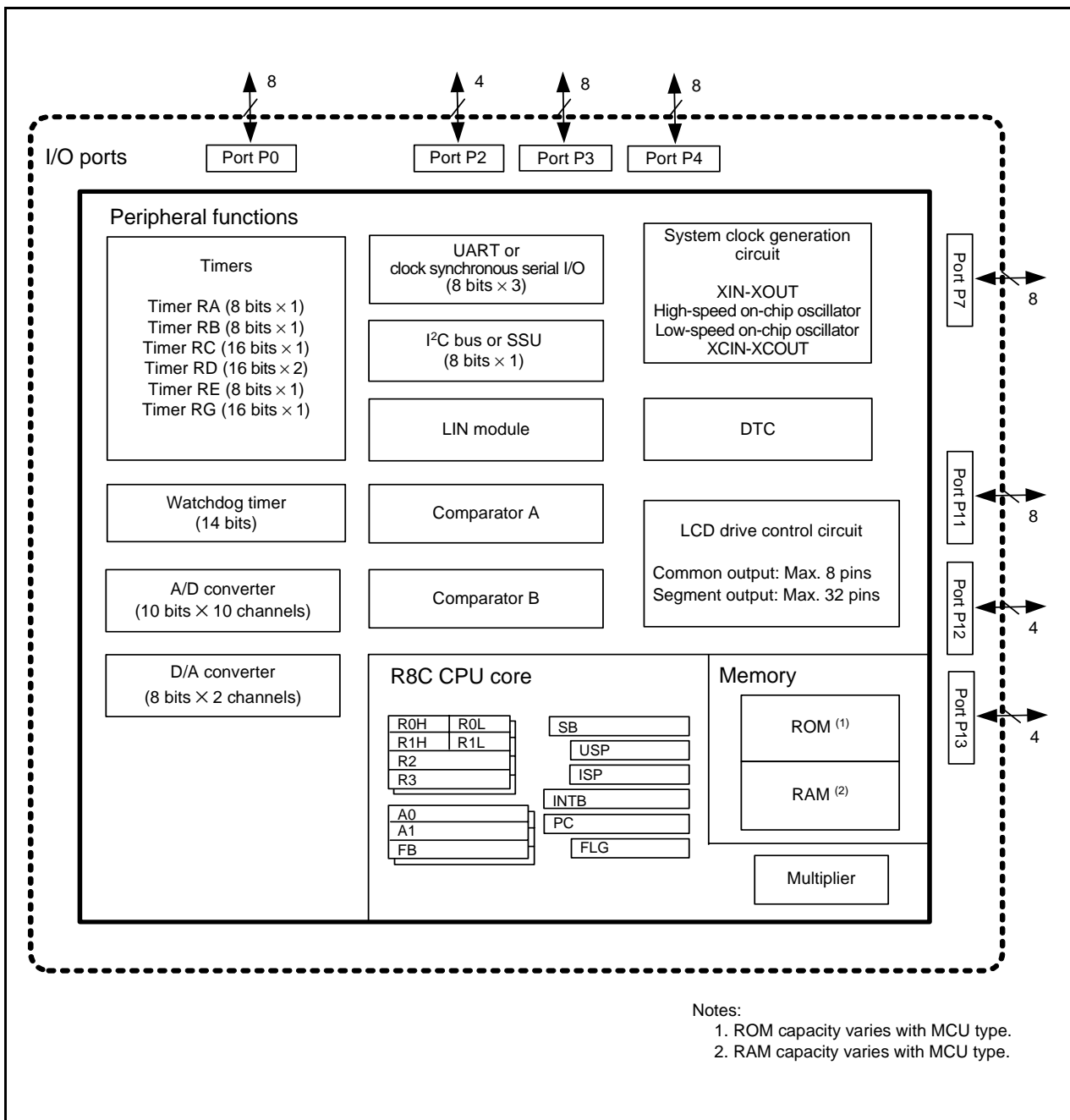


Figure 1.9 Block Diagram of R8C/L35A and R8C/L35B Groups



**Figure 1.10** Block Diagram of R8C/L36A and R8C/L36B Groups

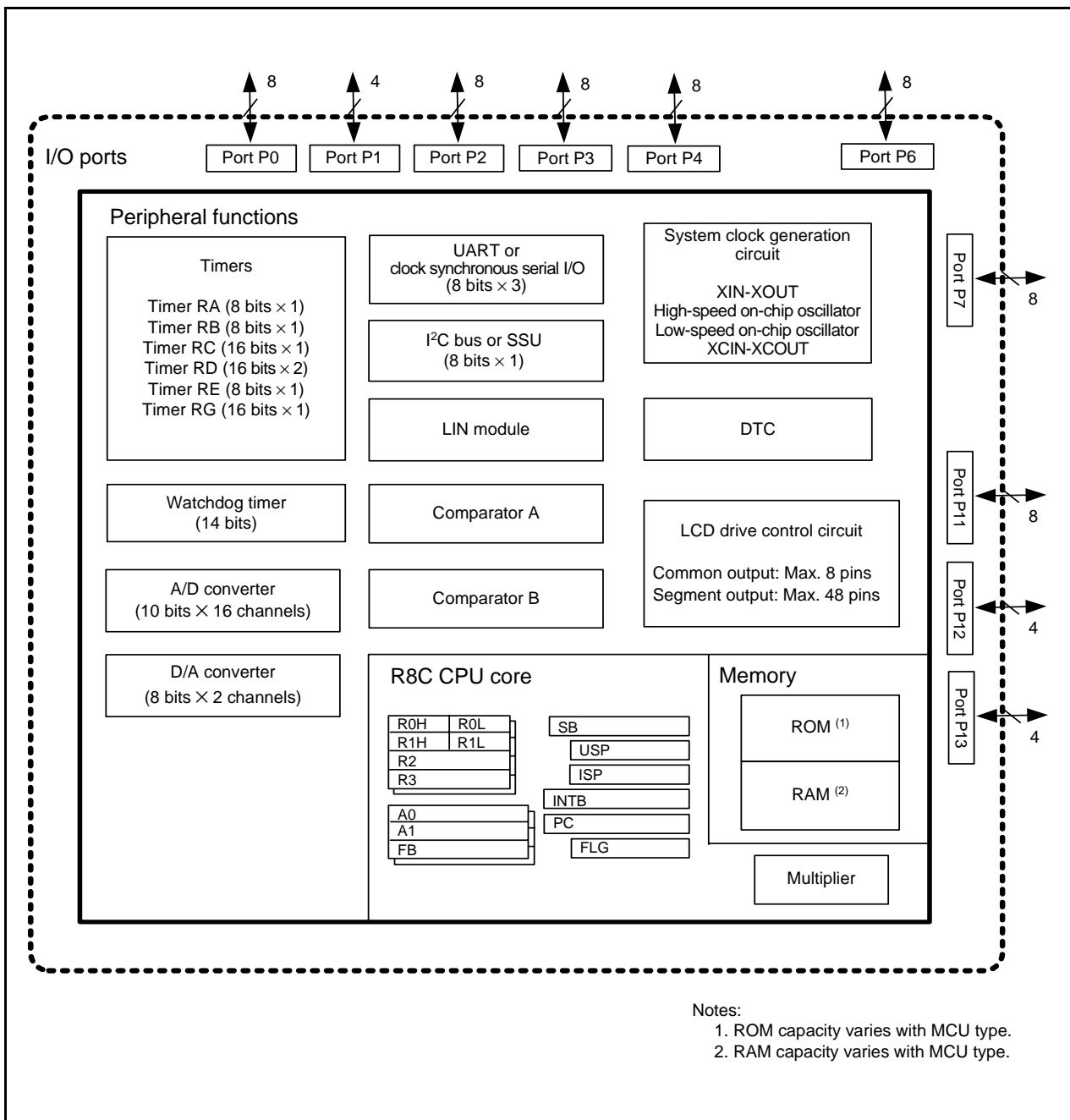
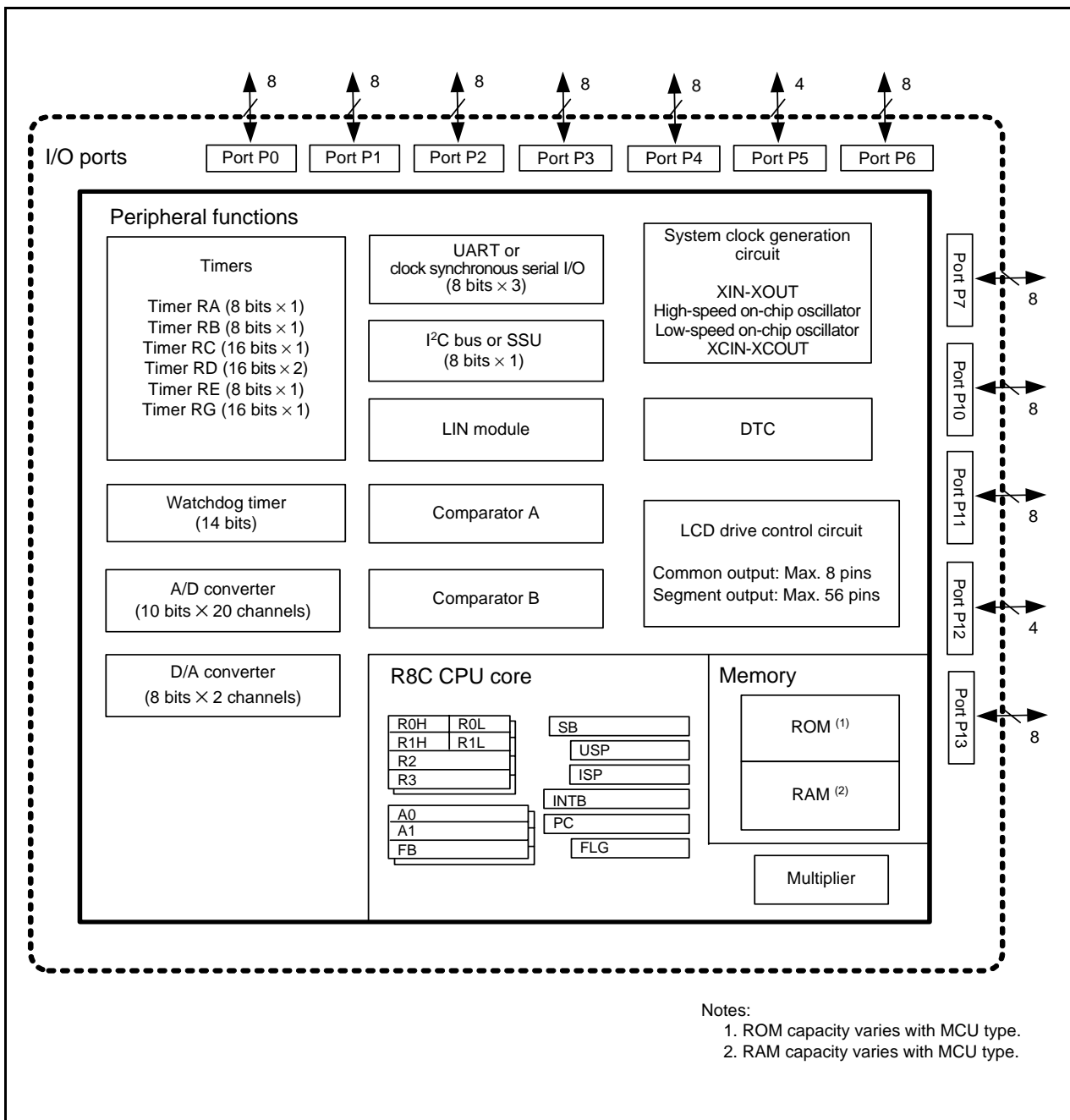


Figure 1.11 Block Diagram of R8C/L38A and R8C/L38B Groups



Notes:  
 1. ROM capacity varies with MCU type.  
 2. RAM capacity varies with MCU type.

**Figure 1.12** Block Diagram of R8C/L3AA and R8C/L3AB Groups

## 1.4 Pin Assignments

Figures 1.13 to 1.17 show pin assignments (top view). Tables 1.16 to 1.18 list the pin name information by pin number.

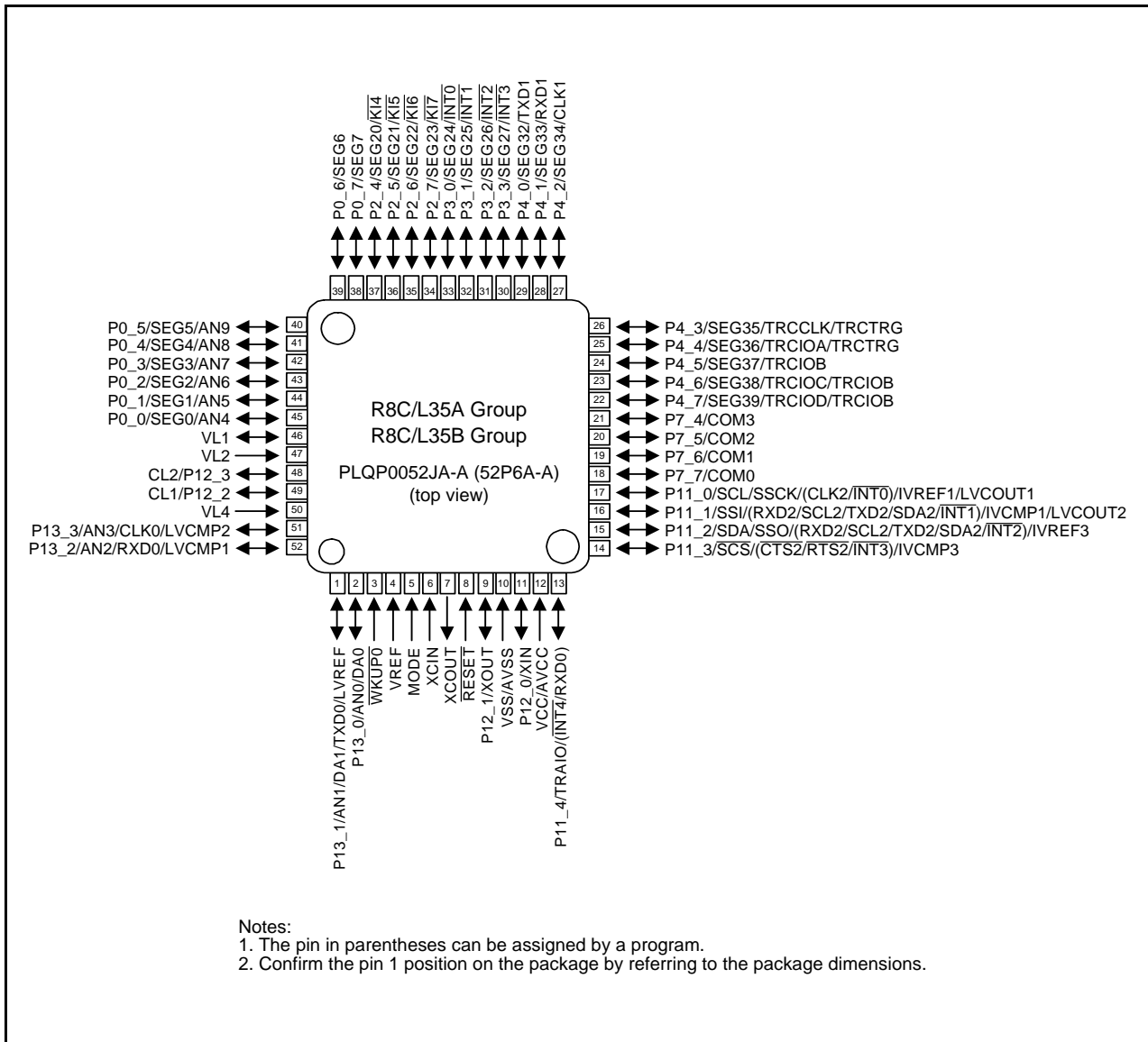


Figure 1.13 Pin Assignment (Top View) of PLQP0052JA-A Package

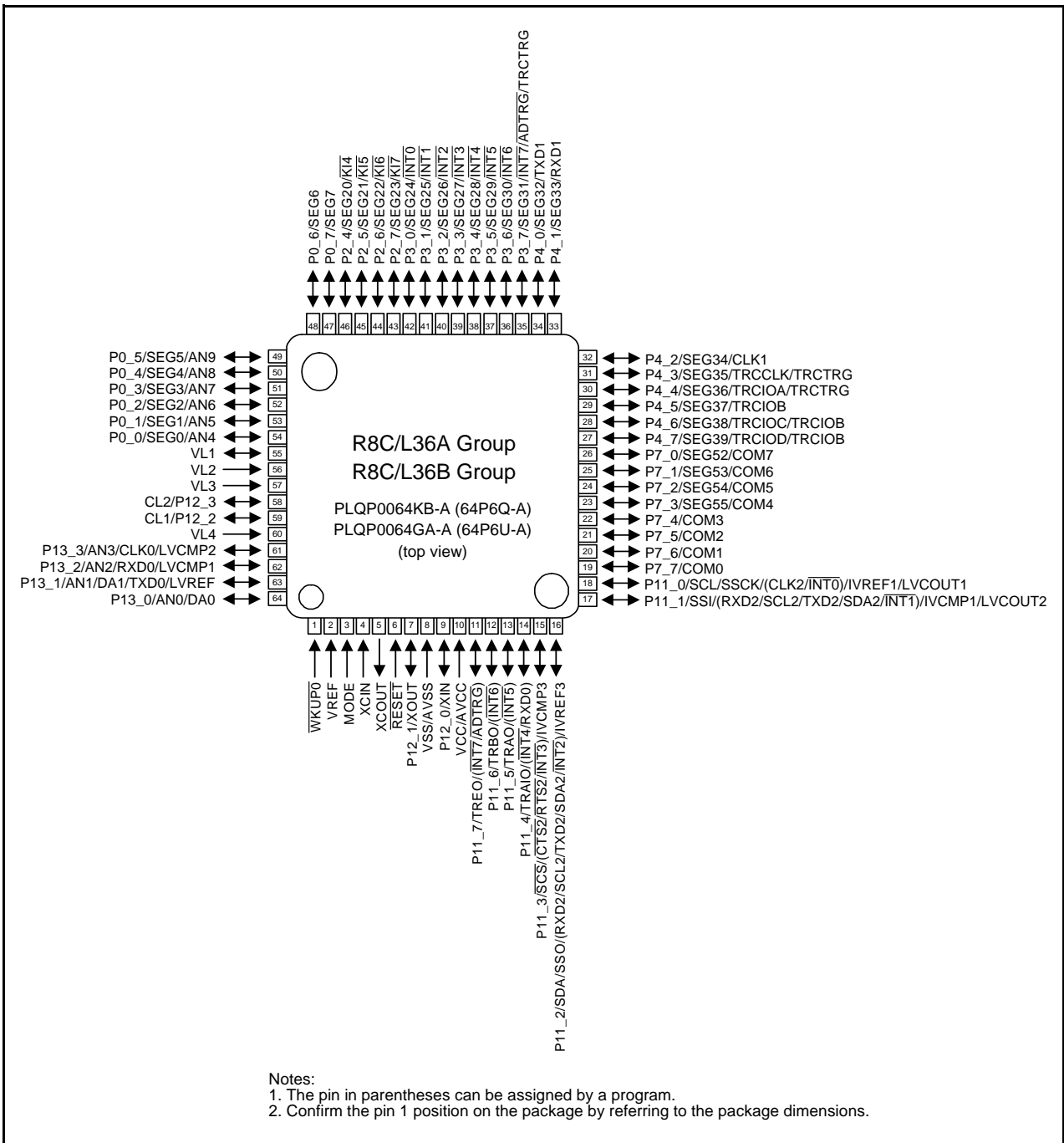


Figure 1.14 Pin Assignment (Top View) of PLQP0064KB-A and PLQP0064GA-A Packages

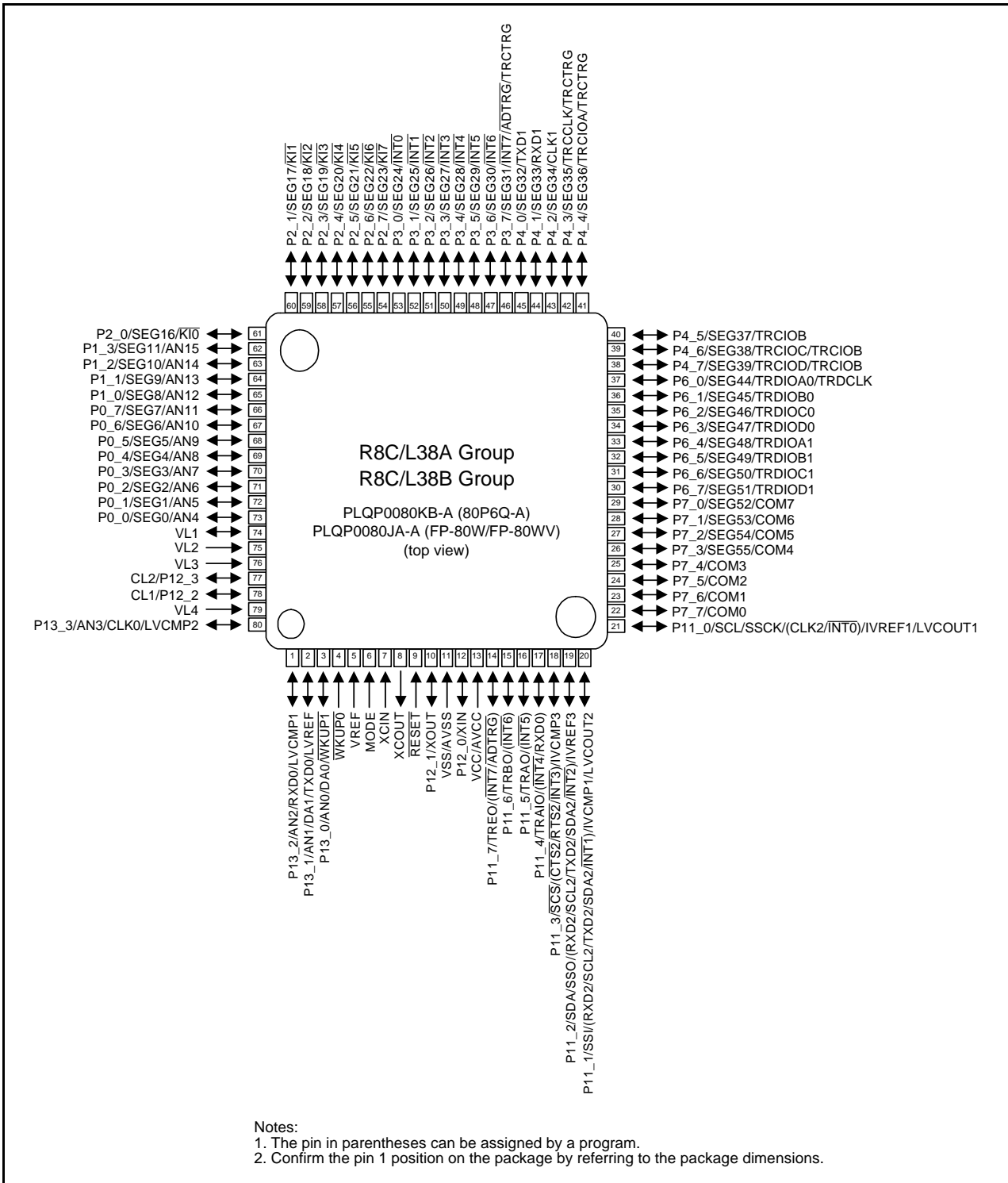


Figure 1.15 Pin Assignment (Top View) of PLQP0080KB-A and PLQP0080JA-A Packages

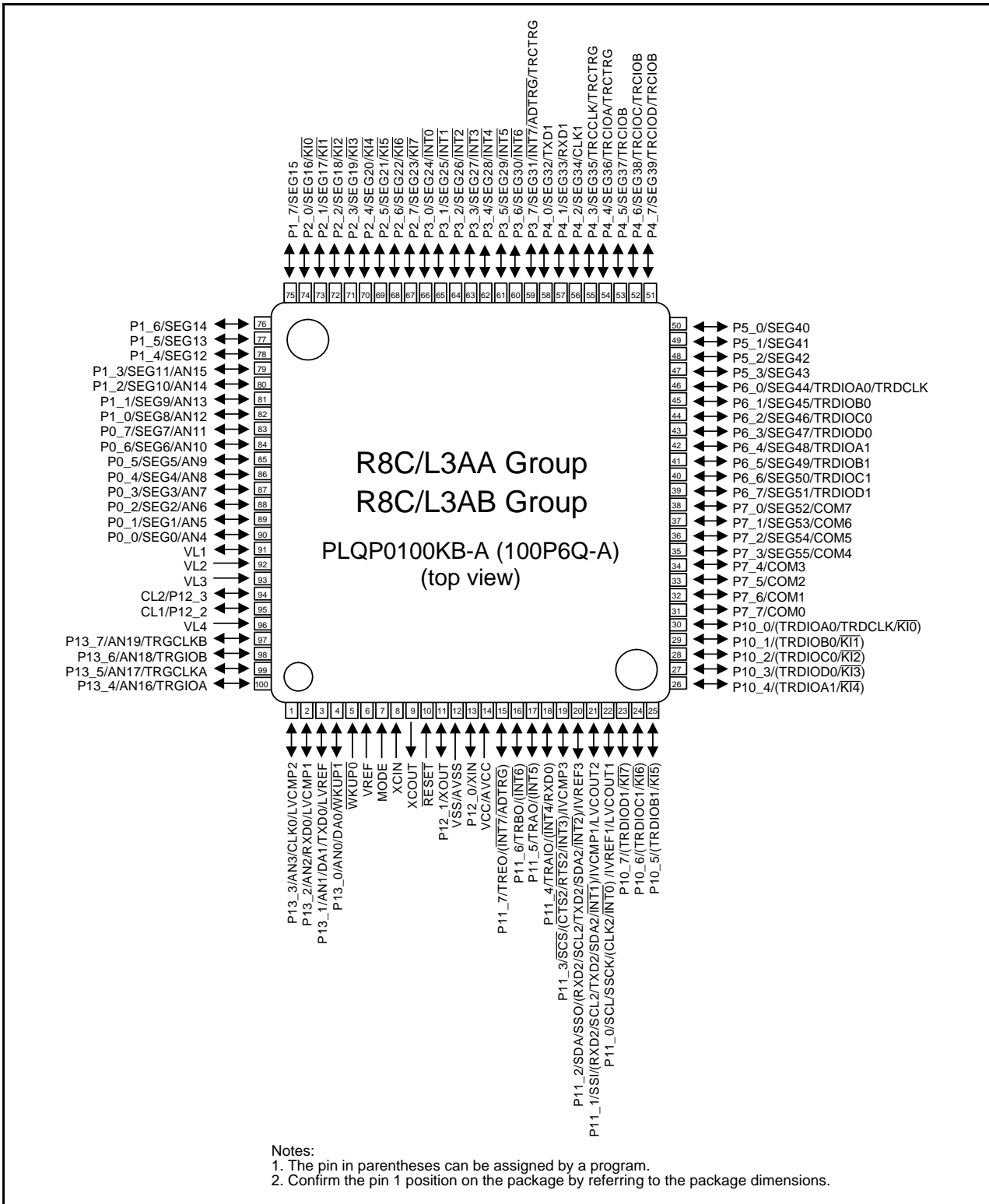


Figure 1.16 Pin Assignment (Top View) of PLQP0100KB-A Package



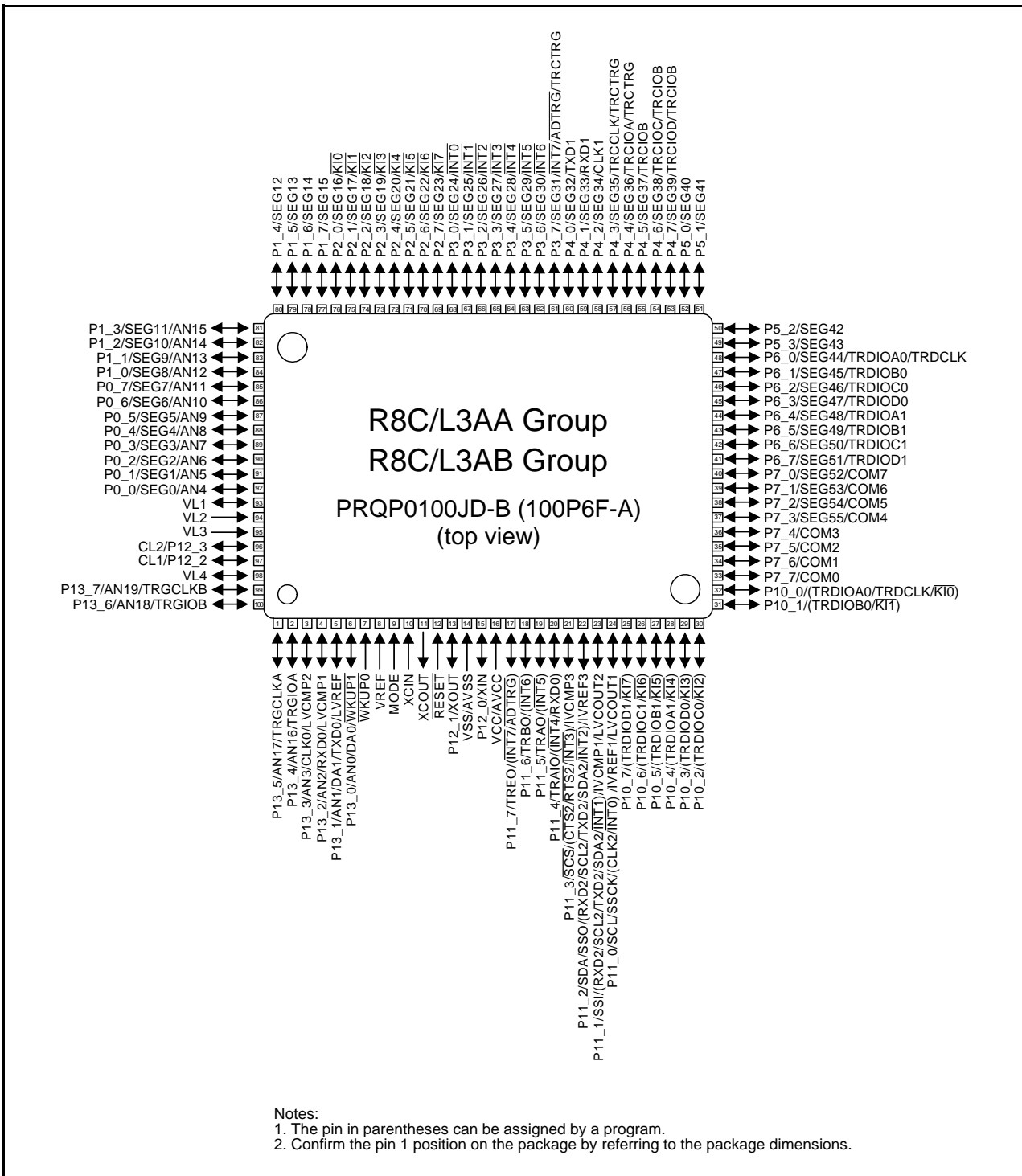


Figure 1.17 Pin Assignment (Top View) of PRQP0100JD-B Package

**Table 1.16 Pin Name Information by Pin Number (1)**

| Pin Number               |              |              |              | Control Pin  | Port  | I/O Pin Functions for Peripheral Modules |                      |                           |      |                      |   |                           |
|--------------------------|--------------|--------------|--------------|--------------|-------|--|----------------------|---------------------------|------|----------------------|---|---------------------------|
| L3AA<br>L3AB<br>(Note 2) | L38A<br>L38B | L36A<br>L36B | L35A<br>L35B |              |       | Interrupt                                | Timer                | Serial Interface          | SSU  | I <sup>2</sup> C bus | A/D Converter, D/A Converter, Comparators A, B, Voltage Detection Circuit | LCD drive control circuit |
| 1 [3]                    | 80           | 61           | 51           |              | P13_3 |  |                      | CLK0                      |      |                      | AN3/LVCMP2  |                           |
| 2 [4]                    | 1            | 62           | 52           |              | P13_2 |  |                      | RXD0                      |      |                      | AN2/LVCMP1  |                           |
| 3 [5]                    | 2            | 63           | 1            |              | P13_1 |  |                      | TXD0                      |      |                      | AN1/DA1/LVREF   |                           |
| 4 [6]                    | 3            | 64           | 2            | WKUP1 (3)    | P13_0 |  |                      |                           |      |                      | AN0/DA0   |                           |
| 5 [7]                    | 4            | 1            | 3            | WKUP0        |       |  |                      |                           |      |                      |   |                           |
| 6 [8]                    | 5            | 2            | 4            | VREF         |       |  |                      |                           |      |                      |   |                           |
| 7 [9]                    | 6            | 3            | 5            | MODE         |       |  |                      |                           |      |                      |   |                           |
| 8 [10]                   | 7            | 4            | 6            | XCIN         |       |  |                      |                           |      |                      |   |                           |
| 9 [11]                   | 8            | 5            | 7            | XCOU         |       |  |                      |                           |      |                      |   |                           |
| 10 [12]                  | 9            | 6            | 8            | RESET        |       |  |                      |                           |      |                      |   |                           |
| 11 [13]                  | 10           | 7            | 9            | XOUT         | P12_1 |  |                      |                           |      |                      |   |                           |
| 12 [14]                  | 11           | 8            | 10           | VSS/<br>AVSS |       |  |                      |                           |      |                      |   |                           |
| 13 [15]                  | 12           | 9            | 11           | XIN          | P12_0 |  |                      |                           |      |                      |   |                           |
| 14 [16]                  | 13           | 10           | 12           | VCC/<br>AVCC |       |  |                      |                           |      |                      |   |                           |
| 15 [17]                  | 14           | 11           |              |              | P11_7 | (INT7)                                   | TREO                 |                           |      |                      | (ADTRG)   |                           |
| 16 [18]                  | 15           | 12           |              |              | P11_6 | (INT6)                                   | TRBO                 |                           |      |                      |   |                           |
| 17 [19]                  | 16           | 13           |              |              | P11_5 | (INT5)                                   | TRAO                 |                           |      |                      |   |                           |
| 18 [20]                  | 17           | 14           | 13           |              | P11_4 | (INT4)                                   | TRAI0                | (RXD0)                    |      |                      |   |                           |
| 19 [21]                  | 18           | 15           | 14           |              | P11_3 | (INT3)                                   |                      | (CTS2/RTS2)               | SCS  |                      | IVCMP3  |                           |
| 20 [22]                  | 19           | 16           | 15           |              | P11_2 | (INT2)                                   |                      | (RXD2/SCL2/<br>TXD2/SDA2) | SSO  | SDA                  | IVREF3  |                           |
| 21 [23]                  | 20           | 17           | 16           |              | P11_1 | (INT1)                                   |                      | (RXD2/SCL2/<br>TXD2/SDA2) | SSI  |                      | IVCMP1/LVCOUT2  |                           |
| 22 [24]                  | 21           | 18           | 17           |              | P11_0 | (INT0)                                   |                      | (CLK2)                    | SSCK | SCL                  | IVREF1/LVCOUT1  |                           |
| 23 [25]                  |              |              |              |              | P10_7 | (KI7)                                    | (TRDIOD1)            |                           |      |                      |   |                           |
| 24 [26]                  |              |              |              |              | P10_6 | (KI6)                                    | (TRDIOD1)            |                           |      |                      |   |                           |
| 25 [27]                  |              |              |              |              | P10_5 | (KI5)                                    | (TRDIOD1)            |                           |      |                      |   |                           |
| 26 [28]                  |              |              |              |              | P10_4 | (KI4)                                    | (TRDIOD1)            |                           |      |                      |   |                           |
| 27 [29]                  |              |              |              |              | P10_3 | (KI3)                                    | (TRDIOD0)            |                           |      |                      |   |                           |
| 28 [30]                  |              |              |              |              | P10_2 | (KI2)                                    | (TRDIOD0)            |                           |      |                      |   |                           |
| 29 [31]                  |              |              |              |              | P10_1 | (KI1)                                    | (TRDIOD0)            |                           |      |                      |   |                           |
| 30 [32]                  |              |              |              |              | P10_0 | (KI0)                                    | (TRDIOD0/<br>TRDCLK) |                           |      |                      |   |                           |
| 31 [33]                  | 22           | 19           | 18           |              | P7_7  |  |                      |                           |      |                      |   | COM0                      |
| 32 [34]                  | 23           | 20           | 19           |              | P7_6  |  |                      |                           |      |                      |   | COM1                      |
| 33 [35]                  | 24           | 21           | 20           |              | P7_5  |  |                      |                           |      |                      |   | COM2                      |
| 34 [36]                  | 25           | 22           | 21           |              | P7_4  |  |                      |                           |      |                      |   | COM3                      |
| 35 [37]                  | 26           | 23           |              |              | P7_3  |  |                      |                           |      |                      |   | SEG55/<br>COM4            |
| 36 [38]                  | 27           | 24           |              |              | P7_2  |  |                      |                           |      |                      |   | SEG54/<br>COM5            |
| 37 [39]                  | 28           | 25           |              |              | P7_1  |  |                      |                           |      |                      |   | SEG53/<br>COM6            |
| 38 [40]                  | 29           | 26           |              |              | P7_0  |  |                      |                           |      |                      |   | SEG52/<br>COM7            |
| 39 [41]                  | 30           |              |              |              | P6_7  |  | TRDIOD1              |                           |      |                      |   | SEG51                     |

Notes:

1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.
3. The WKUP1 pin is not available in the R8C/L35A, R8C/L35B, R8C/L36A, and R8C/L36B Groups.

**Table 1.17 Pin Name Information by Pin Number (2)**

| Pin Number               |              |              |              | Control Pin | Port | I/O Pin Functions for Peripheral Modules |                    |                  |     |                      |   |                           |
|--------------------------|--------------|--------------|--------------|-------------|------|--|--------------------|------------------|-----|----------------------|---|---------------------------|
| L3AA<br>L3AB<br>(Note 2) | L38A<br>L38B | L36A<br>L36B | L35A<br>L35B |             |      | Interrupt                                | Timer              | Serial Interface | SSU | I <sup>2</sup> C bus | A/D Converter,<br>D/A Converter,<br>Comparators A, B,<br>Voltage Detection<br>Circuit | LCD drive control circuit |
| 40 [42]                  | 31           |              |              |             | P6_6 |  | TRDIOC1            |                  |     |                      |   | SEG50                     |
| 41 [43]                  | 32           |              |              |             | P6_5 |  | TRDIOB1            |                  |     |                      |   | SEG49                     |
| 42 [44]                  | 33           |              |              |             | P6_4 |  | TRDIOA1            |                  |     |                      |   | SEG48                     |
| 43 [45]                  | 34           |              |              |             | P6_3 |  | TRDIOD0            |                  |     |                      |   | SEG47                     |
| 44 [46]                  | 35           |              |              |             | P6_2 |  | TRDIOC0            |                  |     |                      |   | SEG46                     |
| 45 [47]                  | 36           |              |              |             | P6_1 |  | TRDIOB0            |                  |     |                      |   | SEG45                     |
| 46 [48]                  | 37           |              |              |             | P6_0 |  | TRDIOA0/<br>TRDCLK |                  |     |                      |   | SEG44                     |
| 47 [49]                  |              |              |              |             | P5_3 |  |                    |                  |     |                      |   | SEG43                     |
| 48 [50]                  |              |              |              |             | P5_2 |  |                    |                  |     |                      |   | SEG42                     |
| 49 [51]                  |              |              |              |             | P5_1 |  |                    |                  |     |                      |   | SEG41                     |
| 50 [52]                  |              |              |              |             | P5_0 |  |                    |                  |     |                      |   | SEG40                     |
| 51 [53]                  | 38           | 27           | 22           |             | P4_7 |  | TRCIOD/<br>TRCIOB  |                  |     |                      |   | SEG39                     |
| 52 [54]                  | 39           | 28           | 23           |             | P4_6 |  | TRCIOA/<br>TRCIOB  |                  |     |                      |   | SEG38                     |
| 53 [55]                  | 40           | 29           | 24           |             | P4_5 |  | TRCIOB             |                  |     |                      |   | SEG37                     |
| 54 [56]                  | 41           | 30           | 25           |             | P4_4 |  | TRCIOA/<br>TRCTRIG |                  |     |                      |   | SEG36                     |
| 55 [57]                  | 42           | 31           | 26           |             | P4_3 |  | TRCCLK/<br>TRCTRIG |                  |     |                      |   | SEG35                     |
| 56 [58]                  | 43           | 32           | 27           |             | P4_2 |  |                    | CLK1             |     |                      |   | SEG34                     |
| 57 [59]                  | 44           | 33           | 28           |             | P4_1 |  |                    | RXD1             |     |                      |   | SEG33                     |
| 58 [60]                  | 45           | 34           | 29           |             | P4_0 |  |                    | TXD1             |     |                      |   | SEG32                     |
| 59 [61]                  | 46           | 35           |              |             | P3_7 | $\overline{\text{INT7}}$                 | TRCTRIG            |                  |     |                      | $\overline{\text{ADTRG}}$   | SEG31                     |
| 60 [62]                  | 47           | 36           |              |             | P3_6 | $\overline{\text{INT6}}$                 |                    |                  |     |                      |   | SEG30                     |
| 61 [63]                  | 48           | 37           |              |             | P3_5 | $\overline{\text{INT5}}$                 |                    |                  |     |                      |   | SEG29                     |
| 62 [64]                  | 49           | 38           |              |             | P3_4 | $\overline{\text{INT4}}$                 |                    |                  |     |                      |   | SEG28                     |
| 63 [65]                  | 50           | 39           | 30           |             | P3_3 | $\overline{\text{INT3}}$                 |                    |                  |     |                      |   | SEG27                     |
| 64 [66]                  | 51           | 40           | 31           |             | P3_2 | $\overline{\text{INT2}}$                 |                    |                  |     |                      |   | SEG26                     |
| 65 [67]                  | 52           | 41           | 32           |             | P3_1 | $\overline{\text{INT1}}$                 |                    |                  |     |                      |   | SEG25                     |
| 66 [68]                  | 53           | 42           | 33           |             | P3_0 | $\overline{\text{INT0}}$                 |                    |                  |     |                      |   | SEG24                     |
| 67 [69]                  | 54           | 43           | 34           |             | P2_7 | $\overline{\text{KI7}}$                  |                    |                  |     |                      |   | SEG23                     |
| 68 [70]                  | 55           | 44           | 35           |             | P2_6 | $\overline{\text{KI6}}$                  |                    |                  |     |                      |   | SEG22                     |
| 69 [71]                  | 56           | 45           | 36           |             | P2_5 | $\overline{\text{KI5}}$                  |                    |                  |     |                      |   | SEG21                     |
| 70 [72]                  | 57           | 46           | 37           |             | P2_4 | $\overline{\text{KI4}}$                  |                    |                  |     |                      |   | SEG20                     |
| 71 [73]                  | 58           |              |              |             | P2_3 | $\overline{\text{KI3}}$                  |                    |                  |     |                      |   | SEG19                     |
| 72 [74]                  | 59           |              |              |             | P2_2 | $\overline{\text{KI2}}$                  |                    |                  |     |                      |   | SEG18                     |
| 73 [75]                  | 60           |              |              |             | P2_1 | $\overline{\text{KI1}}$                  |                    |                  |     |                      |   | SEG17                     |
| 74 [76]                  | 61           |              |              |             | P2_0 | $\overline{\text{KI0}}$                  |                    |                  |     |                      |   | SEG16                     |
| 75 [77]                  |              |              |              |             | P1_7 |  |                    |                  |     |                      |   | SEG15                     |
| 76 [78]                  |              |              |              |             | P1_6 |  |                    |                  |     |                      |   | SEG14                     |
| 77 [79]                  |              |              |              |             | P1_5 |  |                    |                  |     |                      |   | SEG13                     |
| 78 [80]                  |              |              |              |             | P1_4 |  |                    |                  |     |                      |   | SEG12                     |
| 79 [81]                  | 62           |              |              |             | P1_3 |  |                    |                  |     | AN15                 |   | SEG11                     |
| 80 [82]                  | 63           |              |              |             | P1_2 |  |                    |                  |     | AN14                 |   | SEG10                     |
| 81 [83]                  | 64           |              |              |             | P1_1 |  |                    |                  |     | AN13                 |   | SEG9                      |
| 82 [84]                  | 65           |              |              |             | P1_0 |  |                    |                  |     | AN12                 |   | SEG8                      |
| 83 [85]                  | 66           | 47           | 38           |             | P0_7 |  |                    |                  |     | AN11 <sup>(3)</sup>  |   | SEG7                      |
| 84 [86]                  | 67           | 48           | 39           |             | P0_6 |  |                    |                  |     | AN10 <sup>(3)</sup>  |   | SEG6                      |

Notes:

1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.
3. Pins AN10 and AN11 are not available in the R8C/L35A, R8C/L35B, R8C/L36A, and R8C/L36B Groups.

**Table 1.18 Pin Name Information by Pin Number (3)**

| Pin Number               |              |              |              | Control Pin | Port  | I/O Pin Functions for Peripheral Modules |         |                  |     |                      |   |                                    |
|--------------------------|--------------|--------------|--------------|-------------|-------|--|---------|------------------|-----|----------------------|---|------------------------------------|
| L3AA<br>L3AB<br>(Note 2) | L38A<br>L38B | L36A<br>L36B | L35A<br>L35B |             |       | Interrupt                                | Timer   | Serial Interface | SSU | I <sup>2</sup> C bus | A/D Converter,<br>D/A Converter,<br>Comparators A, B,<br>Voltage Detection<br>Circuit | LCD<br>drive<br>control<br>circuit |
| 85 [87]                  | 68           | 49           | 40           |             | P0_5  |  |         |                  |     |                      | AN9   | SEG5                               |
| 86 [88]                  | 69           | 50           | 41           |             | P0_4  |  |         |                  |     |                      | AN8   | SEG4                               |
| 87 [89]                  | 70           | 51           | 42           |             | P0_3  |  |         |                  |     |                      | AN7   | SEG3                               |
| 88 [90]                  | 71           | 52           | 43           |             | P0_2  |  |         |                  |     |                      | AN6   | SEG2                               |
| 89 [91]                  | 72           | 53           | 44           |             | P0_1  |  |         |                  |     |                      | AN5   | SEG1                               |
| 90 [92]                  | 73           | 54           | 45           |             | P0_0  |  |         |                  |     |                      | AN4   | SEG0                               |
| 91 [93]                  | 74           | 55           | 46           |             |       |  |         |                  |     |                      |   | VL1                                |
| 92 [94]                  | 75           | 56           | 47           |             |       |  |         |                  |     |                      |   | VL2                                |
| 93 [95]                  | 76           | 57           |              |             |       |  |         |                  |     |                      |   | VL3                                |
| 94 [96]                  | 77           | 58           | 48           |             | P12_3 |  |         |                  |     |                      |   | CL2                                |
| 95 [97]                  | 78           | 59           | 49           |             | P12_2 |  |         |                  |     |                      |   | CL1                                |
| 96 [98]                  | 79           | 60           | 50           |             |       |  |         |                  |     |                      |   | VL4                                |
| 97 [99]                  |              |              |              |             | P13_7 |  | TRGCLKB |                  |     |                      | AN19  |                                    |
| 98 [100]                 |              |              |              |             | P13_6 |  | TRGIOB  |                  |     |                      | AN18  |                                    |
| 99 [1]                   |              |              |              |             | P13_5 |  | TRGCLKA |                  |     |                      | AN17  |                                    |
| 100 [2]                  |              |              |              |             | P13_4 |  | TRGIOA  |                  |     |                      | AN16  |                                    |

Notes:

1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

## 1.5 Pin Functions

Tables 1.19 and 1.20 list pin functions.

**Table 1.19 Pin Functions (1)**

| Item                                    | Pin Name   | I/O Type | Description   |
|---|--|----------|---|
| Power supply input                      | VCC, VSS   | –        | Apply 1.8 V to 5.5 V to the VCC pin.<br>Apply 0 V to the VSS pin.   |
| Analog power supply input               | AVCC, AVSS   | –        | Power supply for the A/D converter.<br>Connect a capacitor between AVCC and AVSS.   |
| Reset input                             | $\overline{\text{RESET}}$  | I        | Driving this pin low resets the MCU.  |
| MODE                                    | MODE   | I        | Connect this pin to VCC via a resistor.   |
| Power-off mode exit input               | $\overline{\text{WKUP0}}$  | I        | This pin is provided for input to exit the mode used in power-off mode. Connect to VSS when not using power-off mode.   |
|   | $\overline{\text{WKUP1}}$  | I        | This pin is provided for input to exit the mode used in power-off mode.   |
| XIN clock input                         | XIN  | I        | These pins are provided for XIN clock generation circuit I/O. Connect a ceramic oscillator or a crystal oscillator between pins XIN and XOUT. <sup>(1)</sup> To use an external clock, input it to the XIN pin and leave the XOUT pin open. |
| XIN clock output                        | XOUT   | O        |   |
| XCIN clock input                        | XCIN   | I        | These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between pins XCIN and XCOU. <sup>(1)</sup> To use an external clock, input it to the XCIN pin and leave the XCOU pin open.                      |
| XCIN clock output                       | XCOU   | O        |   |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT7}}$                   | I        | $\overline{\text{INT}}$ interrupt input pins.   |
| Key input interrupt                     | $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$                     | I        | Key input interrupt input pins  |
| Timer RA                                | TRAIO  | I/O      | Timer RA I/O pin  |
|   | TRAO   | O        | Timer RA output pin   |
| Timer RB                                | TRBO   | O        | Timer RB output pin   |
| Timer RC                                | TRCLK  | I        | External clock input pin  |
|   | TRCTRG   | I        | External trigger input pin  |
|   | TRCIOA, TRCIOB, TRCIO, TRCIOD  | I/O      | Timer RC I/O pins   |
| Timer RD                                | TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 | I/O      | Timer RD I/O pins   |
|   | TRDCLK   | I        | External clock input pin  |
| Timer RE                                | TREO   | O        | Divided clock output pin  |
| Timer RG                                | TRGCLKA, TRGCLKB   | I        | Timer RG input pins   |
|   | TRGIOA, TRGIOB   | I/O      | Timer RG I/O pins   |
| Serial interface                        | CLK0, CLK1, CLK2   | I/O      | Transfer clock I/O pins   |
|   | RXD0, RXD1, RXD2   | I        | Serial data input pins  |
|   | TXD0, TXD1, TXD2   | O        | Serial data output pins   |
|   | $\overline{\text{CTS2}}$   | I        | Transmission control input pin  |
|   | $\overline{\text{RTS2}}$   | O        | Reception control output pin  |
|   | SCL2   | I/O      | I <sup>2</sup> C mode clock I/O pin   |
|   | SDA2   | I/O      | I <sup>2</sup> C mode data I/O pin  |

I: Input      O: Output      I/O: Input and output

Note:

- Contact the oscillator manufacturer for oscillation characteristics.

**Table 1.20 Pin Functions (2)**

| Item                                     | Pin Name   | I/O Type | Description  |
|--|--|----------|--|
| I <sup>2</sup> C bus                     | SCL  | I/O      | Clock I/O pin  |
|  | SDA  | I/O      | Data I/O pin   |
| SSU                                      | SSI  | I/O      | Data I/O pin   |
|  | $\overline{\text{SCS}}$  | I/O      | Chip-select signal I/O pin   |
|  | SSCK   | I/O      | Clock I/O pin  |
|  | SSO  | I/O      | Data I/O pin   |
| Reference voltage input                  | VREF   | I        | Reference voltage input pin for the A/D converter and the D/A converter  |
| A/D converter                            | AN0 to AN11  | I        | A/D converter analog input pins  |
|  | $\overline{\text{ADTRG}}$  | I        | AD external trigger input pin  |
| D/A converter                            | DA0, DA1   | O        | D/A converter output pins  |
| Comparator A                             | LVCMP1, LVCMP2   | I        | Comparator A analog voltage input pins   |
|  | LVREF  | I        | Comparator A reference voltage input pin   |
|  | LVCOUT1, LVCOUT2   | O        | Comparator A output pins   |
| Comparator B                             | IVCMP1, IVCMP3   | I        | Comparator B analog voltage input pins   |
|  | IVREF1, IVREF3   | I        | Comparator B reference voltage input pins  |
| Voltage detection circuit                | LVCMP2   | I        | Detection target voltage input pin for voltage detection 2   |
| I/O ports                                | P0_0 to P0_7,<br>P1_0 to P1_7,<br>P2_0 to P2_7,<br>P3_0 to P3_7,<br>P4_0 to P4_7,<br>P5_0, P5_3,<br>P6_0 to P6_7<br>P7_0 to P7_7,<br>P10_0 to P10_7,<br>P11_0 to P11_7,<br>P12_0 to P12_3,<br>P13_0 to P13_7 | I/O      | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually.<br>Any port set to input can be set to use a pull-up resistor or not by a program.<br>Ports P10_0 to P10_7 and P11_0 to P11_7 can be used as LED drive ports. |
| Segment output                           | SEG0 to SEG55  | O        | LCD segment output pins  |
| Common output                            | COM0 to COM7   | O        | LCD common output pins   |
| Voltage multiplier capacity connect pins | CL1, CL2   | O        | Connect pins for the LCD control voltage multiplier  |
| LCD power supply                         | VL1  | I/O      | Apply the voltage: $0 \leq VL1 \leq VL2 \leq VL3 \leq VL4$ .   |
|  | VL2 to VL4   | I        | VL1 can be used as the reference potential input or output pin when setting the voltage multiplier.  |

I: Input      O: Output      I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register banks.

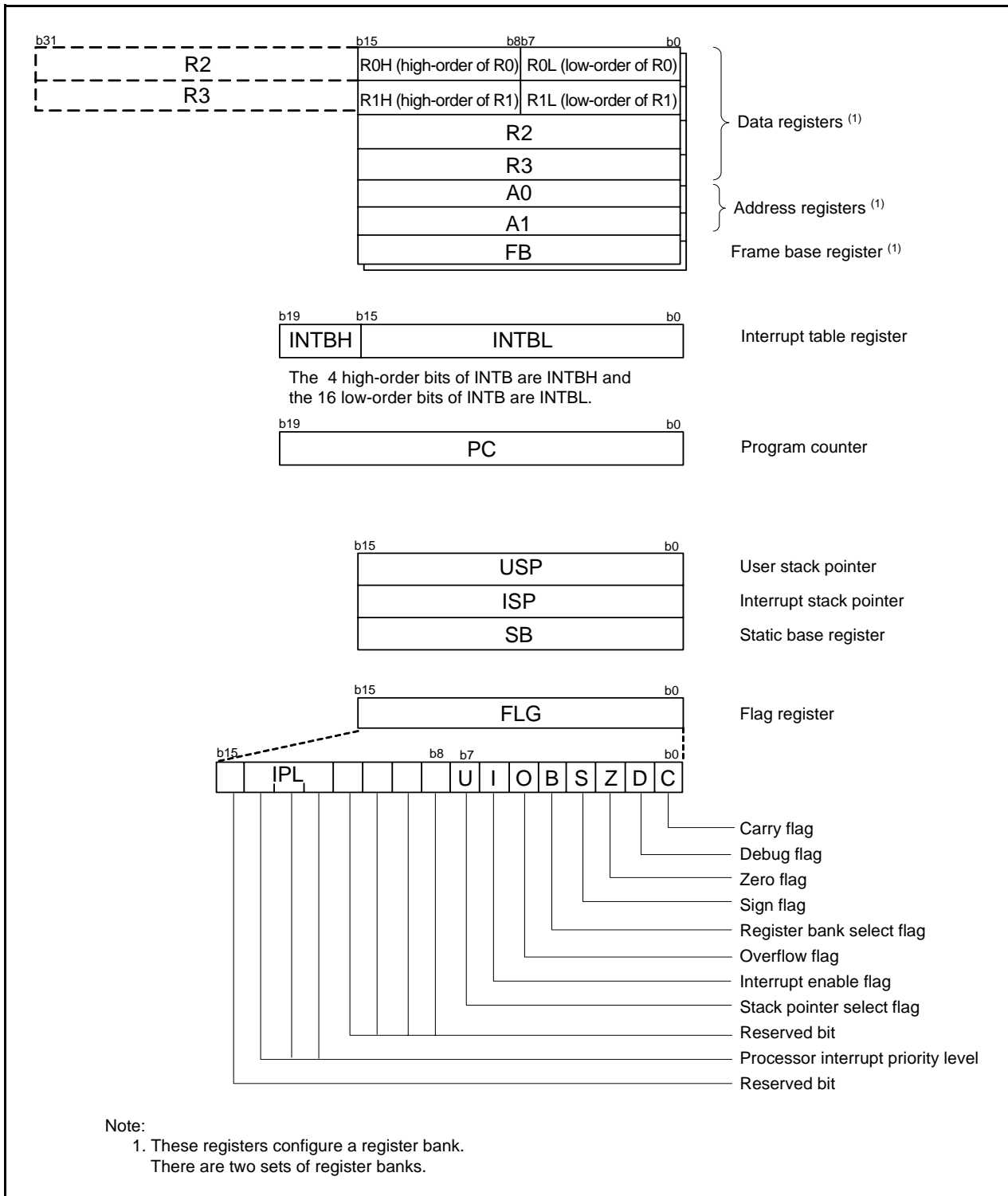


Figure 2.1 CPU Registers

## 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.



### **2.8.7 Interrupt Enable Flag (I)**

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

### **2.8.8 Stack Pointer Select Flag (U)**

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

### **2.8.9 Processor Interrupt Priority Level (IPL)**

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### **2.8.10 Reserved Bit**

If necessary, set to 0. When read, the content is undefined.

### 3. Memory

Figure 3.1 is a Memory Map of each group. Each group has a 1-Mbyte address space from addresses 00000h to FFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

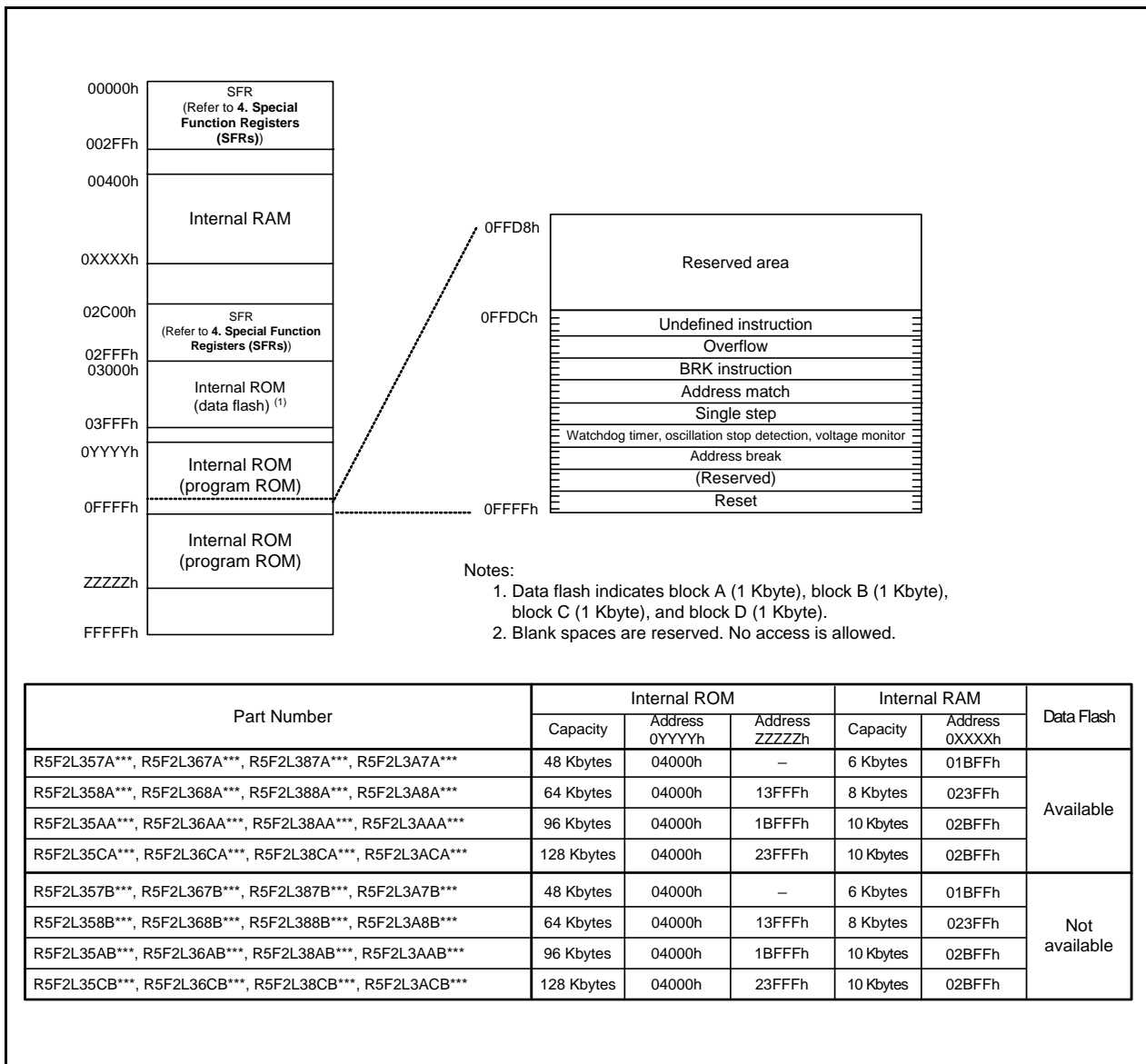


Figure 3.1 Memory Map

## 4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.16 list SFR information.

**Table 4.1 SFR Information (1) (1)**

| Address | Register  | Symbol   | After Reset                    |
|---------|---|----------|--------------------------------|
| 0000h   |   |          |                                |
| 0001h   |   |          |                                |
| 0002h   |   |          |                                |
| 0003h   |   |          |                                |
| 0004h   | Processor Mode Register 0                             | PM0      | 00h                            |
| 0005h   | Processor Mode Register 1                             | PM1      | 00h                            |
| 0006h   | System Clock Control Register 0                       | CM0      | 00100000b                      |
| 0007h   | System Clock Control Register 1                       | CM1      | 00100000b                      |
| 0008h   | Module Standby Control Register                       | MSTCR    | 00h                            |
| 0009h   | System Clock Control Register 3                       | CM3      | 00h                            |
| 000Ah   | Protect Register                                      | PRCR     | 00h                            |
| 000Bh   | Reset Source Determination Register                   | RSTFR    | XXh (2)                        |
| 000Ch   | Oscillation Stop Detection Register                   | OCD      | 00000100b                      |
| 000Dh   | Watchdog Timer Reset Register                         | WDTR     | XXh                            |
| 000Eh   | Watchdog Timer Start Register                         | WDTS     | XXh                            |
| 000Fh   | Watchdog Timer Control Register                       | WDTC     | 00111111b                      |
| 0010h   |   |          |                                |
| 0011h   |   |          |                                |
| 0012h   |   |          |                                |
| 0013h   |   |          |                                |
| 0014h   |   |          |                                |
| 0015h   | High-Speed On-Chip Oscillator Control Register 7      | FRA7     | When shipping                  |
| 0016h   |   |          |                                |
| 0017h   |   |          |                                |
| 0018h   |   |          |                                |
| 0019h   |   |          |                                |
| 001Ah   |   |          |                                |
| 001Bh   |   |          |                                |
| 001Ch   | Count Source Protection Mode Register                 | CSPR     | 00h<br>10000000b (3)           |
| 001Dh   |   |          |                                |
| 001Eh   |   |          |                                |
| 001Fh   |   |          |                                |
| 0020h   | Power-Off Mode Control Register 0                     | POMCR0   | X0000000b                      |
| 0021h   |   |          |                                |
| 0022h   |   |          |                                |
| 0023h   | High-Speed On-Chip Oscillator Control Register 0      | FRA0     | 00h                            |
| 0024h   | High-Speed On-Chip Oscillator Control Register 1      | FRA1     | When shipping                  |
| 0025h   | High-Speed On-Chip Oscillator Control Register 2      | FRA2     | 00h                            |
| 0026h   | On-Chip Reference Voltage Control Register            | OCVREFCR | 00h                            |
| 0027h   |   |          |                                |
| 0028h   |   |          |                                |
| 0029h   | High-Speed On-Chip Oscillator Control Register 4      | FRA4     | When Shipping                  |
| 002Ah   | High-Speed On-Chip Oscillator Control Register 5      | FRA5     | When Shipping                  |
| 002Bh   | High-Speed On-Chip Oscillator Control Register 6      | FRA6     | When Shipping                  |
| 002Ch   |   |          |                                |
| 002Dh   |   |          |                                |
| 002Eh   |   |          |                                |
| 002Fh   | High-Speed On-Chip Oscillator Control Register 3      | FRA3     | When shipping                  |
| 0030h   | Voltage Monitor Circuit/Comparator A Control Register | CMPA     | 00h                            |
| 0031h   | Voltage Monitor Circuit Edge Select Register          | VCAC     | 00h                            |
| 0032h   |   |          |                                |
| 0033h   | Voltage Detect Register 1                             | VCA1     | 00001000b                      |
| 0034h   | Voltage Detect Register 2                             | VCA2     | 00h (4)<br>00100000b (5)       |
| 0035h   |   |          |                                |
| 0036h   | Voltage Detection 1 Level Select Register             | VD1LS    | 00000111b                      |
| 0037h   |   |          |                                |
| 0038h   | Voltage Monitor 0 Circuit Control Register            | VW0C     | 1100X010b (4)<br>1100X011b (5) |
| 0039h   | Voltage Monitor 1 Circuit Control Register            | VW1C     | 10001010b                      |

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- The CWR bit in the RSTFR register is set to 0 after power-on, voltage monitor 0 reset, or exit from power-off mode. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
- The CSPROINI bit in the OFS register is set to 0.
- The LVDAS bit in the OFS register is set to 1.
- The LVDAS bit in the OFS register is set to 0.

**Table 4.2 SFR Information (2) (1)**

| Address | Register  | Symbol      | After Reset |
|---------|---|-------------|-------------|
| 003Ah   | Voltage Monitor 2 Circuit Control Register                              | VW2C        | 1000010b    |
| 003Bh   |   |             |             |
| 003Ch   |   |             |             |
| 003Dh   |   |             |             |
| 003Eh   |   |             |             |
| 003Fh   |   |             |             |
| 0040h   |   |             |             |
| 0041h   | Flash Memory Ready Interrupt Control Register                           | FMRDYIC     | XXXXX000b   |
| 0042h   |   |             |             |
| 0043h   | INT7 Interrupt Control Register   | INT7IC      | XX00X000b   |
| 0044h   | INT6 Interrupt Control Register   | INT6IC      | XX00X000b   |
| 0045h   | INT5 Interrupt Control Register   | INT5IC      | XX00X000b   |
| 0046h   | INT4 Interrupt Control Register   | INT4IC      | XX00X000b   |
| 0047h   | Timer RC Interrupt Control Register                                     | TRCIC       | XXXXX000b   |
| 0048h   | Timer RD0 Interrupt Control Register                                    | TRD0IC      | XXXXX000b   |
| 0049h   | Timer RD1 Interrupt Control Register                                    | TRD1IC      | XXXXX000b   |
| 004Ah   | Timer RE Interrupt Control Register                                     | TREIC       | XXXXX000b   |
| 004Bh   | UART2 Transmit Interrupt Control Register                               | S2TIC       | XXXXX000b   |
| 004Ch   | UART2 Receive Interrupt Control Register                                | S2RIC       | XXXXX000b   |
| 004Dh   | Key Input Interrupt Control Register                                    | KUPIC       | XXXXX000b   |
| 004Eh   | A/D Conversion Interrupt Control Register                               | ADIC        | XXXXX000b   |
| 004Fh   | SSU Interrupt Control Register / IIC bus Interrupt Control Register (2) | SSUIC/IICIC | XXXXX000b   |
| 0050h   |   |             |             |
| 0051h   | UART0 Transmit Interrupt Control Register                               | S0TIC       | XXXXX000b   |
| 0052h   | UART0 Receive Interrupt Control Register                                | S0RIC       | XXXXX000b   |
| 0053h   | UART1 Transmit Interrupt Control Register                               | S1TIC       | XXXXX000b   |
| 0054h   | UART1 Receive Interrupt Control Register                                | S1RIC       | XXXXX000b   |
| 0055h   | INT2 Interrupt Control Register   | INT2IC      | XX00X000b   |
| 0056h   | Timer RA Interrupt Control Register                                     | TRAIC       | XXXXX000b   |
| 0057h   |   |             |             |
| 0058h   | Timer RB Interrupt Control Register                                     | TRBIC       | XXXXX000b   |
| 0059h   | INT1 Interrupt Control Register   | INT1IC      | XX00X000b   |
| 005Ah   | INT3 Interrupt Control Register   | INT3IC      | XX00X000b   |
| 005Bh   |   |             |             |
| 005Ch   |   |             |             |
| 005Dh   | INT0 Interrupt Control Register   | INT0IC      | XX00X000b   |
| 005Eh   | UART2 Bus Collision Detection Interrupt Control Register                | U2BCNIC     | XXXXX000b   |
| 005Fh   |   |             |             |
| 0060h   |   |             |             |
| 0061h   |   |             |             |
| 0062h   |   |             |             |
| 0063h   |   |             |             |
| 0064h   |   |             |             |
| 0065h   |   |             |             |
| 0066h   |   |             |             |
| 0067h   |   |             |             |
| 0068h   |   |             |             |
| 0069h   |   |             |             |
| 006Ah   |   |             |             |
| 006Bh   | Timer RG Interrupt Control Register                                     | TRGIC       | XXXXX000b   |
| 006Ch   |   |             |             |
| 006Dh   |   |             |             |
| 006Eh   |   |             |             |
| 006Fh   |   |             |             |
| 0070h   |   |             |             |
| 0071h   |   |             |             |
| 0072h   | Voltage monitor 1 / Comparator A1 Interrupt Control Register            | VCMP1IC     | XXXXX000b   |
| 0073h   | Voltage monitor 2 / Comparator A2 Interrupt Control Register            | VCMP2IC     | XXXXX000b   |
| 0074h   |   |             |             |
| 0075h   |   |             |             |
| 0076h   |   |             |             |
| 0077h   |   |             |             |
| 0078h   |   |             |             |
| 0079h   |   |             |             |
| 007Ah   |   |             |             |
| 007Bh   |   |             |             |
| 007Ch   |   |             |             |
| 007Dh   |   |             |             |
| 007Eh   |   |             |             |
| 007Fh   |   |             |             |

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUICSR register.

**Table 4.3 SFR Information (3) (1)**

| Address | Register                                      | Symbol | After Reset |
|---------|---|--------|-------------|
| 0080h   | DTC Activation Control Register               | DTCTL  | 00h         |
| 0081h   |   |        |             |
| 0082h   |   |        |             |
| 0083h   |   |        |             |
| 0084h   |   |        |             |
| 0085h   |   |        |             |
| 0086h   |   |        |             |
| 0087h   |   |        |             |
| 0088h   | DTC Activation Enable Register 0              | DTCEN0 | 00h         |
| 0089h   | DTC Activation Enable Register 1              | DTCEN1 | 00h         |
| 008Ah   | DTC Activation Enable Register 2              | DTCEN2 | 00h         |
| 008Bh   | DTC Activation Enable Register 3              | DTCEN3 | 00h         |
| 008Ch   | DTC Activation Enable Register 4              | DTCEN4 | 00h         |
| 008Dh   | DTC Activation Enable Register 5              | DTCEN5 | 00h         |
| 008Eh   | DTC Activation Enable Register 6              | DTCEN6 | 00h         |
| 008Fh   |   |        |             |
| 0090h   |   |        |             |
| 0091h   |   |        |             |
| 0092h   |   |        |             |
| 0093h   |   |        |             |
| 0094h   |   |        |             |
| 0095h   |   |        |             |
| 0096h   |   |        |             |
| 0097h   |   |        |             |
| 0098h   |   |        |             |
| 0099h   |   |        |             |
| 009Ah   |   |        |             |
| 009Bh   |   |        |             |
| 009Ch   |   |        |             |
| 009Dh   |   |        |             |
| 009Eh   |   |        |             |
| 009Fh   |   |        |             |
| 00A0h   | UART0 Transmit/Receive Mode Register          | U0MR   | 00h         |
| 00A1h   | UART0 Bit Rate Register                       | U0BRG  | XXh         |
| 00A2h   | UART0 Transmit Buffer Register                | U0TB   | XXh         |
| 00A3h   |   |        | XXh         |
| 00A4h   | UART0 Transmit/Receive Control Register 0     | U0C0   | 00001000b   |
| 00A5h   | UART0 Transmit/Receive Control Register 1     | U0C1   | 00000010b   |
| 00A6h   | UART0 Receive Buffer Register                 | U0RB   | XXh         |
| 00A7h   |   |        | XXh         |
| 00A8h   | UART2 Transmit/Receive Mode Register          | U2MR   | 00h         |
| 00A9h   | UART2 Bit Rate Register                       | U2BRG  | XXh         |
| 00AAh   | UART2 Transmit Buffer Register                | U2TB   | XXh         |
| 00ABh   |   |        | XXh         |
| 00ACh   | UART2 Transmit/Receive Control Register 0     | U2C0   | 00001000b   |
| 00ADh   | UART2 Transmit/Receive Control Register 1     | U2C1   | 00000010b   |
| 00AEh   | UART2 Receive Buffer Register                 | U2RB   | XXh         |
| 00AFh   |   |        | XXh         |
| 00B0h   | UART2 Digital Filter Function Select Register | URXDF  | 00h         |
| 00B1h   |   |        |             |
| 00B2h   |   |        |             |
| 00B3h   |   |        |             |
| 00B4h   |   |        |             |
| 00B5h   |   |        |             |
| 00B6h   |   |        |             |
| 00B7h   |   |        |             |
| 00B8h   |   |        |             |
| 00B9h   |   |        |             |
| 00BAh   |   |        |             |
| 00BBh   | UART2 Special Mode Register 5                 | U2SMR5 | 00h         |
| 00BCh   | UART2 Special Mode Register 4                 | U2SMR4 | 00h         |
| 00BDh   | UART2 Special Mode Register 3                 | U2SMR3 | 000X0X0Xb   |
| 00BEh   | UART2 Special Mode Register 2                 | U2SMR2 | X0000000b   |
| 00BFh   | UART2 Special Mode Register                   | U2SMR  | X0000000b   |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.4 SFR Information (4) (1)**

| Address | Register                    | Symbol  | After Reset |
|---------|-----------------------------|---------|-------------|
| 00C0h   | A/D Register 0              | AD0     | XXh         |
| 00C1h   |                             |         | 000000XXb   |
| 00C2h   | A/D Register 1              | AD1     | XXh         |
| 00C3h   |                             |         | 000000XXb   |
| 00C4h   | A/D Register 2              | AD2     | XXh         |
| 00C5h   |                             |         | 000000XXb   |
| 00C6h   | A/D Register 3              | AD3     | XXh         |
| 00C7h   |                             |         | 000000XXb   |
| 00C8h   | A/D Register 4              | AD4     | XXh         |
| 00C9h   |                             |         | 000000XXb   |
| 00CAh   | A/D Register 5              | AD5     | XXh         |
| 00CBh   |                             |         | 000000XXb   |
| 00CCh   | A/D Register 6              | AD6     | XXh         |
| 00CDh   |                             |         | 000000XXb   |
| 00CEh   | A/D Register 7              | AD7     | XXh         |
| 00CFh   |                             |         | 000000XXb   |
| 00D0h   |                             |         |             |
| 00D1h   |                             |         |             |
| 00D2h   |                             |         |             |
| 00D3h   |                             |         |             |
| 00D4h   | A/D Mode Register           | ADMOD   | 00h         |
| 00D5h   | A/D Input Select Register   | ADINSEL | 11000000b   |
| 00D6h   | A/D Control Register 0      | ADCON0  | 00h         |
| 00D7h   | A/D Control Register 1      | ADCON1  | 00h         |
| 00D8h   | D/A 0 Register              | DA0     | 00h         |
| 00D9h   | D/A 1 Register              | DA1     | 00h         |
| 00DAh   |                             |         |             |
| 00DBh   |                             |         |             |
| 00DCh   | D/A Control Register        | DACON   | 00h         |
| 00DDh   |                             |         |             |
| 00DEh   |                             |         |             |
| 00DFh   |                             |         |             |
| 00E0h   | Port P0 Register            | P0      | XXh         |
| 00E1h   | Port P1 Register            | P1      | XXh         |
| 00E2h   | Port P0 Direction Register  | PD0     | 00h         |
| 00E3h   | Port P1 Direction Register  | PD1     | 00h         |
| 00E4h   | Port P2 Register            | P2      | XXh         |
| 00E5h   | Port P3 Register            | P3      | XXh         |
| 00E6h   | Port P2 Direction Register  | PD2     | 00h         |
| 00E7h   | Port P3 Direction Register  | PD3     | 00h         |
| 00E8h   | Port P4 Register            | P4      | XXh         |
| 00E9h   | Port P5 Register            | P5      | XXh         |
| 00EAh   | Port P4 Direction Register  | PD4     | 00h         |
| 00EBh   | Port P5 Direction Register  | PD5     | 00h         |
| 00ECh   | Port P6 Register            | P6      | XXh         |
| 00EDh   | Port P7 Register            | P7      | XXh         |
| 00EEh   | Port P6 Direction Register  | PD6     | 00h         |
| 00EFh   | Port P7 Direction Register  | PD7     | 00h         |
| 00F0h   |                             |         |             |
| 00F1h   |                             |         |             |
| 00F2h   |                             |         |             |
| 00F3h   |                             |         |             |
| 00F4h   | Port P10 Register           | P10     | XXh         |
| 00F5h   | Port P11 Register           | P11     | XXh         |
| 00F6h   | Port P10 Direction Register | PD10    | 00h         |
| 00F7h   | Port P11 Direction Register | PD11    | 00h         |
| 00F8h   | Port P12 Register           | P12     | XXh         |
| 00F9h   | Port P13 Register           | P13     | XXh         |
| 00FAh   | Port P12 Direction Register | PD12    | 00h         |
| 00FBh   | Port P13 Direction Register | PD13    | 00h         |
| 00FCh   |                             |         |             |
| 00FDh   |                             |         |             |
| 00FEh   |                             |         |             |
| 00FFh   |                             |         |             |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.5 SFR Information (5) (1)**

| Address | Register   | Symbol  | After Reset |
|---------|--|---------|-------------|
| 0100h   | Timer RA Control Register                                      | TRACR   | 00h         |
| 0101h   | Timer RA I/O Control Register                                  | TRAIOC  | 00h         |
| 0102h   | Timer RA Mode Register   | TRAMR   | 00h         |
| 0103h   | Timer RA Prescaler Register                                    | TRAPRE  | FFh         |
| 0104h   | Timer RA Register  | TRA     | FFh         |
| 0105h   | LIN Control Register 2   | LINCR2  | 00h         |
| 0106h   | LIN Control Register   | LINCR   | 00h         |
| 0107h   | LIN Status Register  | LINST   | 00h         |
| 0108h   | Timer RB Control Register                                      | TRBCR   | 00h         |
| 0109h   | Timer RB One-Shot Control Register                             | TRBOCR  | 00h         |
| 010Ah   | Timer RB I/O Control Register                                  | TRBIOC  | 00h         |
| 010Bh   | Timer RB Mode Register   | TRBMR   | 00h         |
| 010Ch   | Timer RB Prescaler Register                                    | TRBPRE  | FFh         |
| 010Dh   | Timer RB Secondary Register                                    | TRBSC   | FFh         |
| 010Eh   | Timer RB Primary Register                                      | TRBPR   | FFh         |
| 010Fh   |  |         |             |
| 0110h   |  |         |             |
| 0111h   |  |         |             |
| 0112h   |  |         |             |
| 0113h   |  |         |             |
| 0114h   |  |         |             |
| 0115h   |  |         |             |
| 0116h   |  |         |             |
| 0117h   |  |         |             |
| 0118h   | Timer RE Second Data Register / Timer RE Counter Data Register | TRESEC  | XXh         |
| 0119h   | Timer RE Minute Data Register / Timer RE Compare Data Register | TREMIN  | XXh         |
| 011Ah   | Timer RE Hour Data Register                                    | TREHR   | XXh         |
| 011Bh   | Timer RE Day of Week Data Register                             | TREWK   | XXh         |
| 011Ch   | Timer RE Control Register 1                                    | TRECR1  | XXXXX0XXb   |
| 011Dh   | Timer RE Control Register 2                                    | TRECR2  | XXh         |
| 011Eh   | Timer RE Count Source Select Register                          | TRECSR  | 00001000b   |
| 011Fh   |  |         |             |
| 0120h   | Timer RC Mode Register   | TRCMR   | 01001000b   |
| 0121h   | Timer RC Control Register 1                                    | TRCCR1  | 00h         |
| 0122h   | Timer RC Interrupt Enable Register                             | TRCIER  | 01110000b   |
| 0123h   | Timer RC Status Register                                       | TRCSR   | 01110000b   |
| 0124h   | Timer RC I/O Control Register 0                                | TRCIOR0 | 10001000b   |
| 0125h   | Timer RC I/O Control Register 1                                | TRCIOR1 | 10001000b   |
| 0126h   | Timer RC Counter   | TRC     | 00h         |
| 0127h   |  |         | 00h         |
| 0128h   | Timer RC General Register A                                    | TRCGRA  | FFh         |
| 0129h   |  |         | FFh         |
| 012Ah   | Timer RC General Register B                                    | TRCGRB  | FFh         |
| 012Bh   |  |         | FFh         |
| 012Ch   | Timer RC General Register C                                    | TRCGRC  | FFh         |
| 012Dh   |  |         | FFh         |
| 012Eh   | Timer RC General Register D                                    | TRCGRD  | FFh         |
| 012Fh   |  |         | FFh         |
| 0130h   | Timer RC Control Register 2                                    | TRCCR2  | 00011000b   |
| 0131h   | Timer RC Digital Filter Function Select Register               | TRCDF   | 00h         |
| 0132h   | Timer RC Output Master Enable Register                         | TRCOER  | 01111111b   |
| 0133h   | Timer RC Trigger Control Register                              | TRCADCR | 00h         |
| 0134h   |  |         |             |
| 0135h   | Timer RD Control Expansion Register                            | TRDECR  | 00h         |
| 0136h   | Timer RD Trigger Control Register                              | TRDADCR | 00h         |
| 0137h   | Timer RD Start Register  | TRDSTR  | 11111100b   |
| 0138h   | Timer RD Mode Register   | TRDMR   | 00001110b   |
| 0139h   | Timer RD PWM Mode Register                                     | TRDPMR  | 10001000b   |
| 013Ah   | Timer RD Function Control Register                             | TRDFCR  | 10000000b   |
| 013Bh   | Timer RD Output Master Enable Register 1                       | TRDOER1 | FFh         |
| 013Ch   | Timer RD Output Master Enable Register 2                       | TRDOER2 | 01111111b   |
| 013Dh   | Timer RD Output Control Register                               | TRDOCR  | 00h         |
| 013Eh   | Timer RD Digital Filter Function Select Register 0             | TRDDF0  | 00h         |
| 013Fh   | Timer RD Digital Filter Function Select Register 1             | TRDDF1  | 00h         |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.6 SFR Information (6) (1)**

| Address | Register  | Symbol   | After Reset |
|---------|---|----------|-------------|
| 0140h   | Timer RD Control Register 0                       | TRDCR0   | 00h         |
| 0141h   | Timer RD I/O Control Register A0                  | TRDIORA0 | 10001000b   |
| 0142h   | Timer RD I/O Control Register C0                  | TRDIORC0 | 10001000b   |
| 0143h   | Timer RD Status Register 0                        | TRDSR0   | 11100000b   |
| 0144h   | Timer RD Interrupt Enable Register 0              | TRDIER0  | 11100000b   |
| 0145h   | Timer RD PWM Mode Output Level Control Register 0 | TRDPOCR0 | 11111000b   |
| 0146h   | Timer RD Counter 0                                | TRD0     | 00h         |
| 0147h   |   |          | 00h         |
| 0148h   | Timer RD General Register A0                      | TRDGRA0  | FFh         |
| 0149h   |   |          | FFh         |
| 014Ah   | Timer RD General Register B0                      | TRDGRB0  | FFh         |
| 014Bh   |   |          | FFh         |
| 014Ch   | Timer RD General Register C0                      | TRDGRC0  | FFh         |
| 014Dh   |   |          | FFh         |
| 014Eh   | Timer RD General Register D0                      | TRDGRD0  | FFh         |
| 014Fh   |   |          | FFh         |
| 0150h   | Timer RD Control Register 1                       | TRDCR1   | 00h         |
| 0151h   | Timer RD I/O Control Register A1                  | TRDIORA1 | 10001000b   |
| 0152h   | Timer RD I/O Control Register C1                  | TRDIORC1 | 10001000b   |
| 0153h   | Timer RD Status Register 1                        | TRDSR1   | 11000000b   |
| 0154h   | Timer RD Interrupt Enable Register 1              | TRDIER1  | 11100000b   |
| 0155h   | Timer RD PWM Mode Output Level Control Register 1 | TRDPOCR1 | 11111000b   |
| 0156h   | Timer RD Counter 1                                | TRD1     | 00h         |
| 0157h   |   |          | 00h         |
| 0158h   | Timer RD General Register A1                      | TRDGRA1  | FFh         |
| 0159h   |   |          | FFh         |
| 015Ah   | Timer RD General Register B1                      | TRDGRB1  | FFh         |
| 015Bh   |   |          | FFh         |
| 015Ch   | Timer RD General Register C1                      | TRDGRC1  | FFh         |
| 015Dh   |   |          | FFh         |
| 015Eh   | Timer RD General Register D1                      | TRDGRD1  | FFh         |
| 015Fh   |   |          | FFh         |
| 0160h   | UART1 Transmit/Receive Mode Register              | U1MR     | 00h         |
| 0161h   | UART1 Bit Rate Register                           | U1BRG    | XXh         |
| 0162h   | UART1 Transmit Buffer Register                    | U1TB     | XXh         |
| 0163h   |   |          | XXh         |
| 0164h   | UART1 Transmit/Receive Control Register 0         | U1C0     | 00001000b   |
| 0165h   | UART1 Transmit/Receive Control Register 1         | U1C1     | 00000010b   |
| 0166h   | UART1 Receive Buffer Register                     | U1RB     | XXh         |
| 0167h   |   |          | XXh         |
| 0168h   |   |          |             |
| 0169h   |   |          |             |
| 016Ah   |   |          |             |
| 016Bh   |   |          |             |
| 016Ch   |   |          |             |
| 016Dh   |   |          |             |
| 016Eh   |   |          |             |
| 016Fh   |   |          |             |
| 0170h   | Timer RG Mode Register                            | TRGMR    | 01000000b   |
| 0171h   | Timer RG Count Control Register                   | TRGCNTC  | 00h         |
| 0172h   | Timer RG Control Register                         | TRGCR    | 10000000b   |
| 0173h   | Timer RG Interrupt Enable Register                | TRGIER   | 11110000b   |
| 0174h   | Timer RG Status Register                          | TRGSR    | 11100000b   |
| 0175h   | Timer RG I/O Control Register                     | TRGIOR   | 00h         |
| 0176h   | Timer RG Counter                                  | TRG      | 00h         |
| 0177h   |   |          | 00h         |
| 0178h   | Timer RG General Register A                       | TRGGRA   | FFh         |
| 0179h   |   |          | FFh         |
| 017Ah   | Timer RG General Register B                       | TRGGRB   | FFh         |
| 017Bh   |   |          | FFh         |
| 017Ch   | Timer RG General Register C                       | TRGGRC   | FFh         |
| 017Dh   |   |          | FFh         |
| 017Eh   | Timer RG General Register D                       | TRGGRD   | FFh         |
| 017Fh   |   |          | FFh         |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.



**Table 4.7 SFR Information (7) (1)**

| Address | Register   | Symbol      | After Reset         |
|---------|--|-------------|---------------------|
| 0180h   | Timer RA Pin Select Register                                     | TRASR       | 00h                 |
| 0181h   | Timer RB/RC Pin Select Register                                  | TRBRCSR     | 00h                 |
| 0182h   | Timer RC Pin Select Register 0                                   | TRCPSR0     | 00h                 |
| 0183h   | Timer RC Pin Select Register 1                                   | TRCPSR1     | 00h                 |
| 0184h   | Timer RD Pin Select Register 0                                   | TRDPSR0     | 00h                 |
| 0185h   | Timer RD Pin Select Register 1                                   | TRDPSR1     | 00h                 |
| 0186h   |  |             |                     |
| 0187h   | Timer RG Pin Select Register                                     | TRGPSR      | 00h                 |
| 0188h   | UART0 Pin Select Register  | U0SR        | 00h                 |
| 0189h   | UART1 Pin Select Register  | U1SR        | 00h                 |
| 018Ah   | UART2 Pin Select Register 0                                      | U2SR0       | 00h                 |
| 018Bh   | UART2 Pin Select Register 1                                      | U2SR1       | 00h                 |
| 018Ch   | SSU/IIC Pin Select Register                                      | SSUIICSR    | 00h                 |
| 018Dh   | Key Input Pin Select Register                                    | KISR        | 00h                 |
| 018Eh   | INT Interrupt Input Pin Select Register                          | INTSR       | 00h                 |
| 018Fh   | I/O Function Pin Select Register                                 | PINSR       | 00h                 |
| 0190h   |  |             |                     |
| 0191h   |  |             |                     |
| 0192h   |  |             |                     |
| 0193h   | SS Bit Counter Register  | SSBR        | 11111000b           |
| 0194h   | SS Transmit Data Register L / IIC bus Transmit Data Register (2) | SSTDR/ICDRT | FFh                 |
| 0195h   | SS Transmit Data Register H                                      | SSTDRH      | FFh                 |
| 0196h   | SS Receive Data Register L / IIC bus Receive Data Register (2)   | SSRDR/ICDRR | FFh                 |
| 0197h   | SS Receive Data Register H (2)                                   | SSRDRH      | FFh                 |
| 0198h   | SS Control Register H / IIC bus Control Register 1 (2)           | SSCRH/ICCR1 | 00h                 |
| 0199h   | SS Control Register L / IIC bus Control Register 2 (2)           | SSCRL/ICCR2 | 01111101b           |
| 019Ah   | SS Mode Register / IIC bus Mode Register (2)                     | SSMR/ICMR   | 00010000b/00011000b |
| 019Bh   | SS Enable Register / IIC bus Interrupt Enable Register (2)       | SSER/ICIER  | 00h                 |
| 019Ch   | SS Status Register / IIC bus Status Register (2)                 | SSSR/ICSR   | 00h/0000X000b       |
| 019Dh   | SS Mode Register 2 / Slave Address Register (2)                  | SSMR2/SAR   | 00h                 |
| 019Eh   |  |             |                     |
| 019Fh   |  |             |                     |
| 01A0h   |  |             |                     |
| 01A1h   |  |             |                     |
| 01A2h   |  |             |                     |
| 01A3h   |  |             |                     |
| 01A4h   |  |             |                     |
| 01A5h   |  |             |                     |
| 01A6h   |  |             |                     |
| 01A7h   |  |             |                     |
| 01A8h   |  |             |                     |
| 01A9h   |  |             |                     |
| 01AAh   |  |             |                     |
| 01ABh   |  |             |                     |
| 01ACh   |  |             |                     |
| 01ADh   |  |             |                     |
| 01AEh   |  |             |                     |
| 01AFh   |  |             |                     |
| 01B0h   |  |             |                     |
| 01B1h   |  |             |                     |
| 01B2h   | Flash Memory Status Register                                     | FST         | 10000X00b           |
| 01B3h   |  |             |                     |
| 01B4h   | Flash Memory Control Register 0                                  | FMR0        | 00h                 |
| 01B5h   | Flash Memory Control Register 1                                  | FMR1        | 00h                 |
| 01B6h   | Flash Memory Control Register 2                                  | FMR2        | 00h                 |
| 01B7h   |  |             |                     |
| 01B8h   |  |             |                     |
| 01B9h   |  |             |                     |
| 01BAh   |  |             |                     |
| 01BBh   |  |             |                     |
| 01BCh   |  |             |                     |
| 01BDh   |  |             |                     |
| 01BEh   |  |             |                     |
| 01BFh   |  |             |                     |

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- Selectable by the IICSEL bit in the SSUIICSR register.

**Table 4.8 SFR Information (8) (1)**

| Address | Register                                  | Symbol | After Reset |
|---------|---|--------|-------------|
| 01C0h   | Address Match Interrupt Register 0        | RMAD0  | XXh         |
| 01C1h   |   |        | XXh         |
| 01C2h   |   |        | 0000XXXXb   |
| 01C3h   | Address Match Interrupt Enable Register 0 | AIER0  | 00h         |
| 01C4h   | Address Match Interrupt Register 1        | RMAD1  | XXh         |
| 01C5h   |   |        | XXh         |
| 01C6h   |   |        | 0000XXXXb   |
| 01C7h   | Address Match Interrupt Enable Register 1 | AIER1  | 00h         |
| 01C8h   |   |        |             |
| 01C9h   |   |        |             |
| 01CAh   |   |        |             |
| 01CBh   |   |        |             |
| 01CCh   |   |        |             |
| 01CDh   |   |        |             |
| 01CEh   |   |        |             |
| 01CFh   |   |        |             |
| 01D0h   |   |        |             |
| 01D1h   |   |        |             |
| 01D2h   |   |        |             |
| 01D3h   |   |        |             |
| 01D4h   |   |        |             |
| 01D5h   |   |        |             |
| 01D6h   |   |        |             |
| 01D7h   |   |        |             |
| 01D8h   |   |        |             |
| 01D9h   |   |        |             |
| 01DAh   |   |        |             |
| 01DBh   |   |        |             |
| 01DCh   |   |        |             |
| 01DDh   |   |        |             |
| 01DEh   |   |        |             |
| 01DFh   |   |        |             |
| 01E0h   | Port P0 Pull-Up Control Register          | P0PUR  | 00h         |
| 01E1h   | Port P1 Pull-Up Control Register          | P1PUR  | 00h         |
| 01E2h   | Port P2 Pull-Up Control Register          | P2PUR  | 00h         |
| 01E3h   | Port P3 Pull-Up Control Register          | P3PUR  | 00h         |
| 01E4h   | Port P4 Pull-Up Control Register          | P4PUR  | 00h         |
| 01E5h   | Port P5 Pull-Up Control Register          | P5PUR  | 00h         |
| 01E6h   | Port P6 Pull-Up Control Register          | P6PUR  | 00h         |
| 01E7h   | Port P7 Pull-Up Control Register          | P7PUR  | 00h         |
| 01E8h   |   |        |             |
| 01E9h   |   |        |             |
| 01EAh   | Port P10 Pull-Up Control Register         | P10PUR | 00h         |
| 01EBh   | Port P11 Pull-Up Control Register         | P11PUR | 00h         |
| 01ECh   | Port P12 Pull-Up Control Register         | P12PUR | 00h         |
| 01EDh   | Port P13 Pull-Up Control Register         | P13PUR | 00h         |
| 01EEh   |   |        |             |
| 01EFh   |   |        |             |
| 01F0h   | Port P10 Drive Capacity Control Register  | P10DRR | 00h         |
| 01F1h   | Port P11 Drive Capacity Control Register  | P11DRR | 00h         |
| 01F2h   |   |        |             |
| 01F3h   |   |        |             |
| 01F4h   |   |        |             |
| 01F5h   | Input Threshold Control Register 0        | VLT0   | 00h         |
| 01F6h   | Input Threshold Control Register 1        | VLT1   | 00h         |
| 01F7h   | Input Threshold Control Register 2        | VLT2   | 00h         |
| 01F8h   | Comparator B Control Register 0           | INTCMP | 00h         |
| 01F9h   |   |        |             |
| 01FAh   | External Input Enable Register 0          | INTEN  | 00h         |
| 01FBh   | External Input Enable Register 1          | INTEN1 | 00h         |
| 01FCh   | INT Input Filter Select Register 0        | INTF   | 00h         |
| 01FDh   | INT Input Filter Select Register 1        | INTF1  | 00h         |
| 01FEh   | Key Input Enable Register 0               | KIEN   | 00h         |
| 01FFh   | Key Input Enable Register 1               | KIEN1  | 00h         |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.9 SFR Information (9) (1)**

| Address | Register                     | Symbol | After Reset |
|---------|------------------------------|--------|-------------|
| 0200h   | LCD Control Register         | LCR0   | 00h         |
| 0201h   | LCD Bias Control Register    | LCR1   | 00h         |
| 0202h   | LCD Display Control Register | LCR2   | X0000000b   |
| 0203h   | LCD Clock Control Register   | LCR3   | 00h         |
| 0204h   |                              |        |             |
| 0205h   |                              |        |             |
| 0206h   | LCD Port Select Register 0   | LSE0   | 00h         |
| 0207h   | LCD Port Select Register 1   | LSE1   | 00h         |
| 0208h   | LCD Port Select Register 2   | LSE2   | 00h         |
| 0209h   | LCD Port Select Register 3   | LSE3   | 00h         |
| 020Ah   | LCD Port Select Register 4   | LSE4   | 00h         |
| 020Bh   | LCD Port Select Register 5   | LSE5   | 00h         |
| 020Ch   | LCD Port Select Register 6   | LSE6   | 00h         |
| 020Dh   | LCD Port Select Register 7   | LSE7   | 00h         |
| 020Eh   |                              |        |             |
| 020Fh   |                              |        |             |
| 0210h   | LCD Display Data Register    | LRA0L  | XXh         |
| 0211h   |                              | LRA1L  | XXh         |
| 0212h   |                              | LRA2L  | XXh         |
| 0213h   |                              | LRA3L  | XXh         |
| 0214h   |                              | LRA4L  | XXh         |
| 0215h   |                              | LRA5L  | XXh         |
| 0216h   |                              | LRA6L  | XXh         |
| 0217h   |                              | LRA7L  | XXh         |
| 0218h   |                              | LRA8L  | XXh         |
| 0219h   |                              | LRA9L  | XXh         |
| 021Ah   |                              | LRA10L | XXh         |
| 021Bh   |                              | LRA11L | XXh         |
| 021Ch   |                              | LRA12L | XXh         |
| 021Dh   |                              | LRA13L | XXh         |
| 021Eh   |                              | LRA14L | XXh         |
| 021Fh   |                              | LRA15L | XXh         |
| 0220h   |                              | LRA16L | XXh         |
| 0221h   |                              | LRA17L | XXh         |
| 0222h   |                              | LRA18L | XXh         |
| 0223h   |                              | LRA19L | XXh         |
| 0224h   |                              | LRA20L | XXh         |
| 0225h   |                              | LRA21L | XXh         |
| 0226h   |                              | LRA22L | XXh         |
| 0227h   |                              | LRA23L | XXh         |
| 0228h   |                              | LRA24L | XXh         |
| 0229h   |                              | LRA25L | XXh         |
| 022Ah   |                              | LRA26L | XXh         |
| 022Bh   |                              | LRA27L | XXh         |
| 022Ch   |                              | LRA28L | XXh         |
| 022Dh   |                              | LRA29L | XXh         |
| 022Eh   |                              | LRA30L | XXh         |
| 022Fh   |                              | LRA31L | XXh         |
| 0230h   |                              | LRA32L | XXh         |
| 0231h   |                              | LRA33L | XXh         |
| 0232h   |                              | LRA34L | XXh         |
| 0233h   |                              | LRA35L | XXh         |
| 0234h   |                              | LRA36L | XXh         |
| 0235h   |                              | LRA37L | XXh         |
| 0236h   |                              | LRA38L | XXh         |
| 0237h   |                              | LRA39L | XXh         |
| 0238h   |                              | LRA40L | XXh         |
| 0239h   |                              | LRA41L | XXh         |
| 023Ah   |                              | LRA42L | XXh         |
| 023Bh   |                              | LRA43L | XXh         |
| 023Ch   |                              | LRA44L | XXh         |
| 023Dh   |                              | LRA45L | XXh         |
| 023Eh   |                              | LRA46L | XXh         |
| 023Fh   |                              | LRA47L | XXh         |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.10 SFR Information (10) (1)**

| Address | Register                          | Symbol | After Reset |
|---------|-----------------------------------|--------|-------------|
| 0240h   | LCD Display Data Register         | LRA48L | XXh         |
| 0241h   |                                   | LRA49L | XXh         |
| 0242h   |                                   | LRA50L | XXh         |
| 0243h   |                                   | LRA51L | XXh         |
| 0244h   |                                   | LRA52L | XXh         |
| 0245h   |                                   | LRA53L | XXh         |
| 0246h   |                                   | LRA54L | XXh         |
| 0247h   |                                   | LRA55L | XXh         |
| 0248h   |                                   | LRA56L | XXh         |
| 0249h   |                                   | LRA57L | XXh         |
| 024Ah   |                                   | LRA58L | XXh         |
| 024Bh   |                                   | LRA59L | XXh         |
| 024Ch   |                                   | LRA60L | XXh         |
| 024Dh   |                                   | LRA61L | XXh         |
| 024Eh   |                                   | LRA62L | XXh         |
| 024Fh   |                                   | LRA63L | XXh         |
| 0250h   |                                   | LRA64L | XXh         |
| 0251h   |                                   | LRA65L | XXh         |
| 0252h   |                                   | LRA66L | XXh         |
| 0253h   |                                   | LRA67L | XXh         |
| 0254h   |                                   | LRA68L | XXh         |
| 0255h   |                                   | LRA69L | XXh         |
| 0256h   |                                   | LRA70L | XXh         |
| 0257h   |                                   | LRA71L | XXh         |
| 0258h   |                                   | LRA72L | XXh         |
| 0259h   |                                   | LRA73L | XXh         |
| 025Ah   |                                   | LRA74L | XXh         |
| 025Bh   |                                   | LRA75L | XXh         |
| 025Ch   |                                   | LRA76L | XXh         |
| 025Dh   |                                   | LRA77L | XXh         |
| 025Eh   |                                   | LRA78L | XXh         |
| 025Fh   |                                   | LRA79L | XXh         |
| 0260h   |                                   | LRA80L | XXh         |
| 0261h   |                                   | LRA81L | XXh         |
| 0262h   |                                   | LRA82L | XXh         |
| 0263h   |                                   | LRA83L | XXh         |
| 0264h   | LRA84L                            | XXh    |             |
| 0265h   | LRA85L                            | XXh    |             |
| 0266h   | LRA86L                            | XXh    |             |
| 0267h   | LRA87L                            | XXh    |             |
| 0268h   | LRA88L                            | XXh    |             |
| 0269h   | LRA89L                            | XXh    |             |
| 026Ah   | LRA90L                            | XXh    |             |
| 026Bh   | LRA91L                            | XXh    |             |
| 026Ch   | LRA92L                            | XXh    |             |
| 026Dh   | LRA93L                            | XXh    |             |
| 026Eh   | LRA94L                            | XXh    |             |
| 026Fh   | LRA95L                            | XXh    |             |
| 0270h   | LCD Display Control Data Register | LRA0H  | XXh         |
| 0271h   |                                   | LRA1H  | XXh         |
| 0272h   |                                   | LRA2H  | XXh         |
| 0273h   |                                   | LRA3H  | XXh         |
| 0274h   |                                   | LRA4H  | XXh         |
| 0275h   |                                   | LRA5H  | XXh         |
| 0276h   |                                   | LRA6H  | XXh         |
| 0277h   |                                   | LRA7H  | XXh         |
| 0278h   |                                   | LRA8H  | XXh         |
| 0279h   |                                   | LRA9H  | XXh         |
| 027Ah   |                                   | LRA10H | XXh         |
| 027Bh   |                                   | LRA11H | XXh         |
| 027Ch   |                                   | LRA12H | XXh         |
| 027Dh   |                                   | LRA13H | XXh         |
| 027Eh   |                                   | LRA14H | XXh         |
| 027Fh   | LRA15H                            | XXh    |             |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.11 SFR Information (11) (1)**

| Address | Register                          | Symbol | After Reset |
|---------|-----------------------------------|--------|-------------|
| 0280h   | LCD Display Control Data Register | LRA16H | XXh         |
| 0281h   |                                   | LRA17H | XXh         |
| 0282h   |                                   | LRA18H | XXh         |
| 0283h   |                                   | LRA19H | XXh         |
| 0284h   |                                   | LRA20H | XXh         |
| 0285h   |                                   | LRA21H | XXh         |
| 0286h   |                                   | LRA22H | XXh         |
| 0287h   |                                   | LRA23H | XXh         |
| 0288h   |                                   | LRA24H | XXh         |
| 0289h   |                                   | LRA25H | XXh         |
| 028Ah   |                                   | LRA26H | XXh         |
| 028Bh   |                                   | LRA27H | XXh         |
| 028Ch   |                                   | LRA28H | XXh         |
| 028Dh   |                                   | LRA29H | XXh         |
| 028Eh   |                                   | LRA30H | XXh         |
| 028Fh   |                                   | LRA31H | XXh         |
| 0290h   |                                   | LRA32H | XXh         |
| 0291h   |                                   | LRA33H | XXh         |
| 0292h   |                                   | LRA34H | XXh         |
| 0293h   |                                   | LRA35H | XXh         |
| 0294h   |                                   | LRA36H | XXh         |
| 0295h   |                                   | LRA37H | XXh         |
| 0296h   |                                   | LRA38H | XXh         |
| 0297h   |                                   | LRA39H | XXh         |
| 0298h   |                                   | LRA40H | XXh         |
| 0299h   |                                   | LRA41H | XXh         |
| 029Ah   |                                   | LRA42H | XXh         |
| 029Bh   |                                   | LRA43H | XXh         |
| 029Ch   |                                   | LRA44H | XXh         |
| 029Dh   |                                   | LRA45H | XXh         |
| 029Eh   |                                   | LRA46H | XXh         |
| 029Fh   |                                   | LRA47H | XXh         |
| 02A0h   |                                   | LRA48H | XXh         |
| 02A1h   |                                   | LRA49H | XXh         |
| 02A2h   |                                   | LRA50H | XXh         |
| 02A3h   |                                   | LRA51H | XXh         |
| 02A4h   |                                   | LRA52H | XXh         |
| 02A5h   |                                   | LRA53H | XXh         |
| 02A6h   |                                   | LRA54H | XXh         |
| 02A7h   |                                   | LRA55H | XXh         |
| 02A8h   |                                   | LRA56H | XXh         |
| 02A9h   |                                   | LRA57H | XXh         |
| 02AAh   |                                   | LRA58H | XXh         |
| 02ABh   |                                   | LRA59H | XXh         |
| 02ACh   |                                   | LRA60H | XXh         |
| 02ADh   |                                   | LRA61H | XXh         |
| 02AEh   |                                   | LRA62H | XXh         |
| 02AFh   |                                   | LRA63H | XXh         |
| 02B0h   |                                   | LRA64H | XXh         |
| 02B1h   | LRA65H                            | XXh    |             |
| 02B2h   | LRA66H                            | XXh    |             |
| 02B3h   | LRA67H                            | XXh    |             |
| 02B4h   | LRA68H                            | XXh    |             |
| 02B5h   | LRA69H                            | XXh    |             |
| 02B6h   | LRA70H                            | XXh    |             |
| 02B7h   | LRA71H                            | XXh    |             |
| 02B8h   | LRA72H                            | XXh    |             |
| 02B9h   | LRA73H                            | XXh    |             |
| 02BAh   | LRA74H                            | XXh    |             |
| 02BBh   | LRA75H                            | XXh    |             |
| 02BCh   | LRA76H                            | XXh    |             |
| 02BDh   | LRA77H                            | XXh    |             |
| 02BEh   | LRA78H                            | XXh    |             |
| 02BFh   | LRA79H                            | XXh    |             |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.12 SFR Information (12) (1)**

| Address | Register                          | Symbol | After Reset |
|---------|-----------------------------------|--------|-------------|
| 02C0h   | LCD Display Control Data Register | LRA80H | XXh         |
| 02C1h   |                                   | LRA81H | XXh         |
| 02C2h   |                                   | LRA82H | XXh         |
| 02C3h   |                                   | LRA83H | XXh         |
| 02C4h   |                                   | LRA84H | XXh         |
| 02C5h   |                                   | LRA85H | XXh         |
| 02C6h   |                                   | LRA86H | XXh         |
| 02C7h   |                                   | LRA87H | XXh         |
| 02C8h   |                                   | LRA88H | XXh         |
| 02C9h   |                                   | LRA89H | XXh         |
| 02CAh   |                                   | LRA90H | XXh         |
| 02CBh   |                                   | LRA91H | XXh         |
| 02CCh   |                                   | LRA92H | XXh         |
| 02CDh   |                                   | LRA93H | XXh         |
| 02CEh   |                                   | LRA94H | XXh         |
| 02CFh   |                                   | LRA95H | XXh         |
| 02D0h   |                                   |        |             |
| 02D1h   |                                   |        |             |
| 02D2h   |                                   |        |             |
| 02D3h   |                                   |        |             |
| 02D4h   |                                   |        |             |
| 02D5h   |                                   |        |             |
| 02D6h   |                                   |        |             |
| 02D7h   |                                   |        |             |
| 02D8h   |                                   |        |             |
| 02D9h   |                                   |        |             |
| 02DAh   |                                   |        |             |
| 02DBh   |                                   |        |             |
| 02DCh   |                                   |        |             |
| 02DDh   |                                   |        |             |
| 02DEh   |                                   |        |             |
| 02DFh   |                                   |        |             |
| 02E0h   |                                   |        |             |
| 02E1h   |                                   |        |             |
| 02E2h   |                                   |        |             |
| 02E3h   |                                   |        |             |
| 02E4h   |                                   |        |             |
| 02E5h   |                                   |        |             |
| 02E6h   |                                   |        |             |
| 02E7h   |                                   |        |             |
| 02E8h   |                                   |        |             |
| 02E9h   |                                   |        |             |
| 02EAh   |                                   |        |             |
| 02EBh   |                                   |        |             |
| 02ECh   |                                   |        |             |
| 02EDh   |                                   |        |             |
| 02EEh   |                                   |        |             |
| 02EFh   |                                   |        |             |
| 02F0h   |                                   |        |             |
| 02F1h   |                                   |        |             |
| 02F2h   |                                   |        |             |
| 02F3h   |                                   |        |             |
| 02F4h   |                                   |        |             |
| 02F5h   |                                   |        |             |
| 02F6h   |                                   |        |             |
| 02F7h   |                                   |        |             |
| 02F8h   |                                   |        |             |
| 02F9h   |                                   |        |             |
| 02FAh   |                                   |        |             |
| 02FBh   |                                   |        |             |
| 02FCh   |                                   |        |             |
| 02FDh   |                                   |        |             |
| 02FEh   |                                   |        |             |
| 02FFh   |                                   |        |             |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.13 SFR Information (13) (1)**

| Address | Register                 | Symbol | After Reset |
|---------|--------------------------|--------|-------------|
| 2C00h   | DTC Transfer Vector Area |        | XXh         |
| 2C01h   | DTC Transfer Vector Area |        | XXh         |
| 2C02h   | DTC Transfer Vector Area |        | XXh         |
| 2C03h   | DTC Transfer Vector Area |        | XXh         |
| 2C04h   | DTC Transfer Vector Area |        | XXh         |
| 2C05h   | DTC Transfer Vector Area |        | XXh         |
| 2C06h   | DTC Transfer Vector Area |        | XXh         |
| 2C07h   | DTC Transfer Vector Area |        | XXh         |
| 2C08h   | DTC Transfer Vector Area |        | XXh         |
| 2C09h   | DTC Transfer Vector Area |        | XXh         |
| 2C0Ah   | DTC Transfer Vector Area |        | XXh         |
| :       | DTC Transfer Vector Area |        | XXh         |
| :       | DTC Transfer Vector Area |        | XXh         |
| 2C3Ah   | DTC Transfer Vector Area |        | XXh         |
| 2C3Bh   | DTC Transfer Vector Area |        | XXh         |
| 2C3Ch   | DTC Transfer Vector Area |        | XXh         |
| 2C3Dh   | DTC Transfer Vector Area |        | XXh         |
| 2C3Eh   | DTC Transfer Vector Area |        | XXh         |
| 2C3Fh   | DTC Transfer Vector Area |        | XXh         |
| 2C40h   | DTC Control Data 0       | DTCD0  | XXh         |
| 2C41h   |                          |        | XXh         |
| 2C42h   |                          |        | XXh         |
| 2C43h   |                          |        | XXh         |
| 2C44h   |                          |        | XXh         |
| 2C45h   |                          |        | XXh         |
| 2C46h   |                          |        | XXh         |
| 2C47h   |                          |        | XXh         |
| 2C48h   | DTC Control Data 1       | DTCD1  | XXh         |
| 2C49h   |                          |        | XXh         |
| 2C4Ah   |                          |        | XXh         |
| 2C4Bh   |                          |        | XXh         |
| 2C4Ch   |                          |        | XXh         |
| 2C4Dh   |                          |        | XXh         |
| 2C4Eh   |                          |        | XXh         |
| 2C4Fh   |                          |        | XXh         |
| 2C50h   | DTC Control Data 2       | DTCD2  | XXh         |
| 2C51h   |                          |        | XXh         |
| 2C52h   |                          |        | XXh         |
| 2C53h   |                          |        | XXh         |
| 2C54h   |                          |        | XXh         |
| 2C55h   |                          |        | XXh         |
| 2C56h   |                          |        | XXh         |
| 2C57h   |                          |        | XXh         |
| 2C58h   | DTC Control Data 3       | DTCD3  | XXh         |
| 2C59h   |                          |        | XXh         |
| 2C5Ah   |                          |        | XXh         |
| 2C5Bh   |                          |        | XXh         |
| 2C5Ch   |                          |        | XXh         |
| 2C5Dh   |                          |        | XXh         |
| 2C5Eh   |                          |        | XXh         |
| 2C5Fh   |                          |        | XXh         |
| 2C60h   | DTC Control Data 4       | DTCD4  | XXh         |
| 2C61h   |                          |        | XXh         |
| 2C62h   |                          |        | XXh         |
| 2C63h   |                          |        | XXh         |
| 2C64h   |                          |        | XXh         |
| 2C65h   |                          |        | XXh         |
| 2C66h   |                          |        | XXh         |
| 2C67h   |                          |        | XXh         |
| 2C68h   | DTC Control Data 5       | DTCD5  | XXh         |
| 2C69h   |                          |        | XXh         |
| 2C6Ah   |                          |        | XXh         |
| 2C6Bh   |                          |        | XXh         |
| 2C6Ch   |                          |        | XXh         |
| 2C6Dh   |                          |        | XXh         |
| 2C6Eh   |                          |        | XXh         |
| 2C6Fh   |                          |        | XXh         |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.14 SFR Information (14) (1)**

| Address | Register            | Symbol | After Reset |
|---------|---------------------|--------|-------------|
| 2C70h   | DTC Control Data 6  | DTCD6  | XXh         |
| 2C71h   |                     |        | XXh         |
| 2C72h   |                     |        | XXh         |
| 2C73h   |                     |        | XXh         |
| 2C74h   |                     |        | XXh         |
| 2C75h   |                     |        | XXh         |
| 2C76h   |                     |        | XXh         |
| 2C77h   |                     |        | XXh         |
| 2C78h   | DTC Control Data 7  | DTCD7  | XXh         |
| 2C79h   |                     |        | XXh         |
| 2C7Ah   |                     |        | XXh         |
| 2C7Bh   |                     |        | XXh         |
| 2C7Ch   |                     |        | XXh         |
| 2C7Dh   |                     |        | XXh         |
| 2C7Eh   |                     |        | XXh         |
| 2C7Fh   |                     |        | XXh         |
| 2C80h   | DTC Control Data 8  | DTCD8  | XXh         |
| 2C81h   |                     |        | XXh         |
| 2C82h   |                     |        | XXh         |
| 2C83h   |                     |        | XXh         |
| 2C84h   |                     |        | XXh         |
| 2C85h   |                     |        | XXh         |
| 2C86h   |                     |        | XXh         |
| 2C87h   |                     |        | XXh         |
| 2C88h   | DTC Control Data 9  | DTCD9  | XXh         |
| 2C89h   |                     |        | XXh         |
| 2C8Ah   |                     |        | XXh         |
| 2C8Bh   |                     |        | XXh         |
| 2C8Ch   |                     |        | XXh         |
| 2C8Dh   |                     |        | XXh         |
| 2C8Eh   |                     |        | XXh         |
| 2C8Fh   |                     |        | XXh         |
| 2C90h   | DTC Control Data 10 | DTCD10 | XXh         |
| 2C91h   |                     |        | XXh         |
| 2C92h   |                     |        | XXh         |
| 2C93h   |                     |        | XXh         |
| 2C94h   |                     |        | XXh         |
| 2C95h   |                     |        | XXh         |
| 2C96h   |                     |        | XXh         |
| 2C97h   |                     |        | XXh         |
| 2C98h   | DTC Control Data 11 | DTCD11 | XXh         |
| 2C99h   |                     |        | XXh         |
| 2C9Ah   |                     |        | XXh         |
| 2C9Bh   |                     |        | XXh         |
| 2C9Ch   |                     |        | XXh         |
| 2C9Dh   |                     |        | XXh         |
| 2C9Eh   |                     |        | XXh         |
| 2C9Fh   |                     |        | XXh         |
| 2CA0h   | DTC Control Data 12 | DTCD12 | XXh         |
| 2CA1h   |                     |        | XXh         |
| 2CA2h   |                     |        | XXh         |
| 2CA3h   |                     |        | XXh         |
| 2CA4h   |                     |        | XXh         |
| 2CA5h   |                     |        | XXh         |
| 2CA6h   |                     |        | XXh         |
| 2CA7h   |                     |        | XXh         |
| 2CA8h   | DTC Control Data 13 | DTCD13 | XXh         |
| 2CA9h   |                     |        | XXh         |
| 2CAAh   |                     |        | XXh         |
| 2CABh   |                     |        | XXh         |
| 2CACH   |                     |        | XXh         |
| 2CADh   |                     |        | XXh         |
| 2CAEh   |                     |        | XXh         |
| 2CAFh   |                     |        | XXh         |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.



**Table 4.15 SFR Information (15) (1)**

| Address | Register            | Symbol | After Reset |
|---------|---------------------|--------|-------------|
| 2CB0h   | DTC Control Data 14 | DTCD14 | XXh         |
| 2CB1h   |                     |        | XXh         |
| 2CB2h   |                     |        | XXh         |
| 2CB3h   |                     |        | XXh         |
| 2CB4h   |                     |        | XXh         |
| 2CB5h   |                     |        | XXh         |
| 2CB6h   |                     |        | XXh         |
| 2CB7h   |                     |        | XXh         |
| 2CB8h   | DTC Control Data 15 | DTCD15 | XXh         |
| 2CB9h   |                     |        | XXh         |
| 2CBAh   |                     |        | XXh         |
| 2CBBh   |                     |        | XXh         |
| 2CBCh   |                     |        | XXh         |
| 2CBDh   |                     |        | XXh         |
| 2CBEh   |                     |        | XXh         |
| 2CBFh   |                     |        | XXh         |
| 2CC0h   | DTC Control Data 16 | DTCD16 | XXh         |
| 2CC1h   |                     |        | XXh         |
| 2CC2h   |                     |        | XXh         |
| 2CC3h   |                     |        | XXh         |
| 2CC4h   |                     |        | XXh         |
| 2CC5h   |                     |        | XXh         |
| 2CC6h   |                     |        | XXh         |
| 2CC7h   |                     |        | XXh         |
| 2CC8h   | DTC Control Data 17 | DTCD17 | XXh         |
| 2CC9h   |                     |        | XXh         |
| 2CCAh   |                     |        | XXh         |
| 2CCBh   |                     |        | XXh         |
| 2CCCh   |                     |        | XXh         |
| 2CCDh   |                     |        | XXh         |
| 2CCEh   |                     |        | XXh         |
| 2CCFh   |                     |        | XXh         |
| 2CD0h   | DTC Control Data 18 | DTCD18 | XXh         |
| 2CD1h   |                     |        | XXh         |
| 2CD2h   |                     |        | XXh         |
| 2CD3h   |                     |        | XXh         |
| 2CD4h   |                     |        | XXh         |
| 2CD5h   |                     |        | XXh         |
| 2CD6h   |                     |        | XXh         |
| 2CD7h   |                     |        | XXh         |
| 2CD8h   | DTC Control Data 19 | DTCD19 | XXh         |
| 2CD9h   |                     |        | XXh         |
| 2CDAh   |                     |        | XXh         |
| 2CDBh   |                     |        | XXh         |
| 2CDCh   |                     |        | XXh         |
| 2CDDh   |                     |        | XXh         |
| 2CDEh   |                     |        | XXh         |
| 2CDFh   |                     |        | XXh         |
| 2CE0h   | DTC Control Data 20 | DTCD20 | XXh         |
| 2CE1h   |                     |        | XXh         |
| 2CE2h   |                     |        | XXh         |
| 2CE3h   |                     |        | XXh         |
| 2CE4h   |                     |        | XXh         |
| 2CE5h   |                     |        | XXh         |
| 2CE6h   |                     |        | XXh         |
| 2CE7h   |                     |        | XXh         |
| 2CE8h   | DTC Control Data 21 | DTCD21 | XXh         |
| 2CE9h   |                     |        | XXh         |
| 2CEAh   |                     |        | XXh         |
| 2CEBh   |                     |        | XXh         |
| 2CECh   |                     |        | XXh         |
| 2CEDh   |                     |        | XXh         |
| 2CEEh   |                     |        | XXh         |
| 2CEFh   |                     |        | XXh         |

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

**Table 4.16 SFR Information (16) (1)**

| Address | Register                          | Symbol | After Reset |
|---------|-----------------------------------|--------|-------------|
| 2CF0h   | DTC Control Data 22               | DTCD22 | XXh         |
| 2CF1h   |                                   |        | XXh         |
| 2CF2h   |                                   |        | XXh         |
| 2CF3h   |                                   |        | XXh         |
| 2CF4h   |                                   |        | XXh         |
| 2CF5h   |                                   |        | XXh         |
| 2CF6h   |                                   |        | XXh         |
| 2CF7h   |                                   |        | XXh         |
| 2CF8h   | DTC Control Data 23               | DTCD23 | XXh         |
| 2CF9h   |                                   |        | XXh         |
| 2CFAh   |                                   |        | XXh         |
| 2CFBh   |                                   |        | XXh         |
| 2CFCh   |                                   |        | XXh         |
| 2CFDh   |                                   |        | XXh         |
| 2CFEh   |                                   |        | XXh         |
| 2CFFh   |                                   |        | XXh         |
| 2D00h   |                                   |        |             |
| 2D01h   |                                   |        |             |
| 0FFDBh  | Option Function Select Register 2 | OFS2   | (Note 2)    |
| :       |                                   |        |             |
| 0FFFh   | Option Function Select Register   | OFS    | (Note 2)    |

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- This register cannot be changed by a program. Use a flash programmer to write to it.

## 5. Electrical Characteristics

### 5.1 Absolute Maximum Ratings

**Table 5.1 Absolute Maximum Ratings**

| Symbol                            | Parameter                     |               | Condition   | Rated Value                                      | Unit |
|-----------------------------------|-------------------------------|---------------|---|--|------|
| V <sub>CC</sub> /AV <sub>CC</sub> | Supply voltage                |               |   | -0.3 to 6.5                                      | V    |
| V <sub>i</sub>                    | Input voltage                 | XIN           | XIN-XOUT oscillation on (oscillation buffer ON) <sup>(1)</sup>  | -0.3 to 1.65                                     | V    |
|                                   |                               | XIN           | XIN-XOUT oscillation on (oscillation buffer OFF) <sup>(1)</sup> | -0.3 to V <sub>CC</sub> + 0.3                    | V    |
|                                   |                               | VL1           |   | -0.3 to VL2                                      | V    |
|                                   |                               | VL2           | R8C/L35A, R8C/L35B  | VL1 to VL4                                       | V    |
|                                   |                               |               | R8C/L36A, R8C/L36B, R8C/L38A, R8C/L38B, R8C/L3AA, R8C/L3AB      | VL1 to VL3                                       | V    |
|                                   |                               | VL3           |   | VL2 to VL4                                       | V    |
|                                   |                               | VL4           |   | VL3 to 6.5                                       | V    |
|                                   |                               | Other pins    |   | -0.3 to V <sub>CC</sub> + 0.3                    | V    |
| V <sub>o</sub>                    | Output voltage                | XOUT          | XIN-XOUT oscillation on (oscillation buffer ON) <sup>(1)</sup>  | -0.3 to 1.65                                     | V    |
|                                   |                               | XOUT          | XIN-XOUT oscillation on (oscillation buffer OFF) <sup>(1)</sup> | -0.3 to V <sub>CC</sub> + 0.3                    | V    |
|                                   |                               | VL1           |   | -0.3 to VL2                                      | V    |
|                                   |                               | VL2           | R8C/L35A, R8C/L35B  | VL1 to VL4                                       | V    |
|                                   |                               |               | R8C/L36A, R8C/L36B, R8C/L38A, R8C/L38B, R8C/L3AA, R8C/L3AB      | VL1 to VL3                                       | V    |
|                                   |                               | VL3           |   | VL2 to VL4                                       | V    |
|                                   |                               | VL4           |   | -0.3 to 6.5                                      | V    |
|                                   |                               | CL1, CL2      |   | -0.3 to 6.5                                      | V    |
|                                   |                               | COM0 to COM7  |   | -0.3 to VL4                                      | V    |
|                                   |                               | SEG0 to SEG55 |   | -0.3 to VL4                                      | V    |
|                                   |                               | Other pins    |   | -0.3 to V <sub>CC</sub> + 0.3                    | V    |
| P <sub>d</sub>                    | Power dissipation             |               | -40°C ≤ T <sub>opr</sub> ≤ 85°C                                 | 500  | mW   |
| T <sub>opr</sub>                  | Operating ambient temperature |               |   | -20 to 85 (N version) /<br>-40 to 85 (D version) | °C   |
| T <sub>stg</sub>                  | Storage temperature           |               |   | -65 to 150                                       | °C   |

Note:

1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** of Hardware Manual (REJ09B0441).

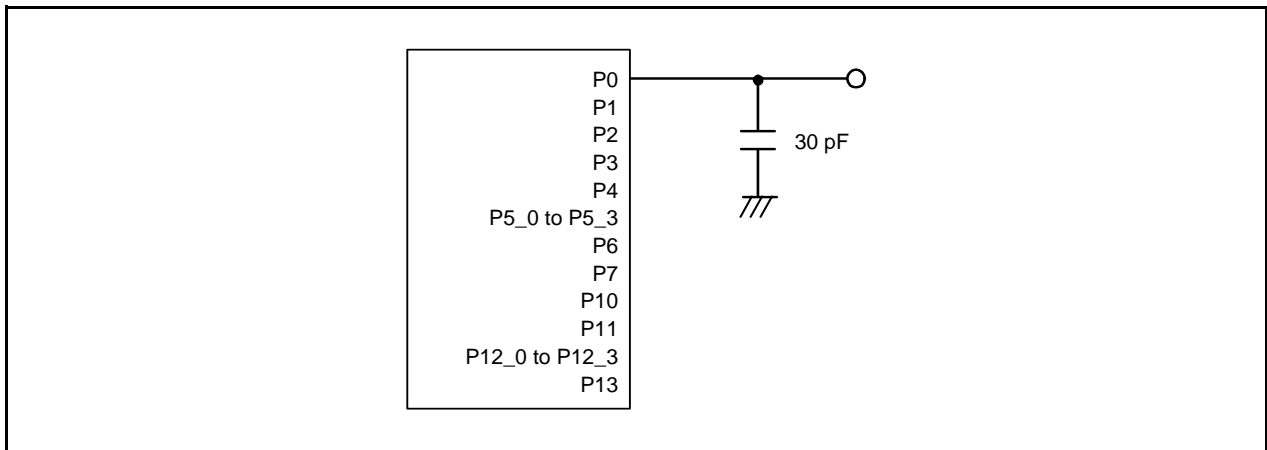
## 5.2 Recommended Operating Conditions

**Table 5.2 Recommended Operating Conditions**  
(VCC = 1.8 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

| Symbol    | Parameter   |                           | Conditions                                | Standard                         |                     |          | Unit     |          |   |
|-----------|---|---------------------------|---|----------------------------------|---------------------|----------|----------|----------|---|
|           |   |                           |   | Min.                             | Typ.                | Max.     |          |          |   |
| Vcc/AVcc  | Supply voltage  |                           |   | 1.8                              | –                   | 5.5      | V        |          |   |
| Vss/AVss  | Supply voltage  |                           |   | –                                | 0                   | –        | V        |          |   |
| VIH       | Input “H” voltage   | Other than CMOS input     |   | 4.0 V ≤ Vcc ≤ 5.5 V              | 0.8 Vcc             | –        | Vcc      | V        |   |
|           |   |                           |   | 2.7 V ≤ Vcc < 4.0 V              | 0.8 Vcc             | –        | Vcc      | V        |   |
|           |   |                           |   | 1.8 V ≤ Vcc < 2.7 V              | 0.9 Vcc             | –        | Vcc      | V        |   |
|           |   | CMOS input                | Input level switching function (I/O port) | Input level selection : 0.35 Vcc | 4.0 V ≤ Vcc ≤ 5.5 V | 0.5 Vcc  | –        | Vcc      | V |
|           |   |                           |   |                                  | 2.7 V ≤ Vcc < 4.0 V | 0.55 Vcc | –        | Vcc      | V |
|           |   |                           |   |                                  | 1.8 V ≤ Vcc < 2.7 V | 0.65 Vcc | –        | Vcc      | V |
|           |   |                           |   | Input level selection : 0.5 Vcc  | 4.0 V ≤ Vcc ≤ 5.5 V | 0.65 Vcc | –        | Vcc      | V |
|           |   |                           |   |                                  | 2.7 V ≤ Vcc < 4.0 V | 0.7 Vcc  | –        | Vcc      | V |
|           |   |                           |   |                                  | 1.8 V ≤ Vcc < 2.7 V | 0.8 Vcc  | –        | Vcc      | V |
|           |   |                           |   | Input level selection : 0.7 Vcc  | 4.0 V ≤ Vcc ≤ 5.5 V | 0.85 Vcc | –        | Vcc      | V |
|           |   |                           |   |                                  | 2.7 V ≤ Vcc < 4.0 V | 0.85 Vcc | –        | Vcc      | V |
|           |   |                           |   |                                  | 1.8 V ≤ Vcc < 2.7 V | 0.85 Vcc | –        | Vcc      | V |
| VIL       | Input “L” voltage   | Other than CMOS input     |   | 4.0 V ≤ Vcc ≤ 5.5 V              | 0                   | –        | 0.2 Vcc  | V        |   |
|           |   |                           |   | 2.7 V ≤ Vcc < 4.0 V              | 0                   | –        | 0.2 Vcc  | V        |   |
|           |   |                           |   | 1.8 V ≤ Vcc < 2.7 V              | 0                   | –        | 0.05 Vcc | V        |   |
|           |   | CMOS input                | Input level switching function (I/O port) | Input level selection : 0.35 Vcc | 4.0 V ≤ Vcc ≤ 5.5 V | 0        | –        | 0.2 Vcc  | V |
|           |   |                           |   |                                  | 2.7 V ≤ Vcc < 4.0 V | 0        | –        | 0.2 Vcc  | V |
|           |   |                           |   |                                  | 1.8 V ≤ Vcc < 2.7 V | 0        | –        | 0.2 Vcc  | V |
|           |   |                           |   | Input level selection : 0.5 Vcc  | 4.0 V ≤ Vcc ≤ 5.5 V | 0        | –        | 0.4 Vcc  | V |
|           |   |                           |   |                                  | 2.7 V ≤ Vcc < 4.0 V | 0        | –        | 0.3 Vcc  | V |
|           |   |                           |   |                                  | 1.8 V ≤ Vcc < 2.7 V | 0        | –        | 0.2 Vcc  | V |
|           |   |                           |   | Input level selection : 0.7 Vcc  | 4.0 V ≤ Vcc ≤ 5.5 V | 0        | –        | 0.55 Vcc | V |
|           |   |                           |   |                                  | 2.7 V ≤ Vcc < 4.0 V | 0        | –        | 0.45 Vcc | V |
|           |   |                           |   |                                  | 1.8 V ≤ Vcc < 2.7 V | 0        | –        | 0.35 Vcc | V |
| IOH(sum)  | Peak sum output “H” current   | Sum of all pins IOH(peak) |   | –                                | –                   | –160     | mA       |          |   |
| IOH(sum)  | Average sum output “H” current  | Sum of all pins IOH(avg)  |   | –                                | –                   | –80      | mA       |          |   |
| IOH(peak) | Peak output “H” current   | Port P10, P11 (2)         |   | –                                | –                   | –40      | mA       |          |   |
|           |   | Other pins                |   | –                                | –                   | –10      | mA       |          |   |
| IOH(avg)  | Average output “H” current (1)  | Port P10, P11 (2)         |   | –                                | –                   | –20      | mA       |          |   |
|           |   | Other pins                |   | –                                | –                   | –5       | mA       |          |   |
| IOI(sum)  | Peak sum output “L” current   | Sum of all pins IOI(peak) |   | –                                | –                   | 160      | mA       |          |   |
| IOI(sum)  | Average sum output “L” current  | Sum of all pins IOI(avg)  |   | –                                | –                   | 80       | mA       |          |   |
| IOI(peak) | Peak output “L” current   | Port P10, P11 (2)         |   | –                                | –                   | 40       | mA       |          |   |
|           |   | Other pins                |   | –                                | –                   | 10       | mA       |          |   |
| IOI(avg)  | Average output “L” current (1)  | Port P10, P11 (2)         |   | –                                | –                   | 20       | mA       |          |   |
|           |   | Other pins                |   | –                                | –                   | 5        | mA       |          |   |
| f(XIN)    | XIN clock input oscillation frequency                                 |                           | 2.7 V ≤ Vcc ≤ 5.5 V                       | –                                | –                   | 20       | MHz      |          |   |
|           |   |                           | 1.8 V ≤ Vcc < 2.7 V                       | –                                | –                   | 5        | MHz      |          |   |
| f(XCIN)   | XCIN clock input oscillation frequency                                |                           | 1.8 V ≤ Vcc ≤ 5.5 V                       | –                                | 32.768              | 50       | kHz      |          |   |
| fOCO40M   | When used as the count source for timer RC, timer RD, or timer RG (3) |                           | 2.7 V ≤ Vcc ≤ 5.5 V                       | 32                               | –                   | 40       | MHz      |          |   |
| fOCO-F    | fOCO-F frequency  |                           | 2.7 V ≤ Vcc ≤ 5.5 V                       | –                                | –                   | 20       | MHz      |          |   |
|           |   |                           | 1.8 V ≤ Vcc < 2.7 V                       | –                                | –                   | 5        | MHz      |          |   |
| –         | System clock frequency  |                           | 2.7 V ≤ Vcc ≤ 5.5 V                       | –                                | –                   | 20       | MHz      |          |   |
|           |   |                           | 1.8 V ≤ Vcc < 2.7 V                       | –                                | –                   | 5        | MHz      |          |   |
| f(BCLK)   | CPU clock frequency   |                           | 2.7 V ≤ Vcc ≤ 5.5 V                       | 0                                | –                   | 20       | MHz      |          |   |
|           |   |                           | 1.8 V ≤ Vcc < 2.7 V                       | 0                                | –                   | 5        | MHz      |          |   |

Notes:

- The average output current indicates the average value of current measured during 100 ms.
- This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.
- fOCO40M can be used as the count source for timer RC, timer RD, or timer RG in the range of VCC = 2.7 V to 5.5V.



**Figure 5.1** Ports P0 to P4, P5\_0 to P5\_3, P6, P7, P10, P11, P12\_0 to P12\_3, and P13 Timing Measurement Circuit

### 5.3 Peripheral Function Characteristics

**Table 5.3 A/D Converter Characteristics**  
 ( $V_{CC}/AV_{CC} = V_{ref} = 2.2$  to  $5.5$  V,  $V_{SS} = 0$  V, and  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version) /  
 $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)

| Symbol      | Parameter                        |             | Conditions  | Standard |      |           | Unit          |
|-------------|----------------------------------|-------------|---|----------|------|-----------|---------------|
|             |                                  |             |   | Min.     | Typ. | Max.      |               |
| –           | Resolution                       |             | $V_{ref} = AV_{CC}$                               | –        | –    | 10        | Bit           |
| –           | Absolute accuracy                | 10-bit mode | $V_{ref} = AV_{CC} = 5.0$ V AN0 to AN19 input     | –        | –    | $\pm 3$   | LSB           |
|             |                                  |             | $V_{ref} = AV_{CC} = 3.3$ V AN0 to AN19 input     | –        | –    | $\pm 5$   | LSB           |
|             |                                  |             | $V_{ref} = AV_{CC} = 3.0$ V AN0 to AN19 input     | –        | –    | $\pm 5$   | LSB           |
|             |                                  |             | $V_{ref} = AV_{CC} = 2.2$ V AN0 to AN19 input     | –        | –    | $\pm 5$   | LSB           |
|             |                                  | 8-bit mode  | $V_{ref} = AV_{CC} = 5.0$ V AN0 to AN19 input     | –        | –    | $\pm 2$   | LSB           |
|             |                                  |             | $V_{ref} = AV_{CC} = 3.3$ V AN0 to AN19 input     | –        | –    | $\pm 2$   | LSB           |
|             |                                  |             | $V_{ref} = AV_{CC} = 3.0$ V AN0 to AN19 input     | –        | –    | $\pm 2$   | LSB           |
|             |                                  |             | $V_{ref} = AV_{CC} = 2.2$ V AN0 to AN19 input     | –        | –    | $\pm 2$   | LSB           |
| $\phi_{AD}$ | A/D conversion clock             |             | $4.0 \leq V_{ref} = AV_{CC} \leq 5.5$ V (1)       | 2        | –    | 20        | MHz           |
|             |                                  |             | $3.2 \leq V_{ref} = AV_{CC} \leq 5.5$ V (1)       | 2        | –    | 16        | MHz           |
|             |                                  |             | $2.7 \leq V_{ref} = AV_{CC} \leq 5.5$ V (1)       | 2        | –    | 10        | MHz           |
|             |                                  |             | $2.2 \leq V_{ref} = AV_{CC} \leq 5.5$ V (1)       | 2        | –    | 5         | MHz           |
| –           | Tolerance level impedance        |             |   | –        | 3    | –         | k $\Omega$    |
| DNL         | Differential non-linearity error |             |   | –        | –    | $\pm 1$   | LSB           |
| $t_{CONV}$  | Conversion time                  | 10-bit mode | $V_{ref} = AV_{CC} = 5.0$ V, $\phi_{AD} = 20$ MHz | 2.15     | –    | –         | $\mu\text{s}$ |
|             |                                  | 8-bit mode  | $V_{ref} = AV_{CC} = 5.0$ V, $\phi_{AD} = 20$ MHz | 2.15     | –    | –         | $\mu\text{s}$ |
| $t_{SAMP}$  | Sampling time                    |             | $\phi_{AD} = 20$ MHz                              | 0.75     | –    | –         | $\mu\text{s}$ |
| $I_{Vref}$  | $V_{ref}$ current                |             | $V_{CC} = 5$ V, $XIN = f1 = \phi_{AD} = 20$ MHz   | –        | 45   | –         | $\mu\text{A}$ |
| $V_{ref}$   | Reference voltage                |             |   | 2.2      | –    | $AV_{CC}$ | V             |
| $V_{IA}$    | Analog input voltage (2)         |             |   | 0        | –    | $V_{ref}$ | V             |

Notes:

1. When the CPU and flash memory stop, the A/D conversion result will be undefined.
2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

**Table 5.4 D/A Converter Characteristics**  
**( $V_{CC}/AV_{CC} = V_{ref} = 2.7$  to  $5.5$  V and  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version) /  $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)**

| Symbol     | Parameter                     | Conditions | Standard |      |      | Unit             |
|------------|-------------------------------|------------|----------|------|------|------------------|
|            |                               |            | Min.     | Typ. | Max. |                  |
| –          | Resolution                    |            | –        | –    | 8    | Bit              |
| –          | Absolute accuracy             |            | –        | –    | 2.5  | LSB              |
| $t_{su}$   | Setup time                    |            | –        | –    | 3    | $\mu\text{s}$    |
| $R_O$      | Output resistor               |            | –        | 6    | –    | $\text{k}\Omega$ |
| $I_{Vref}$ | Reference power input current | (Note 1)   | –        | –    | 1.5  | mA               |

Note:

1. This applies when one D/A converter is used and the value of the  $DA_i$  register ( $i = 0$  or  $1$ ) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

**Table 5.5 Comparator A Characteristics**  
**( $V_{CC} = 2.7$  to  $5.5$  V and  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version) /  $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)**

| Symbol            | Parameter                                   | Condition                                  | Standard |      |                | Unit          |
|-------------------|---|--|----------|------|----------------|---------------|
|                   |   |  | Min.     | Typ. | Max.           |               |
| LVREF             | External reference voltage input range      |  | 1.4      | –    | $V_{CC}$       | V             |
| LVCMP1,<br>LVCMP2 | External comparison voltage input range     |  | –0.3     | –    | $V_{CC} + 0.3$ | V             |
| –                 | Offset                                      |  | –        | 50   | 200            | mV            |
| –                 | Comparator output delay time <sup>(1)</sup> | At falling, $V_i = V_{ref} - 100$ mV       | –        | 3    | –              | $\mu\text{s}$ |
| –                 |   | At falling, $V_i = V_{ref} - 1$ V or below | –        | 1.5  | –              | $\mu\text{s}$ |
| –                 |   | At rising, $V_i = V_{ref} + 100$ mV        | –        | 2    | –              | $\mu\text{s}$ |
| –                 |   | At rising, $V_i = V_{ref} + 1$ V or above  | –        | 0.5  | –              | $\mu\text{s}$ |
| –                 | Comparator operating current                | $V_{CC} = 5.0$ V                           | –        | 0.5  | –              | $\mu\text{A}$ |

Note:

1. When the digital filter is disabled.

**Table 5.6 Comparator B Characteristics**  
**( $V_{CC} = 2.7$  to  $5.5$  V and  $T_{opr} = -20$  to  $85^{\circ}\text{C}$  (N version) /  $-40$  to  $85^{\circ}\text{C}$  (D version), unless otherwise specified.)**

| Symbol    | Parameter                                   | Condition                  | Standard |      |                | Unit          |
|-----------|---|----------------------------|----------|------|----------------|---------------|
|           |   |                            | Min.     | Typ. | Max.           |               |
| $V_{ref}$ | IVREF1, IVREF3 input reference voltage      |                            | 0        | –    | $V_{CC} - 1.4$ | V             |
| $V_i$     | IVCMP1, IVCMP3 input voltage                |                            | –0.3     | –    | $V_{CC} + 0.3$ | V             |
| –         | Offset                                      |                            | –        | 5    | 100            | mV            |
| $t_d$     | Comparator output delay time <sup>(1)</sup> | $V_i = V_{ref} \pm 100$ mV | –        | 0.1  | –              | $\mu\text{s}$ |
| ICMP      | Comparator operating current                | $V_{CC} = 5.0$ V           | –        | 17.5 | –              | $\mu\text{A}$ |

Note:

1. When the digital filter is disabled.

**Table 5.7 Flash Memory (Program ROM) Characteristics**  
**(VCC = 2.7 to 5.5 V and T<sub>opr</sub> = 0 to 60°C, unless otherwise specified.)**

| Symbol                  | Parameter   | Conditions                 | Standard  |      |                             | Unit  |
|-------------------------|---|----------------------------|-----------|------|-----------------------------|-------|
|                         |   |                            | Min.      | Typ. | Max.                        |       |
| –                       | Program/erase endurance (1)                                       |                            | 1,000 (2) | –    | –                           | times |
| –                       | Byte program time   |                            | –         | 80   | TBD                         | μs    |
| –                       | Block erase time  |                            | –         | 0.3  | TBD                         | s     |
| t <sub>d</sub> (SR-SUS) | Time delay from suspend request until suspend                     |                            | –         | –    | 5 + CPU clock<br>× 3 cycles | ms    |
| –                       | Interval from erase start/restart until following suspend request |                            | 0         | –    | –                           | μs    |
| –                       | Suspend interval necessary for auto-erasure to complete           |                            | 33        | –    | –                           | ms    |
| –                       | Time from suspend until erase restart                             |                            | –         | –    | 30 + CPU clock<br>× 1 cycle | μs    |
| –                       | Program, erase voltage  |                            | 2.7       | –    | 5.5                         | V     |
| –                       | Read voltage  |                            | 1.8       | –    | 5.5                         | V     |
| –                       | Program, erase temperature  |                            | 0         | –    | 60                          | °C    |
| –                       | Data hold time (6)  | Ambient temperature = 55°C | 20        | –    | –                           | year  |

Notes:

- Definition of programming/erasure endurance  
 The programming and erasure endurance is defined on a per-block basis.  
 If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
 However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.

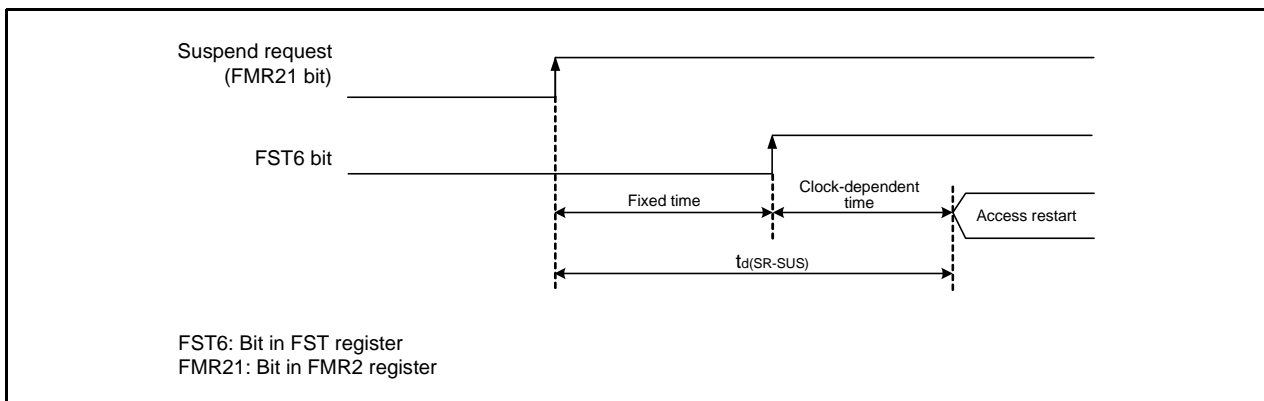


**Table 5.8 Flash Memory (Data flash Block A to Block D) Characteristics  
 (VCC = 2.7 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless  
 otherwise specified.)**

| Symbol     | Parameter   | Conditions                  | Standard   |      |                             | Unit  |
|------------|---|-----------------------------|------------|------|-----------------------------|-------|
|            |   |                             | Min.       | Typ. | Max.                        |       |
| –          | Program/erase endurance (1)                                       |                             | 10,000 (2) | –    | –                           | times |
| –          | Byte program time<br>(program/erase endurance ≤ 1,000 times)      |                             | –          | 160  | TBD                         | μs    |
| –          | Byte program time<br>(program/erase endurance > 1,000 times)      |                             | –          | 300  | –                           | μs    |
| –          | Block erase time<br>(program/erase endurance ≤ 1,000 times)       |                             | –          | 0.2  | –                           | s     |
| –          | Block erase time<br>(program/erase endurance > 1,000 times)       |                             | –          | 0.3  | –                           | s     |
| td(SR-SUS) | Time delay from suspend request until suspend                     |                             | –          | –    | 5 + CPU clock<br>× 3 cycles | ms    |
| –          | Interval from erase start/restart until following suspend request |                             | 0          | –    | –                           | μs    |
| –          | Suspend interval necessary for auto-erasure to complete           |                             | 33         | –    | –                           | ms    |
| –          | Time from suspend until erase restart                             |                             | –          | –    | 30 + CPU clock<br>× 1 cycle | μs    |
| –          | Program, erase voltage  |                             | 2.7        | –    | 5.5                         | V     |
| –          | Read voltage  |                             | 1.8        | –    | 5.5                         | V     |
| –          | Program, erase temperature  |                             | -20 (6)    | –    | 85                          | °C    |
| –          | Data hold time (7)  | Ambient temperature = 55 °C | 20         | –    | –                           | year  |

Notes:

- Definition of programming/erasure endurance  
 The programming and erasure endurance is defined on a per-block basis.  
 If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.  
 However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 40°C for D version.
- The data hold time includes time that the power supply is off or the clock is not supplied.



**Figure 5.2 Time delay until Suspend**

**Table 5.9 Voltage Detection 0 Circuit Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol              | Parameter   | Condition   | Standard |      |      | Unit |
|---------------------|---|---|----------|------|------|------|
|                     |   |   | Min.     | Typ. | Max. |      |
| V <sub>det0</sub>   | Voltage detection level V <sub>det0_0</sub> (1)                   |   | TBD      | 1.90 | TBD  | V    |
|                     | Voltage detection level V <sub>det0_1</sub> (1)                   |   | TBD      | 2.35 | TBD  | V    |
|                     | Voltage detection level V <sub>det0_2</sub> (1)                   |   | TBD      | 2.85 | TBD  | V    |
|                     | Voltage detection level V <sub>det0_3</sub> (1)                   |   | TBD      | 3.80 | TBD  | V    |
| –                   | Voltage detection 0 circuit response time (3)                     | At the falling of V <sub>CC</sub> from 5 V to (V <sub>det0_0</sub> - 0.1) V | –        | 6    | 150  | μs   |
| –                   | Voltage detection circuit self power consumption                  | VCA25 = 1, V <sub>CC</sub> = 5.0 V  | –        | 1.5  | –    | μA   |
| t <sub>d(E-A)</sub> | Waiting time until voltage detection circuit operation starts (2) |   | –        | –    | 100  | μs   |

Notes:

1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V<sub>det0</sub>.

**Table 5.10 Voltage Detection 1 Circuit Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol              | Parameter  | Condition   | Standard |      |      | Unit |
|---------------------|--|---|----------|------|------|------|
|                     |  |   | Min.     | Typ. | Max. |      |
| V <sub>det1</sub>   | Voltage detection level V <sub>det1_0</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 2.20 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_1</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 2.35 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_2</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 2.50 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_3</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 2.65 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_4</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 2.80 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_5</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 2.95 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_6</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 3.10 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_7</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 3.25 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_8</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 3.40 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_9</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 3.55 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_A</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 3.70 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_B</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 3.85 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_C</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 4.00 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_D</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 4.15 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_E</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 4.30 | TBD  | V    |
|                     | Voltage detection level V <sub>det1_F</sub> (1)                                  | At the falling of V <sub>CC</sub>   | TBD      | 4.45 | TBD  | V    |
| –                   | Hysteresis width at the rising of V <sub>CC</sub> in voltage detection 1 circuit | V <sub>det1_0</sub> to V <sub>det1_5</sub> selected                         | –        | 0.07 | –    | V    |
| –                   |  | V <sub>det1_6</sub> to V <sub>det1_F</sub> selected                         | –        | 0.10 | –    | V    |
| –                   | Voltage detection 1 circuit response time (2)                                    | At the falling of V <sub>CC</sub> from 5 V to (V <sub>det1_0</sub> - 0.1) V | –        | 60   | 150  | μs   |
| –                   | Voltage detection circuit self power consumption                                 | VCA26 = 1, V <sub>CC</sub> = 5.0 V  | –        | 1.7  | –    | μA   |
| t <sub>d(E-A)</sub> | Waiting time until voltage detection circuit operation starts (3)                |   | –        | –    | 100  | μs   |

Notes:

1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V<sub>det1</sub>.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

**Table 5.11 Voltage Detection 2 Circuit Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol              | Parameter  | Condition   | Standard |      |      | Unit |
|---------------------|--|---|----------|------|------|------|
|                     |  |   | Min.     | Typ. | Max. |      |
| V <sub>det2</sub>   | Voltage detection level V <sub>det2_0</sub> <sup>(1)</sup>                       | At the falling of V <sub>CC</sub>   | TBD      | 4.00 | TBD  | V    |
|                     | Voltage detection level V <sub>det2_EXT</sub> <sup>(1)</sup>                     | At the falling of LVCMP2  | TBD      | 1.34 | TBD  | V    |
| –                   | Hysteresis width at the rising of V <sub>CC</sub> in voltage detection 2 circuit |   | –        | 0.10 | –    | V    |
| –                   | Voltage detection 2 circuit response time <sup>(2)</sup>                         | At the falling of V <sub>CC</sub> from 5 V to (V <sub>det2_0</sub> – 0.1) V | –        | 20   | 150  | μs   |
| –                   | Voltage detection circuit self power consumption                                 | VCA27 = 1, V <sub>CC</sub> = 5.0 V  | –        | 1.7  | –    | μA   |
| t <sub>d(E-A)</sub> | Waiting time until voltage detection circuit operation starts <sup>(3)</sup>     |   | –        | –    | 100  | μs   |

Notes:

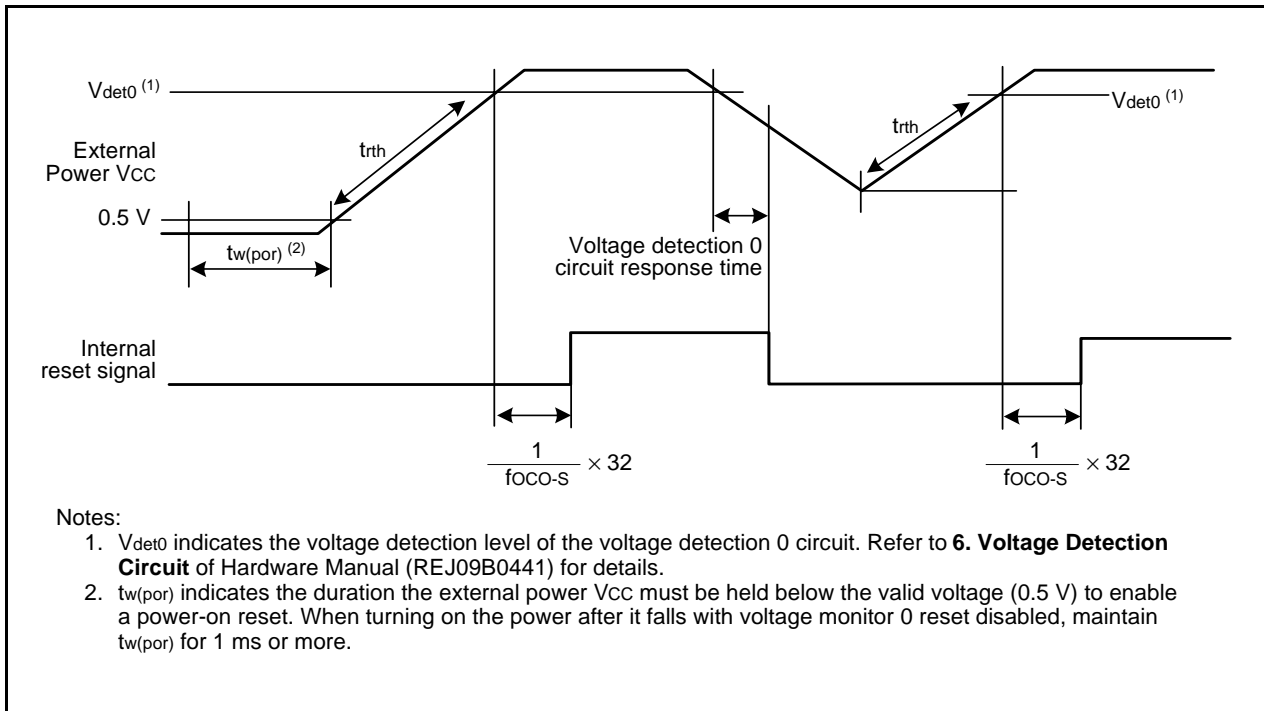
1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V<sub>det2</sub>.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

**Table 5.12 Power-on Reset Circuit Characteristics <sup>(2)</sup>**  
**(T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol           | Parameter   | Condition | Standard |      |       | Unit    |
|------------------|---|-----------|----------|------|-------|---------|
|                  |   |           | Min.     | Typ. | Max.  |         |
| t <sub>rth</sub> | External power V <sub>CC</sub> rise gradient <sup>(1)</sup> |           | 0        | –    | 50000 | mV/msec |

Notes:

1. This condition (external power V<sub>CC</sub> rise gradient) does not apply if V<sub>CC</sub> ≥ 1.0 V.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:

1. V<sub>det0</sub> indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual (REJ09B0441) for details.
2. t<sub>w(por)</sub> indicates the duration the external power V<sub>CC</sub> must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain t<sub>w(por)</sub> for 1 ms or more.

**Figure 5.3 Power-on Reset Circuit Characteristics**

**Table 5.13 High-speed On-Chip Oscillator Circuit Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol  | Parameter   | Condition   | Standard |        |      | Unit |
|---|---|---|----------|--------|------|------|
|   |   |   | Min.     | Typ.   | Max. |      |
| -   | High-speed on-chip oscillator frequency after reset   | V <sub>CC</sub> = 5.0 V, T <sub>opr</sub> = 25°C                    | TBD      | 40     | TBD  | MHz  |
|   | High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (2) |   | TBD      | 36.864 | TBD  | MHz  |
|   | High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register     |   | TBD      | 32     | TBD  | MHz  |
|   | High-speed on-chip oscillator frequency temperature • supply voltage dependence (1)   | V <sub>CC</sub> = 2.7 V to 5.5 V<br>-20°C ≤ T <sub>opr</sub> ≤ 85°C | TBD      | -      | TBD  | %    |
|   |   | V <sub>CC</sub> = 2.7 V to 5.5 V<br>-40°C ≤ T <sub>opr</sub> ≤ 85°C | TBD      | -      | TBD  | %    |
|   |   | V <sub>CC</sub> = 2.2 V to 5.5 V<br>-20°C ≤ T <sub>opr</sub> ≤ 85°C | TBD      | -      | TBD  | %    |
|   |   | V <sub>CC</sub> = 2.2 V to 5.5 V<br>-40°C ≤ T <sub>opr</sub> ≤ 85°C | TBD      | -      | TBD  | %    |
| V <sub>CC</sub> = 1.8 V to 5.5 V<br>-20°C ≤ T <sub>opr</sub> ≤ 85°C |   | TBD   | -        | TBD    | %    |      |
| V <sub>CC</sub> = 1.8 V to 5.5 V<br>-40°C ≤ T <sub>opr</sub> ≤ 85°C | TBD   | -   | TBD      | %      |      |      |
| -   | Oscillation stability time  | V <sub>CC</sub> = 5.0 V, T <sub>opr</sub> = 25°C                    | -        | 100    | 450  | μs   |
| -   | Self power consumption at oscillation   | V <sub>CC</sub> = 5.0 V, T <sub>opr</sub> = 25°C                    | -        | 400    | -    | μA   |

Notes:

1. This indicates the precision error for the oscillation frequency of the high-speed on-chip oscillator.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

**Table 5.14 Low-speed On-Chip Oscillator Circuit Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol   | Parameter   | Condition  | Standard |      |       | Unit |
|----------|---|--|----------|------|-------|------|
|          |   |  | Min.     | Typ. | Max.  |      |
| fOCO-S   | Low-speed on-chip oscillator frequency                        |  | 112.5    | 125  | 137.5 | kHz  |
| -        | Oscillation stability time                                    | V <sub>CC</sub> = 5.0 V, T <sub>opr</sub> = 25°C | -        | 30   | 100   | μs   |
| -        | Self power consumption at oscillation                         | V <sub>CC</sub> = 5.0 V, T <sub>opr</sub> = 25°C | -        | 3    | -     | μA   |
| fOCO-WDT | Low-speed on-chip oscillator frequency for the watchdog timer |  | 60       | 125  | 250   | kHz  |
| -        | Oscillation stability time                                    | V <sub>CC</sub> = 5.0 V, T <sub>opr</sub> = 25°C | -        | 30   | 100   | μs   |
| -        | Self power consumption at oscillation                         | V <sub>CC</sub> = 5.0 V, T <sub>opr</sub> = 25°C | -        | 2    | -     | μA   |

**Table 5.15 Power Supply Circuit Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = 25°C, unless otherwise specified.)**

| Symbol               | Parameter  | Condition | Standard |      |      | Unit |
|----------------------|--|-----------|----------|------|------|------|
|                      |  |           | Min.     | Typ. | Max. |      |
| t <sub>d</sub> (P-R) | Time for internal power supply stabilization during power-on (1) |           | -        | -    | 2000 | μs   |

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

**Table 5.16 LCD Drive Control Circuit Characteristics**  
**(V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = –20 to 85°C (N version) / –40 to 85°C**  
**(D version), unless otherwise specified.)**

| Symbol | Parameter  | Condition  | Standard                   |                    |                            | Unit |
|--------|--|--|----------------------------|--------------------|----------------------------|------|
|        |  |  | Min.                       | Typ.               | Max.                       |      |
| VLCD   | LCD power supply voltage                                 | VLCD = VL4   | 2.2                        | –                  | 5.5                        | V    |
| VL3    | VL3 voltage  |  | VL2                        | –                  | VL4                        | V    |
| VL2    | VL2 voltage  | R8C/L35A, R8C/L35B   | VL1                        | –                  | VL4                        | V    |
|        |  | R8C/L36A, R8C/L36B,<br>R8C/L38A, R8C/L38B,<br>R8C/L3AA, R8C/L3AB | VL1                        | –                  | VL3                        | V    |
| VL1    | VL1 voltage  |  | 1                          | –                  | VL2                        | V    |
| –      | VL1 internally-generated voltage accuracy <sup>(1)</sup> |  | Setting<br>voltage<br>–0.4 | Setting<br>voltage | Setting<br>voltage<br>+0.4 | V    |
| f(FR)  | Frame frequency  |  | 50                         | –                  | 180                        | Hz   |
| ILCD   | LCD drive control circuit current                        |  | –                          | (Note 2)           | –                          | μA   |

Notes:

1. The voltage is selected with bits LVLS0 to LVLS3 in the LCR1 register.
2. Refer to Table 5.19 DC Characteristics (2), Table 5.21 DC Characteristics (4), and Table 5.23 DC Characteristics (6).

**Table 5.17 Power-Off Mode Characteristics**  
**(V<sub>CC</sub> = 2.2 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = –20 to 85°C (N version) / –40 to 85°C**  
**(D version), unless otherwise specified.)**

| Symbol | Parameter                               | Condition | Standard |      |      | Unit |
|--------|---|-----------|----------|------|------|------|
|        |   |           | Min.     | Typ. | Max. |      |
| –      | Power-off mode operating supply voltage |           | 2.2      | –    | 5.5  | V    |



**Table 5.19 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V]  
 (Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)**

| Symbol         | Parameter                |                                    | Condition           |        |                    |           |                            |  |  | Standard  |          |      | Unit |    |
|----------------|--------------------------|------------------------------------|---------------------|--------|--------------------|-----------|----------------------------|--|--|---|----------|------|------|----|
|                |                          |                                    | Oscillation Circuit |        | On-Chip Oscillator |           | CPU Clock                  | Low-Power-Consumption Setting  | Other  | Min.  | Typ. (3) | Max. |      |    |
|                |                          |                                    | XIN (2)             | XCIN   | High-Speed         | Low-Speed |                            |  |  |   |          |      |      |    |
| Icc            | Power supply current (1) | High-speed clock mode              | 20 MHz              | Off    | Off                | 125 kHz   | No division                | –  |  | –   | 7.0      | 15   | mA   |    |
|                |                          |                                    | 16 MHz              | Off    | Off                | 125 kHz   | No division                | –  |  | –   | 5.6      | 12.5 | mA   |    |
|                |                          |                                    | 10 MHz              | Off    | Off                | 125 kHz   | No division                | –  |  | –   | 3.6      | –    | mA   |    |
|                |                          |                                    | 20 MHz              | Off    | Off                | 125 kHz   | Divide-by-8                | –  |  | –   | 3.0      | –    | mA   |    |
|                |                          |                                    | 16 MHz              | Off    | Off                | 125 kHz   | Divide-by-8                | –  |  | –   | 2.2      | –    | mA   |    |
|                |                          |                                    | 10 MHz              | Off    | Off                | 125 kHz   | Divide-by-8                | –  |  | –   | 1.5      | –    | mA   |    |
|                |                          | High-speed on-chip oscillator mode | Off                 | Off    | 20 MHz             | 125 kHz   | No division                | –  |  | –   | 7.0      | 15   | mA   |    |
|                |                          |                                    | Off                 | Off    | 20 MHz             | 125 kHz   | Divide-by-8                | –  |  | –   | 3.0      | –    | mA   |    |
|                |                          |                                    | Off                 | Off    | 4 MHz              | 125 kHz   | Divide-by-16               | MSTIIC = 1<br>MSTTRD = 1<br>MSTTRC = 1<br>MSTTRG = 1                     |  | –   | 1        | –    | mA   |    |
|                |                          | Low-speed on-chip oscillator mode  | Off                 | Off    | Off                | 125 kHz   | Divide-by-8                | FMR27 = 1<br>VCA20 = 0   |  | –   | 90       | 400  | μA   |    |
|                |                          |                                    | Off                 | 32 kHz | Off                | Off       | No division                | FMR27 = 1<br>VCA20 = 0   |  | –   | 100      | 400  | μA   |    |
|                |                          | Low-speed clock mode               | Off                 | 32 kHz | Off                | Off       | No division                | FMSTP = 1<br>VCA20 = 0   | Flash memory off<br>Program operation on RAM   | –   | 55       | –    | μA   |    |
|                |                          |                                    | Off                 | 32 kHz | Off                | Off       | No division                | FMSTP = 1<br>VCA20 = 0   | Flash memory off<br>Program operation on RAM   | –   | 55       | –    | μA   |    |
|                |                          | Wait mode                          | Off                 | Off    | Off                | 125 kHz   | –                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1                         | While a WAIT instruction is executed<br>Peripheral clock operation   | –   | 15       | 100  | μA   |    |
|                |                          |                                    | Off                 | Off    | Off                | 125 kHz   | –                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off   | –   | 4        | 90   | μA   |    |
|                |                          |                                    | Off                 | 32 kHz | Off                | Off       | –                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 0 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RE operation in real-time clock mode | LCD drive control circuit (4)<br>When external division resistors are used    | –        | 7    | –    | μA |
|                |                          |                                    | Off                 | 32 kHz | Off                | Off       | –                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RE operation in real-time clock mode | LCD drive control circuit (5)<br>When the internal voltage multiplier is used | –        | 12   | –    | μA |
|                |                          |                                    | Off                 | 32 kHz | Off                | Off       | –                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RE operation in real-time clock mode |   | –        | 3.5  | –    | μA |
|                |                          | Stop mode                          | Off                 | Off    | Off                | Off       | –                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | Topr = 25°C<br>Peripheral clock off  | –   | 2.0      | 5.0  | μA   |    |
|                |                          |                                    | Off                 | Off    | Off                | Off       | –                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | Topr = 85°C<br>Peripheral clock off  | –   | 15       | –    | μA   |    |
| Power-off mode | Off                      | Off                                | Off                 | Off    | –                  | –         | Power-off 0<br>Topr = 25°C | –  | 0.02   | 0.2   | μA       |      |      |    |
|                | Off                      | Off                                | Off                 | Off    | –                  | –         | Power-off 0<br>Topr = 85°C | –  | 0.4  | –   | μA       |      |      |    |
|                | Off                      | 32 kHz                             | Off                 | Off    | –                  | –         | Power-off 1<br>Topr = 25°C | –  | 1.3  | 2.6   | μA       |      |      |    |
|                | Off                      | 32 kHz                             | Off                 | Off    | –                  | –         | Power-off 1<br>Topr = 85°C | –  | 1.5  | –   | μA       |      |      |    |

Notes:

- Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.
- XIN is set to square wave input.
- Vcc = 5.0 V
- VLCD = Vcc, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
- The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.





**Table 5.21 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V]  
 (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

| Symbol | Parameter                |                                    | Condition           |        |                    |           |                            |  |  | Standard  |          |      | Unit |    |
|--------|--------------------------|------------------------------------|---------------------|--------|--------------------|-----------|----------------------------|--|--|---|----------|------|------|----|
|        |                          |                                    | Oscillation Circuit |        | On-Chip Oscillator |           | CPU Clock                  | Low-Power-Consumption Setting  | Other  | Min.  | Typ. (3) | Max. |      |    |
|        |                          |                                    | XIN (2)             | XCIN   | High-Speed         | Low-Speed |                            |  |  |   |          |      |      |    |
| Icc    | Power supply current (1) | High-speed clock mode              | 20 MHz              | Off    | Off                | 125 kHz   | No division                | -  |  | -   | 7.0      | 14.5 | mA   |    |
|        |                          |                                    | 10 MHz              | Off    | Off                | 125 kHz   | No division                | -  |  | -   | 3.6      | 10   | mA   |    |
|        |                          |                                    | 20 MHz              | Off    | Off                | 125 kHz   | Divide-by-8                | -  |  | -   | 3.0      | -    | mA   |    |
|        |                          |                                    | 10 MHz              | Off    | Off                | 125 kHz   | Divide-by-8                | -  |  | -   | 1.5      | -    | mA   |    |
|        |                          | High-speed on-chip oscillator mode | Off                 | Off    | 20 MHz             | 125 kHz   | No division                | -  |  | -   | 7.0      | 14.5 | mA   |    |
|        |                          |                                    | Off                 | Off    | 20 MHz             | 125 kHz   | Divide-by-8                | -  |  | -   | 3.0      | -    | mA   |    |
|        |                          |                                    | Off                 | Off    | 10 MHz             | 125 kHz   | No division                | -  |  | -   | 4.0      | -    | mA   |    |
|        |                          |                                    | Off                 | Off    | 10 MHz             | 125 kHz   | Divide-by-8                | -  |  | -   | 1.7      | -    | mA   |    |
|        |                          | Low-speed on-chip oscillator mode  | Off                 | Off    | Off                | 125 kHz   | Divide-by-8                | FMR27 = 1<br>VCA20 = 0   |  | -   | 85       | 390  | μA   |    |
|        |                          |                                    | Off                 | 32 kHz | Off                | Off       | No division                | FMR27 = 1<br>VCA20 = 0   |  | -   | 90       | 400  | μA   |    |
|        |                          | Low-speed clock mode               | Off                 | 32 kHz | Off                | Off       | No division                | FMSTP = 1<br>VCA20 = 0   | Flash memory off<br>Program operation on RAM   | -   | 50       | -    | μA   |    |
|        |                          |                                    | Off                 | Off    | Off                | 125 kHz   | -                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1                         | While a WAIT instruction is executed<br>Peripheral clock operation   | -   | 15       | 90   | μA   |    |
|        |                          | Wait mode                          | Off                 | Off    | Off                | 125 kHz   | -                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off   | -   | 5        | 80   | μA   |    |
|        |                          |                                    | Off                 | 32 kHz | Off                | Off       | -                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 0 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RE operation in real-time clock mode | LCD drive control circuit (4)<br>When external division resistors are used    | -        | 5    | -    | μA |
|        |                          |                                    | Off                 | 32 kHz | Off                | Off       | -                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RE operation in real-time clock mode | LCD drive control circuit (5)<br>When the internal voltage multiplier is used | -        | 11   | -    | μA |
|        |                          |                                    | Off                 | 32 kHz | Off                | Off       | -                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RE operation in real-time clock mode | -   | 3.5      | -    | μA   |    |
|        |                          | Stop mode                          | Off                 | Off    | Off                | Off       | -                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | Topr = 25°C<br>Peripheral clock off  | -   | 2        | 5.0  | μA   |    |
|        |                          |                                    | Off                 | Off    | Off                | Off       | -                          | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>CM10 = 1                          | Topr = 85°C<br>Peripheral clock off  | -   | 13.0     | -    | μA   |    |
|        |                          | Power-off mode                     | Off                 | Off    | Off                | Off       | -                          | -  | Power-off 0<br>Topr = 25°C   | -   | 0.02     | 0.2  | μA   |    |
|        |                          |                                    | Off                 | Off    | Off                | Off       | -                          | -  | Power-off 0<br>Topr = 85°C   | -   | 0.3      | -    | μA   |    |
| Off    | 32 kHz                   |                                    | Off                 | Off    | -                  | -         | Power-off 1<br>Topr = 25°C | -  | 1.0  | 2.0   | μA       |      |      |    |
| Off    | 32 kHz                   |                                    | Off                 | Off    | -                  | -         | Power-off 1<br>Topr = 85°C | -  | 1.2  | -   | μA       |      |      |    |

Notes:

- Vcc = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are Vss.
- XIN is set to square wave input.
- Vcc = 3.0 V.
- VLCD = Vcc, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
- The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.



**Table 5.23 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]  
 (Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)**

| Symbol                     | Parameter                |                                    | Condition           |        |                    |           |              |  |  | Standard   |          |      | Unit |    |    |
|----------------------------|--------------------------|------------------------------------|---------------------|--------|--------------------|-----------|--------------|--|--|--|----------|------|------|----|----|
|                            |                          |                                    | Oscillation Circuit |        | On-Chip Oscillator |           | CPU Clock    | Low-Power-Consumption Setting  | Other  | Min.   | Typ. (3) | Max. |      |    |    |
|                            |                          |                                    | XIN (2)             | XCIN   | High-Speed         | Low-Speed |              |  |  |  |          |      |      |    |    |
| Icc                        | Power supply current (1) | High-speed clock mode              | 5 MHz               | Off    | Off                | 125 kHz   | No division  | –  | –  | 2.2  | –        | mA   |      |    |    |
|                            |                          |                                    | 5 MHz               | Off    | Off                | 125 kHz   | Divide-by-8  | –  | –  | 0.8  | –        | mA   |      |    |    |
|                            |                          | High-speed on-chip oscillator mode | Off                 | Off    | 5 MHz              | 125 kHz   | No division  | –  | –  | –  | 2.5      | 10   | mA   |    |    |
|                            |                          |                                    | Off                 | Off    | 5 MHz              | 125 kHz   | Divide-by-8  | –  | –  | –  | 1.7      | –    | mA   |    |    |
|                            |                          |                                    | Off                 | Off    | 4 MHz              | 125 kHz   | Divide-by-16 | MSTIIC = 1<br>MSTTRD = 1<br>MSTTRC = 1<br>MSTTRG = 1                     | –  | –  | 1        | –    | mA   |    |    |
|                            |                          | Low-speed on-chip oscillator mode  | Off                 | Off    | Off                | 125 kHz   | Divide-by-8  | FMR27 = 1<br>VCA20 = 0   | –  | –  | 90       | 300  | μA   |    |    |
|                            |                          | Low-speed clock mode               | Off                 | 32 kHz | Off                | Off       | No division  | FMR27 = 1<br>VCA20 = 0   | –  | –  | 90       | 400  | μA   |    |    |
|                            |                          |                                    | Off                 | 32 kHz | Off                | Off       | No division  | FMSTP = 1<br>VCA20 = 0   | Flash memory off<br>Program operation on RAM   | –  | –        | 45   | –    | μA |    |
|                            |                          | Wait mode                          | Off                 | Off    | Off                | 125 kHz   | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1                         | While a WAIT instruction is executed<br>Peripheral clock operation   | –  | –        | 15   | 90   | μA |    |
|                            |                          |                                    |                     |        |                    |           |              |  | While a WAIT instruction is executed<br>Peripheral clock off   | –  | –        | 4    | 80   | μA |    |
|                            |                          |                                    | Off                 | 32 kHz | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | While a WAIT instruction is executed<br>Peripheral clock off<br>Timer RE operation in real-time clock mode | LCD drive control circuit (4)<br>When external division resistors are used | –        | –    | 4    | –  | μA |
|                            |                          |                                    |                     |        |                    |           |              |  | LCD drive control circuit (5)<br>When the internal voltage multiplier is used                              | –  | –        | 11   | –    | μA |    |
|                            |                          | Stop mode                          | Off                 | Off    | Off                | Off       | –            | VCA27 = 0<br>VCA26 = 0<br>VCA25 = 0<br>VCA20 = 1<br>CM02 = 1<br>CM01 = 1 | Topr = 25°C<br>Peripheral clock off  | –  | –        | 2.0  | 5.0  | μA |    |
|                            |                          |                                    |                     |        |                    |           |              |  | Topr = 85°C<br>Peripheral clock off  | –  | –        | 13   | –    | μA |    |
|                            |                          | Power-off mode                     | Off                 | Off    | Off                | Off       | –            | –  | Power-off 0<br>Topr = 25°C   | –  | –        | 0.02 | 0.2  | μA |    |
|                            |                          |                                    |                     |        |                    |           |              |  | Power-off 0<br>Topr = 85°C   | –  | –        | 0.3  | –    | μA |    |
| Power-off 1<br>Topr = 25°C | –                        |                                    |                     |        |                    |           |              |  | –  | 0.8  | 1.6      | μA   |      |    |    |
| Power-off 1<br>Topr = 85°C | –                        |                                    |                     |        |                    |           |              |  | –  | 1.1  | –        | μA   |      |    |    |

Notes:

- Vcc = 1.8 V to 2.7 V, single chip mode, output pins are open, and other pins are Vss.
- XIN is set to square wave input.
- Vcc = 2.2 V
- VLCD = Vcc, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
- The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

## 5.5 AC Characteristics

**Table 5.24 Timing Requirements of Clock Synchronous Serial I/O with Chip Select  
 (V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C  
 (D version), unless otherwise specified.)**

| Symbol | Parameter                          |        | Conditions                      | Standard   |      |               | Unit     |
|--------|------------------------------------|--------|---------------------------------|------------|------|---------------|----------|
|        |                                    |        |                                 | Min.       | Typ. | Max.          |          |
| tsucyc | SSCK clock cycle time              |        |                                 | 4          | -    | -             | tcyc (1) |
| tHI    | SSCK clock "H" width               |        |                                 | 0.4        | -    | 0.6           | tsucyc   |
| tLO    | SSCK clock "L" width               |        |                                 | 0.4        | -    | 0.6           | tsucyc   |
| tRISE  | SSCK clock rising time             | Master |                                 | -          | -    | 1             | tcyc (1) |
|        |                                    | Slave  |                                 | -          | -    | 1             | μs       |
| tFALL  | SSCK clock falling time            | Master |                                 | -          | -    | 1             | tcyc (1) |
|        |                                    | Slave  |                                 | -          | -    | 1             | μs       |
| tsu    | SSO, SSI data input setup time     |        |                                 | 100        | -    | -             | ns       |
| tH     | SSO, SSI data input hold time      |        |                                 | 1          | -    | -             | tcyc (1) |
| tLEAD  | $\overline{\text{SCS}}$ setup time | Slave  |                                 | 1tcyc + 50 | -    | -             | ns       |
| tLAG   | $\overline{\text{SCS}}$ hold time  | Slave  |                                 | 1tcyc + 50 | -    | -             | ns       |
| tOD    | SSO, SSI data output delay time    |        |                                 | -          | -    | 1             | tcyc (1) |
| tSA    | SSI slave access time              |        | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V | -          | -    | 1.5tcyc + 100 | ns       |
|        |                                    |        | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | -          | -    | 1.5tcyc + 200 | ns       |
| tOR    | SSI slave out open time            |        | 2.7 V ≤ V <sub>CC</sub> ≤ 5.5 V | -          | -    | 1.5tcyc + 100 | ns       |
|        |                                    |        | 1.8 V ≤ V <sub>CC</sub> < 2.7 V | -          | -    | 1.5tcyc + 200 | ns       |

Note:

- 1tcyc = 1/f1(s)

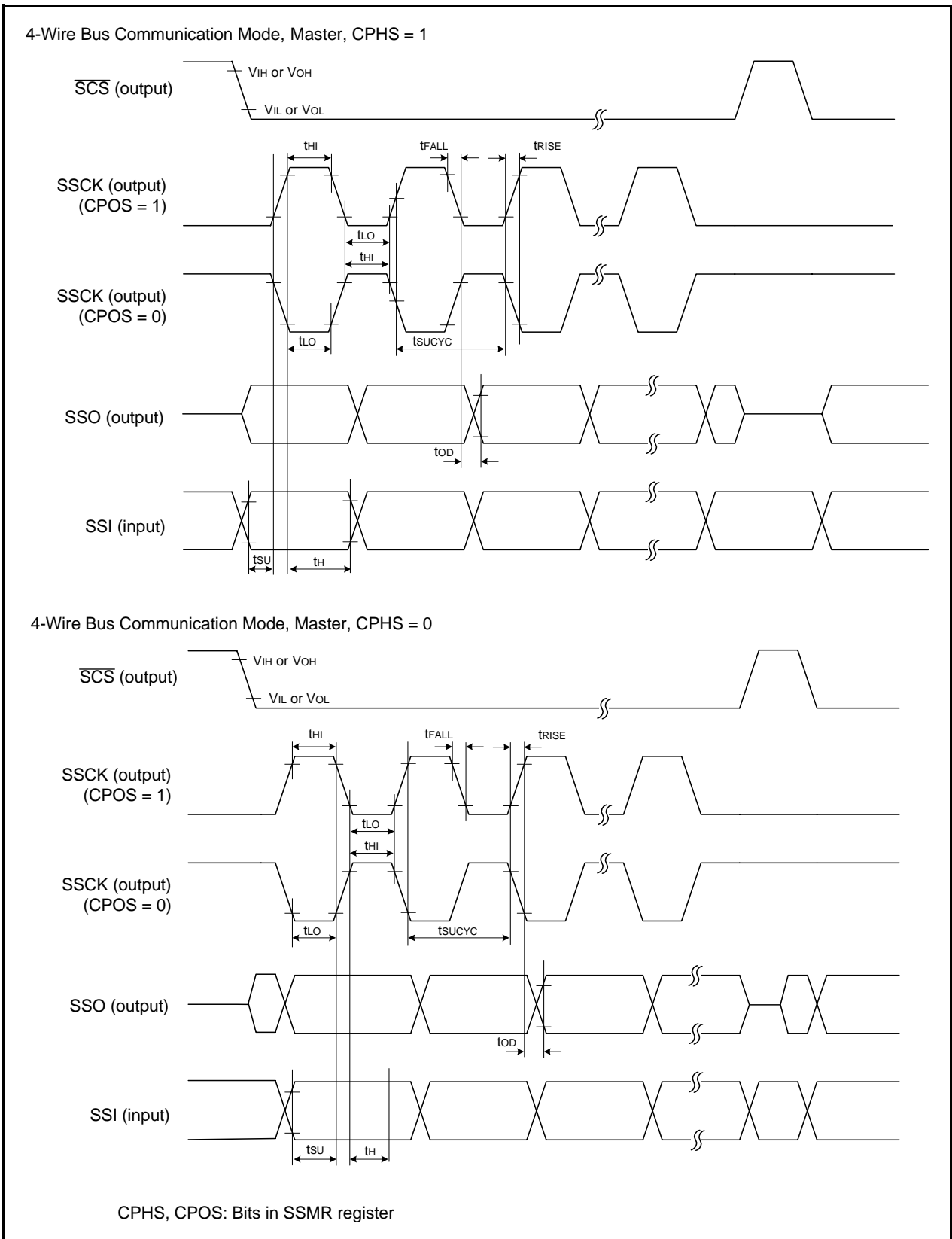


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

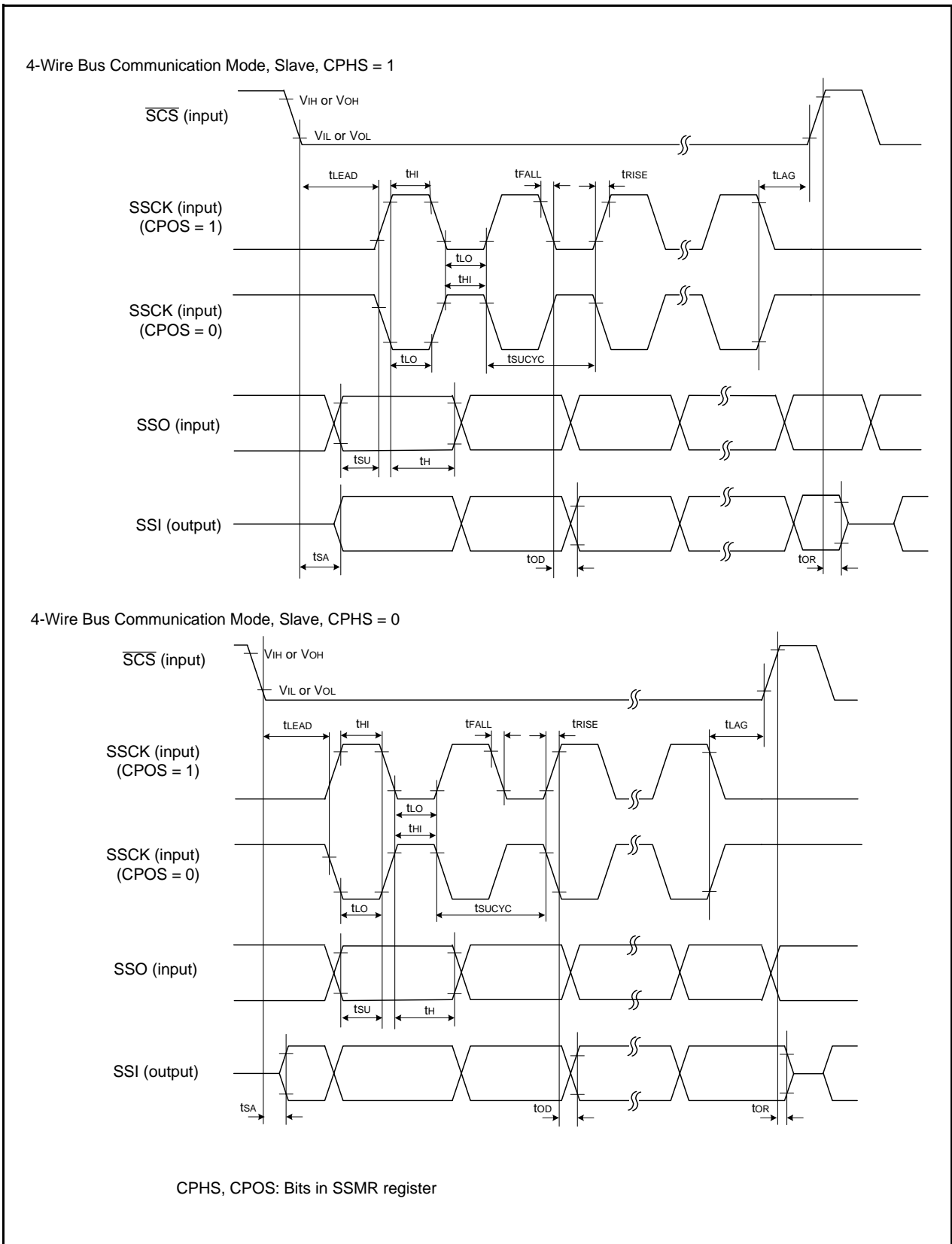
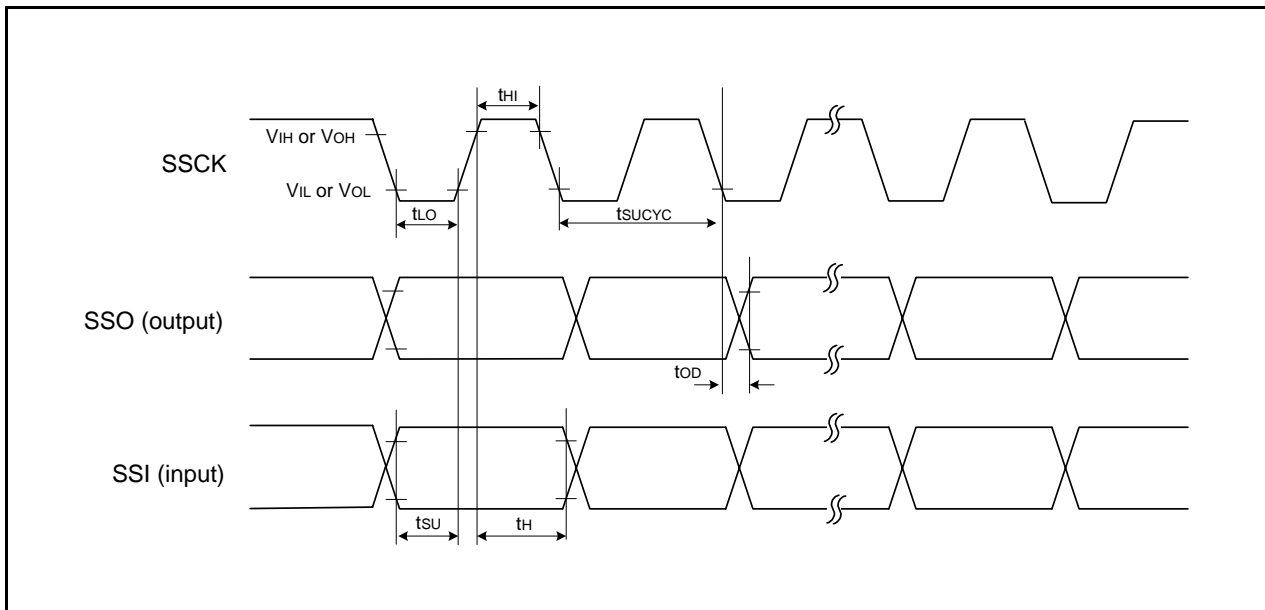


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)



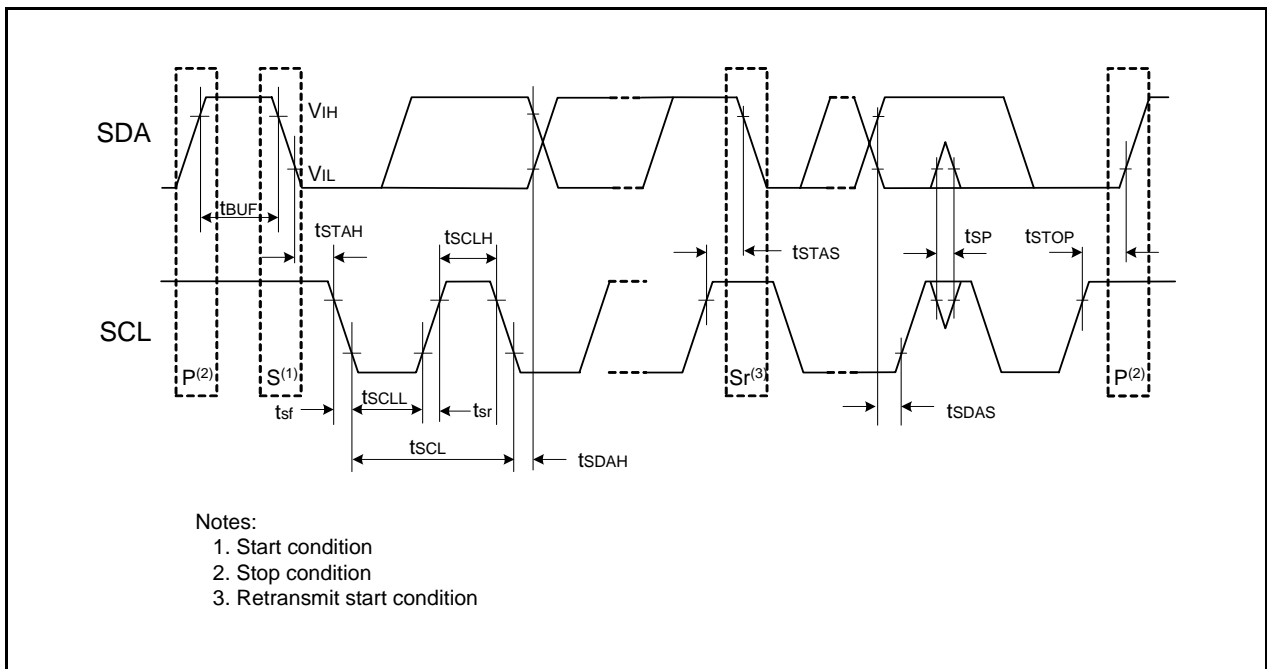
**Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)**

**Table 5.25 Timing Requirements of I<sup>2</sup>C bus Interface (1)**  
 (V<sub>CC</sub> = 1.8 to 5.5 V, V<sub>SS</sub> = 0 V, and T<sub>opr</sub> = -20 to 85°C (N version) / -40 to 85°C (D version),  
 unless otherwise specified.)

| Symbol            | Parameter                                   | Condition | Standard                     |      |                       | Unit |
|-------------------|---|-----------|------------------------------|------|-----------------------|------|
|                   |   |           | Min.                         | Typ. | Max.                  |      |
| t <sub>SCL</sub>  | SCL input cycle time                        |           | 12t <sub>CYC</sub> + 600 (1) | –    | –                     | ns   |
| t <sub>SCLH</sub> | SCL input “H” width                         |           | 3t <sub>CYC</sub> + 300 (1)  | –    | –                     | ns   |
| t <sub>SCLL</sub> | SCL input “L” width                         |           | 5t <sub>CYC</sub> + 500 (1)  | –    | –                     | ns   |
| t <sub>sf</sub>   | SCL, SDA input fall time                    |           | –                            | –    | 300                   | ns   |
| t <sub>SP</sub>   | SCL, SDA input spike pulse rejection time   |           | –                            | –    | 1t <sub>CYC</sub> (1) | ns   |
| t <sub>BUF</sub>  | SDA input bus-free time                     |           | 5t <sub>CYC</sub> (1)        | –    | –                     | ns   |
| t <sub>STAH</sub> | Start condition input hold time             |           | 3t <sub>CYC</sub> (1)        | –    | –                     | ns   |
| t <sub>STAS</sub> | Retransmit start condition input setup time |           | 3t <sub>CYC</sub> (1)        | –    | –                     | ns   |
| t <sub>STOP</sub> | Stop condition input setup time             |           | 3t <sub>CYC</sub> (1)        | –    | –                     | ns   |
| t <sub>SDAS</sub> | Data input setup time                       |           | 1t <sub>CYC</sub> + 40 (1)   | –    | –                     | ns   |
| t <sub>SDAH</sub> | Data input hold time                        |           | 10                           | –    | –                     | ns   |

Note:

- 1t<sub>CYC</sub> = 1/f<sub>1</sub>(s)

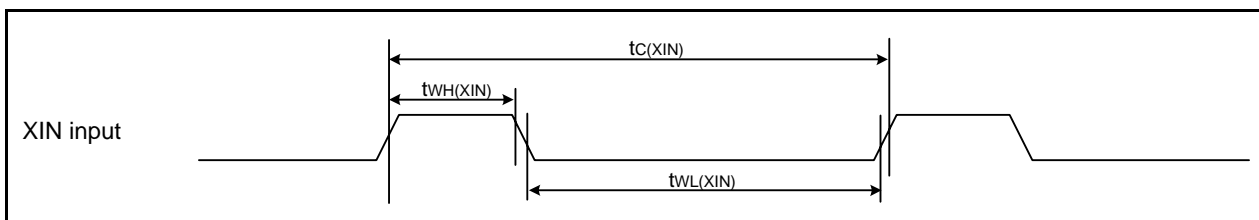


**Figure 5.7 I/O Timing of I<sup>2</sup>C bus Interface**



**Table 5.26 Timing Requirements of XIN and XCIN**  
 (Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = -20 to 85°C (N version) / -40 to 85°C (D version),  
 unless otherwise specified.)

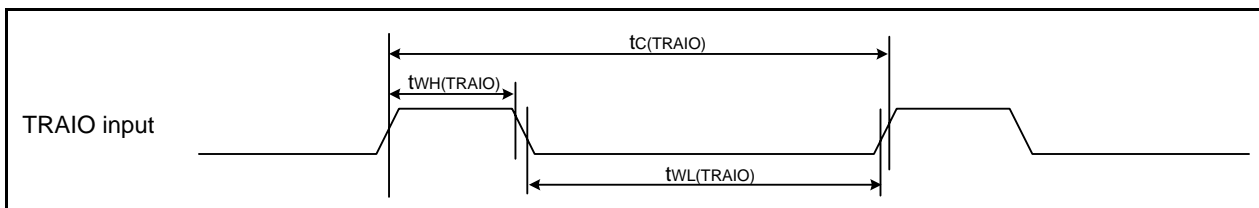
| Symbol                 | Parameter             | Standard                |      |                       |      |                       |      | Unit |
|------------------------|-----------------------|-------------------------|------|-----------------------|------|-----------------------|------|------|
|                        |                       | Vcc = 2.2V, Topr = 25°C |      | Vcc = 3V, Topr = 25°C |      | Vcc = 5V, Topr = 25°C |      |      |
|                        |                       | Min.                    | Max. | Min.                  | Max. | Min.                  | Max. |      |
| t <sub>c</sub> (XIN)   | XIN input cycle time  | 200                     | -    | 50                    | -    | 50                    | -    | ns   |
| t <sub>WH</sub> (XIN)  | XIN input "H" width   | 90                      | -    | 24                    | -    | 24                    | -    | ns   |
| t <sub>WL</sub> (XIN)  | XIN input "L" width   | 90                      | -    | 24                    | -    | 24                    | -    | ns   |
| t <sub>c</sub> (XCIN)  | XCIN input cycle time | 14                      | -    | 14                    | -    | 14                    | -    | μs   |
| t <sub>WH</sub> (XCIN) | XCIN input "H" width  | 7                       | -    | 7                     | -    | 7                     | -    | μs   |
| t <sub>WL</sub> (XCIN) | XCIN input "L" width  | 7                       | -    | 7                     | -    | 7                     | -    | μs   |



**Figure 5.8 Input Timing of XIN and XCIN**

**Table 5.27 Timing Requirements of TRAIO**  
 (Vcc = 1.8 to 5.5 V, Vss = 0 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version),  
 unless otherwise specified.)

| Symbol                  | Parameter              | Standard                |      |                       |      |                       |      | Unit |
|-------------------------|------------------------|-------------------------|------|-----------------------|------|-----------------------|------|------|
|                         |                        | Vcc = 2.2V, Topr = 25°C |      | Vcc = 3V, Topr = 25°C |      | Vcc = 5V, Topr = 25°C |      |      |
|                         |                        | Min.                    | Max. | Min.                  | Max. | Min.                  | Max. |      |
| t <sub>c</sub> (TRAIO)  | TRAIO input cycle time | 500                     | -    | 300                   | -    | 100                   | -    | ns   |
| t <sub>WH</sub> (TRAIO) | TRAIO input "H" width  | 200                     | -    | 120                   | -    | 40                    | -    | ns   |
| t <sub>WL</sub> (TRAIO) | TRAIO input "L" width  | 200                     | -    | 120                   | -    | 40                    | -    | ns   |

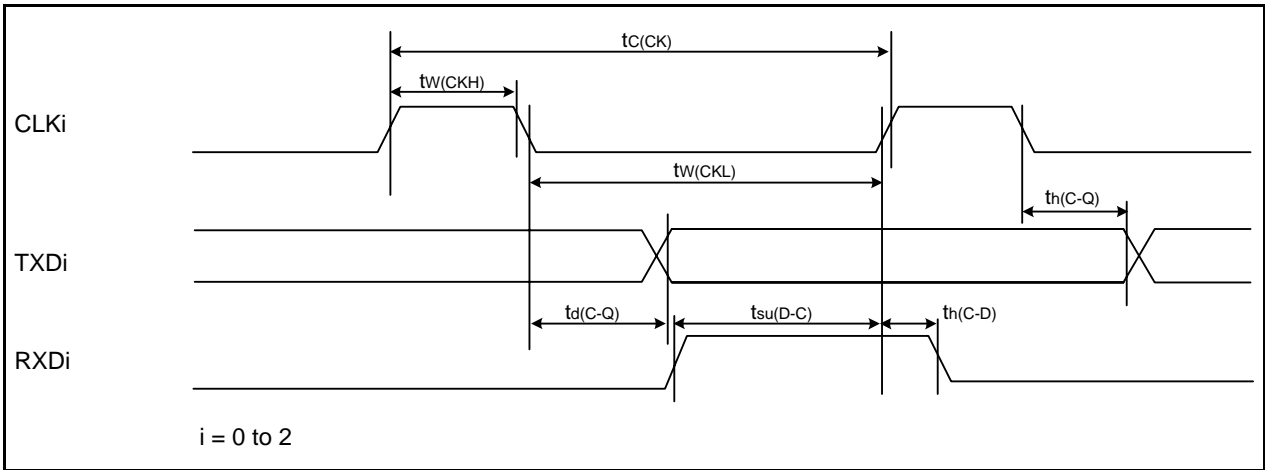


**Figure 5.9 Input Timing of TRAIO**

**Table 5.28 Timing Requirements of Serial Interface**  
 (Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = -20 to 85°C (N version) / -40 to 85°C (D version),  
 unless otherwise specified.)

| Symbol   | Parameter              | Standard                |      |                       |      |                       |      | Unit |
|----------|------------------------|-------------------------|------|-----------------------|------|-----------------------|------|------|
|          |                        | Vcc = 2.2V, Topr = 25°C |      | Vcc = 3V, Topr = 25°C |      | Vcc = 5V, Topr = 25°C |      |      |
|          |                        | Min.                    | Max. | Min.                  | Max. | Min.                  | Max. |      |
| tc(CK)   | CLKi input cycle time  | 800                     | -    | 300                   | -    | 200                   | -    | ns   |
| tw(CKH)  | CLKi input "H" width   | 400                     | -    | 150                   | -    | 100                   | -    | ns   |
| tw(CKL)  | CLKi input "L" width   | 400                     | -    | 150                   | -    | 100                   | -    | ns   |
| td(C-Q)  | TXDi output delay time | -                       | 200  | -                     | 80   | -                     | 50   | ns   |
| th(C-Q)  | TXDi hold time         | 0                       | -    | 0                     | -    | 0                     | -    | ns   |
| tsu(D-C) | RXDi input setup time  | 150                     | -    | 70                    | -    | 50                    | -    | ns   |
| th(C-D)  | RXDi input hold time   | 90                      | -    | 90                    | -    | 90                    | -    | ns   |

i = 0 to 2



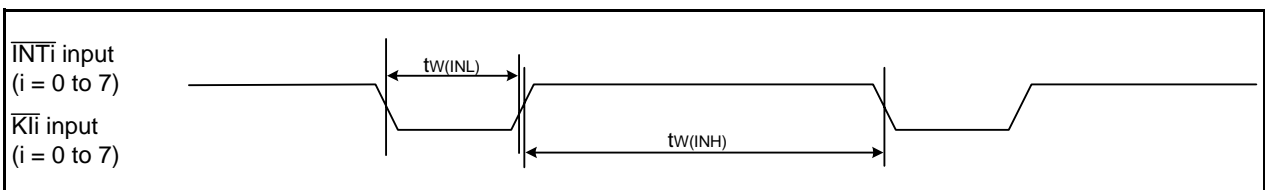
**Figure 5.10 Input and Output Timing of Serial Interface**

**Table 5.29 Timing Requirements of External Interrupt  $\overline{\text{INT}}_i$  (i = 0 to 7) and Key Input Interrupt  $\overline{\text{K}}_i$  (i = 0 to 7)**  
 (Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = -20 to 85°C (N version) / -40 to 85°C (D version),  
 unless otherwise specified.)

| Symbol  | Parameter  | Standard                |      |                       |      |                       |      | Unit |
|---------|--|-------------------------|------|-----------------------|------|-----------------------|------|------|
|         |  | Vcc = 2.2V, Topr = 25°C |      | Vcc = 3V, Topr = 25°C |      | Vcc = 5V, Topr = 25°C |      |      |
|         |  | Min.                    | Max. | Min.                  | Max. | Min.                  | Max. |      |
| tw(INH) | $\overline{\text{INT}}_i$ input "H" width, $\overline{\text{K}}_i$ input "H" width | 1000 (1)                | -    | 380 (1)               | -    | 250 (1)               | -    | ns   |
| tw(INL) | $\overline{\text{INT}}_i$ input "L" width, $\overline{\text{K}}_i$ input "L" width | 1000 (2)                | -    | 380 (2)               | -    | 250 (2)               | -    | ns   |

Notes:

- When selecting the digital filter by the  $\overline{\text{INT}}_i$  input filter select bit, use an  $\overline{\text{INT}}_i$  input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the  $\overline{\text{INT}}_i$  input filter select bit, use an  $\overline{\text{INT}}_i$  input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

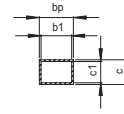
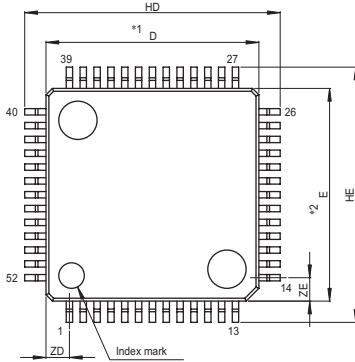


**Figure 5.11 Input Timing of External Interrupt  $\overline{\text{INT}}_i$  and Key Input Interrupt  $\overline{\text{K}}_i$**

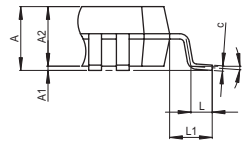
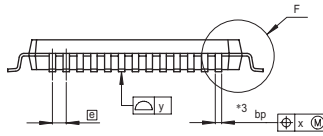
## Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology web site.

|                     |              |               |            |
|---------------------|--------------|---------------|------------|
| JEITA Package Code  | RENESAS Code | Previous Code | MASS[Typ.] |
| P-LQFP52-10x10-0.65 | PLQP0052JA-A | 52P6A-A       | 0.3g       |



Terminal cross section

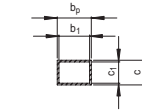
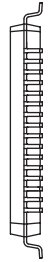
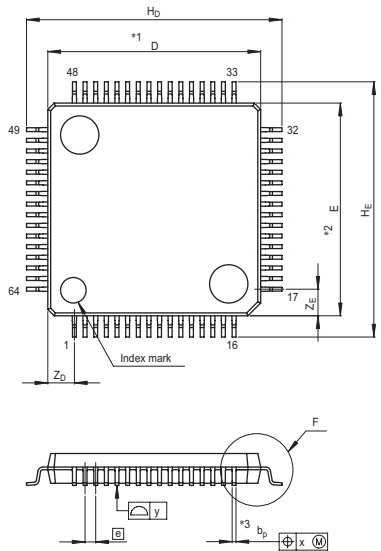


Detail F

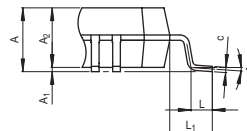
NOTE)  
 1. DIMENSIONS \*\*1\* AND \*\*2\* DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3\* DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters |       |      |
|------------------|--------------------------|-------|------|
|                  | Min                      | Nom   | Max  |
| D                | 9.9                      | 10.0  | 10.1 |
| E                | 9.9                      | 10.0  | 10.1 |
| A <sub>2</sub>   | —                        | 1.4   | —    |
| H <sub>D</sub>   | 11.8                     | 12.0  | 12.2 |
| H <sub>E</sub>   | 11.8                     | 12.0  | 12.2 |
| A                | —                        | —     | 1.7  |
| A <sub>1</sub>   | 0.05                     | 0.1   | 0.15 |
| b <sub>p</sub>   | 0.27                     | 0.32  | 0.37 |
| b <sub>1</sub>   | —                        | 0.30  | —    |
| c                | 0.09                     | 0.145 | 0.20 |
| c <sub>1</sub>   | —                        | 0.125 | —    |
| θ                | 0°                       | —     | 8°   |
| Ⓜ                | —                        | 0.65  | —    |
| x                | —                        | —     | 0.13 |
| y                | —                        | —     | 0.10 |
| Z <sub>D</sub>   | —                        | 1.1   | —    |
| Z <sub>E</sub>   | —                        | 1.1   | —    |
| L                | 0.35                     | 0.5   | 0.65 |
| L <sub>1</sub>   | —                        | 1.0   | —    |

|                     |              |                            |            |
|---------------------|--------------|----------------------------|------------|
| JEITA Package Code  | RENESAS Code | Previous Code              | MASS[Typ.] |
| P-LQFP64-10x10-0.50 | PLQP0064KB-A | 64P6Q-A / FP-64K / FP-64KV | 0.3g       |



Terminal cross section

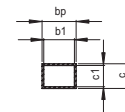
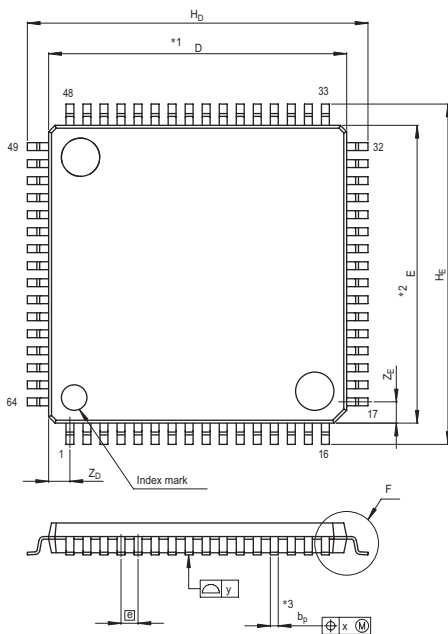


Detail F

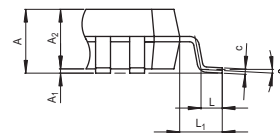
NOTE)  
 1. DIMENSIONS \*\*1\* AND \*\*2\* DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3\* DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters |       |      |
|------------------|--------------------------|-------|------|
|                  | Min                      | Nom   | Max  |
| D                | 9.9                      | 10.0  | 10.1 |
| E                | 9.9                      | 10.0  | 10.1 |
| A <sub>2</sub>   | —                        | 1.4   | —    |
| H <sub>D</sub>   | 11.8                     | 12.0  | 12.2 |
| H <sub>E</sub>   | 11.8                     | 12.0  | 12.2 |
| A                | —                        | —     | 1.7  |
| A <sub>1</sub>   | 0.05                     | 0.1   | 0.15 |
| b <sub>p</sub>   | 0.15                     | 0.20  | 0.25 |
| b <sub>1</sub>   | —                        | 0.18  | —    |
| c                | 0.09                     | 0.145 | 0.20 |
| c <sub>1</sub>   | —                        | 0.125 | —    |
| θ                | 0°                       | —     | 8°   |
| Ⓜ                | —                        | 0.5   | —    |
| x                | —                        | —     | 0.08 |
| y                | —                        | —     | 0.08 |
| Z <sub>D</sub>   | —                        | 1.25  | —    |
| Z <sub>E</sub>   | —                        | 1.25  | —    |
| L                | 0.35                     | 0.5   | 0.65 |
| L <sub>1</sub>   | —                        | 1.0   | —    |

|                     |              |               |            |
|---------------------|--------------|---------------|------------|
| JEITA Package Code  | RENESAS Code | Previous Code | MASS[Typ.] |
| P-LQFP64-14x14-0.80 | PLQP0064GA-A | 64P6U-A       | 0.7g       |



Terminal cross section

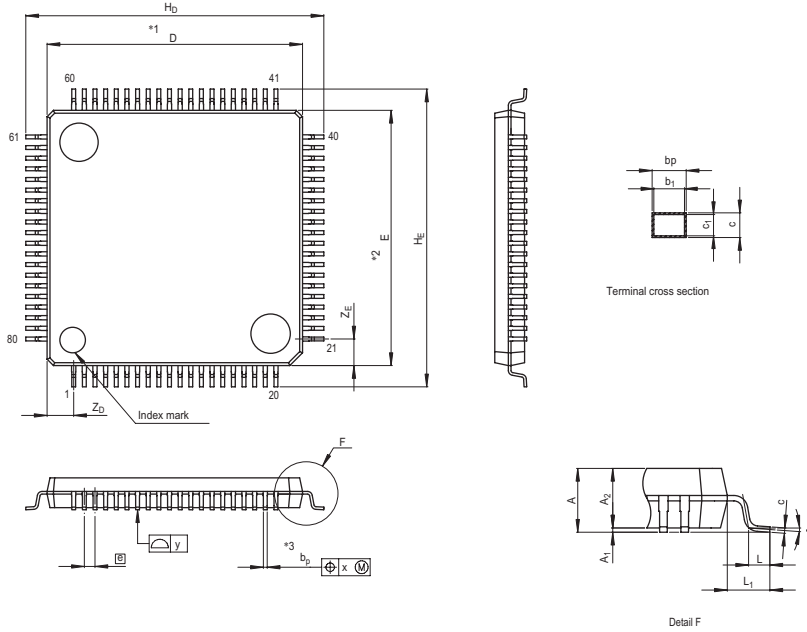


Detail F

NOTE)  
 1. DIMENSIONS \*\*1\* AND \*\*2\* DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3\* DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters |       |      |
|------------------|--------------------------|-------|------|
|                  | Min                      | Nom   | Max  |
| D                | 13.9                     | 14.0  | 14.1 |
| E                | 13.9                     | 14.0  | 14.1 |
| A <sub>2</sub>   | —                        | 1.4   | —    |
| H <sub>D</sub>   | 15.8                     | 16.0  | 16.2 |
| H <sub>E</sub>   | 15.8                     | 16.0  | 16.2 |
| A                | —                        | —     | 1.7  |
| A <sub>1</sub>   | 0                        | 0.1   | 0.2  |
| b <sub>p</sub>   | 0.32                     | 0.37  | 0.42 |
| b <sub>1</sub>   | —                        | 0.35  | —    |
| c                | 0.09                     | 0.145 | 0.20 |
| c <sub>1</sub>   | —                        | 0.125 | —    |
| θ                | 0°                       | —     | 8°   |
| Ⓜ                | —                        | 0.8   | —    |
| x                | —                        | —     | 0.20 |
| y                | —                        | —     | 0.10 |
| Z <sub>D</sub>   | —                        | 1.0   | —    |
| Z <sub>E</sub>   | —                        | 1.0   | —    |
| L                | 0.3                      | 0.5   | 0.7  |
| L <sub>1</sub>   | —                        | 1.0   | —    |

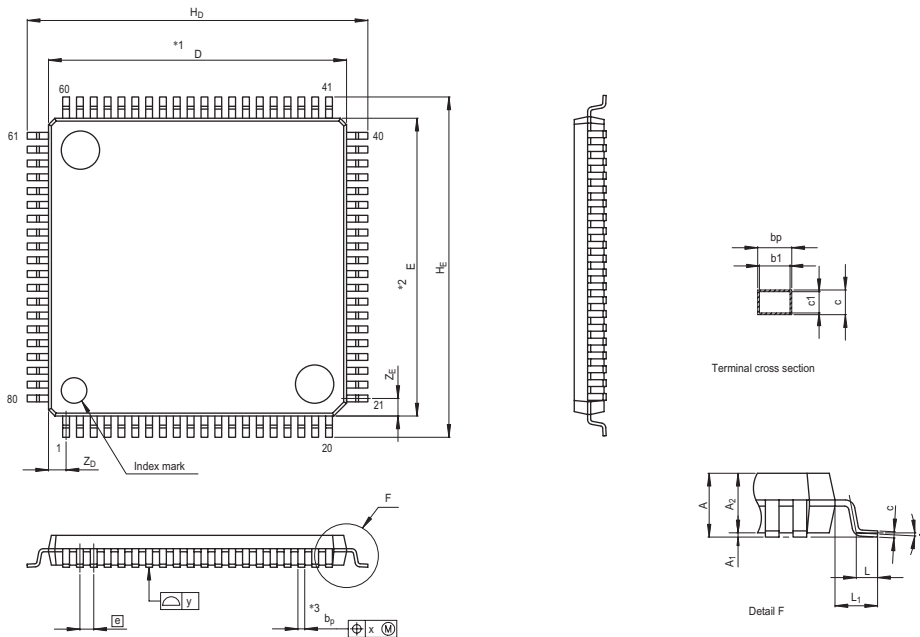
|                     |              |               |            |
|---------------------|--------------|---------------|------------|
| JEITA Package Code  | RENESAS Code | Previous Code | MASS[Typ.] |
| P-LQFP80-12x12-0.50 | PLQP0080KB-A | 80P6Q-A       | 0.5g       |



NOTE)  
 1. DIMENSIONS \*\*1\* AND \*\*2\*  
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3\* DOES NOT  
 INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters |       |      |
|------------------|--------------------------|-------|------|
|                  | Min                      | Nom   | Max  |
| D                | 11.9                     | 12.0  | 12.1 |
| E                | 11.9                     | 12.0  | 12.1 |
| A <sub>2</sub>   | —                        | 1.4   | —    |
| H <sub>D</sub>   | 13.8                     | 14.0  | 14.2 |
| H <sub>E</sub>   | 13.8                     | 14.0  | 14.2 |
| A                | —                        | —     | 1.7  |
| A <sub>1</sub>   | 0                        | 0.1   | 0.2  |
| b <sub>p</sub>   | 0.15                     | 0.20  | 0.25 |
| b <sub>1</sub>   | —                        | 0.18  | —    |
| c                | 0.09                     | 0.145 | 0.20 |
| c <sub>1</sub>   | —                        | 0.125 | —    |
| $\theta$         | 0°                       | —     | 10°  |
| $\text{ⓐ}$       | —                        | 0.5   | —    |
| x                | —                        | —     | 0.08 |
| y                | —                        | —     | 0.08 |
| Z <sub>D</sub>   | —                        | 1.25  | —    |
| Z <sub>E</sub>   | —                        | 1.25  | —    |
| L                | 0.3                      | 0.5   | 0.7  |
| L <sub>1</sub>   | —                        | 1.0   | —    |

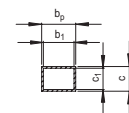
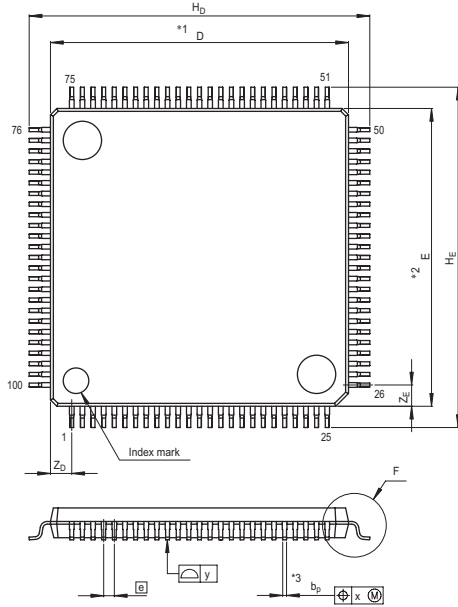
|                     |              |                  |            |
|---------------------|--------------|------------------|------------|
| JEITA Package Code  | RENESAS Code | Previous Code    | MASS[Typ.] |
| P-LQFP80-14x14-0.65 | PLQP0080JA-A | FP-80W / FP-80WV | 0.6g       |



NOTE)  
 1. DIMENSIONS \*\*1\* AND \*\*2\*  
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION \*\*3\* DOES NOT  
 INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters |       |      |
|------------------|--------------------------|-------|------|
|                  | Min                      | Nom   | Max  |
| D                | 13.9                     | 14.0  | 14.1 |
| E                | 13.9                     | 14.0  | 14.1 |
| A <sub>2</sub>   | —                        | 1.4   | —    |
| H <sub>D</sub>   | 15.8                     | 16.0  | 16.2 |
| H <sub>E</sub>   | 15.8                     | 16.0  | 16.2 |
| A                | —                        | —     | 1.7  |
| A <sub>1</sub>   | 0.05                     | 0.1   | 0.15 |
| b <sub>p</sub>   | 0.27                     | 0.32  | 0.37 |
| b <sub>1</sub>   | —                        | 0.30  | —    |
| c                | 0.09                     | 0.145 | 0.20 |
| c <sub>1</sub>   | —                        | 0.125 | —    |
| $\theta$         | 0°                       | —     | 8°   |
| $\text{ⓐ}$       | —                        | 0.65  | —    |
| x                | —                        | —     | 0.13 |
| y                | —                        | —     | 0.10 |
| Z <sub>D</sub>   | —                        | 0.825 | —    |
| Z <sub>E</sub>   | —                        | 0.825 | —    |
| L                | 0.35                     | 0.5   | 0.65 |
| L <sub>1</sub>   | —                        | 1.0   | —    |

| JEITA Package Code   | RENESAS Code | Previous Code                 | MASS[Typ.] |
|----------------------|--------------|-------------------------------|------------|
| P-LQFP100-14x14-0.50 | PLQP0100KB-A | 100P6Q-A / FP-100U / FP-100UV | 0.6g       |

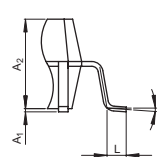
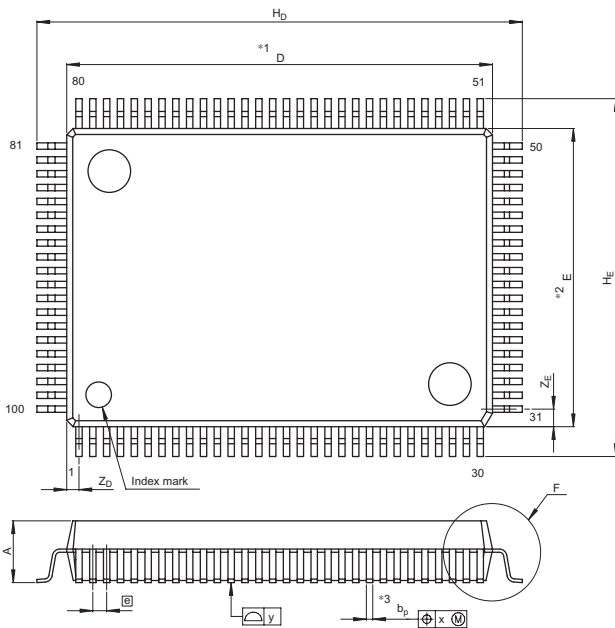


Terminal cross section

NOTE)  
 1. DIMENSIONS  $*1$  AND  $*2$   
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION  $*3$  DOES NOT  
 INCLUDE TRIM OFFSET.

| Reference Symbol  | Dimension in Millimeters |       |      |
|-------------------|--------------------------|-------|------|
|                   | Min                      | Nom   | Max  |
| D                 | 13.9                     | 14.0  | 14.1 |
| E                 | 13.9                     | 14.0  | 14.1 |
| $A_2$             | —                        | 1.4   | —    |
| $H_D$             | 15.8                     | 16.0  | 16.2 |
| $H_E$             | 15.8                     | 16.0  | 16.2 |
| A                 | —                        | —     | 1.7  |
| $A_1$             | 0.05                     | 0.1   | 0.15 |
| $b_p$             | 0.15                     | 0.20  | 0.25 |
| $b_1$             | —                        | 0.18  | —    |
| c                 | 0.09                     | 0.145 | 0.20 |
| $c_1$             | —                        | 0.125 | —    |
| $\theta$          | 0°                       | —     | 8°   |
| $\textcircled{E}$ | —                        | 0.5   | —    |
| x                 | —                        | —     | 0.08 |
| y                 | —                        | —     | 0.08 |
| $Z_D$             | —                        | 1.0   | —    |
| $Z_E$             | —                        | 1.0   | —    |
| L                 | 0.35                     | 0.5   | 0.65 |
| $L_1$             | —                        | 1.0   | —    |

| JEITA Package Code  | RENESAS Code | Previous Code | MASS[Typ.] |
|---------------------|--------------|---------------|------------|
| P-QFP100-14x20-0.65 | PRQP0100JD-B | 100P6F-A      | 1.8g       |



Detail F

Under development

NOTE)  
 1. DIMENSIONS  $*1$  AND  $*2$   
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION  $*3$  DOES NOT  
 INCLUDE TRIM OFFSET.

| Reference Symbol  | Dimension in Millimeters |       |      |
|-------------------|--------------------------|-------|------|
|                   | Min                      | Nom   | Max  |
| D                 | 19.8                     | 20.0  | 20.2 |
| E                 | 13.8                     | 14.0  | 14.2 |
| $A_2$             | —                        | 2.8   | —    |
| $H_D$             | 22.5                     | 22.8  | 23.1 |
| $H_E$             | 16.5                     | 16.8  | 17.1 |
| A                 | —                        | —     | 3.05 |
| $A_1$             | 0                        | 0.1   | 0.2  |
| $b_p$             | 0.25                     | 0.3   | 0.4  |
| c                 | 0.13                     | 0.15  | 0.2  |
| $\theta$          | 0°                       | —     | 10°  |
| $\textcircled{E}$ | —                        | 0.65  | —    |
| x                 | —                        | —     | 0.13 |
| y                 | —                        | —     | 0.10 |
| $Z_D$             | —                        | 0.575 | —    |
| $Z_E$             | —                        | 0.825 | —    |
| L                 | 0.4                      | 0.6   | 0.8  |

## REVISION HISTORY

R8C/L35A Group, R8C/L36A Group, R8C/L38A Group, R8C/L3AA Group,  
R8C/L35B Group, R8C/L36B Group, R8C/L38B Group, R8C/L3AB Group Datasheet

| Rev. | Date                                 | Description |   |
|------|--------------------------------------|-------------|---|
|      |                                      | Page        | Summary   |
| 0.01 | May 19, 2008                         | –           | First Edition issued  |
| 0.02 | Jul 10, 2008                         | 3           | Table 1.4<br>CPU Specification: Minimum instruction execution time revised<br>DTC Specification: Activation sources 33→38   |
|      |                                      | 4           | Table 1.5<br>R8C/L35A, R8C/L35B Groups: Specification revised   |
|      |                                      | 5           | Table 1.6<br>Operating Frequency/Supply Voltage: Specification revised  |
|      |                                      | 6 to 13     | Table 1.7 to Table 1.14<br>Current of May 2008→Current of Jul 2008  |
|      |                                      | 10 to 11    | Table 1.11 and Table 1.12 (P)→(D)   |
|      |                                      | 23          | Table 1.15<br>$\overline{WKUP1}$ → $\overline{WKUP1(3)}$  |
|      |                                      | 32          | Table 4.1<br>RSTFR: 0XXX00XXb→XXXX00XXb<br>POMCR0: 00h→XX0000XXb  |
|      |                                      | 33          | Table 4.2<br>0072h Voltage monitor 1/Compare A1 interrupt Control Register<br>→Voltage monitor 1/Comparator A1 interrupt Control Register<br>0073h Voltage monitor 2/Compare A2 interrupt Control Register<br>→Voltage monitor 2/Comparator A2 interrupt Control Register   |
|      |                                      | 36          | Table 4.5<br>TRECRC1: XXX0X0XXb→XXXXX0XXb   |
|      |                                      | 38          | Table 4.7<br>0194h<br>SS Transmit Data Register→SS Transmit Data Register L<br>0195h<br>SS Transmit Data Register SSTDR<br>→SS Transmit Data Register H SSTDRH<br>0196h<br>SS Receive Data Register→SS Receive Data Register L<br>IIC bus Shift Register ICDRS deleted<br>0197h<br>SS Receive Data Register SSRDR<br>→SS Receive Data Register H SSRDRH |
| 39   | Table 4.8<br>01E0h to 01E7h: FFh→00h |             |   |
| 0.10 | Jul 30, 2008                         | 3           | Table 1.4<br>Watchdog Timer: Specification 15 bits→14 bits  |
|      |                                      | 5           | Table 1.6<br>Flash Memory: Function R8C/L36B Group→R8C/L36A Group   |
|      |                                      | 14 to 17    | Figure 1.9 to Figure 1.12<br>Watchdog Timer 15 bits→14 bits   |

## REVISION HISTORY

R8C/L35A Group, R8C/L36A Group, R8C/L38A Group, R8C/L3AA Group,  
R8C/L35B Group, R8C/L36B Group, R8C/L38B Group, R8C/L3AB Group Datasheet

| Rev. | Date  | Description |  |
|------|---|-------------|--|
|      |   | Page        | Summary  |
| 0.10 | Jul 30, 2008                                  | 18 to 22    | Figure 1.13 to Figure 1.17<br>P4_6/SEG38/TRCIOC→P4_6/SEG38/TRCIOC/TRCIOB<br>P4_7/SEG39/TRCIOD→P4_7/SEG39/TRCIOD/TRCIOB |
|      |   | 24          | Table 1.16<br>Timer TRCIOD→TRCIOD/TRCIOB<br>TRCIOC→TRCIOC/TRCIOB   |
|      |   | 32          | Table 4.1<br>0020h: After Reset XX0000XXb→X0000000b<br>Note 2 revised  |
| 0.30 | Jan 21, 2009                                  | 1           | 1.1 revised  |
|      |   | 2           | 1.1.2 revised<br>Table 1.2 revised   |
|      |   | 3           | Table 1.3 Note 2 added<br>Table 1.4 added  |
|      |   | 5           | Table 1.6 revised  |
|      |   | 6           | Table 1.7 revised  |
|      |   | 7 to 14     | Table 1.8 to Table 1.15 revised  |
|      |   | 15          | Figure 1.9 revised   |
|      |   | 16          | Figure 1.10 revised  |
|      |   | 19          | Figure 1.13 revised  |
|      |   | 20          | Figure 1.14 revised  |
|      |   | 24          | Table 1.16 Note 3 revised  |
|      |   | 25          | Table 1.17 Note 3 added  |
|      |   | 33          | Table 4.1<br>000Bh: After Reset XXXX00XXb→XXh<br>Note 2 revised  |
| 39   | Table 4.7<br>018Fh added                      |             |  |
| 41   | Table 4.9<br>0202h: After Reset 00h→X0000000b |             |  |

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# RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Renesas Technology Corp.

|                     |  |         |                      |                        |      |      |
|---------------------|--|---------|----------------------|------------------------|------|------|
| Product Category    | MPU&MCU  |         | Document No.         | TN-R8C-A002B/E         | Rev. | 2.00 |
| Title               | Specification Changes in the R8C/L35A Group, R8C/L35B Group, R8C/L36A Group, R8C/L36B Group, R8C/L38A Group, R8C/L38B Group, R8C/L3AA Group R8C/L3AB Group Hardware Manual |         | Information Category | Technical Notification |      |      |
| Applicable Products | R8C/L35A Group, R8C/L35B Group<br>R8C/L36A Group, R8C/L36B Group<br>R8C/L38A Group, R8C/L38B Group<br>R8C/L3AA Group and R8C/L3AB Group                                    | Lot No. | Reference Document   | Described below        |      |      |
|                     |  | ---     |                      |                        |      |      |

(8) in section 1-1 and section 2-8 have been revised in Revision 2.00.

## 1. Overview

The below changes have been made to the specifications described in the datasheet and hardware manual of the R8C/L3AA Group, R8C/L3AB Group, R8C/L38A Group, R8C/L38B Group, R8C/L36A Group, R8C/L36B Group, R8C/L35A Group and R8C/L35B Group.

### 1-1. Changes

- (1) Removed the high-speed on-chip oscillator
- (2) Changed the flash memory suspend function specifications
- (3) Changed the flash memory suspend electrical characteristics
- (4) Changed the timer RG specifications
- (5) Changed the LCD port specifications
- (6) Removed the voltage monitor 0 reset/power-on reset
- (7) Removed the voltage monitor 1 /comparator A1 and voltage monitor 2 / comparator A2 functions
- (8) Note on reducing power current

### 1-2. Reference Documents

The information in this document applies to the R8C/L35A Group, R8C/L35B Group, R8C/L36A Group, R8C/L36B Group, R8C/L35A Group, R8C/L38B Group, R8C/L3AA Group, R8C/L3AB Group Hardware Manual Rev.0.30 and Datasheet Rev.0.30.

## 2. Description

### 2-1. Removed the High-Speed On-Chip Oscillator

The high-speed on-chip oscillator function has been removed.

Do NOT select the high-speed on-chip oscillator as the clock source for the CPU clock or peripheral functions.

Descriptions regarding the high-speed on-chip oscillator in the reference documents shown in 1-2, other than descriptions shown in this technical update, are invalid.

## 2-1-1. Register Settings Related to the Clock Generation Circuit

### 2-1-1-1. High-Speed On-Chip Oscillator Control Register 0 (FRA0)

- (1) Do NOT set FRA00 bit to 1 (high-speed on-chip oscillator on) [refer to Figure 2-1]
- (2) Do NOT set FRA01 bit to 1 (high-speed on-chip oscillator selected as fOCO clock source) [refer to Figure 2-1].  
The fOCO is a clock source of timer RA.
- (3) Do NOT set FRA03 bit to 1 (fOCO-F divided by 128 selected as a clock source of fOCO128) [refer to Figure 2-1].  
fOCO128 is used as an input-capture signal of timers RC and RD.

### 2-1-1-2. System Clock Control Register 3 (CM3)

- (1) Do NOT set bits CM37 to CM36 bits to 10b (high-speed on-chip oscillator selected as CPU clock when the MCU exits wait mode or stop mode) [refer to Figure 2-2].

### 2-1-1-3. High-Speed On-Chip Oscillator Control Register i (FRAi) (i = 1 to 7)

- (1) Do NOT set the register related to the high-speed on-chip oscillator division select (FRA2) or registers related to frequency adjustment (FRA1 and FRA3 to FRA7).

## 2-1-2. Register Settings Related to Timer RA

### 2-1-2-1. High-Speed On-chip Oscillator Control Register 0 (FRA0)

- (1) Do NOT set the FRA01 bit to 1 (high-speed on-chip oscillator selected for the fOCO clock) [refer to Figure 2-1]. The high-speed on-chip oscillator clock cannot be selected as the timer RA count source.

## 2-1-3 Register Settings Related to Timer RC

### 2-1-3-1. Timer RC Control Register 1 (TRCCR1)

- (1) Do NOT set bits TCK2 to TCK0 to 110b (fOCO40M selected as the timer RC count source) [refer to Figure 2-3].
- (2) Do NOT set bits TCK2 to TCK0 to 111b (fOCO-F selected as the timer RC count source) [refer to Figure 2-3].

### 2-1-3-2. High-speed On-Chip Oscillator Control Register 0 (FRA0)

- (1) Do NOT set the FRA03 bit to 1 (fOCO-F divided by 128 selected as the fOCO 128 clock) [refer to Figure 2-1]. For the timer RC input-capture function, fOCO-F divided by 128 cannot be selected for the input-capture trigger input of the TRCGRA register.

## 2-1-4. Register Settings Related to Timer RD

### 2-1-4-1. Timer RD Control Register 0, 1 (TRDCR0, TRDCR1)

- (1) Do NOT set bits TCK2 to TCK0 to 110b (fOCO40M selected as the timer RD count source) [refer to Figure 2-4].
- (2) Do NOT set bits TCK2 to TCK0 to 111b (fOCO-F selected as the timer RD count source) [refer to Figure 2-4].

### 2-1-4-2. High-speed On-Chip Oscillator Control Register 0 (FRA0)

- (1) Do NOT set the FRA03 bit to 1 (fOCO-F divided by 128 cannot be selected for the input-capture trigger input of the TRDGRA0 register [refer to Figure 2-1]. For the timer RD input-capture function, fOCO-F divided by 128 cannot be selected for the input-capture trigger input of the TRDGRA register.

2-1-5. Timer RG Control Register Settings

2-1-5-1. Timer RG Control Register (TRGCR)

(1) Do NOT set bits TCK2 to TCK0, the count source select bits in the timer RG control register (TRGCR), to 110b (fOCO40M selected as a count source of timer RG) [refer to Figure 2-5].

2-1-6. Register Settings for the A/D Converter

2-1-6-1. A/D Mode Register (ADMOD)

(1) Do NOT set the CKS2 bit to 1 (fOCO-F selected as the A/D converter operating clock source) [refer to Figure 2-6].

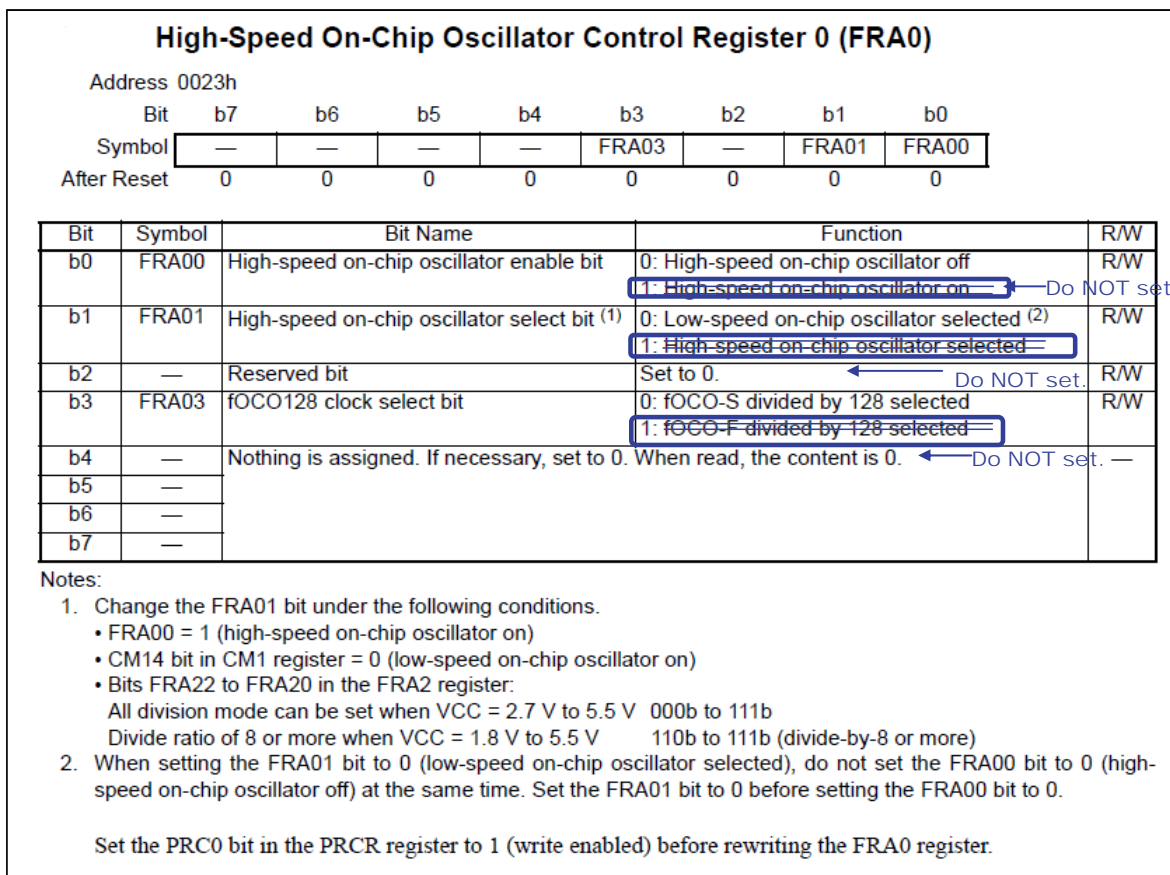


Figure 2-1.High-Speed On-Chip Oscillator Control Register 0 (FRA0) Setting

### System Clock Control Register 3 (CM3)

Address 0009h

|             |      |      |      |    |    |    |    |      |
|-------------|------|------|------|----|----|----|----|------|
| Bit         | b7   | b6   | b5   | b4 | b3 | b2 | b1 | b0   |
| Symbol      | CM37 | CM36 | CM35 | —  | —  | —  | —  | CM30 |
| After Reset | 0    | 0    | 0    | 0  | 0  | 0  | 0  | 0    |

| Bit | Symbol | Bit Name  | Function   | R/W |
|-----|--------|---|--|-----|
| b0  | CM30   | Wait control bit (1)  | 0: Other than wait mode<br>1: MCU enters wait mode   | R/W |
| b1  | —      | Nothing is assigned. If necessary, set to 0. When read, the content is 0. |  | —   |
| b2  | —      |   |  |     |
| b3  | —      | Reserved bits   | Set to 0.  | R/W |
| b4  | —      |   |  |     |
| b5  | CM35   | CPU clock division ratio select bit when exiting wait mode (2)            | 0: Following settings are enabled:<br>CM06 bit in CM0 register<br>Bits CM16 and CM17 in CM1 register<br>1: No division   | R/W |
| b6  | CM36   | System clock select bit when exiting wait or stop mode                    | <sup>b7 b6</sup><br>0 0: MCU exits with the CPU clock used immediately before entering wait or stop mode<br>0 1: Do not set.<br>1 0: High-speed on-chip oscillator clock selected (3)<br>1 1: XIN clock selected (4) → Do NOT set. | R/W |
| b7  | CM37   |   |  | R/W |

**Notes:**

- When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
- Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
- ~~When bits CM37 to CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode or stop mode:~~
  - ~~• OCD2 bit in OCD register = 1 (on-chip oscillator selected)~~
  - ~~• FRA00 bit in FRA0 register = 1 (high-speed on-chip oscillator on)~~
  - ~~• FRA01 bit in FRA0 register = 1 (high-speed on-chip oscillator selected)~~
- When bits CM37 to CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
  - OM05 bit in OM0 register = 1 (XIN clock oscillates)
  - OM13 bit in OM1 register = 1 (XIN-XOUT pin)
  - OCD2 bit in OCD register = 0 (XIN clock selected)

When the MCU enters wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock when exiting wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0.

However, if an externally generated clock is used as the XIN clock, do not set bits CM37 to CM36 to 11b (XIN clock selected).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM3 register.

Figure 2-2. System Clock Control Register 3 (CM3) Setting

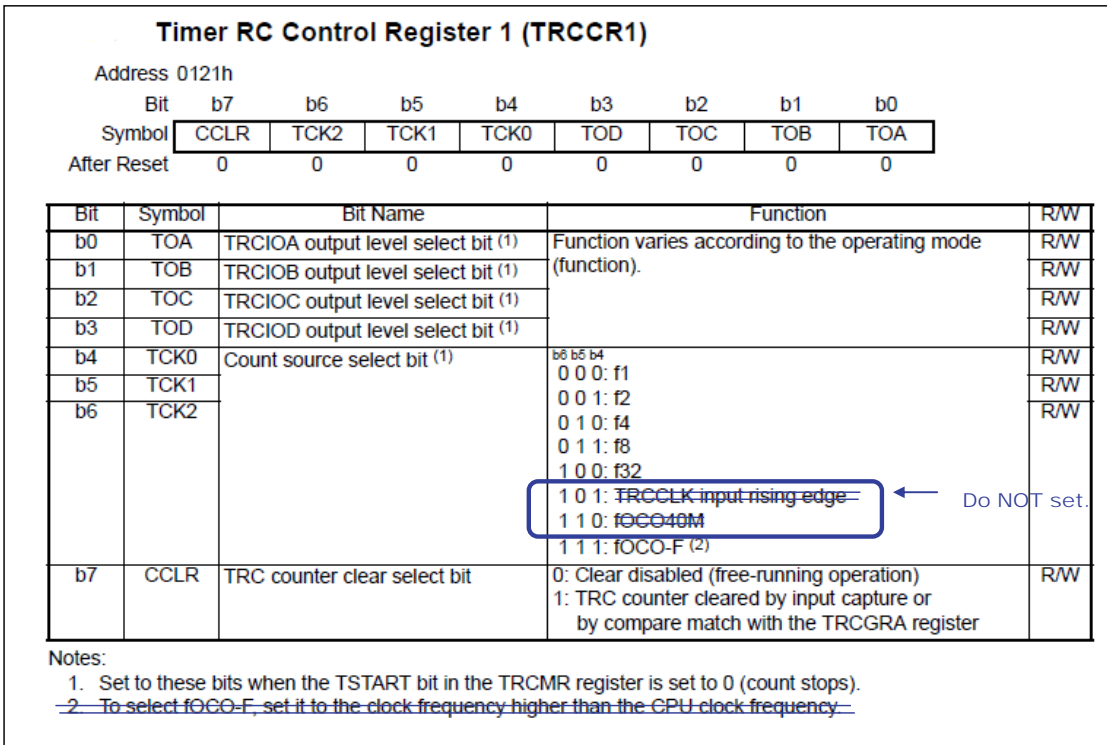


Figure 2-3. Timer RC Control Register 1 (TRCCR1) Setting

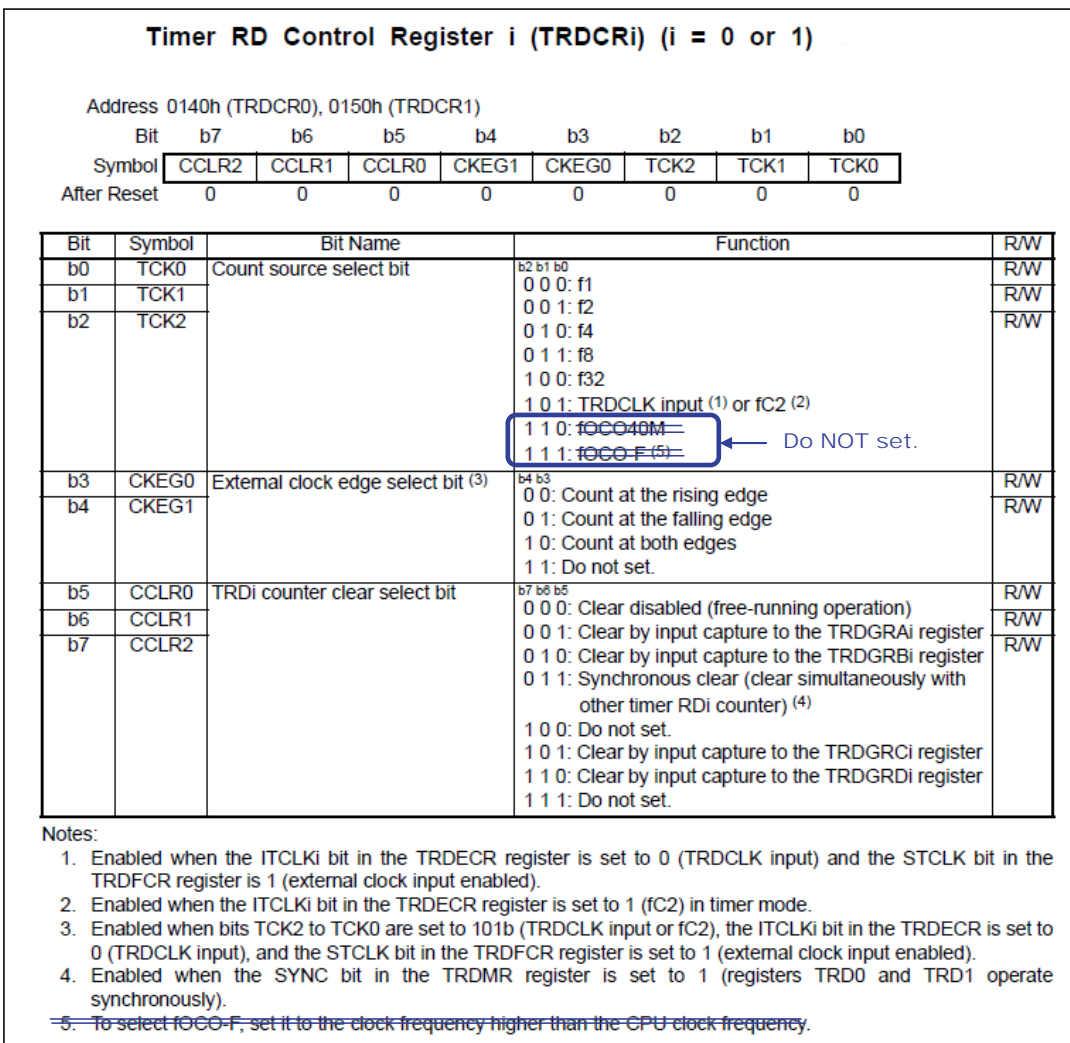


Figure 2-4. Timer RD Control Register 0,1 (TRDCR0, TRDCR1) Setting



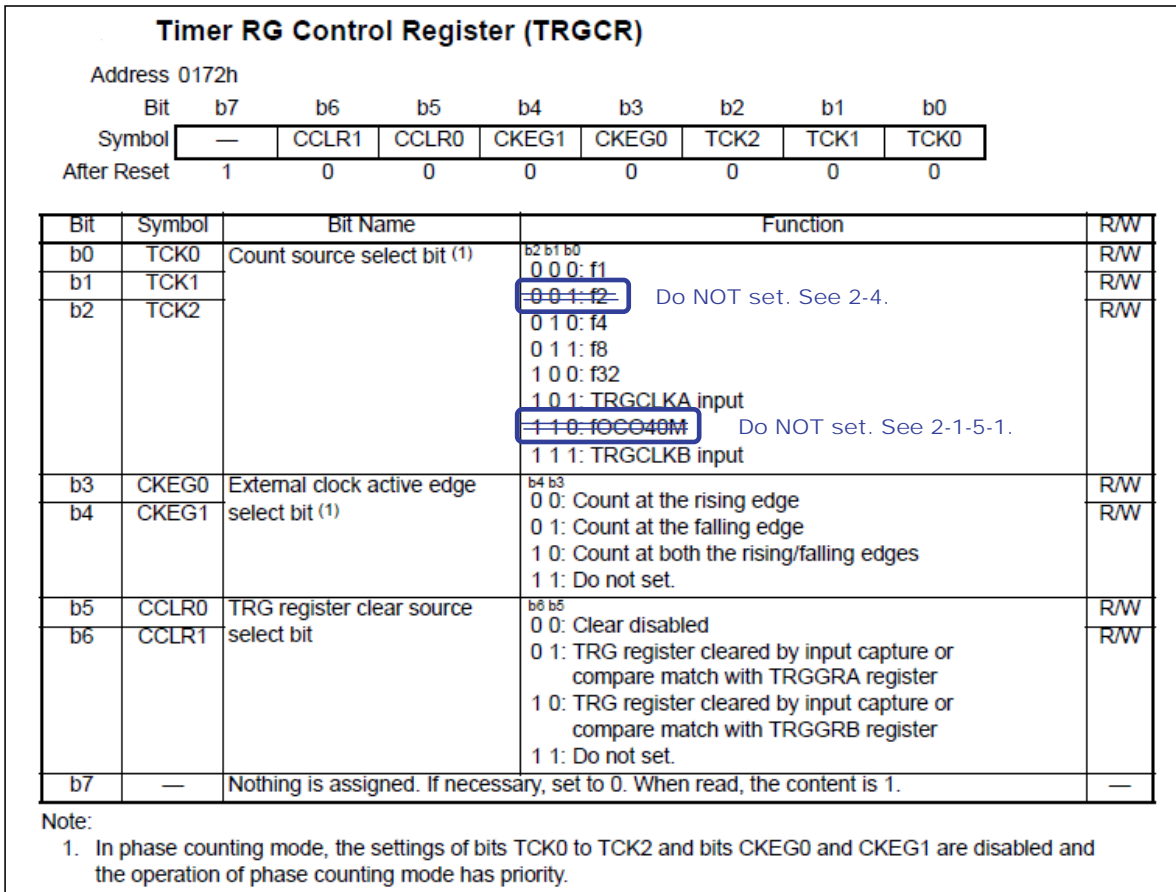


Figure 2-5. Timer RG Control Register (TRGCR) Setting

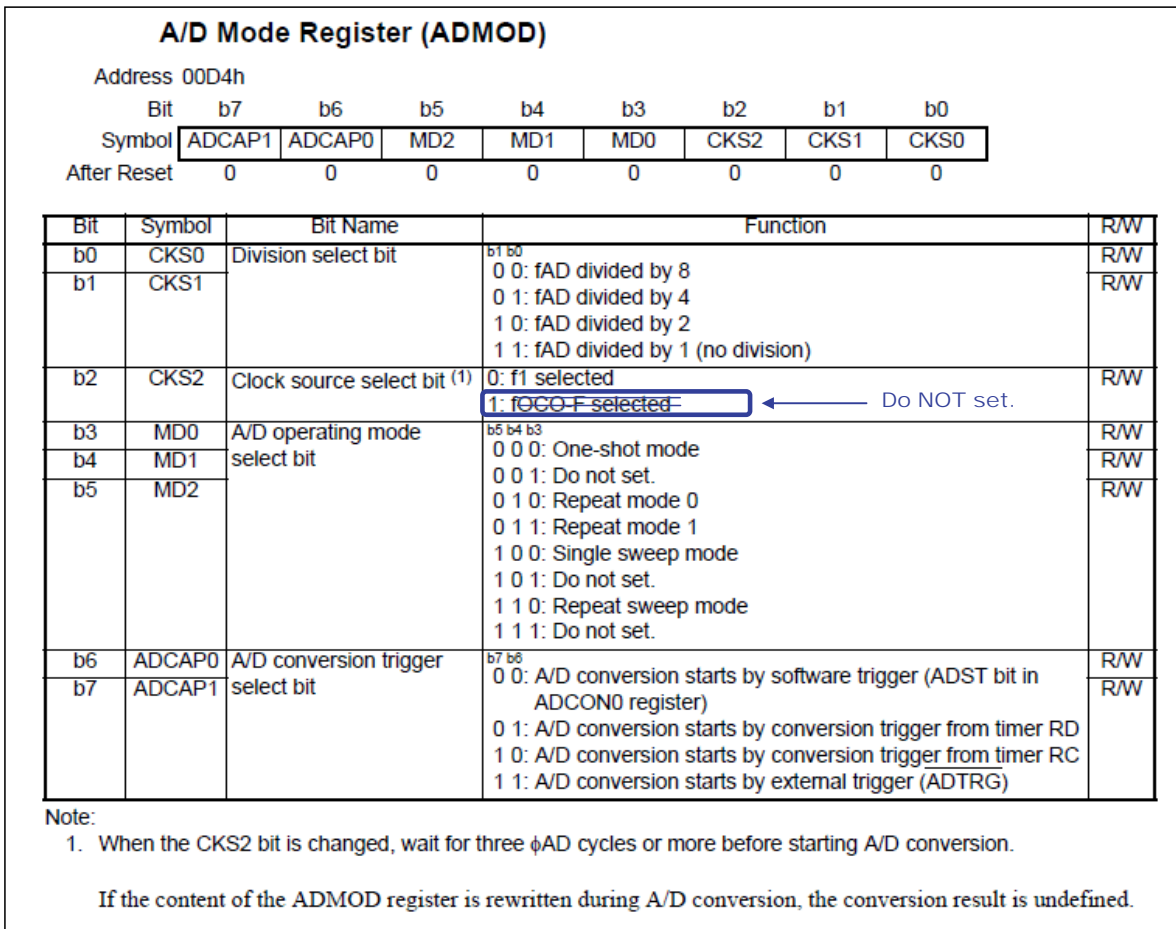


Figure 2-6. A/D Mode Register (ADMOD) Setting

2-2. Changes in the Flash Memory Suspend Function

Flash programming operation is disabled when the auto-erasure is suspended while using the flash memory suspend function.

**Executable Operation during Suspend**

|  |             | Operation during Suspend   |         |      |   |         |      |   |         |      |  |         |                  |
|--|-------------|--|---------|------|---|---------|------|---|---------|------|--|---------|------------------|
|  |             | Data flash<br>(Block during erasure execution before entering suspend) |         |      | Data flash<br>(Block during no erasure execution before entering suspend) |         |      | Program ROM<br>(Block during erasure execution before entering suspend) |         |      | Program ROM<br>(Block during no erasure execution before entering suspend) |         |                  |
|  |             | Erase  | Program | Read | Erase   | Program | Read | Erase   | Program | Read | Erase  | Program | Read             |
| Areas during erasure execution before entering suspend | Data flash  | ×  | ×       | ×    | ×   | ⊖       | ○    | —   | —       | —    | ×  | ⊖       | ○ <sup>(5)</sup> |
|  | Program ROM | —  | —       | —    | ×   | ⊖       | ○    | ×   | ×       | ×    | ×  | ⊖       | ○                |

Notes:

- indicates operation is enabled by using the suspend function, × indicates operation is disabled, and — indicates no combination is available.
- Operation cannot be suspended during programming.
- The block erase command can be executed for erasure. The program, lock bit program, and read lock bit status commands can be executed for programming. The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready). The operation of block blank check is disabled during suspend.
- The MCU enters read array mode immediately after entering erase-suspend.
- The program ROM area can be read with the BGO function while programming or block erasing data flash.

Program is also not available with Data Flash driver in condition indicated in   .

Figure 2-7. Flash Memory Suspend Function

2-3. Changes in the Flash Memory Suspend Function Electrical Characteristics

Wait for at least 33 ms after the erase start/restart request before the making the next erase/suspend request. This is described as the "Interval from erase start/restart until suspend" in the hardware manual [refer to Figure 2-7].

**Flash Memory (Program ROM) Characteristics**  
(VCC = 2.7 to 5.5 V and Topr = 0 to 60°C, unless otherwise specified.)

|   |   |  |           |   |   |           |
|---|---|--|-----------|---|---|-----------|
| — | Interval from erase start/restart until following suspend request |  | ⊖<br>→ 33 | — | — | ⊖<br>→ ms |
| — | Suspend interval necessary for auto-erasure to complete           |  | 33        | — | — | ms        |

**Flash Memory (Data flash Block A to Block D) Characteristics**  
(VCC = 2.7 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

|   |   |  |           |   |   |           |
|---|---|--|-----------|---|---|-----------|
| — | Interval from erase start/restart until following suspend request |  | ⊖<br>→ 33 | — | — | ⊖<br>→ ms |
| — | Suspend interval necessary for auto-erasure to complete           |  | 33        | — | — | ms        |

Figure 2-8. Flash Memory Suspend Electrical Characteristics



#### 2-4. Change in the Timer RG Function

Do NOT set the count source select bits (TCK2 to TCK0) in the timer RG control register (TRGCR) to 001b (f2 selected as the count source of timer RG) [refer to Figure 2-5].

#### 2-5. Changes in the LCD Port Function

##### 2-5-1. LCD Port Select Register 0 (LSE0)

This information applies to the R8C/L35A Group, R8C/L36A Group, R8C/L35B Group, and R8C/L36B Group.

Do NOT set bits LSE06 and LSE07 to 1 (SEG6 and SEG7 port functions selected). P0\_6/SEG6 and P0\_7/SEG7 cannot be used as segment pins SEG6 and SEG7. P0\_6/SEG6 and P0\_7/SEG7 can be used as I/O ports P0\_6 and P0\_7.

##### 2-5-2. LCD Port Select Register 2 (LSE2)

This information applies to the R8C/L38A Group and R8C/L38B Group.

Do NOT set the LSE16 bit to 1 (SEG16 port function selected). P2\_0/SEG16/KI0 cannot be used as segment pin SEG16. P2\_0/SEG16/KI0 can be used as I/O port P0\_2 and KI0.

#### 2-6. Voltage Monitor 0 Reset and Power-On Reset

The voltage monitor 0 reset and power-on reset cannot be used. Use a hardware reset to reset the MCU. In the documents listed in section 1-2, descriptions of the voltage monitor 0 reset and power-on reset are invalid.

#### 2-7. Removed the Voltage Monitor 1 / Comparator A1 Interrupt and Voltage Monitor 2 / Comparator A2 Interrupt Functions

Voltage monitor 1 / comparator A1 and voltage monitor 2 / comparator A2 cannot be used. In the documents listed in section 1-2, description of the voltage monitor 0 reset or power-on reset are invalid.

#### 2-8. Note on Reducing Power Current

Write 00h to the POMCR0 register (address 0020h) by a program. Current consumption may increase until 00h is written to the POMCR0 register.

Sample code: MOV.B #00H, 0020H

#### 3. Other Note

Note regarding pins P12\_1 and P12\_0.

P12\_1 and P12\_0 are shared with XIN and XOUT. When XIN is used as a clock, these ports cannot be used as I/O ports.

#### 4. Slated Changes

Contact the Renesas Technology sales department for schedule and products with high-speed on-chip oscillator.

- End of description -