PRESETTABLE UP/DOWN COUNTERS: MMC 4510 PRESETTABLE BCD UP/DOWN COUNTERS MMC 4516 PRESETTABLE BINARY UP/DOWN COUNTER

GENERAL DESCRIPTION

The MMC 4510, MMC 4516 are monolithic integrated circuits available in 16-lead dual in-line plastic package.
The MMC 4510 Presetable BCD Up/Down Counter and MMC 4516 Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The MMC 4510 will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode. If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage. The MMC 4510 and MMC 4516 can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

FEATURES

- Medium speed operation f_{cl} = 8 MHz typ. at 10 V
- Synchronous internal CARRY propagation
- RESET and PRESET capability

ABSOLUTE MAXIMUM RATINGS

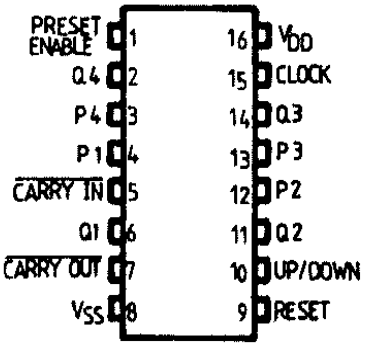
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_I	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_I	Imput voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS
(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		±10 [5]	±0.1		±1	μA
		E, F types	0/15			15		±0.3		±10 [5]	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

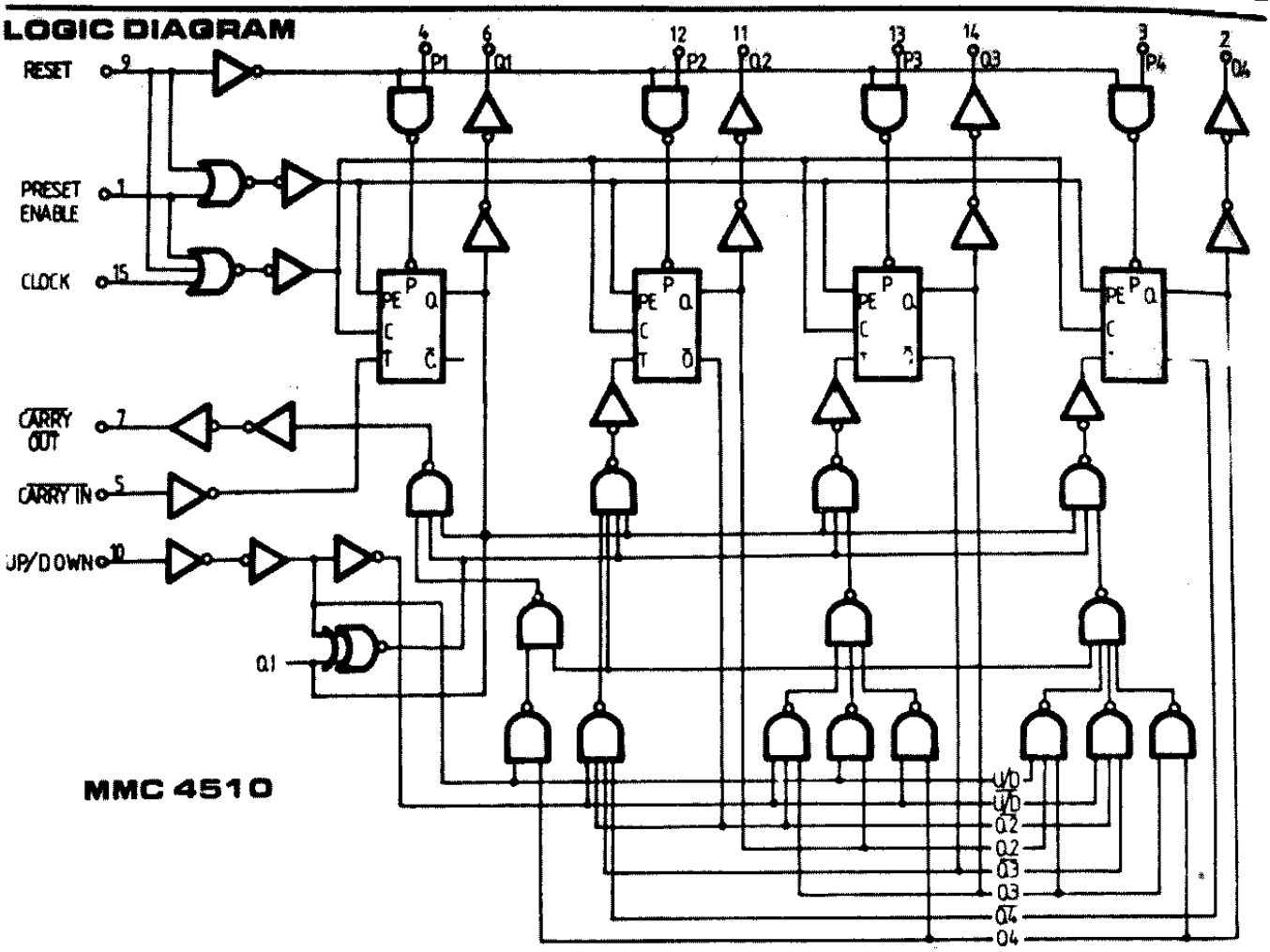
(T_{amb} = 25°C, C_L = 50 pF, R_L = 200 k, typical temperature coeficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

	PARAMETER	TEST CONDITIONS V_{DD} (V)	VALUES MIN.	VALUES TYP.	VALUES MAX.	UNIT
t_{PHL}, t_{PLH}	Propagation delay time, Clock to Q output	5 10 15		200 100 75	400 200 150	ns
t_{PHL}, t_{PLH}	Propagation delay time preset or reset to Q output	5 10 15		210 105 80	420 210 160	ns
t_{PHL}, t_{PLH}	Propagation delay time clock to carry out	5 10 15		240 120 90	480 240 180	ns
t_{PHL}, t_{PLH}	Propagation delay time carry in to carry out	5 10 15		125 60 50	250 120 100	ns
t_{PHL}, t_{PLH}	Propagation delay time preset or reset to carry out	5 10 15		320 160 125	640 320 250	ns
t_{TLH}, t_{THL}	Transition time	5 10 15		100 50 40	200 100 80	ns
f_{max},	Max. clock frequency	5 10 15	2 4 5.5	4 8 11		MHz
t_W,	Clock pulse width	5 10 15	150 75 60			ns
	(*) Preset enble or removal time	5 10 15	150 80 60			ns
t_r t_f	** Clock rise and fall time	5 10 15			15 5 5	ns
t_{setup}	Carry in setup time	5 10 15	130 60 45			ns
t_{setup}	Up-down setup time	5 10 15	360 160 110			ns
t_W	Preset enable or reset pulse width	5 10 15	220 100 75			ns

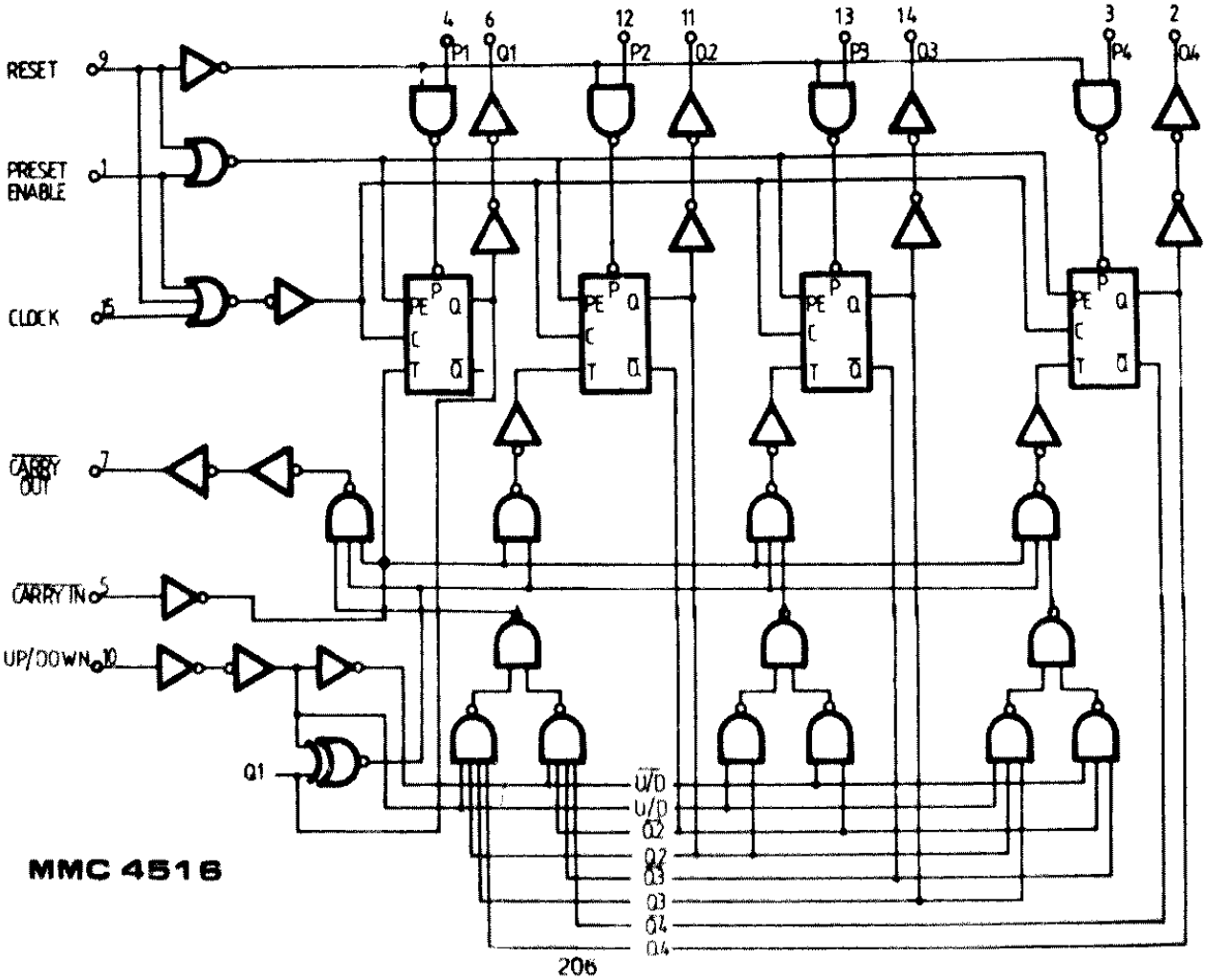
(*) Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time).

** If more than unit is cascaded in the parallel clocked application, t. clock should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

LOGIC DIAGRAM



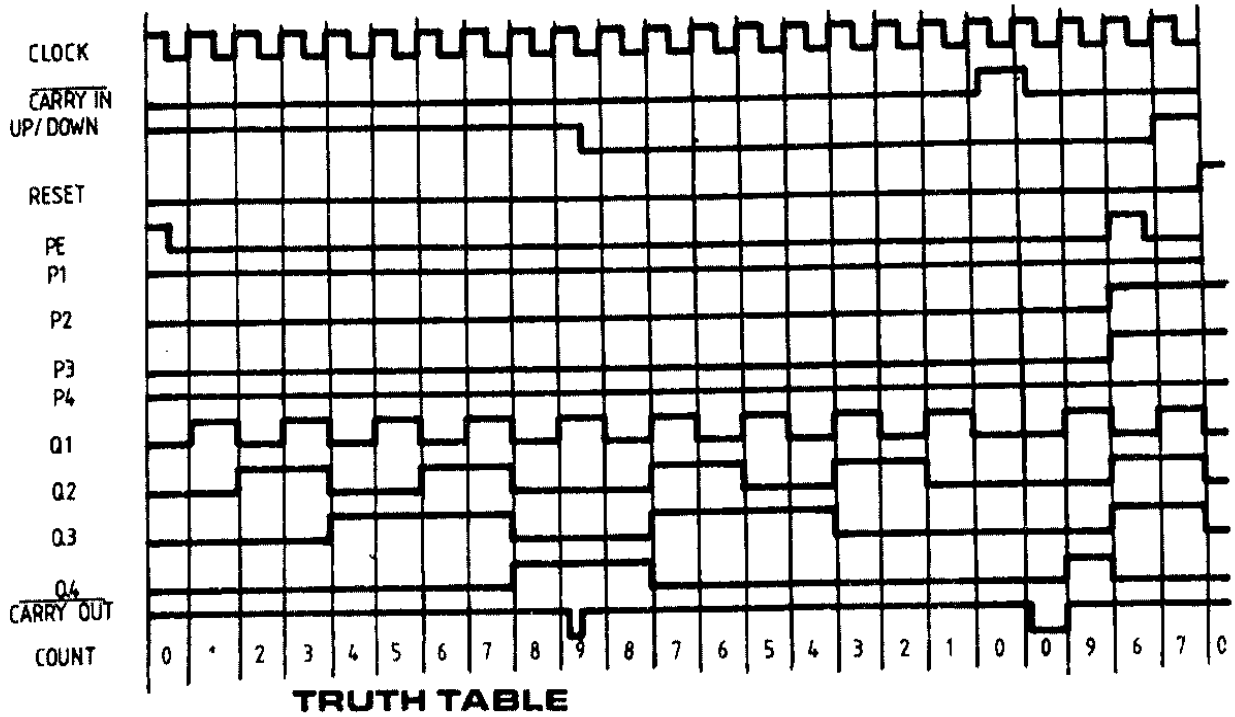
MMC 4510



MMC 4516

TIMING DIAGRAMS

MMC 4510



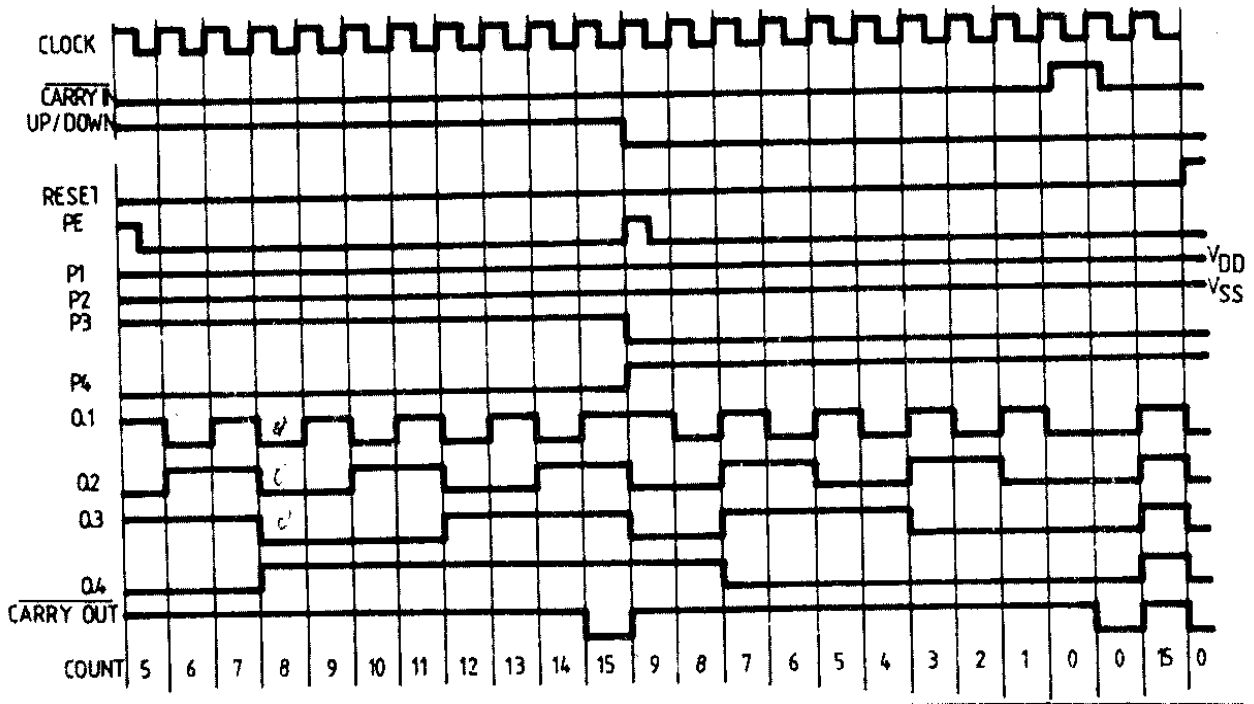
TRUTH TABLE

CL	CI	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
⎍	0	1	0	0	COUNT UP
⎍	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

X = Don't care

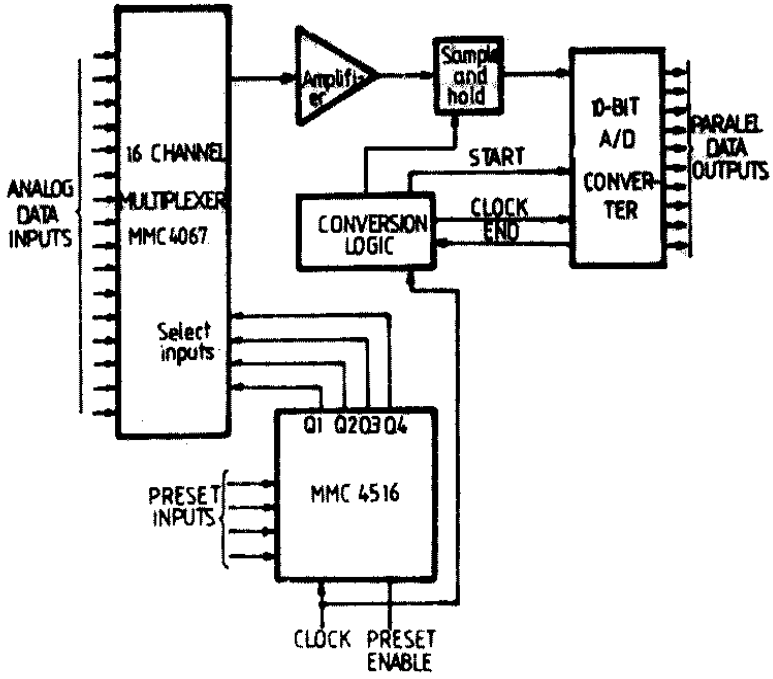
TIMING DIAGRAM

MMC 4516



TYPICAL APPLICATIONS

Typical 16-channel 10 bit data aquisition system



This aquisition system can be operated in the random access mode by jamming in the channel number at the present inputs, or in the sequential mode by clocking the MMC 4516.