

DUAL 4-BIT LATCH

The MMC 4508 dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET and OUTPUT DISABLE controls. With the STROBE line in high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the RESET line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line application by a high level on the DISABLE input.

The MMC 4508 E/F/G/H types are supplied in the 24-lead dual-in-line ceramic or plastic packages.

FEATURES

- Two independent 4-bit latches
- Individual master reset for each 4-bit latch
- 3-state outputs with high-impedance state for bus line applications
- Medium-speed operation: $t_{PLH} = t_{PHL} = 70$ ns (typ.) at $V_{DD} = 10$ V and $C_L = 50$ pF

APPLICATIONS

- Buffer storage
- Holding register
- Data storage and multiplexing

ABSOLUTE MAXIMUM RATINGS

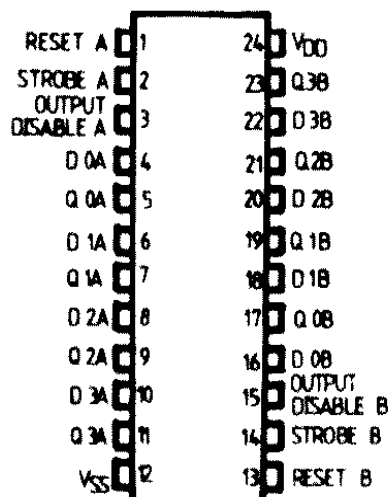
V_{DD}^*	Supply voltage: G and H types E and F types	-0.5 to -0.5 to -0.5 to	20 18 $V_{DD}+0.5$	V V V
V_i	Input voltage			
I_i	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package) Dissipation per output transistor for $T_A =$ full package-temperature range		200	mW
T_A	Operating temperature: G and H types E and F types	-55 to -40 to -65 to	125 85 150	$^{\circ}$ C $^{\circ}$ C $^{\circ}$ C
T_{stg}	Storage temperature			

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage: G and H types E and F types	3 to 3 to 0 to	18 15 V_{DD}	V V V
V_i	Input voltage			
T_A	Operating temperature: G and H types E and F types	-55 to -40 to	125 85	$^{\circ}$ C $^{\circ}$ C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES						UNIT		
		V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}			
						min.	max.	min.	typ	max.	min.		max.	
I _L	Quiescent current	G, H types	0/5			5		5		0.04	5		150	μ A
			0/10			10		10		0.04	10		300	
0/15				15		20		0.04	20		600			
0/20				20		100		0.08	100		3000			
E, F types	0/5			5		20		0.04	20		150			
	0/10			10		40		0.04	40		300			
	0/15			15		80		0.04	80		600			
V _{OH}	Output high voltage			< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V _{OL}	Output low voltage			< 1	5		0.05			0.05		0.05	V	
		5/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		
V _{IH}	Input high voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V	
			1/9	< 1	10	7		7			7			
			1.5/13.5	< 1	15	11		11			11			
V _{IL}	Input low voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V	
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
I _{OH}	Output drive current	G, H types	0/5	2.5		5	-2		-1.6	-3.2		-1.15	mA	
			0/5	4.6		5	-0.64		-0.51	-1		-0.36		
0/10	9.5			10	-1.6		-1.3	-2.6		-0.9				
0/15	13.5			15	-4.2		-3.4	-6.8		-2.4				
E, F types	0/5	2.5		5	-1.53		-1.36	-3.2		-1.1				
	0/5	4.6		5	-0.52		-0.44	-1		-0.36				
	0/10	9.5		10	-1.3		-1.1	-2.6		-0.9				
	0/15	13.5		15	-3.6		-3.0	-6.8		-2.4				
I _{OL}	Output sink current	G, H types	0/5	0.4		5	0.64		0.51	1		0.36	mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9		
0/15	1.5			15	4.2		3.4	6.8		2.4				
E, F types	0/5	0.4		5	0.52		0.44	1		0.36				
	0/10	0.5		10	1.3		1.1	2.6		0.9				
	0/15	1.5		15	3.6		3.0	6.8		2.4				
I _{IH} , I _{IL}	Input leakage current	G, H types	0/18	Any input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μ A
		E, F types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
I _{OX}	3-state output	G, H types	0/18	0/18		18		± 0.4		$\pm 10^{-4}$	± 0.4		± 12	μ A
		E, F types	0/15	0/15		15		± 1.0		$\pm 10^{-4}$	± 1.0		± 7.5	

PARAMETER	TEST CONDITIONS				VALUES						UNIT	
	V _I (V)	V _O (V)	I _O (μ A)	V _{DD} (V)	T _{LOW}		25°C			T _{HIGH}		
					min.	max.	min.	typ.	max.	min.		max.
C _I —input capacitance		Any input						5	7.5			pF

* T_{LOW} = -55°C for G, H devices; -40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

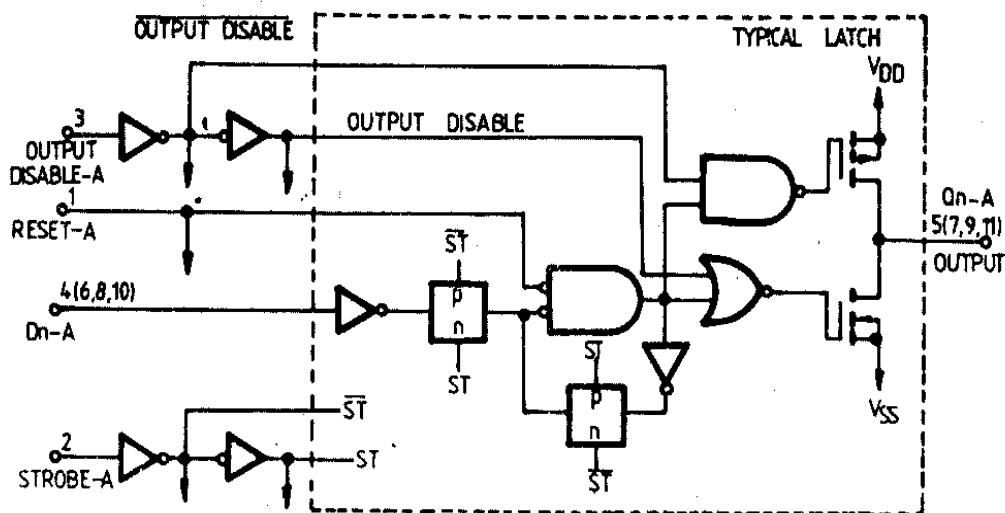
(T_a = 25°C, input t_r, t_f = 20 ns, C_L = 50 pF, R_i = 200 k Ω , unless otherwise specified)

PARAMETER	TEST CONDITIONS	VALUES			UNIT	
		V _{DD} (V)	min.	typ.		max.
t _{THL} Transition time t _{TLH}		5		100	200	ns
		10		50	100	
		15		40	80	
t _{W(R)} Reset pulse width		5	200	100		ns
		10	140	70		
		15	100	50		
t _{W(st)} Strobe pulse width		5	140	70		ns
		10	80	40		
		15	70	35		
t _{setup} Setup time		5	50	25		ns
		10	30	15		
		15	20	10		
t _h Hold time		5	0	0		ns
		10	0	0		
		15	0	0		
t _{prop} Propagation delay times	Strobe to data out	5		130	260	ns
		10		70	140	
		15		50	100	
	Data in to data out	5		105	210	ns
		10		60	120	
		15		45	90	
	Reset to data out	5		90	180	ns
		10		50	100	
		15		40	80	
t _{prop} 3-state propagation delay times output high to high impedance		5		90	180	ns
		10		50	100	
		15		35	70	
t _{low} High impedance to output high		5		90	180	ns
		10		50	100	
		15		35	70	
t _{low} Output low to high impedance		5		90	180	ns
		10		50	100	
		15		35	70	

PARAMETER	TEST CONDITIONS	VALUES			UNIT	
		V_{DD} (V)	min.	typ.		max.
t_{pZL} High impedance to output low		5 10 15		90 50 35	180 100 70	ns

LOGIC DIAGRAM (A Section)

1 of 4 identical latches with common output disable, reset and strobe



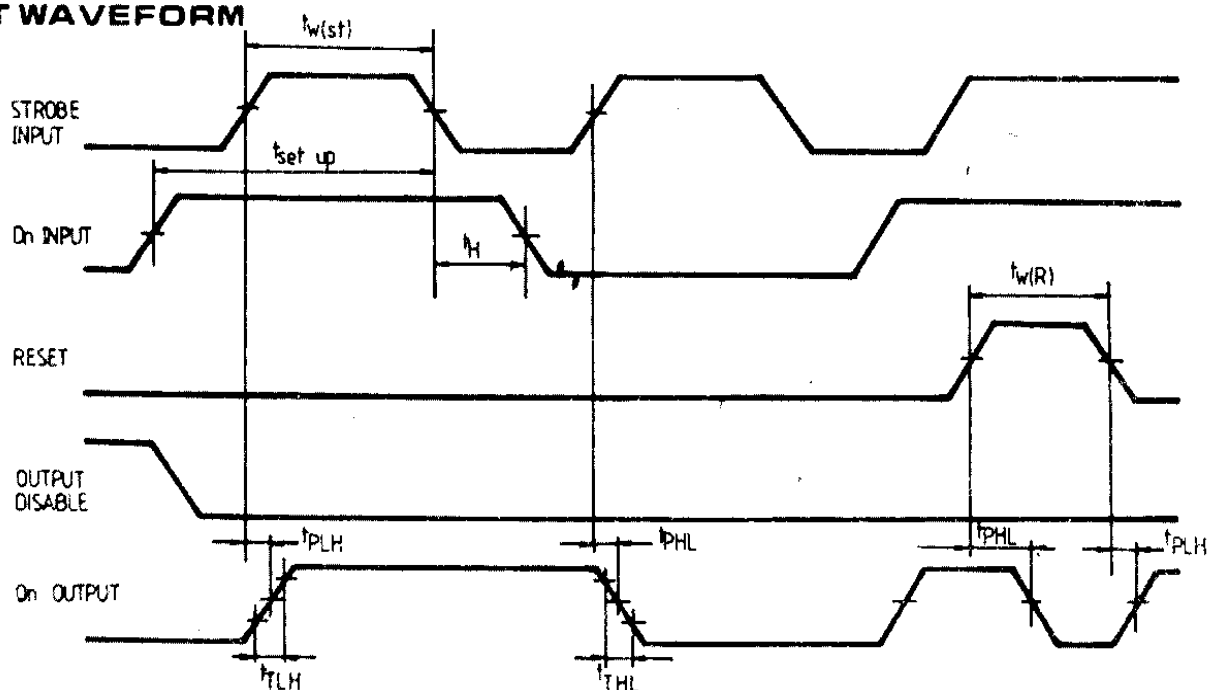
TRUTH TABLE

RESET	DISAB	STROBE	D INPUT	Q INPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	Latched
1	0	X	X	0
X	1	X	X	Z

1 = High level
0 = Low level

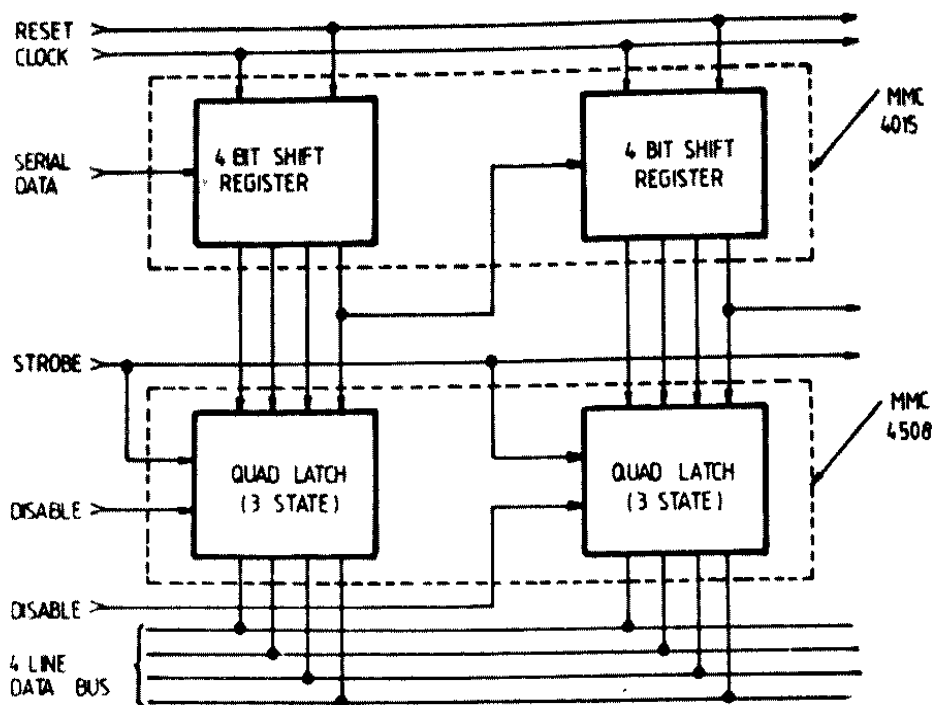
X = Don't care
Z = High impedance

TEST WAVEFORM



TYPICAL APPLICATIONS

Bus register



Dual multiplexed bus register with function select

