

# 16-bit Microcontroller

CMOS

## F<sup>2</sup>MC-16LX MB90820B Series

### MB90822B/823B/F822B/F823B/F828B/V820B

#### ■ DESCRIPTION

The MB90820B series is a line of general-purpose, Fujitsu 16-bit microcontrollers designed for process control applications which require high-speed real-time processing, such as consumer products.

While inheriting the AT architecture of the F<sup>2</sup>MC family, the instruction set for the F<sup>2</sup>MC-16LX CPU core of the MB90820B series incorporates additional instructions for high-level languages, supports extended addressing modes, and contains enhanced multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, the MB90820B series has an on-chip 32-bit accumulator which enables processing of long-word data.

The peripheral resources integrated in the MB90820B series include : an 8/10-bit A/D converter, 8-bit D/A converters, UARTs (SCI) 0, 1, multi-functional timer (16-bit free-run timer, input capture units (ICUs) 0 to 3, output compare units (OCUs) 0 to 5, 16-bit PPG timer 0, waveform generator), 16-bit PPG timer 1, 2, PWC 0, 1, 16-bit reload timer 0, 1 and DTP/external interrupt.

Note : F<sup>2</sup>MC is the abbreviation of FUJITSU Flexible Microcontroller.

#### ■ FEATURES

- Minimum execution time of instruction : 42 ns / 4 MHz oscillation (uses PLL clock multiplication) maximum multiplier = 6
- Maximum memory space 16 M bytes, Linear/bank access
- Instruction set optimized for controller applications
  - Supported data types : bit, byte, word, and long-word types
  - Standard addressing modes : 23 types
  - 32-bit accumulator enhancing high-precision operations
  - Signed multiplication/division instructions and enhanced RETI instructions

(Continued)

For the information for microcontroller supports, see the following web site.

<http://edevic.fujitsu.com/micom/en-support/>

# MB90820B Series

(Continued)

- Enhanced high level language (C) and multi-tasking support instructions
  - Use of a system stack pointer
  - Symmetrical instruction set and barrel shift instructions
- Program patch function (for two address pointers)
- Increased execution speed : 4-byte instruction queue
- Powerful interrupt function
  - Up to eight priority levels programmable
  - External interrupt inputs : 8 channels
- Automatic data transmission function independent of CPU operation
  - Up to 16 channels for the extended intelligent I/O service
  - DTP request inputs : 8 channels
- Internal ROM
  - Flash memory : 64 K/128 K bytes with flash security
  - MASK ROM : 64 K/128 K bytes
- Internal RAM
  - Evaluation product : 16 K bytes
  - Flash memory : 4 K/8 K bytes
  - MASK ROM : 4 K bytes
- General-purpose ports
  - Up to 66 channels (ports where pull-up resistor can be configured : 32 channels)
- A/D Converter (RC) : 16 channels
  - 8/10-bit resolution selectable
  - Conversion time : Min 3  $\mu$ s (24 MHz operation, including sampling time)
- 8-bit D/A Converter : 2 channels
- UART : 2 channels
- 16-bit PPG timer : 3 channels
  - Mode switching function provided (PWM mode or one-shot mode)
  - ch.0 can be worked with multi-functional timer or independently
- 16-bit reload timer : 2 channels
- 16-bit PWC timer : 2 channels
- Clock supervisor
- Multi-functional timer
  - Input capture : 4 channels
  - Output compare with selectable buffer : 6 channels
  - Free-run timer with up or up-down mode selection and selectable buffer: 1 channel
  - 16-bit PPG timer : 1 channel
  - Waveform generator : (16-bit timer : 3 channels, 3-phase waveform or dead time)
- Time-base timer/watchdog timer : 18-bit
- Low-power consumption mode :
  - Sleep mode
  - Stop mode
  - CPU intermittent operation mode
- Package :
  - LQFP-80 (FPT-80P-M21 : 0.50 mm pitch)
  - LQFP-80 (FPT-80P-M22 : 0.65 mm pitch)
  - QFP-80 (FPT-80P-M06 : 0.80 mm pitch)
- CMOS technology

# MB90820B Series

## ■ PRODUCT LINEUP

Part number Item	MB90V820B	MB90F822B	MB90F823B	MB90F828B	MB90822B	MB90823B
Classification	Evaluation product	Flash memory product with flash security			MASK ROM product	
ROM size	—	64 K bytes	128 K bytes	128 K bytes	64 K bytes	128 K bytes
RAM size	16 K bytes	4 K bytes		8 K bytes	4 K bytes	
CPU function	Number of instruction : 351 Minimum execution time : 42 ns / 4 MHz (PLL × 6) Addressing mode : 23 Data bit length : 1, 8, 16 bits Maximum memory space: 16 M bytes					
I/O port	I/O port (CMOS) : 66					
PWC	Pulse width counter timer : 2 channels Timer function (select the counter timer from three internal clocks) Various pulse width measuring function (“H” pulse width, “L” pulse width, rising edge to falling edge period, falling edge to rising edge period, rising edge to rising edge period and falling edge to falling edge period)					
UART	UART : 2 channels With full-duplex double buffer (8-bit length) Clock asynchronous or clock synchronized transmission (with start and stop bits) can be selected and used. Transmission can be one-to-one (bidirectional communication) or one-to-n (master-slave communication).					
16-bit reload timer	Reload timer : 2 channels Reload mode, single-shot mode or event count mode selectable					
16-bit PPG timer	PPG timer : 3 channels PWM mode or single-shot mode selectable Ch.0 can be worked with multi-functional timer or independently.					
Multi-functional timer (for AC/DC motor control)	16-bit free-run timer with up or up-down mode selection and buffer : 1 channel 16-bit output compare : 6 channels 16-bit input capture : 4 channels 16-bit PPG timer : 1 channel Waveform generator (16-bit timer : 3 channels, 3-phase waveform or dead time)					
8/10-bit A/D converter	8/10-bit resolution (16 channels) Conversion time : Min 3 μs (24 MHz internal clock, including sampling time)					
8-bit D/A converter	8-bit resolution (2 channels)					
DTP/External interrupt	8 independent channels Interrupt trigger : Rising edge, falling edge, “L” level or “H” level					
Clock supervisor	No		Yes		No	
Low-power consumption	Stop mode / Sleep mode / CPU intermittent operation mode					

(Continued)

# MB90820B Series

(Continued)

Part number Item	MB90V820B	MB90F822B	MB90F823B	MB90F828B	MB90822B	MB90823B
Package	PGA-299	LQFP-80 (FPT-80P-M21 : 0.50 mm pitch) LQFP-80 (FPT-80P-M22 : 0.65 mm pitch) QFP-80 (FPT-80P-M06 : 0.80 mm pitch)				
Power supply voltage for operation	4.5 V to 5.5 V*1	3.5 V to 5.5 V : Normal operation when A/D converter and D/A converter are not used 4.0 V to 5.5 V : Normal operation when D/A converter is not used 4.5 V to 5.5 V : Normal operation when A/D converter and D/A converter are used				
Process	CMOS					
Emulator power supply*2	Included	—				

\*1 : MB90V820B is operating guaranteed temperature 0 °C to + 25 °C.

\*2 : Configured by a jumper switch (TOOL VCC) when emulator (MB2147-01) is used.  
Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply switching) about details.

## ■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90V820B	MB90F822B	MB90F823B	MB90F828B	MB90822B	MB90823B
PGA-299	○	X	X	X	X	X
FPT-80P-M21	X	○	○	○	○	○
FPT-80P-M22	X	○	○	○	○	○
FPT-80P-M06	X	○	○	○	○	○

○ : Available

X : Not available

Note: For more information about each package, refer to “■ PACKAGE DIMENSIONS”.

## ■ DIFFERENCES AMONG PRODUCTS

### Memory Size

In evaluation with an evaluation product, note the difference between the evaluation product and the product actually used. The following items must be taken into consideration.

- The MB90V820B does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.
- In the MB90V820B, images from FF8000<sub>H</sub> to FFFFFFF<sub>H</sub> are mapped to bank 00, and FE0000<sub>H</sub> to FF7FFF<sub>H</sub> are mapped to bank FE and bank FF only. (This setting can be changed by configuring the development tool.)
- In the MB90822B/F822B/F828B, images from FF8000<sub>H</sub> to FFFFFFF<sub>H</sub> are mapped to bank 00, and FF0000<sub>H</sub> to FF7FFF<sub>H</sub> are mapped to bank FF only. In the MB90823B/F823B/F828B, images from FF8000<sub>H</sub> to FFFFFFF<sub>H</sub> are mapped to bank 00, and FE0000<sub>H</sub> to FF7FFF<sub>H</sub> are mapped to bank FE and bank FF only.

### Clock Supervisor Function

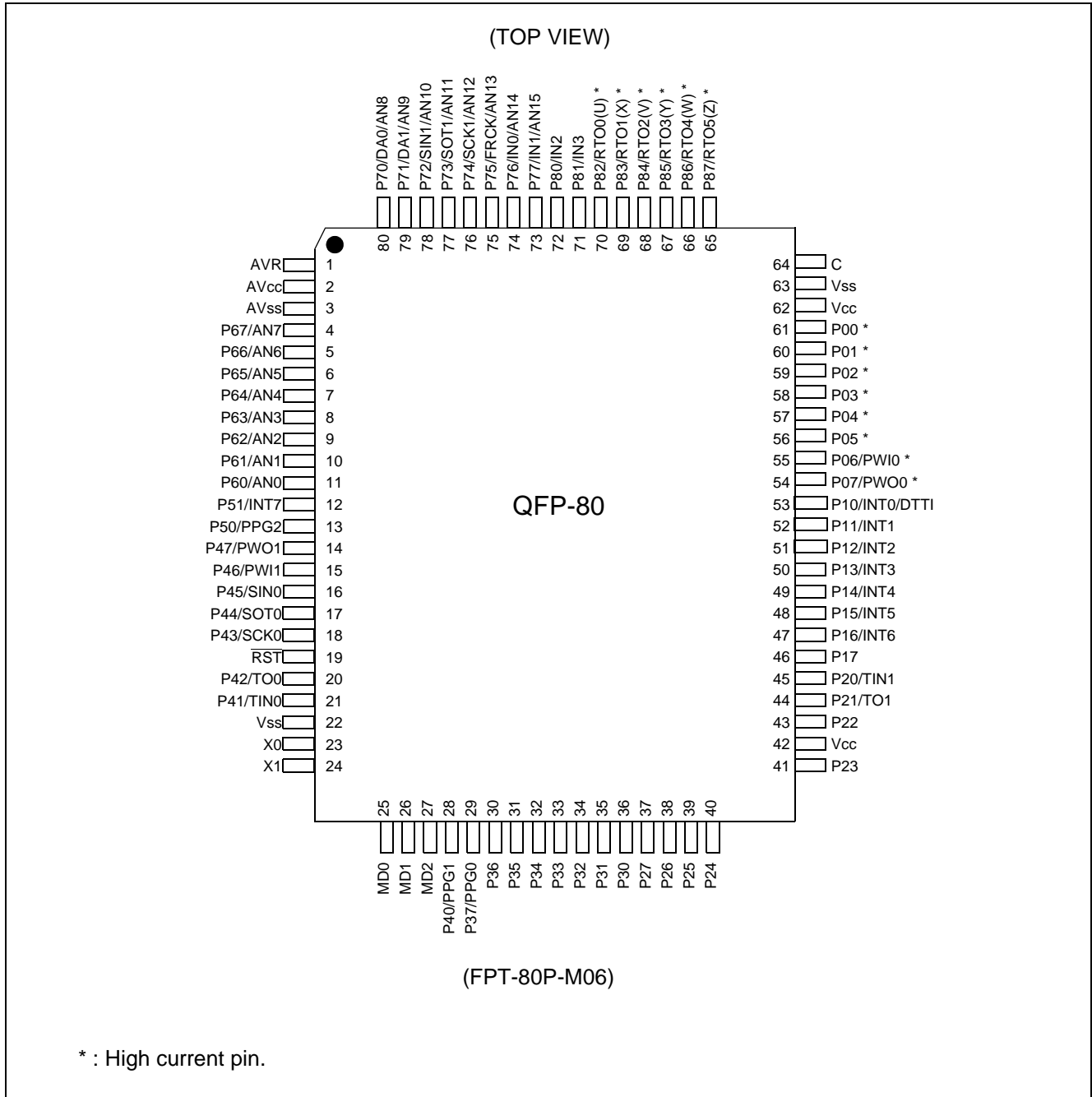
The clock supervisor is built-in in MB90F828B only. Note that the evaluation products and products actually used are different when evaluating evaluation products. Please contact the sales representatives for more information on evaluation of this function.

### Modify ROM data

The registers include this function between 001FF0<sub>H</sub> and 001FF5<sub>H</sub> which overlap the RAM area of MB90F828B. Do not access to the RAM when using this function in MB90F828B.

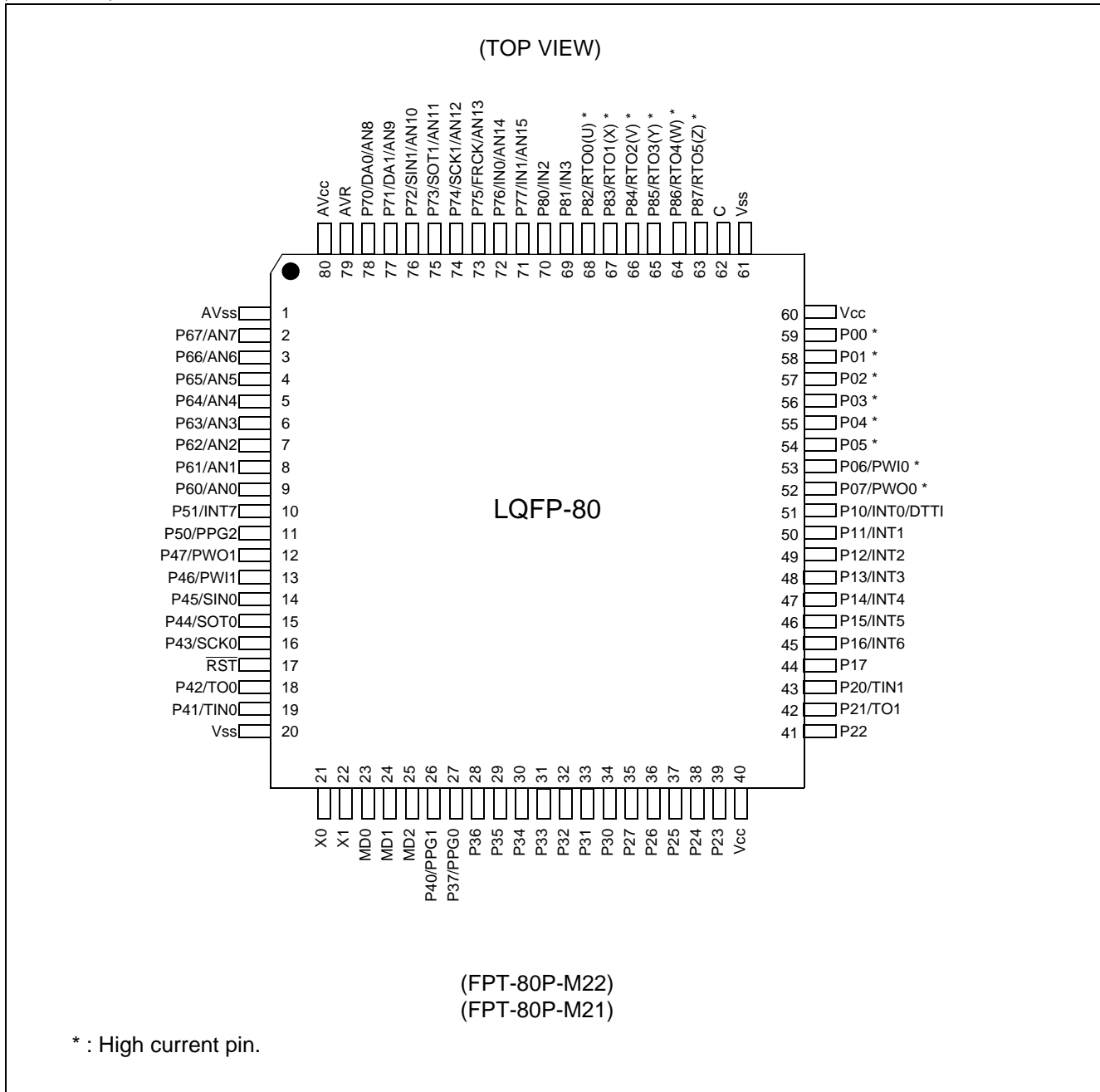
# MB90820B Series

## PIN ASSIGNMENT



(Continued)

(Continued)



# MB90820B Series

## ■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit *3	Pin status during reset	Function
LQFP *1	QFP *2				
21, 22	23, 24	X0,X1	A	Oscillating	Oscillation pins.
17	19	$\overline{\text{RST}}$	B	Reset input	External reset input pin.
59 to 54	61 to 56	P00 to P05	C	Port input	General-purpose I/O ports.
53	55	P06	C		General-purpose I/O port.
		PWIO			PWC ch.0 signal input pin.
52	54	P07	C		General-purpose I/O port.
		PW00			PWC ch.0 signal output pin.
51	53	P10	D		General-purpose I/O port.
		INT0			External interrupt request input ch.0 pin.
		DTTI			RTO0 to RTO5 pins for fixed-level input. This function is enabled when the waveform generator specifies its input bits.
50 to 45	52 to 47	P11 to P16	D		General-purpose I/O ports.
		INT1 to INT6			External interrupt request input ch.1 to ch.6 pins.
44	46	P17	D		General-purpose I/O port.
43	45	P20	D		General-purpose I/O port.
		TIN1			External clock input pin for reload timer ch.1.
42	44	P21	D		General-purpose I/O port.
		TO1			Event output pin for reload timer ch.1.
41, 39 to 35	43, 41 to 37	P22 to P27	D		General-purpose I/O ports.
34 to 28	36 to 30	P30 to P36	E		General-purpose I/O ports.
27	29	P37	E		General-purpose I/O port.
		PPG0			Output pin for PPG timer ch.0.
26	28	P40	F		General-purpose I/O port.
		PPG1		Output pin for PPG timer ch.1.	
19	21	P41	F	General-purpose I/O port.	
		TIN0		External clock input pin for reload timer ch.0.	
18	20	P42	F	General-purpose I/O port.	
		TO0		Event output pin for reload timer ch.0.	

(Continued)



# MB90820B Series

Pin no.		Pin name	I/O circuit *3	Pin status during reset	Function	
LQFP *1	QFP *2					
16	18	P43	F	Port Input	General-purpose I/O port.	
		SCK0			Serial clock I/O pin for UART ch.0.	
15	17	P44	F		General-purpose I/O port.	
		SOT0			Serial data output pin for UART ch.0.	
14	16	P45	G		General-purpose I/O port.	
		SIN0			Serial data input pin for UART ch.0.	
13	15	P46	F		General-purpose I/O port.	
		PWI1			PWC ch.1 signal input pin.	
12	14	P47	F		General-purpose I/O port.	
		PWO1			PWC ch.1 signal output pin.	
11	13	P50	F		General-purpose I/O port.	
		PPG2			Output pin for PPG timer ch.2.	
10	12	P51	F		General-purpose I/O port.	
		INT7			External interrupt request input ch.7 pin.	
9 to 2	11 to 4	P60 to P67	H		Analog input	General-purpose I/O ports.
		AN0 to AN7				A/D converter analog input pins.
78, 77	80, 79	P70, P71	I	General-purpose I/O ports.		
		DA0, DA1		D/A converter analog output pins.		
		AN8, AN9		A/D converter analog input pins.		
76	78	P72	J	General-purpose I/O port.		
		SIN1		Serial data input pin for UART ch.1.		
		AN10		A/D converter analog input pin.		
75	77	P73	K	General-purpose I/O port.		
		SOT1		Serial data output pin for UART ch.1.		
		AN11		A/D converter analog input pin.		
74	76	P74	K	General-purpose I/O port.		
		SCK1		Serial clock I/O pin for UART ch.1.		
		AN12		A/D converter analog input pin.		
73	75	P75	K	General-purpose I/O port.		
		FRCK		External clock input pin for free-run timer.		
		AN13		A/D converter analog input pin.		

(Continued)

# MB90820B Series

(Continued)

Pin no.		Pin name	I/O circuit *3	Pin status during reset	Function
LQFP *1	QFP *2				
72, 71	74, 73	P76, P77	K	Analog input	General-purpose I/O ports.
		IN0, IN1			Trigger input pins for input capture ch.0, ch.1.
		AN14, AN15			A/D converter analog input pins.
70, 69	72, 71	P80, P81	F	Port input	General-purpose I/O ports.
		IN2, IN3			Trigger input pins for input capture ch.2, ch.3.
68 to 63	70 to 65	P82 to P87	L	Port input	General-purpose I/O ports.
		RTO0 (U) to RTO5 (Z)			Waveform generator output pins. (U) to (Z) represent the coils for controlling a 3-phase motor.
25	27	MD2	M	Mode input	Input pin for operation mode specification.
24, 23	26, 25	MD1, MD0	N		Input pins for operation mode specification.
80	2	AV <sub>CC</sub>	—	—	Analog power supply pin.
79	1	AVR	—		Vref + pin for the A/D converter. Vref - is fixed to AV <sub>SS</sub> internally.
1	3	AV <sub>SS</sub>	—		Analog power supply (Ground) pin.
20, 61	22, 63	V <sub>SS</sub>	—		Power (Ground) pins.
40, 60	42, 62	V <sub>CC</sub>	—		Power pins.
62	64	C	—		Connect pin for smoothing capacitor to stabilize internal power supply.

\*1 : FPT-80P-M21,  
FPT-80P-M22

\*2 : FPT-80P-M06

\*3 : Refer to "■ I/O CIRCUIT TYPE" for details on the I/O circuit types.

## I/O CIRCUIT TYPE

Classification	Type	Remarks
A		<p>Oscillation feedback resistor : approx. 1 MΩ</p>
B		<ul style="list-style-type: none"> <li>• Hysteresis input</li> <li>• Pull-up resistor : approx. 50 kΩ</li> </ul>
C		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Selectable pull-up resistor : approx. 50 kΩ</li> <li>• <math>I_{OL} = 12 \text{ mA}</math></li> </ul>
D		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Selectable pull-up resistor : approx. 50 kΩ</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
E		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• With pull-up control</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>

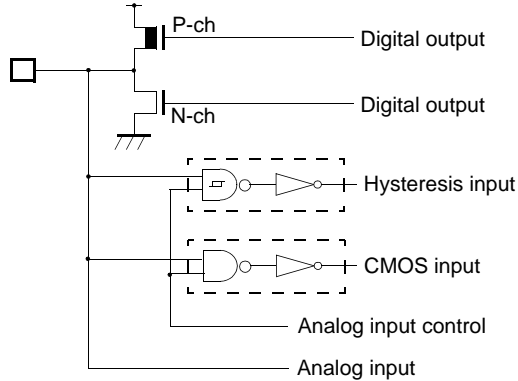
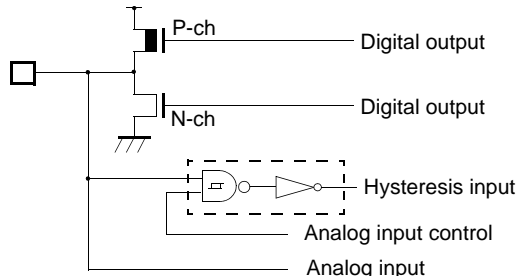
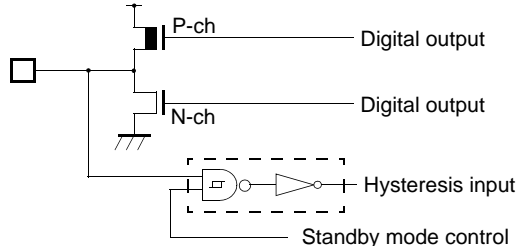
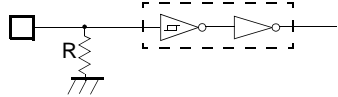
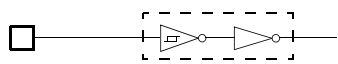
(Continued)

# MB90820B Series

Classification	Type	Remarks
F	<p>P-ch — Digital output N-ch — Digital output Hysteresis input Standby mode control</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
G	<p>P-ch — Digital output N-ch — Digital output Hysteresis input CMOS input Standby mode control</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• CMOS input (selectable for UART ch.0 data input pin)</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
H	<p>P-ch — Digital output N-ch — Digital output CMOS input Analog input control Analog input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Analog input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
I	<p>P-ch — Digital output N-ch — Digital output Hysteresis input Analog I/O control Analog output Analog input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Analog output</li> <li>• Analog input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>

(Continued)

(Continued)

Classification	Type	Remarks
J	 <p>P-ch — Digital output N-ch — Digital output Hysteresis input CMOS input Analog input control Analog input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• CMOS input (selectable for UART ch.1 data input pin)</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
K	 <p>P-ch — Digital output N-ch — Digital output Hysteresis input Analog input control Analog input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Analog input</li> <li>• <math>I_{OL} = 4 \text{ mA}</math></li> </ul>
L	 <p>P-ch — Digital output N-ch — Digital output Hysteresis input Standby mode control</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• <math>I_{OL} = 12 \text{ mA}</math></li> </ul>
M	 <p>R Ground</p>	<p>MASK ROM / evaluation product</p> <ul style="list-style-type: none"> <li>• Hysteresis input</li> <li>• Pull-down resistor : approx. <math>50 \text{ k}\Omega</math></li> </ul> <p>Flash memory product</p> <ul style="list-style-type: none"> <li>• CMOS input</li> <li>• No pull-down resistor</li> </ul>
N		<p>MASK ROM / evaluation product</p> <ul style="list-style-type: none"> <li>• Hysteresis input</li> </ul> <p>Flash memory product</p> <ul style="list-style-type: none"> <li>• CMOS input</li> </ul>

# MB90820B Series

## ■ HANDLING DEVICES

Special care is required for the following when handling the device :

- Preventing latch-up
- Stabilization of supply voltage
- Treatment of unused pins
- Using external clock
- Power supply pins ( $V_{CC}$  /  $V_{SS}$  )
- Pull-up/pull-down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter
- Notes on turning the power on
- Notes on During Operation of PLL Clock Mode

### 1. Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  and  $V_{SS}$  pins.
- The  $AV_{CC}$  power supply is applied before the  $V_{CC}$  voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

In using the devices, take sufficient care to avoid exceeding maximum ratings.

For the same reason, also be careful not to let the analog power-supply voltage ( $AV_{CC}$ ,  $AVR$ ) exceed the digital power-supply voltage.

### 2. Stabilization of supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified  $V_{CC}$  supply voltage operation range. Therefore, the  $V_{CC}$  supply voltage should be stabilized.

For reference, the supply voltage should be controlled so that  $V_{CC}$  ripple variations (peak-to-peak values) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard  $V_{CC}$  supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

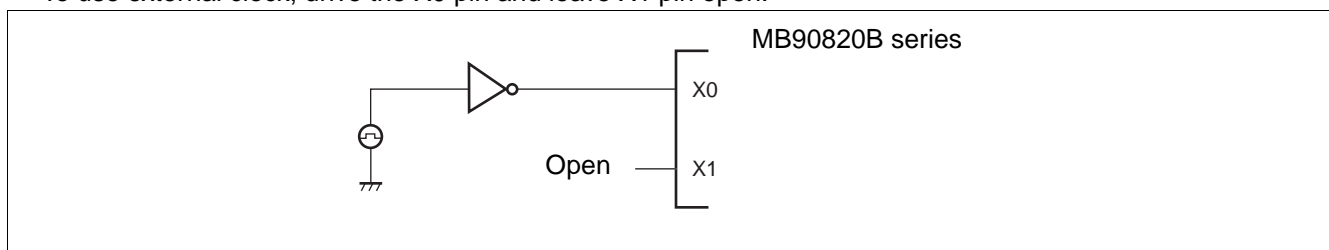
### 3. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 k $\Omega$ .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

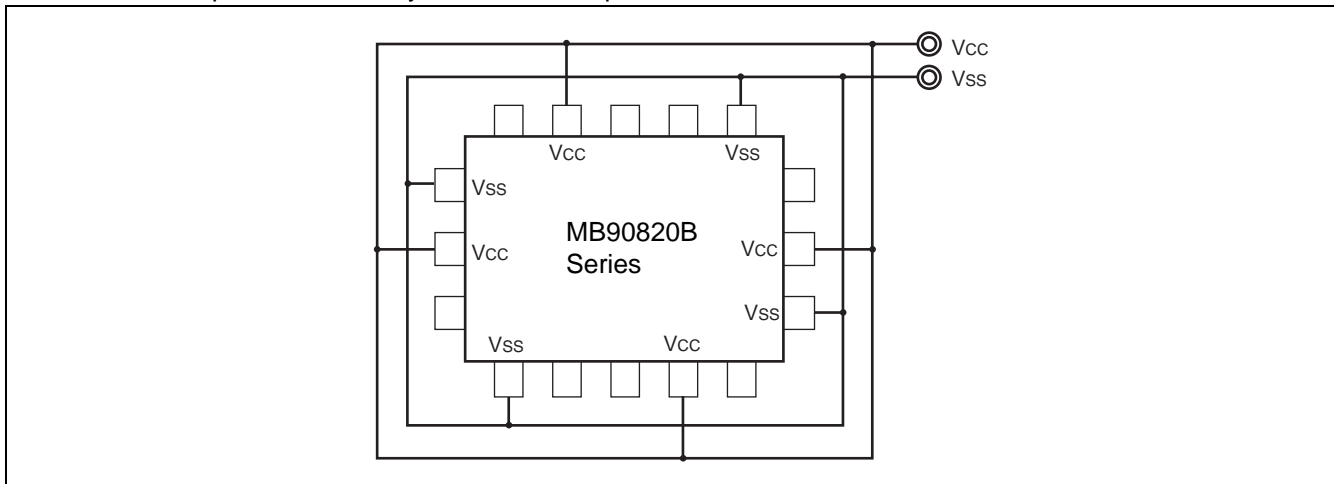
### 4. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



## 5. Power supply pins ( $V_{CC}/V_{SS}$ )

- If there are multiple  $V_{CC}$  and  $V_{SS}$  pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the  $V_{CC}$  and  $V_{SS}$  pins to the power supply and ground externally.
- Connect  $V_{CC}$  and  $V_{SS}$  pins to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1  $\mu\text{F}$  as a bypass capacitor between  $V_{CC}$  and  $V_{SS}$  pins in the vicinity of  $V_{CC}$  and  $V_{SS}$  pins of the device.



## 6. Pull-up/pull-down resistors

The MB90820B series does not support internal pull-up/pull-down resistors option (Port 0 to Port 3 : built-in pull-up resistors) . Use external components where needed.

## 7. Crystal oscillator circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit do not cross the lines of other circuits while you design a printed circuit board.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

## 8. Turning-on sequence of power supply to A/D converter and D/A converter, and analog inputs

Make sure to turn on the A/D converter power supply, D/A converter power supply ( $AV_{CC}$ ,  $AVRH$ ,  $AVR$ ) and analog inputs ( $AN0$  to  $AN15$ ) after turning-on the digital power supply ( $V_{CC}$ ).

Turn-off the digital power after turning off the A/D converter power supply, D/A converter power supply, and analog inputs. In this case, make sure that the voltage not exceed  $AVR$  or  $AV_{CC}$  (turning on/off the analog and digital power supplies simultaneously is acceptable).

## 9. Pin connections when A/D converter and D/A converter are unused

When the A/D converter and D/A converter are not used, connect  $AV_{CC} = V_{CC}$ ,  $AV_{SS} = AVRH = AVR = V_{SS}$ .

# MB90820B Series

## 10. Notes on turning the power on

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power on at 50  $\mu$ s or more (0.2 V to 2.7 V) .

## 11. Notes on During Operation of PLL Clock Mode

If the PLL clock mode is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit within the PLL even if the external oscillator is disconnected or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

## 12. Internal CR Oscillation Circuit

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Oscillation frequency	$f_{RC}$	50	100	200	kHz
Oscillation stabilization waiting time	$t_{stab}$	—	—	100	$\mu$ s



## ■ SECTOR CONFIGURATION OF FLASH MEMORY

The flash memory has the sector configuration illustrated below. The addresses in the illustration are the upper and lower addresses of each sector.

When 512K bits flash memory is accessed from the CPU, SA0 to SA3 are allocated in the FF bank.

Flash memory	CPU address	*Writer address
SA3 (16K bytes)	FFFFFF <sub>H</sub>	7FFFF <sub>H</sub>
	FFC000 <sub>H</sub>	7C000 <sub>H</sub>
SA2 (8K bytes)	FFBFFF <sub>H</sub>	7BFFF <sub>H</sub>
	FFA000 <sub>H</sub>	7A000 <sub>H</sub>
SA1 (8K bytes)	FF9FFF <sub>H</sub>	79FFF <sub>H</sub>
	FF8000 <sub>H</sub>	78000 <sub>H</sub>
SA0 (32K bytes)	FF7FFF <sub>H</sub>	77FFF <sub>H</sub>
	FF0000 <sub>H</sub>	70000 <sub>H</sub>

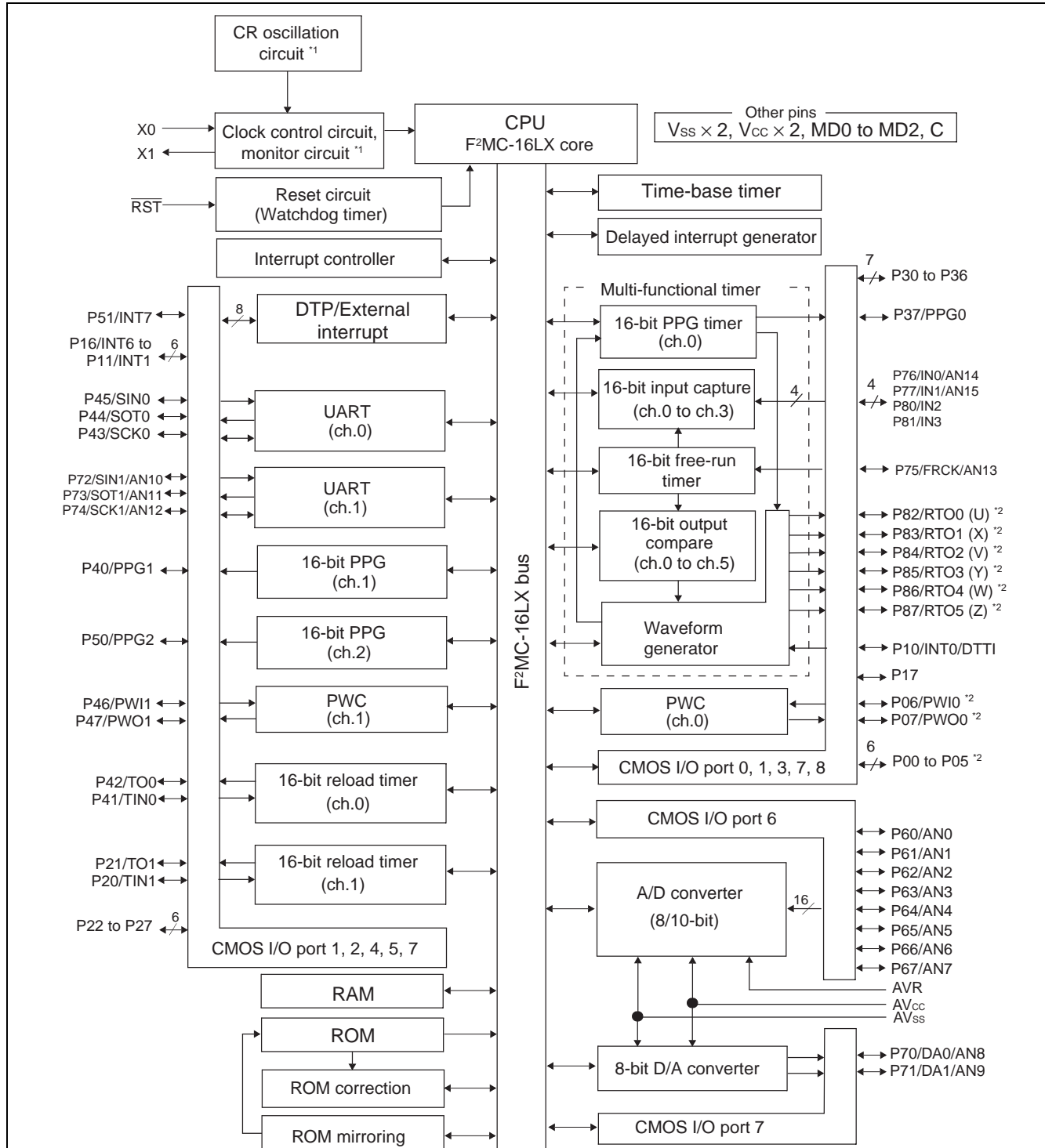
When 1024K bits flash memory is accessed from the CPU, SA0 to SA4 are allocated in the FE and FF bank.

Flash memory	CPU address	*Writer address
SA4 (16K bytes)	FFFFFF <sub>H</sub>	7FFFF <sub>H</sub>
	FFC000 <sub>H</sub>	7C000 <sub>H</sub>
SA3 (8K bytes)	FFBFFF <sub>H</sub>	7BFFF <sub>H</sub>
	FFA000 <sub>H</sub>	7A000 <sub>H</sub>
SA2 (8K bytes)	FF9FFF <sub>H</sub>	79FFF <sub>H</sub>
	FF8000 <sub>H</sub>	78000 <sub>H</sub>
SA1 (32K bytes)	FF7FFF <sub>H</sub>	77FFF <sub>H</sub>
	FF0000 <sub>H</sub>	70000 <sub>H</sub>
SA0 (64K bytes)	FEFFFF <sub>H</sub>	6FFFF <sub>H</sub>
	FE0000 <sub>H</sub>	60000 <sub>H</sub>

\* : The writer address is the address corresponding to the CPU address when writing data from a parallel flash memory writer. Use the writer address when programming or erasing using a general-purpose parallel writer.

# MB90820B Series

## ■ BLOCK DIAGRAM

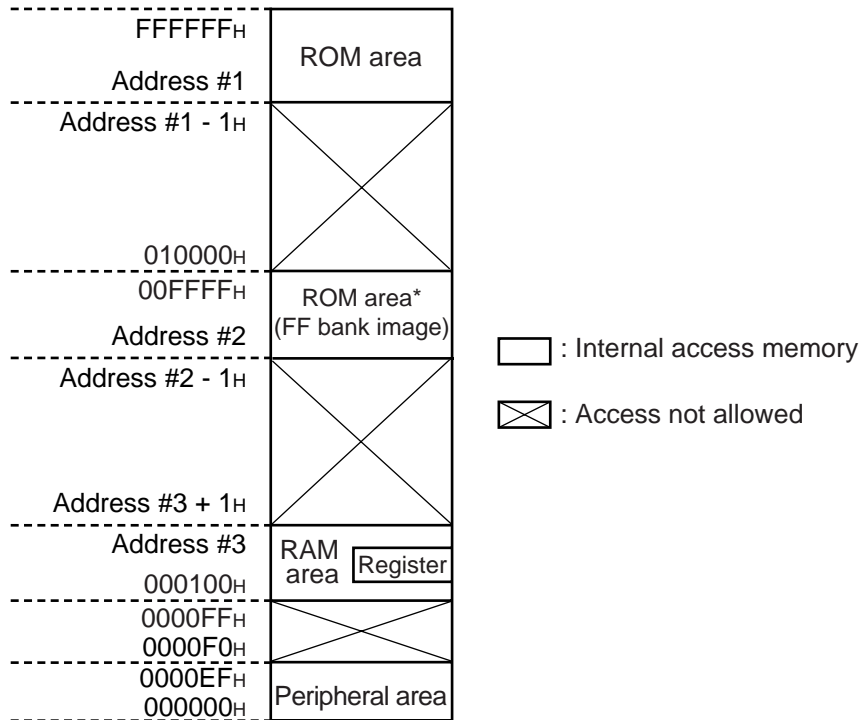


Note : P00 to P07, P10 to P17, P20 to P27 and P30 to P37: With build-in resistors that can be used as input pull-up resistors.

\*1 : MB90F828B

\*2 : High current drive pin.

## ■ MEMORY MAP



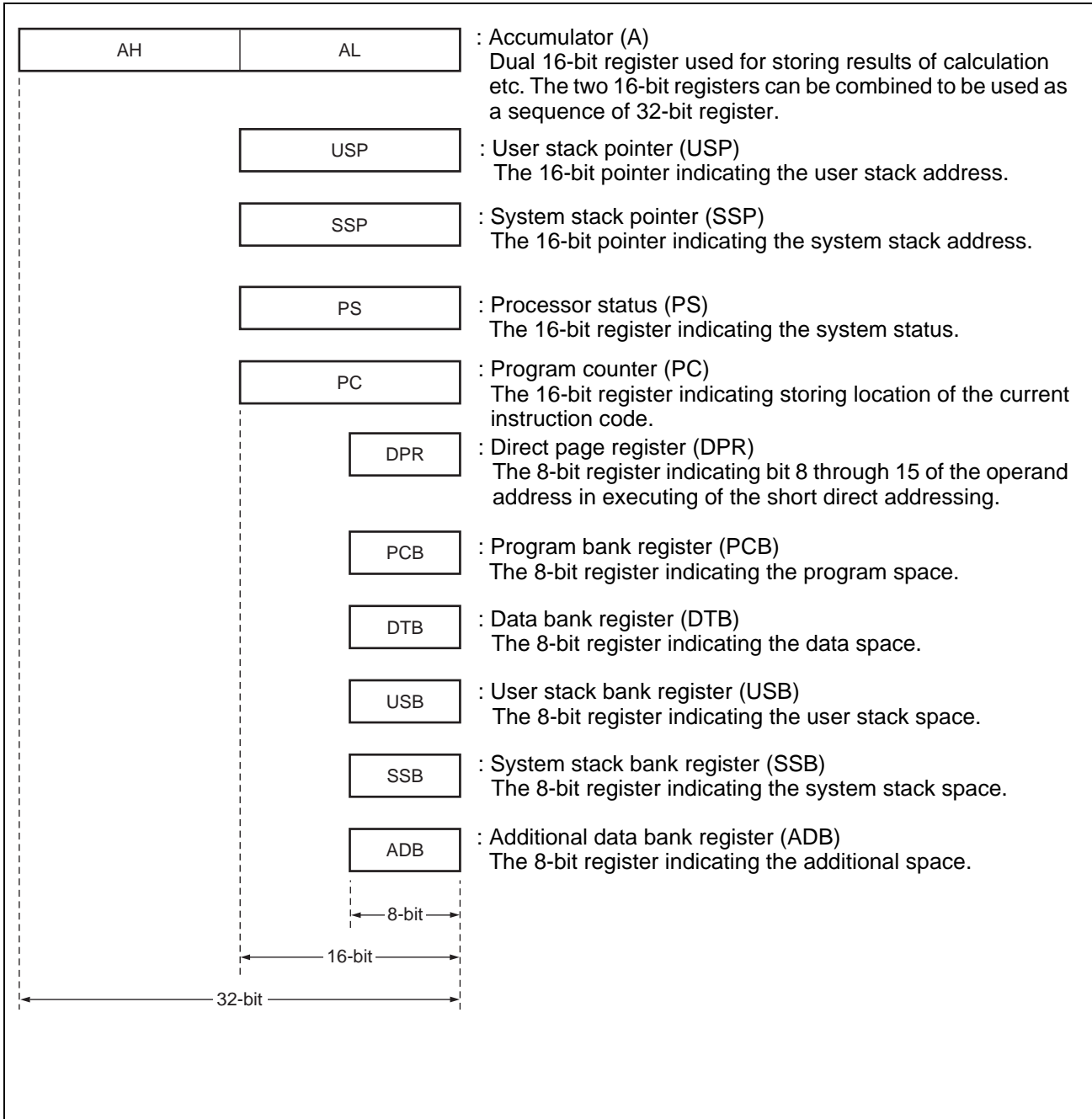
\* : In Single chip mode, the mirror function is supported.

Parts no.	Address#1	Address#2	Address#3
MB90822B	FF0000 <sub>H</sub>	008000 <sub>H</sub>	0010FF <sub>H</sub>
MB90823B	FE0000 <sub>H</sub>	008000 <sub>H</sub>	0010FF <sub>H</sub>
MB90F822B	FF0000 <sub>H</sub>	008000 <sub>H</sub>	0010FF <sub>H</sub>
MB90F823B	FE0000 <sub>H</sub>	008000 <sub>H</sub>	0010FF <sub>H</sub>
MB90F828B	FE0000 <sub>H</sub>	008000 <sub>H</sub>	0020FF <sub>H</sub>
MB90V820B	(FE0000 <sub>H</sub> )	008000 <sub>H</sub>	0040FF <sub>H</sub>

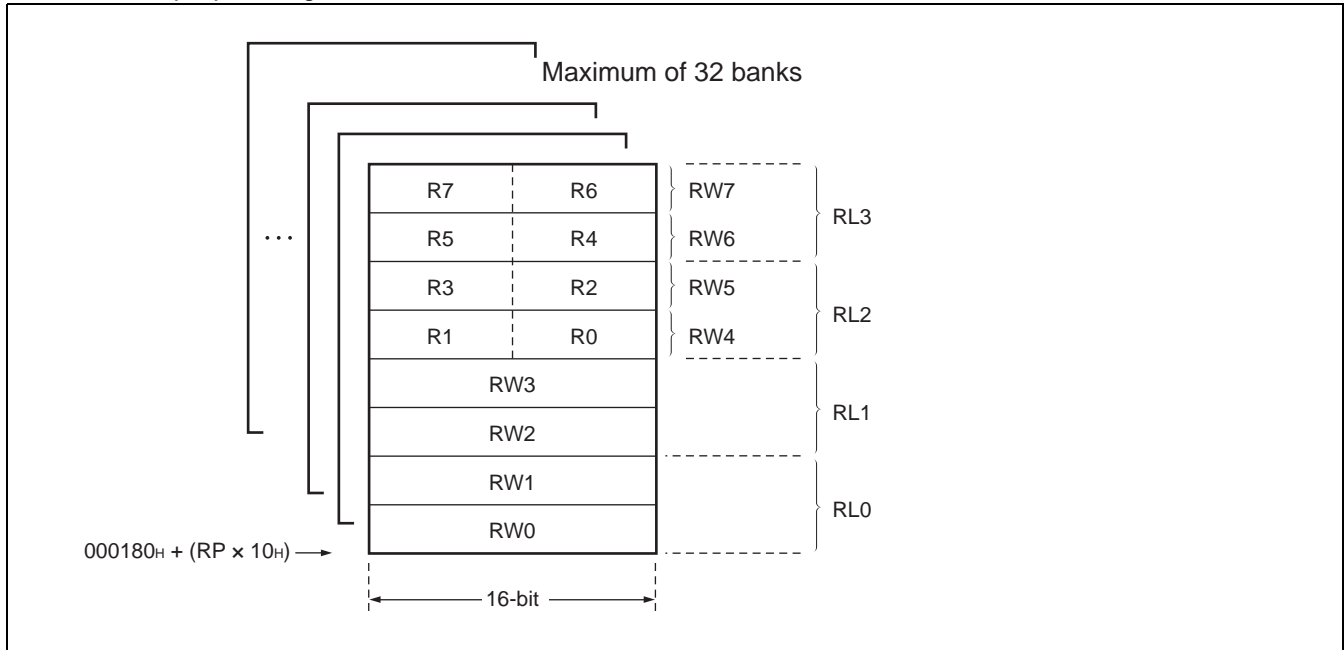
Note: The ROM data of bank FF is reflected to the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit is assigned to the same address, enabling reference of the table on the ROM without stating "far". For example, if an attempt has been made to access 00C000<sub>H</sub>, the contents of the ROM at FFC000<sub>H</sub> are accessed actually. Since the ROM area of the FF bank exceeds 32 K bytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF8000<sub>H</sub> to FFFFFFF<sub>H</sub> looks, therefore, as if it were the image for 008000<sub>H</sub> to 00FFFF<sub>H</sub>. Thus, it is recommended that the ROM data table be stored in the area of FF8000<sub>H</sub> to FFFFFFF<sub>H</sub>.

## ■ F<sup>2</sup>MC-16LX CPU PROGRAMMING MODEL

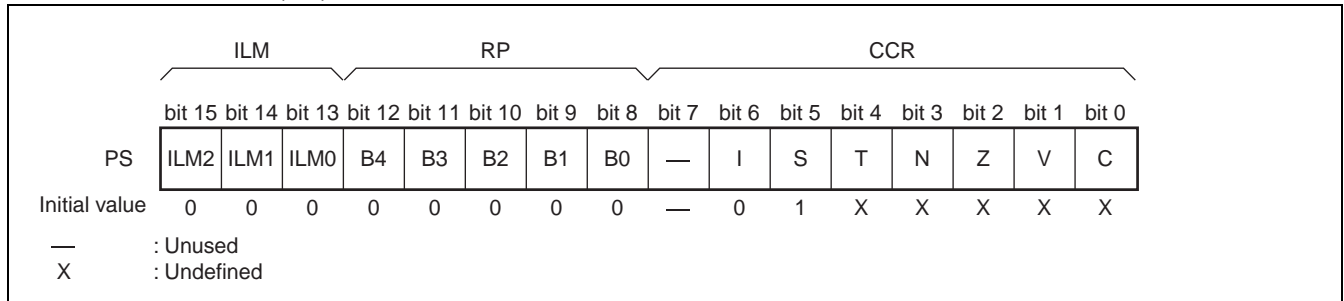
- Dedicated registers



- General-purpose registers



- Processor status (PS)



# MB90820B Series

## ■ I/O MAP

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000000 <sub>H</sub>	PDR0	Port 0 data register	R/W	R/W	Port 0	XXXXXXXX <sub>B</sub>
000001 <sub>H</sub>	PDR1	Port 1 data register	R/W	R/W	Port 1	XXXXXXXX <sub>B</sub>
000002 <sub>H</sub>	PDR2	Port 2 data register	R/W	R/W	Port 2	XXXXXXXX <sub>B</sub>
000003 <sub>H</sub>	PDR3	Port 3 data register	R/W	R/W	Port 3	XXXXXXXX <sub>B</sub>
000004 <sub>H</sub>	PDR4	Port 4 data register	R/W	R/W	Port 4	XXXXXXXX <sub>B</sub>
000005 <sub>H</sub>	PDR5	Port 5 data register	R/W	R/W	Port 5	XXXXXXXX <sub>B</sub>
000006 <sub>H</sub>	PDR6	Port 6 data register	R/W	R/W	Port 6	XXXXXXXX <sub>B</sub>
000007 <sub>H</sub>	PDR7	Port 7 data register	R/W	R/W	Port 7	XXXXXXXX <sub>B</sub>
000008 <sub>H</sub>	PDR8	Port 8 data register	R/W	R/W	Port 8	XXXXXXXX <sub>B</sub>
000009 <sub>H</sub> to 00000F <sub>H</sub>	Prohibited area					
000010 <sub>H</sub>	DDR0	Port 0 data direction register	R/W	R/W	Port 0	00000000 <sub>B</sub>
000011 <sub>H</sub>	DDR1	Port 1 data direction register	R/W	R/W	Port 1	00000000 <sub>B</sub>
000012 <sub>H</sub>	DDR2	Port 2 data direction register	R/W	R/W	Port 2	00000000 <sub>B</sub>
000013 <sub>H</sub>	DDR3	Port 3 data direction register	R/W	R/W	Port 3	00000000 <sub>B</sub>
000014 <sub>H</sub>	DDR4	Port 4 data direction register	R/W	R/W	Port 4	00000000 <sub>B</sub>
000015 <sub>H</sub>	DDR5	Port 5 data direction register	R/W	R/W	Port 5	XXXXXX00 <sub>B</sub>
000016 <sub>H</sub>	DDR6	Port 6 data direction register	R/W	R/W	Port 6	00000000 <sub>B</sub>
000017 <sub>H</sub>	DDR7	Port 7 data direction register	R/W	R/W	Port 7	00000000 <sub>B</sub>
000018 <sub>H</sub>	DDR8	Port 8 data direction register	R/W	R/W	Port 8	00000000 <sub>B</sub>
000019 <sub>H</sub> to 00001F <sub>H</sub>	Prohibited area					
000020 <sub>H</sub>	SMR0	Serial mode register ch.0	R/W	R/W	UART ch.0	00000000 <sub>B</sub>
000021 <sub>H</sub>	SCR0	Serial control register ch.0	W, R/W	W, R/W		0000100 <sub>B</sub>
000022 <sub>H</sub>	SIDR0 / SODR0	Serial input data register ch.0 / Serial output data register ch.0	R/W	R/W		XXXXXXXX <sub>B</sub>
000023 <sub>H</sub>	SSR0	Serial status register ch.0	R, R/W	R, R/W		00001000 <sub>B</sub>
000024 <sub>H</sub>	SMR1	Serial mode register ch.1	R/W	R/W	UART ch.1	00000000 <sub>B</sub>
000025 <sub>H</sub>	SCR1	Serial control register ch.1	W, R/W	W, R/W		0000100 <sub>B</sub>
000026 <sub>H</sub>	SIDR1 / SODR1	Serial input data register ch.1 / Serial output data register ch.1	R/W	R/W		XXXXXXXX <sub>B</sub>
000027 <sub>H</sub>	SSR1	Serial status register ch.1	R, R/W	R, R/W		00001000 <sub>B</sub>

(Continued)

# MB90820B Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000028 <sub>H</sub>	PWCSL1	PWC control status register ch.1	R/W	R/W	PWC timer ch.1	00000000 <sub>B</sub>
000029 <sub>H</sub>	PWCSH1		R, R/W	R, R/W		00000000 <sub>B</sub>
00002A <sub>H</sub>	PWC1	PWC data buffer register ch.1	—	R/W		XXXXXXXX <sub>B</sub>
00002B <sub>H</sub>						XXXXXXXX <sub>B</sub>
00002C <sub>H</sub>	DIV1	Divide ratio control register ch.1	R/W	R/W		XXXXXXXX00 <sub>B</sub>
00002D <sub>H</sub> , 00002E <sub>H</sub>	Prohibited area					
00002F <sub>H</sub>	PCKCR	PLL clock control register	W	W	PLL	XXXX0000 <sub>B</sub>
000030 <sub>H</sub>	ENIR	DTP / Interrupt enable register	R/W	R/W	DTP/ external interrupt ch.0 to ch.7	00000000 <sub>B</sub>
000031 <sub>H</sub>	EIRR	DTP / Interrupt cause register	R/W	R/W		XXXXXXXX <sub>B</sub>
000032 <sub>H</sub>	ELVRL	Request level setting register (lower byte)	R/W	R/W		00000000 <sub>B</sub>
000033 <sub>H</sub>	ELVRH	Request level setting register (higher byte)	R/W	R/W		00000000 <sub>B</sub>
000034 <sub>H</sub>	Prohibited area					
000035 <sub>H</sub>	CDCR0	Clock division ratio control register ch.0	R/W	R/W	Communication prescaler ch.0	00XXX000 <sub>B</sub>
000036 <sub>H</sub>	Prohibited area					
000037 <sub>H</sub>	CDCR1	Clock division ratio control register ch.1	R/W	R/W	Communication prescaler ch.1	00XXX000 <sub>B</sub>
000038 <sub>H</sub>	PDCR0	PPG down counter register ch.0	—	R	16-bit PPG timer ch.0	11111111 <sub>B</sub>
000039 <sub>H</sub>						11111111 <sub>B</sub>
00003A <sub>H</sub>	PCSR0	PPG cycle setting register ch.0	—	W		XXXXXXXX <sub>B</sub>
00003B <sub>H</sub>						XXXXXXXX <sub>B</sub>
00003C <sub>H</sub>	PDUT0	PPG duty setting register ch.0	—	W		XXXXXXXX <sub>B</sub>
00003D <sub>H</sub>						XXXXXXXX <sub>B</sub>
00003E <sub>H</sub>	PCNTL0	PPG control status register ch.0	R/W	R/W		XX000000 <sub>B</sub>
00003F <sub>H</sub>	PCNTH0		R/W	R/W		00000000 <sub>B</sub>
000040 <sub>H</sub>	PDCR1	PPG down counter register ch.1	—	R	16-bit PPG timer ch.1	11111111 <sub>B</sub>
000041 <sub>H</sub>						11111111 <sub>B</sub>
000042 <sub>H</sub>	PCSR1	PPG cycle setting register ch.1	—	W		XXXXXXXX <sub>B</sub>
000043 <sub>H</sub>						XXXXXXXX <sub>B</sub>
000044 <sub>H</sub>	PDUT1	PPG duty setting register ch.1	—	W		XXXXXXXX <sub>B</sub>
000045 <sub>H</sub>						XXXXXXXX <sub>B</sub>
000046 <sub>H</sub>	PCNTL1	PPG control status register ch.1	R/W	R/W		XX000000 <sub>B</sub>
000047 <sub>H</sub>	PCNTH1		R/W	R/W		00000000 <sub>B</sub>

(Continued)

# MB90820B Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value	
000048 <sub>H</sub>	PDCR2	PPG down counter register ch.2	—	R	16-bit PPG timer ch.2	11111111 <sub>B</sub>	
000049 <sub>H</sub>						11111111 <sub>B</sub>	
00004A <sub>H</sub>	PCSR2	PPG cycle setting register ch.2	—	W		XXXXXXXX <sub>B</sub>	
00004B <sub>H</sub>						XXXXXXXX <sub>B</sub>	
00004C <sub>H</sub>	PDUT2	PPG duty setting register ch.2	—	W		XXXXXXXX <sub>B</sub>	
00004D <sub>H</sub>						XXXXXXXX <sub>B</sub>	
00004E <sub>H</sub>	PCNTL2	PPG control status register ch.2	R/W	R/W		XX000000 <sub>B</sub>	
00004F <sub>H</sub>	PCNTH2		R/W	R/W		00000000 <sub>B</sub>	
000050 <sub>H</sub>	TMRR0	16-bit timer register ch.0	—	R/W	Waveform generator	XXXXXXXX <sub>B</sub>	
000051 <sub>H</sub>						XXXXXXXX <sub>B</sub>	
000052 <sub>H</sub>	TMRR1	16-bit timer register ch.1	—	R/W		XXXXXXXX <sub>B</sub>	
000053 <sub>H</sub>						XXXXXXXX <sub>B</sub>	
000054 <sub>H</sub>	TMRR2	16-bit timer register ch.2	—	R/W		XXXXXXXX <sub>B</sub>	
000055 <sub>H</sub>						XXXXXXXX <sub>B</sub>	
000056 <sub>H</sub>	DTCR0	16-bit timer control register ch.0	R/W	R/W		00000000 <sub>B</sub>	
000057 <sub>H</sub>	DTCR1	16-bit timer control register ch.1	R/W	R/W		00000000 <sub>B</sub>	
000058 <sub>H</sub>	DTCR2	16-bit timer control register ch.2	R/W	R/W		00000000 <sub>B</sub>	
000059 <sub>H</sub>	SIGCR	Waveform control register	R/W	R/W		00000000 <sub>B</sub>	
00005A <sub>H</sub>	CPCLRB / CPCLR	Compare clear buffer register/ Compare clear register	—	R/W		16-bit free-run timer	11111111 <sub>B</sub>
00005B <sub>H</sub>							11111111 <sub>B</sub>
00005C <sub>H</sub>	TCDT	Timer data register	—	R/W			00000000 <sub>B</sub>
00005D <sub>H</sub>							00000000 <sub>B</sub>
00005E <sub>H</sub>	TCCSL	Timer control status register (lower)	R/W	R/W			X0100000 <sub>B</sub>
00005F <sub>H</sub>	TCCSH	Timer control status register (upper)	R/W	R/W			00000000 <sub>B</sub>
000060 <sub>H</sub>	IPCP0	Input capture data register ch.0	—	R	16-bit input capture (ch.0 to ch.3)		XXXXXXXX <sub>B</sub>
000061 <sub>H</sub>							XXXXXXXX <sub>B</sub>
000062 <sub>H</sub>	IPCP1	Input capture data register ch.1	—	R		XXXXXXXX <sub>B</sub>	
000063 <sub>H</sub>						XXXXXXXX <sub>B</sub>	
000064 <sub>H</sub>	IPCP2	Input capture data register ch.2	—	R		XXXXXXXX <sub>B</sub>	
000065 <sub>H</sub>						XXXXXXXX <sub>B</sub>	
000066 <sub>H</sub>	IPCP3	Input capture data register ch.3	—	R		XXXXXXXX <sub>B</sub>	
000067 <sub>H</sub>						XXXXXXXX <sub>B</sub>	

(Continued)



# MB90820B Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000068 <sub>H</sub>	PICSL01	Input capture control status register ch.0,ch.1 (lower)	R/W	R/W	16-bit input capture (ch.0 to ch.3)	00000000 <sub>B</sub>
000069 <sub>H</sub>	PICSH01	PPG output control / Input capture control status register ch.0,ch.1 (upper)	R, R/W	R, R/W		00000000 <sub>B</sub>
00006A <sub>H</sub>	ICSL23	Input capture control status register ch.2,ch.3 (lower)	R/W	R/W		00000000 <sub>B</sub>
00006B <sub>H</sub>	ICSH23	Input capture control status register ch.2,ch.3 (upper)	R	R		XXXXXXXX00 <sub>B</sub>
00006C <sub>H</sub> to 00006E <sub>H</sub>	Prohibited area					
00006F <sub>H</sub>	ROMM	ROM mirroring function selection register	W	W	ROM mirroring function	XXXXXXXX1 <sub>B</sub>
000070 <sub>H</sub>	OCCPB0 / OCCP0	Output compare buffer register / Output compare register ch.0	—	R/W	Output compare (ch.0 to ch.5)	XXXXXXXX <sub>B</sub>
000071 <sub>H</sub>						XXXXXXXX <sub>B</sub>
000072 <sub>H</sub>	OCCPB1 / OCCP1	Output compare buffer register / Output compare register ch.1	—	R/W		XXXXXXXX <sub>B</sub>
000073 <sub>H</sub>						XXXXXXXX <sub>B</sub>
000074 <sub>H</sub>	OCCPB2 / OCCP2	Output compare buffer register / Output compare register ch.2	—	R/W		XXXXXXXX <sub>B</sub>
000075 <sub>H</sub>						XXXXXXXX <sub>B</sub>
000076 <sub>H</sub>	OCCPB3 / OCCP3	Output compare buffer register / Output compare register ch.3	—	R/W		XXXXXXXX <sub>B</sub>
000077 <sub>H</sub>						XXXXXXXX <sub>B</sub>
000078 <sub>H</sub>	OCCPB4 / OCCP4	Output compare buffer register / Output compare register ch.4	—	R/W		XXXXXXXX <sub>B</sub>
000079 <sub>H</sub>						XXXXXXXX <sub>B</sub>
00007A <sub>H</sub>	OCCPB5 / OCCP5	Output compare buffer register / Output compare register ch.5	—	R/W		XXXXXXXX <sub>B</sub>
00007B <sub>H</sub>						XXXXXXXX <sub>B</sub>
00007C <sub>H</sub>	OCS0	Compare control register ch.0	R/W	R/W		00001100 <sub>B</sub>
00007D <sub>H</sub>	OCS1	Compare control register ch.1	R/W	R/W		X1100000 <sub>B</sub>
00007E <sub>H</sub>	OCS2	Compare control register ch.2	R/W	R/W		00001100 <sub>B</sub>
00007F <sub>H</sub>	OCS3	Compare control register ch.3	R/W	R/W		X1100000 <sub>B</sub>
000080 <sub>H</sub>	OCS4	Compare control register ch.4	R/W	R/W		00001100 <sub>B</sub>
000081 <sub>H</sub>	OCS5	Compare control register ch.5	R/W	R/W		X1100000 <sub>B</sub>
000082 <sub>H</sub>	TMCSRL0	Timer control status register ch.0 (lower)	R/W	R/W	16-bit reload timer (ch.0)	00000000 <sub>B</sub>
000083 <sub>H</sub>	TMCSRH0	Timer control status register ch.0 (upper)	R/W	R/W		XXX10000 <sub>B</sub>
000084 <sub>H</sub> 000085 <sub>H</sub>	TMR0 / TMRD0	16 bit timer register ch.0 / 16-bit reload register ch.0	—	R/W		XXXXXXXX <sub>B</sub> XXXXXXXX <sub>B</sub>
000086 <sub>H</sub>	TMCSRL1	Timer control status register ch.1 (lower)	R/W	R/W	16-bit reload timer (ch.1)	00000000 <sub>B</sub>

(Continued)

# MB90820B Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000087 <sub>H</sub>	TMCSRH1	Timer control status register ch.1 (upper)	R/W	R/W	16-bit reload timer (ch.1)	XXX10000 <sub>B</sub>
000088 <sub>H</sub>	TMR1 /	16 bit timer register ch.1 / 16-bit reload register ch.1	—	R/W		XXXXXXXX <sub>B</sub>
000089 <sub>H</sub>	TMRD1					XXXXXXXX <sub>B</sub>
00008A <sub>H</sub>	CSVCR	Clock supervisor control register*	R, R/W	—	Clock supervisor	00011100 <sub>B</sub>
00008B <sub>H</sub>	Prohibited area					
00008C <sub>H</sub>	RDR0	Port 0 pull-up resistor setting register	R/W	R/W	Port 0	00000000 <sub>B</sub>
00008D <sub>H</sub>	RDR1	Port 1 pull-up resistor setting register	R/W	R/W	Port 1	00000000 <sub>B</sub>
00008E <sub>H</sub>	RDR2	Port 2 pull-up resistor setting register	R/W	R/W	Port 2	00000000 <sub>B</sub>
00008F <sub>H</sub>	RDR3	Port 3 pull-up resistor setting register	R/W	R/W	Port 3	00000000 <sub>B</sub>
000090 <sub>H</sub> to 00009D <sub>H</sub>	Prohibited area					
00009E <sub>H</sub>	PACSR	Program address detection control status register	R/W	R/W	Address match detection	XXXX0000 <sub>B</sub>
00009F <sub>H</sub>	DIRR	Delayed interrupt cause / clear register	R/W	R/W	Delayed interrupt	XXXXXXXX0 <sub>B</sub>
0000A0 <sub>H</sub>	LPMCR	Low-power consumption mode control register	W, R/W	W, R/W	Low-power consumption control register	00011000 <sub>B</sub>
0000A1 <sub>H</sub>	CKSCR	Clock selection register	R, R/W	R, R/W		11111100 <sub>B</sub>
0000A2 <sub>H</sub> to 0000A7 <sub>H</sub>	Prohibited area					
0000A8 <sub>H</sub>	WDTC	Watchdog timer control register	R, W	R, W	Watchdog timer	XXXXX111 <sub>B</sub>
0000A9 <sub>H</sub>	TBTC	Time-base timer control register	W, R/W	W, R/W	Time-base timer	1XX00100 <sub>B</sub>
0000AA <sub>H</sub> to 0000AD <sub>H</sub>	Prohibited area					
0000AE <sub>H</sub>	FMCS	Flash memory control status register	R, R/W	R, R/W	Flash memory interface circuit	000X0000 <sub>B</sub>
0000AF <sub>H</sub>	Prohibited area					

(Continued)

# MB90820B Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000B0 <sub>H</sub>	ICR00	Interrupt control register 00	R/W	R/W	Interrupt controller	00000111 <sub>B</sub>
0000B1 <sub>H</sub>	ICR01	Interrupt control register 01	R/W	R/W		00000111 <sub>B</sub>
0000B2 <sub>H</sub>	ICR02	Interrupt control register 02	R/W	R/W		00000111 <sub>B</sub>
0000B3 <sub>H</sub>	ICR03	Interrupt control register 03	R/W	R/W		00000111 <sub>B</sub>
0000B4 <sub>H</sub>	ICR04	Interrupt control register 04	R/W	R/W		00000111 <sub>B</sub>
0000B5 <sub>H</sub>	ICR05	Interrupt control register 05	R/W	R/W		00000111 <sub>B</sub>
0000B6 <sub>H</sub>	ICR06	Interrupt control register 06	R/W	R/W	Interrupt controller	00000111 <sub>B</sub>
0000B7 <sub>H</sub>	ICR07	Interrupt control register 07	R/W	R/W		00000111 <sub>B</sub>
0000B8 <sub>H</sub>	ICR08	Interrupt control register 08	R/W	R/W		00000111 <sub>B</sub>
0000B9 <sub>H</sub>	ICR09	Interrupt control register 09	R/W	R/W		00000111 <sub>B</sub>
0000BA <sub>H</sub>	ICR10	Interrupt control register 10	R/W	R/W		00000111 <sub>B</sub>
0000BB <sub>H</sub>	ICR11	Interrupt control register 11	R/W	R/W		00000111 <sub>B</sub>
0000BC <sub>H</sub>	ICR12	Interrupt control register 12	R/W	R/W		00000111 <sub>B</sub>
0000BD <sub>H</sub>	ICR13	Interrupt control register 13	R/W	R/W		00000111 <sub>B</sub>
0000BE <sub>H</sub>	ICR14	Interrupt control register 14	R/W	R/W		00000111 <sub>B</sub>
0000BF <sub>H</sub>	ICR15	Interrupt control register 15	R/W	R/W		00000111 <sub>B</sub>
0000C0 <sub>H</sub>	PWCSL0	PWC control status register ch.0	R/W	R/W	PWC timer (ch.0)	00000000 <sub>B</sub>
0000C1 <sub>H</sub>	PWCSH0		R, R/W	R, R/W		00000000 <sub>B</sub>
0000C2 <sub>H</sub>	PWC0	PWC data buffer register ch.0	—	R/W		XXXXXXXX <sub>B</sub>
0000C3 <sub>H</sub>			—	R/W		XXXXXXXX <sub>B</sub>
0000C4 <sub>H</sub>	DIV0	Divide ratio control register ch.0	R/W	R/W		XXXXXXXX00 <sub>B</sub>
0000C5 <sub>H</sub>	ADER0	A/D input enable register 0	R/W	R/W	Port 6, A/D	11111111 <sub>B</sub>
0000C6 <sub>H</sub>	ADCS0	A/D control status register 0	R/W	R/W	8/10-bit A/D converter	000XXXX0 <sub>B</sub>
0000C7 <sub>H</sub>	ADCS1	A/D control status register 1	W, R/W	W, R/W		0000000X <sub>B</sub>
0000C8 <sub>H</sub>	ADCR0	A/D data register 0	R	R		XXXXXXXX <sub>B</sub>
0000C9 <sub>H</sub>	ADCR1	A/D data register 1	R	R		XXXXXXXX <sub>B</sub>
0000CA <sub>H</sub>	ADSR0	A/D setting register 0	R/W	R/W		00000000 <sub>B</sub>
0000CB <sub>H</sub>	ADSR1	A/D setting register 1	R/W	R/W		00000000 <sub>B</sub>
0000CC <sub>H</sub>	DAT0	D/A data register 0	R/W	R/W		8-bit D/A converter
0000CD <sub>H</sub>	DAT1	D/A data register 1	R/W	R/W	XXXXXXXX <sub>B</sub>	
0000CE <sub>H</sub>	DACR0	D/A control register 0	R/W	R/W	XXXXXXXX0 <sub>B</sub>	
0000CF <sub>H</sub>	DACR1	D/A control register 1	R/W	R/W	XXXXXXXX0 <sub>B</sub>	
0000D0 <sub>H</sub>	ADER1	A/D input enable register 1	R/W	R/W	Port 7, A/D	11111111 <sub>B</sub>
0000D1 <sub>H</sub> to 0000EF <sub>H</sub>	Prohibited area					

(Continued)

# MB90820B Series

(Continued)

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000F0 <sub>H</sub> to 0000FF <sub>H</sub>	External area					
001FF0 <sub>H</sub>	PADRL0	Program address detection register 0 (lower)	R/W	R/W	Address match detection	XXXXXXXX <sub>B</sub>
001FF1 <sub>H</sub>	PADRM0	Program address detection register 0 (middle)	R/W	R/W		XXXXXXXX <sub>B</sub>
001FF2 <sub>H</sub>	PADRH0	Program address detection register 0 (higher)	R/W	R/W	Address match detection	XXXXXXXX <sub>B</sub>
001FF3 <sub>H</sub>	PADRL1	Program address detection register 1 (lower)	R/W	R/W		XXXXXXXX <sub>B</sub>
001FF4 <sub>H</sub>	PADRM1	Program address detection register 1 (middle)	R/W	R/W		XXXXXXXX <sub>B</sub>
001FF5 <sub>H</sub>	PADRH1	Program address detection register 1 (higher)	R/W	R/W		XXXXXXXX <sub>B</sub>

\* : For MB90F828B only. Prohibited for the other products.

- Meaning of abbreviations used for reading and writing
  - R/W: Read and write enabled
  - R : Read-only
  - W : Write-only
- Explanation of initial values
  - 0 : The bit is initialized to "0".
  - 1 : The bit is initialized to "1".
  - X : The initial value of the bit is undefined.

## ■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI <sup>2</sup> OS support	Interrupt vector		Interrupt control register		Priority	
		Number	Address	ICR	Address		
Reset	×	#08	08 <sub>H</sub>	FFFFDC <sub>H</sub>	—	<div style="display: flex; align-items: center; justify-content: center;"> <span style="margin-right: 5px;">High</span> <span style="margin-left: 5px;">Low</span> </div>	
INT9 instruction	×	#09	09 <sub>H</sub>	FFFFD8 <sub>H</sub>	—		
Exception processing	×	#10	0A <sub>H</sub>	FFFFD4 <sub>H</sub>	—		
A/D converter conversion complete	○	#11	0B <sub>H</sub>	FFFFD0 <sub>H</sub>	ICR00		0000B0 <sub>H</sub>
Output compare ch.0 match	○	#12	0C <sub>H</sub>	FFFFCC <sub>H</sub>			
End of measurement by PWC timer ch.0 / PWC timer ch.0 overflow	○	#13	0D <sub>H</sub>	FFFFC8 <sub>H</sub>	ICR01		0000B1 <sub>H</sub>
16-bit PPG timer ch.0	○	#14	0E <sub>H</sub>	FFFFC4 <sub>H</sub>			
Output compare ch.1 match	○	#15	0F <sub>H</sub>	FFFFC0 <sub>H</sub>	ICR02		0000B2 <sub>H</sub>
16-bit PPG timer ch.1	○	#16	10 <sub>H</sub>	FFFFBC <sub>H</sub>			
Output compare ch.2 match	○	#17	11 <sub>H</sub>	FFFFB8 <sub>H</sub>	ICR03		0000B3 <sub>H</sub>
16-bit reload timer ch.1 underflow	○	#18	12 <sub>H</sub>	FFFFB4 <sub>H</sub>			
Output compare ch.3 match	○	#19	13 <sub>H</sub>	FFFFB0 <sub>H</sub>	ICR04		0000B4 <sub>H</sub>
DTP/ext. interrupt ch.0/ch.1 detection	○	#20	14 <sub>H</sub>	FFFFAC <sub>H</sub>			
DTTI	△						
Output compare ch.4 match	○	#21	15 <sub>H</sub>	FFFFA8 <sub>H</sub>	ICR05		0000B5 <sub>H</sub>
DTP/ext. interrupt ch.2/ch.3 detection	○	#22	16 <sub>H</sub>	FFFFA4 <sub>H</sub>			
Output compare ch.5 match	○	#23	17 <sub>H</sub>	FFFFA0 <sub>H</sub>	ICR06		0000B6 <sub>H</sub>
End of measurement by PWC timer ch.1 / PWC timer ch.1 overflow	○	#24	18 <sub>H</sub>	FFFF9C <sub>H</sub>			
DTP/ext. interrupt ch.4 detection	○	#25	19 <sub>H</sub>	FFFF98 <sub>H</sub>	ICR07		0000B7 <sub>H</sub>
DTP/ext. interrupt ch.5 detection	○	#26	1A <sub>H</sub>	FFFF94 <sub>H</sub>			
DTP/ext. interrupt ch.6 detection	○	#27	1B <sub>H</sub>	FFFF90 <sub>H</sub>	ICR08		0000B8 <sub>H</sub>
DTP/ext. interrupt ch.7 detection	○	#28	1C <sub>H</sub>	FFFF8C <sub>H</sub>			
Waveform generator 16-bit timers ch.0/ ch.1/ch.2 underflow	△	#29	1D <sub>H</sub>	FFFF88 <sub>H</sub>	ICR09		0000B9 <sub>H</sub>
16-bit reload timer ch.0 underflow	○	#30	1E <sub>H</sub>	FFFF84 <sub>H</sub>			
16-bit free-run timer zero detect	△	#31	1F <sub>H</sub>	FFFF80 <sub>H</sub>	ICR10		0000BA <sub>H</sub>
16-bit PPG timer ch.2	○	#32	20 <sub>H</sub>	FFFF7C <sub>H</sub>			
Input capture ch.0/ch.1	○	#33	21 <sub>H</sub>	FFFF78 <sub>H</sub>	ICR11		0000BB <sub>H</sub>
16-bit free-run timer compare clear	△	#34	22 <sub>H</sub>	FFFF74 <sub>H</sub>			
Input capture ch.2/ch.3	○	#35	23 <sub>H</sub>	FFFF70 <sub>H</sub>	ICR12		0000BC <sub>H</sub>
Time-base timer	△	#36	24 <sub>H</sub>	FFFF6C <sub>H</sub>			
UART ch.1 receive	◎	#37	25 <sub>H</sub>	FFFF68 <sub>H</sub>	ICR13		0000BD <sub>H</sub>
UART ch.1 send	△	#38	26 <sub>H</sub>	FFFF64 <sub>H</sub>			
UART ch.0 receive	◎	#39	27 <sub>H</sub>	FFFF60 <sub>H</sub>	ICR14		0000BE <sub>H</sub>
UART ch.0 send	△	#40	28 <sub>H</sub>	FFFF5C <sub>H</sub>			
Flash memory status	△	#41	29 <sub>H</sub>	FFFF58 <sub>H</sub>	ICR15		0000BF <sub>H</sub>
Delayed interrupt generator module	△	#42	2A <sub>H</sub>	FFFF54 <sub>H</sub>			

◎ : Can be used and support the EI<sup>2</sup>OS stop request.

○ : Can be used and interrupt request flag is cleared by EI<sup>2</sup>OS interrupt clear signal.

×

△ : Usable when an interrupt cause that shares the ICR is not used.

# MB90820B Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	$AV_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *2
	$AVR$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVR, AVR \geq AV_{SS}$
Input voltage*1	$V_I$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	$V_O$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum clamp current	$I_{CLAMP}$	-2.0	+2.0	mA	*5
Total maximum clamp current	$\Sigma  I_{CLAMP} $	—	20	mA	*5
“L” level maximum output current	$I_{OL}$	—	15	mA	*4
“L” level average output current	$I_{OLAV1}$	—	4	mA	Except for P00 to P07, P82 to P87
	$I_{OLAV2}$	—	12	mA	P00 to P07, P82 to P87
“L” level total maximum output current	$\Sigma I_{OL}$	—	100	mA	
“L” level total average output current	$\Sigma I_{OLAV}$	—	50	mA	
“H” level maximum output current	$I_{OH}$	—	-15	mA	*4
“H” level average output current	$I_{OHAV}$	—	-4	mA	
“H” level total maximum output current	$\Sigma I_{OH}$	—	-100	mA	
“H” level total average output current	$\Sigma I_{OHAV}$	—	-50	mA	
Power consumption	$P_D$	—	430	mW	
Operating temperature	$T_A$	-40	+85	°C	
Storage temperature	$T_{stg}$	-55	+150	°C	

\*1 : This parameter is based on  $V_{SS} = AV_{SS} = 0.0$  V.

\*2 :  $AV_{CC}$  must never exceed  $V_{CC}$  when the power is turned on.

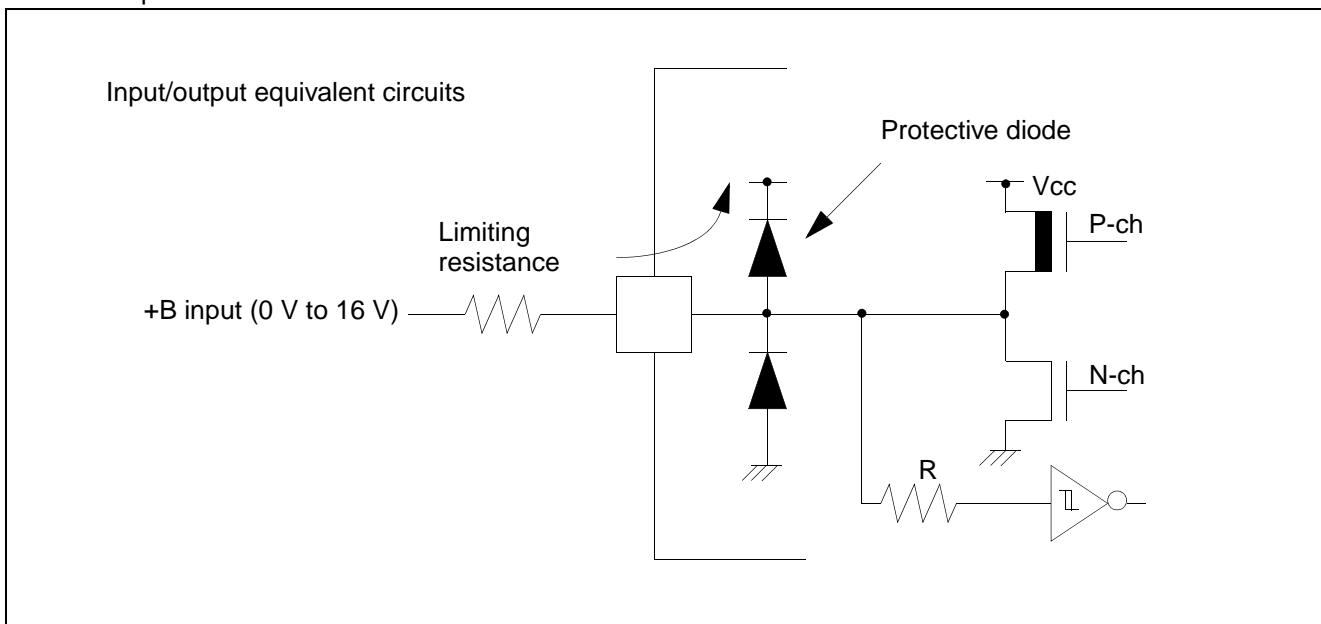
\*3 :  $V_I$  and  $V_O$  must never exceed  $V_{CC} + 0.3$  V. However if the maximum current to/from an input is limited by some means with external components, the  $I_{CLAMP}$  rating supersedes the  $V_I$  rating.

\*4 : The maximum output current is a peak value for a corresponding pin.

(Continued)

(Continued)

- \*5 :
- Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50, P51, P80 to P87.
  - Use within recommended operating conditions.
  - Use at DC voltage (current).
  - The +B signal is an input signal exceeding  $V_{CC}$  voltage. The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
  - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
  - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this may affect other devices.
  - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
  - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
  - Care must be taken not to leave the +B input pin open.
  - Note that analog system input/output pins (LCD drive pins and comparator input pins, etc.) other than the A/D input pins cannot accept +B input.
  - Sample recommended circuits:



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# MB90820B Series

## 2. Recommended Operating Conditions

( $V_{SS} = AV_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply voltage	$V_{CC}$ $AV_{CC}$	—	—	4.5	5.5	V	At normal operation $T_A = -40\text{ °C}$ to $+85\text{ °C}$
		—	—	4.0	5.5	V	Normal operation when D/A converter is not used $T_A = -40\text{ °C}$ to $+85\text{ °C}$
		—	—	3.5	5.5	V	Normal operation when A/D converter and D/A converter are not used $T_A = -40\text{ °C}$ to $+85\text{ °C}$
		—	—	3.0	5.5	V	Maintains state in stop mode
“H” level input voltage	$V_{IH}$	P30 to P37, P60 to P67	$V_{CC} = 5\text{ V}$ $\pm 10\%$	$0.7 V_{CC}$	$V_{CC} + 0.3$	V	CMOS input
	$V_{IHS}$	P00 to P07, P10 to P17, P20 to P27, P40 to P44, P45*1, P46, P47, P50, P51, P70, P71, P72*1, P73 to P77, P80 to P87, $\overline{RST}$		$0.8 V_{CC}$	$V_{CC} + 0.3$	V	CMOS hysteresis input
	$V_{IHM}$	MD0, MD1, MD2		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V	MD input
“L” level input voltage	$V_{IL}$	P30 to P37, P60 to P67	$V_{CC} = 5\text{ V}$ $\pm 10\%$	$V_{SS} - 0.3$	$0.3 V_{CC}$	V	CMOS input
	$V_{ILS}$	P00 to P07, P10 to P17, P20 to P27, P40 to P44, P45*1, P46, P47, P50, P51, P70, P71, P72*1, P73 to P77, P80 to P87, $\overline{RST}$		$V_{SS} - 0.3$	$0.2 V_{CC}$	V	CMOS hysteresis input
	$V_{ILM}$	MD0, MD1, MD2		$V_{SS} - 0.3$	$V_{SS} + 0.3$	V	MD input
Smoothing capacitor	$C_s$	—	—	0.1	1.0	$\mu\text{F}$	*2
Reference input voltage of A/D converter	AVR	—	—	2.7	$AV_{CC}$	V	
Operating temperature	$T_A$	—	—	-40	+85	$^{\circ}\text{C}$	

\*1 : UART ch.0/ch.1 data input pins P45/SIN0, P72/SIN1/AN10 can be used as CMOS input by the communication prescaler control register (CDRR).

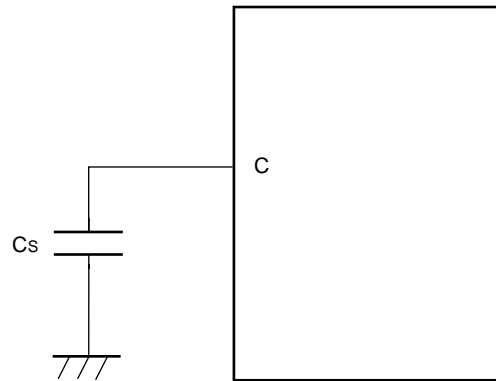
\*2 : Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. On the  $V_{CC}$  pin, connect a bypass capacitor that has a larger capacity than that of  $C_s$ . Refer to the following figure for connection of smoothing capacitor  $C_s$ .

(Continued)



(Continued)

• C pin connection circuit



**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.

Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

# MB90820B Series

## 3. DC Characteristics

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	$V_{OH}$	All output pins	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
"L" level output voltage	$V_{OL1}$	All pins except P00 to P07 P82 to P87	$V_{CC} = 4.5\text{ V}$ , $I_{OL1} = 4.0\text{ mA}$	—	—	0.4	V	
	$V_{OL2}$	P00 to P07 P82 to P87	$V_{CC} = 4.5\text{ V}$ , $I_{OL2} = 12.0\text{ mA}$	—	—	0.4	V	
Input leakage current	$I_{IL}$	All input pins	$V_{CC} = 5.5\text{ V}$ , $V_{SS} < V_I < V_{CC}$	-5	—	+5	$\mu\text{A}$	At pull-up disabled
Pull-up resistance	$R_{UP}$	P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{RST}$	—	25	50	100	$\text{k}\Omega$	MASK ROM product
Pull-down resistance	$R_{DOWN}$	MD2	—	25	50	100	$\text{k}\Omega$	MASK ROM product

(Continued)

# MB90820B Series

(Continued)

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub> = 5.0 V, Internal frequency: 24 MHz, At normal operation	—	35	50	mA	MASK ROM product
			—	45	60	mA	Flash memory product	
			V <sub>CC</sub> = 5.0 V, Internal frequency: 24 MHz, At writing in flash memory	—	60	75	mA	Flash memory product
			V <sub>CC</sub> = 5.0 V, Internal frequency: 24 MHz, At erasing memory	—	65	80	mA	Flash memory product
	I <sub>CCS</sub>		V <sub>CC</sub> = 5.0 V, Internal frequency: 24 MHz, At sleep mode	—	15	25	mA	MASK ROM product
			—	mA			Flash memory product	
	I <sub>CTS</sub>		V <sub>CC</sub> = 5.0 V, Internal frequency: 2 MHz, At main timer mode	—	0.3	0.8	mA	MASK ROM product
			—	mA			Flash memory product	
	I <sub>CTT</sub>		V <sub>CC</sub> = 5.0 V, Internal frequency: 8 MHz, At timer mode, T <sub>A</sub> = +25 °C	—	3	7	mA	MASK ROM product
			—	mA			Flash memory product	
I <sub>CCH</sub>	In stop mode, T <sub>A</sub> = +25 °C	—	5	20	μA	MASK ROM product		
		—			mA	Flash memory product		
Input capacitance	C <sub>IN</sub>	Except AV <sub>CC</sub> , AV <sub>SS</sub> , AVR, C, V <sub>CC</sub> and V <sub>SS</sub>	—	5	15	pF		

\* : The power supply current is regulated with an external clock.

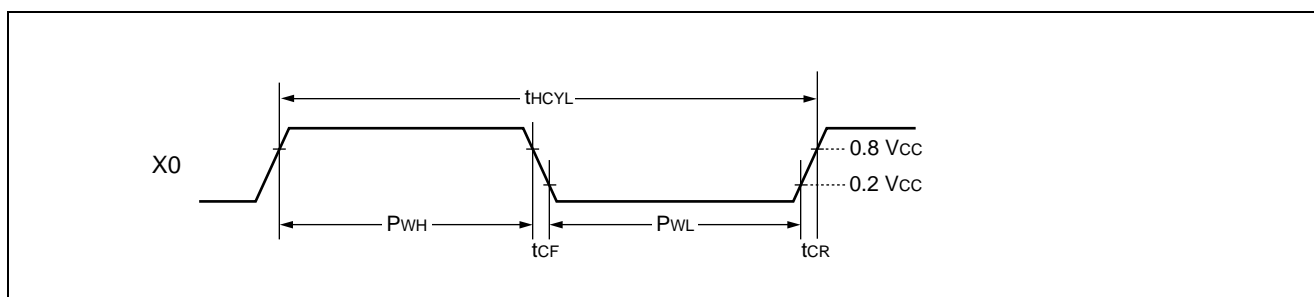
# MB90820B Series

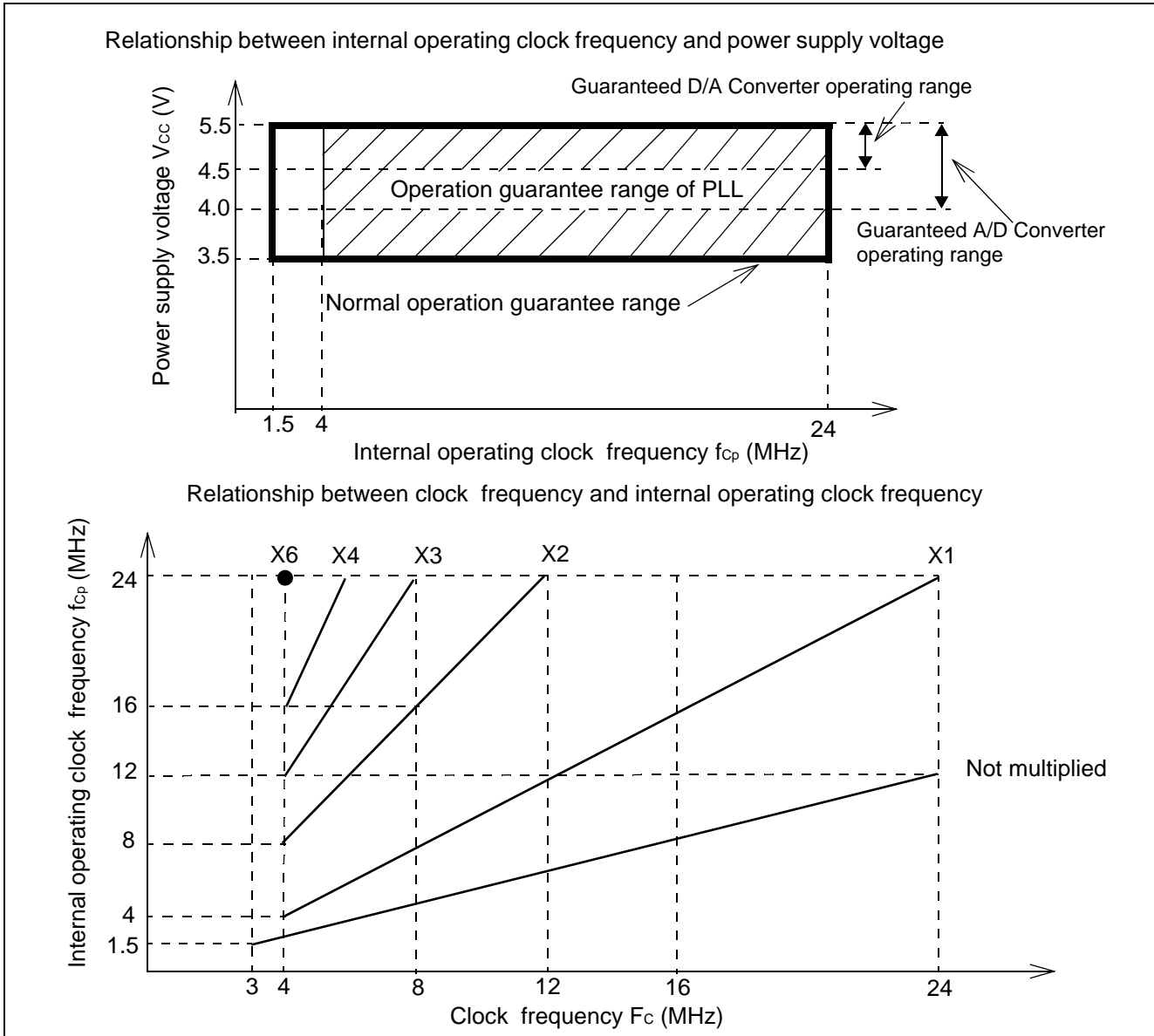
## 4. AC Characteristics

### (1) Clock Timings

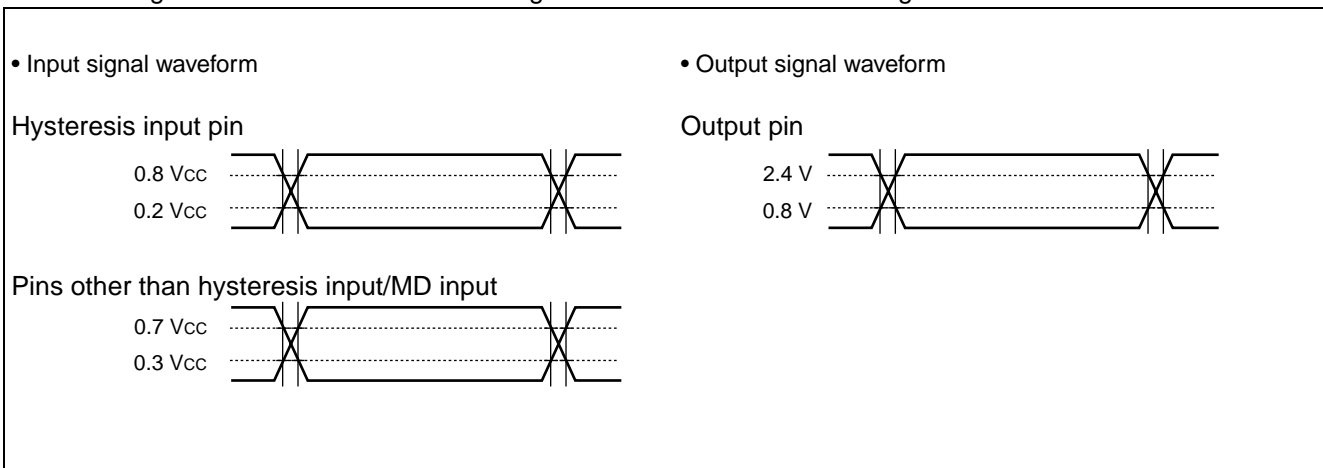
( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0 V$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$F_C$	X0, X1	3	—	16	MHz	When using oscillation circuit
			3	—	24		When using external clock
			4	—	24		1 multiplied PLL
			4	—	12		2 multiplied PLL
			4	—	8		3 multiplied PLL
			4	—	6		4 multiplied PLL
			4	—	4		6 multiplied PLL
Clock cycle time	$t_{HCYL}$	X0, X1	62.5	—	333	ns	When using oscillation circuit
			41.67	—	333	ns	When using external clock
Input clock pulse width	$P_{WH}$ , $P_{WL}$	X0	10	—	—	ns	When using external clock, duty ratio is about 30% to 70%.
Input clock rise/fall time	$t_{CR}$ $t_{CF}$	X0	—	—	5	ns	When using external clock
Internal operating clock frequency	$f_{CP}$	—	1.5	—	24	MHz	
Internal operating clock cycle time	$t_{CP}$	—	41.67	—	666	ns	





The AC ratings are measured for the following measurement reference voltages



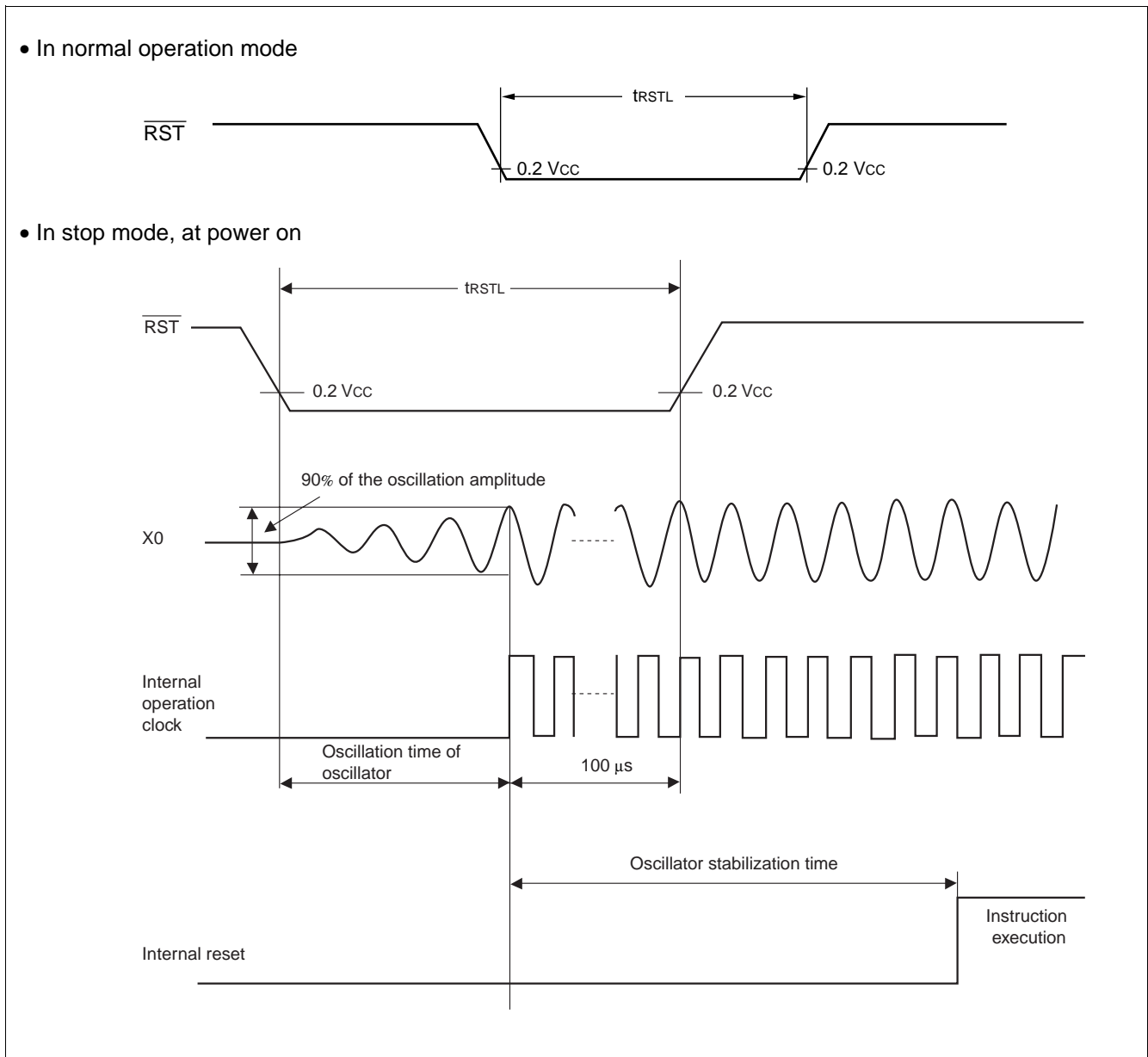
# MB90820B Series

## (2) External Reset

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	$t_{RSTL}$	$\overline{\text{RST}}$	500	—	ns	In normal operation
			Oscillation time of oscillator* + 100	—	$\mu\text{s}$	In stop mode
			100	—	$\mu\text{s}$	In time-base timer mode

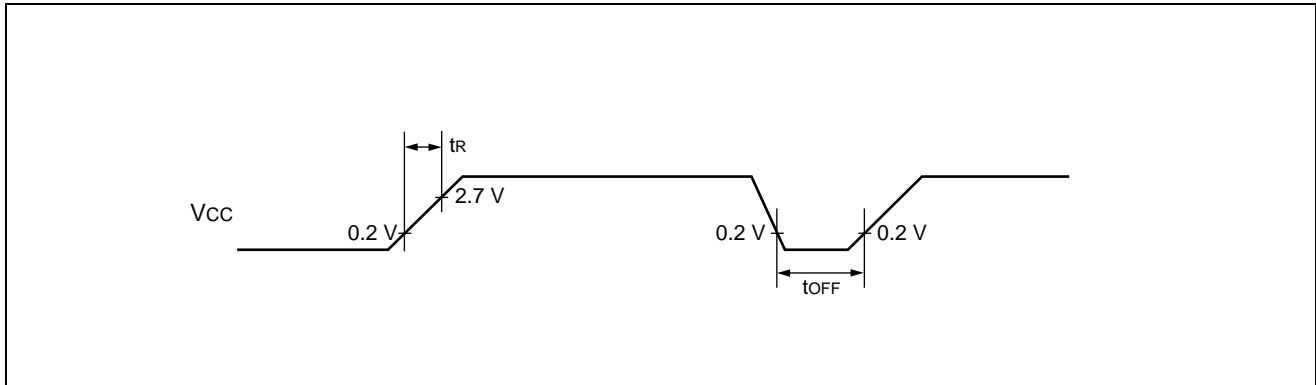
\* : Oscillation time of oscillator is the time to reach to 90% of the oscillation amplitude from stand still. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of  $\mu\text{s}$  to several ms. In the external clock, the oscillation time is 0 ms.



## (3) Power-on Reset

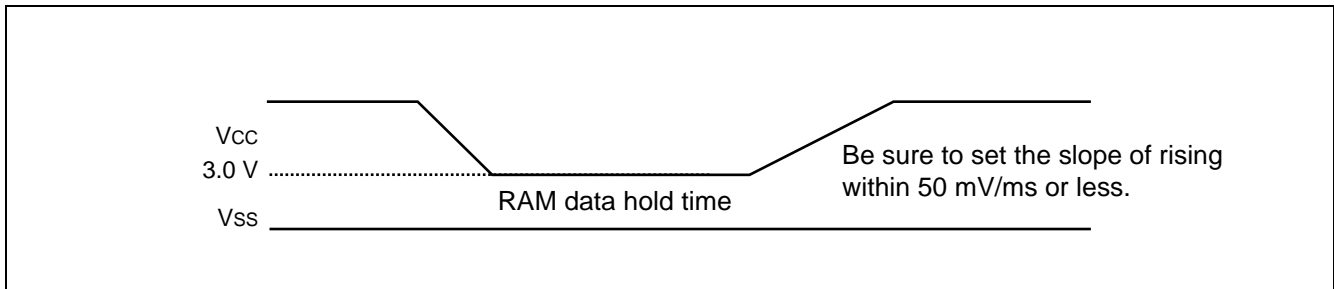
( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	$t_R$	$V_{CC}$	—	0.05	30	ms	
Power supply cut-off time	$t_{OFF}$	$V_{CC}$		1	—	ms	Waiting time for power supply on



Note : Sudden changes in the power supply voltage may cause a power-on reset.

To change the power supply voltage while the device is in operation, be sure to set the slope of rising within 50 mV/ms or less as shown below.



# MB90820B Series

## (4) UART

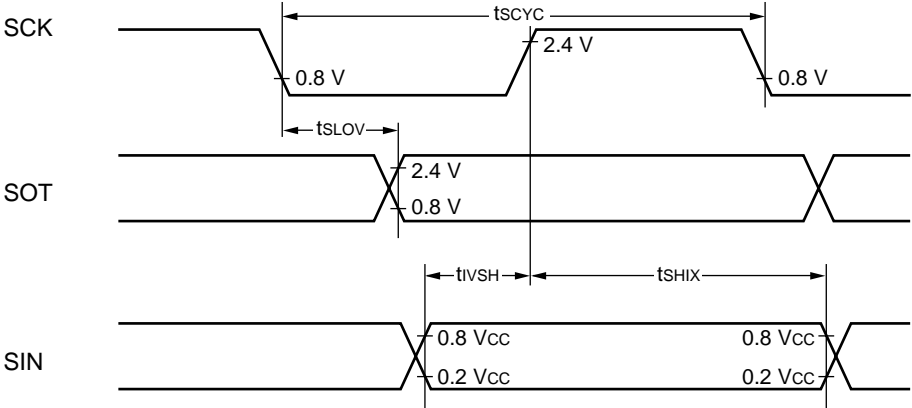
( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0 V$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK0 to SCK1	$C_L = 80\text{ pF} + 1\text{ TTL}$ for an output pin of internal shift clock mode	8 $t_{CP}$	—	ns
SCK ↓ → SOT delay time	$t_{SLOV}$	SCK0 to SCK1 SOT0 to SOT1		-80	+ 80	ns
Valid SIN → SCK ↑	$t_{IVSH}$	SCK0 to SCK1 SIN0 to SIN1		100	—	ns
SCK ↑ → valid SIN hold time	$t_{SHIX}$	SCK0 to SCK1 SIN0 to SIN1		60	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCK0 to SCK1	$C_L = 80\text{ pF} + 1\text{ TTL}$ for an output pin of ex- ternal shift clock mode	4 $t_{CP}$	—	ns
Serial clock "L" pulse width	$t_{LSLH}$	SCK0 to SCK1		4 $t_{CP}$	—	ns
SCK ↓ → SOT delay time	$t_{SLOV}$	SCK0 to SCK1 SOT0 to SOT1		—	150	ns
Valid SIN → SCK ↑	$t_{IVSH}$	SCK0 to SCK1 SIN0 to SIN1		60	—	ns
SCK ↑ → valid SIN hold time	$t_{SHIX}$	SCK0 to SCK1 SIN0 to SIN1		60	—	ns

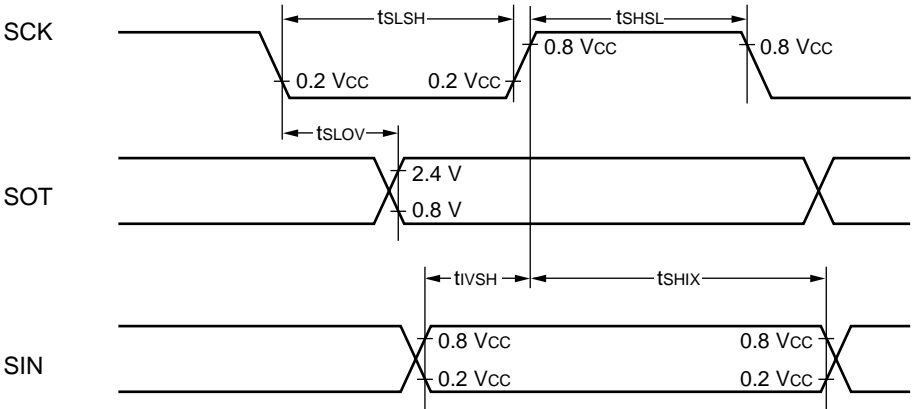
- Notes :
- These are AC ratings in the CLK synchronous mode.
  - $C_L$  is the load capacitance value connected to pins while testing.
  - $t_{CP}$  is machine cycle time (unit : ns).



• Internal shift clock mode



• External shift clock mode



# MB90820B Series

## (5) Resources Input Timing

( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0 V$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

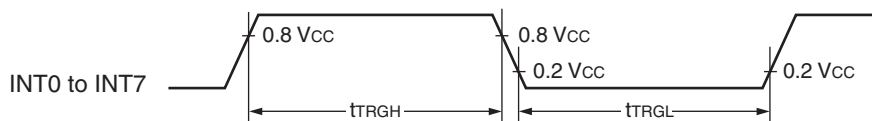
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	$t_{TIWH}$ $t_{TIWL}$	IN0 to IN3, TIN0 to TIN1, PWIO to PWI1, DTTI	—	4 $t_{CP}$	—	ns



## (6) Trigger Input Timing

( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0.0 V$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	$t_{TRGH}$ $t_{TRGL}$	INT0 to INT7	—	5 $t_{CP}$	—	ns



## 5. A/D Converter Electrical Characteristics

( $3.0\text{ V} \leq \text{AVR} - \text{AV}_{\text{SS}}$ ,  $V_{\text{CC}} = \text{AV}_{\text{CC}} = 5.0\text{ V} \pm 10\%$ ,  $V_{\text{SS}} = \text{AV}_{\text{SS}} = 0.0\text{ V}$ ,  $T_{\text{A}} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ )

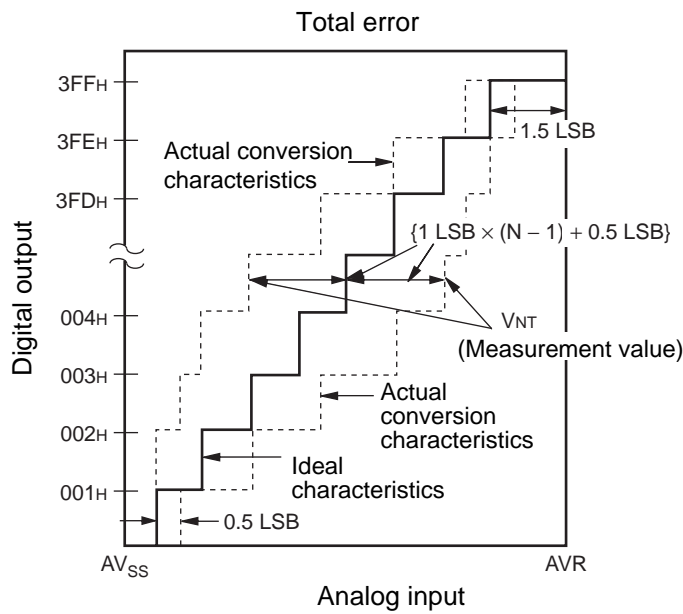
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	10	—	bit	
Total error	—	—		—	—	$\pm 3.0$	LSB	
Non-linearity error	—	—		—	—	$\pm 2.5$	LSB	
Differential linearity error	—	—		—	—	$\pm 1.9$	LSB	
Zero transition voltage	$V_{\text{OT}}$	AN0 to AN15		$\text{AV}_{\text{SS}} - 1.5\text{ LSB}$	$\text{AV}_{\text{SS}} + 0.5\text{ LSB}$	$\text{AV}_{\text{SS}} + 2.5\text{ LSB}$	V	
Full-scale transition voltage	$V_{\text{FST}}$	AN0 to AN15		$\text{AVR} - 3.5\text{ LSB}$	$\text{AVR} - 1.5\text{ LSB}$	$\text{AVR} + 0.5\text{ LSB}$	V	
Compare time	—	—		1.0	—	—	$\mu\text{s}$	$4.5\text{ V} \leq \text{AV}_{\text{CC}} \leq 5.5\text{ V}$
				2.0	—	—	$\mu\text{s}$	$4.0\text{ V} \leq \text{AV}_{\text{CC}} < 4.5\text{ V}$
Sampling time	—	—		0.5	—	—	$\mu\text{s}$	$4.5\text{ V} \leq \text{AV}_{\text{CC}} \leq 5.5\text{ V}$
				1.2	—	—	$\mu\text{s}$	$4.0\text{ V} \leq \text{AV}_{\text{CC}} < 4.5\text{ V}$
Analog port input current	$I_{\text{AIN}}$	AN0 to AN15		-0.3	—	+0.3	$\mu\text{A}$	
Analog input voltage	$V_{\text{AIN}}$	AN0 to AN15		$\text{AV}_{\text{SS}}$	—	AVR	V	
Reference voltage	—	AVR		$\text{AV}_{\text{SS}} + 2.7$	—	$\text{AV}_{\text{CC}}$	V	
Power supply current	$I_{\text{A}}$	$\text{AV}_{\text{CC}}$		—	2.4	4.7	mA	
	$I_{\text{AH}}$			—	—	5	$\mu\text{A}$	*
Reference voltage supply current	$I_{\text{R}}$	AVR		—	600	900	$\mu\text{A}$	
	$I_{\text{RH}}$			—	—	5	$\mu\text{A}$	*
Offset between channels	—	AN0 to AN15	—	—	4	LSB		

\* : The current when the A/D converter is not operating or the CPU is in stop mode (for  $V_{\text{CC}} = \text{AV}_{\text{CC}} = \text{AVR} = 5.0\text{ V}$ )

Note : The error increases proportionally as  $|\text{AVR} - \text{AV}_{\text{SS}}|$  decreases.

## 6. A/D Converter Glossary

- Resolution : Analog variation that is recognized by an A/D converter.
- Non linearity error : Deviation between a line across zero-transition line (“00 0000 0000”↔“00 0000 0001”) and full-scale transition line (“11 1111 1110”↔“11 1111 1111”) and actual conversion characteristics.
- Differential linearity error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value
- Total error : Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$1 \text{ LSB} = (\text{Ideal value}) \frac{AVR - AV_{SS}}{1024} \quad [\text{V}]$$

N : A/D converter digital output value

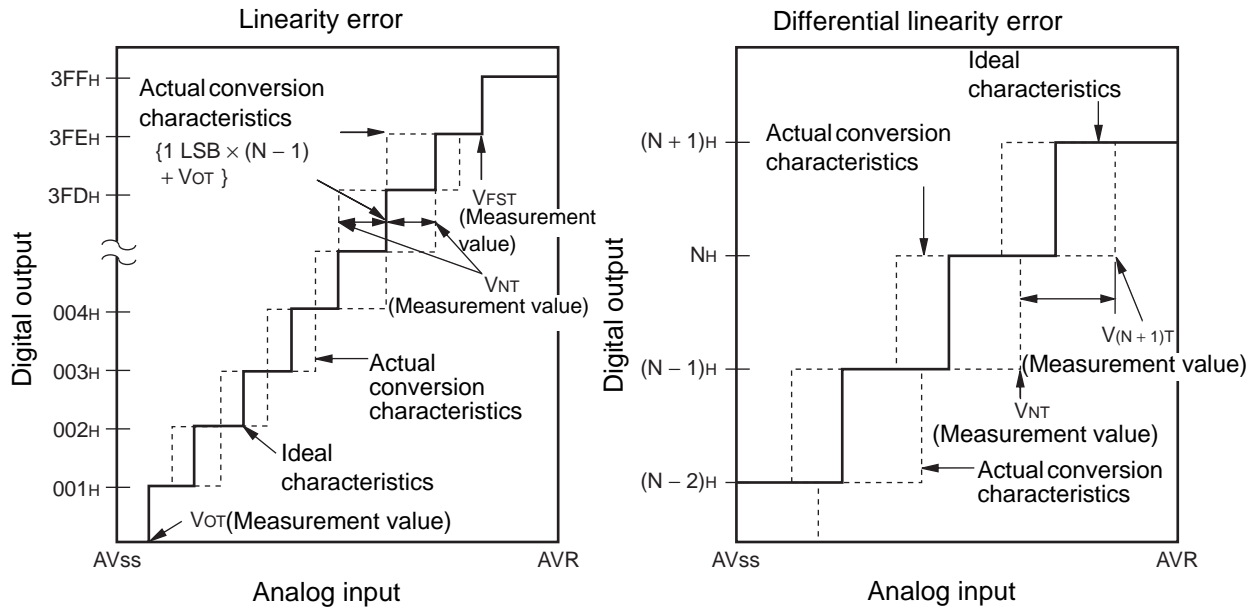
$V_{OT}(\text{Ideal value}) = AV_{SS} + 0.5 \text{ LSB} \quad [\text{V}]$

$V_{FST}(\text{Ideal value}) = AVR - 1.5 \text{ LSB} \quad [\text{V}]$

$V_{NT}$  : Voltage at which of digital output transitions from  $(N - 1)_H$  to  $N_H$ .

(Continued)

(Continued)



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \quad [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

N : A/D converter digital output value

$V_{OT}$  : Voltage at which of digital output transmissions from "000H" to "001H".

$V_{FST}$  : Voltage at which of digital output transmissions from "3FEH" to "3FFH".

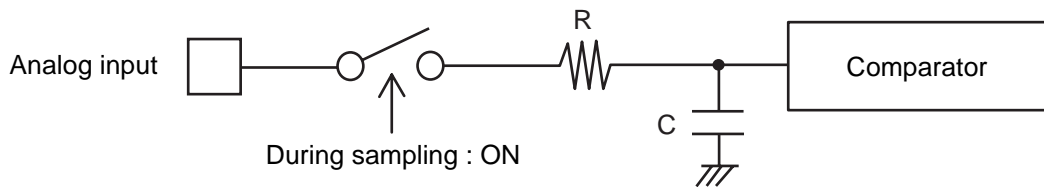
# MB90820B Series

## 7. Notes on Using A/D Converter

### • About the external impedance of the analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. And if the sampling time cannot be sufficient, connect a capacitor of about 0.1  $\mu\text{F}$  to the analog input pin.

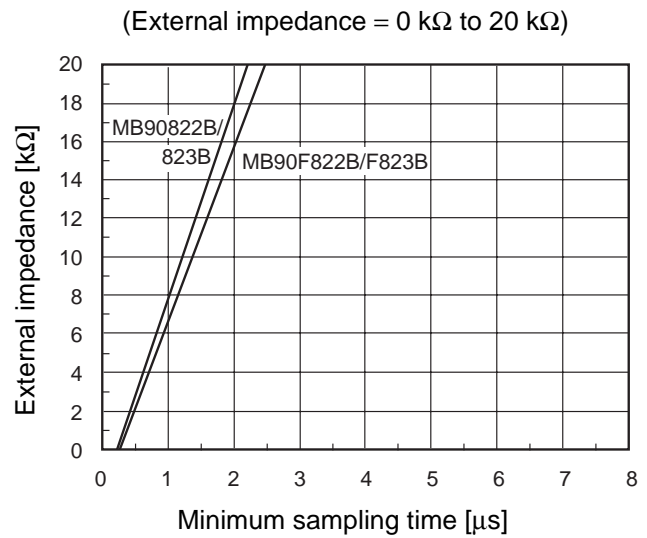
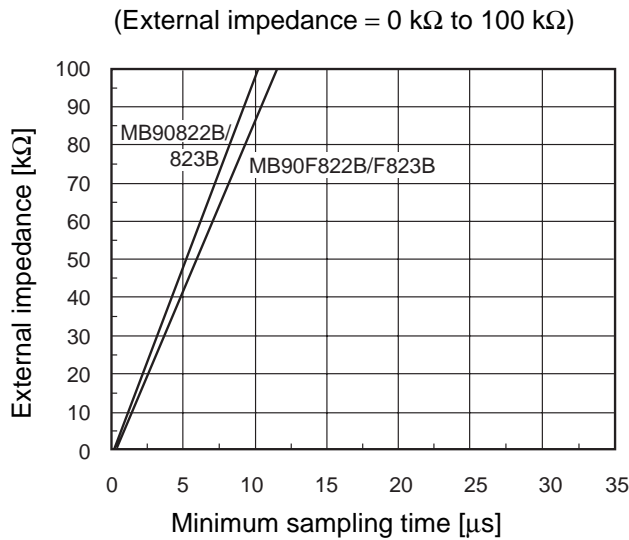
#### • Analog input circuit model



	R	C
MB90822B/823B	2.0 k $\Omega$ (Max)	14.4 pF (Max)
MB90F822B/F823B	2.0 k $\Omega$ (Max)	16.0 pF (Max)

Note : The values are reference values.

#### • The relationship between the external impedance and minimum sampling time



#### • About the error

The accuracy gets worse as  $|AVR - AV_{SS}|$  becomes smaller.

## 8. Electrical Characteristics of D/A convertor

( $V_{CC} = AV_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS} = AV_{SS} = 0.0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	8	—	bit	
Differential linearity error	—	—		—	—	$\pm 0.5$	LSB	
Conversion time	—	—		—	0.45	—	$\mu\text{s}$	*
Analog output impedance	—	—		—	2.9	3.8	$\text{k}\Omega$	
Power supply current	$I_{DVR}$	$AV_{CC}$		—	160	920	$\mu\text{A}$	
	$I_{DVRS}$			—	0.1	—	$\mu\text{A}$	D/A stops

\* : With load capacitance 20 pF.

# MB90820B Series

## 9. Flash Memory Program/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T <sub>A</sub> = +25 °C V <sub>CC</sub> = 5.0 V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16 bit width) programming time		—	16	3,600	μs	Except for the overhead time of the system
Program/Erase cycle	—	10,000	—	—	cycle	
Flash data retention time	Average T <sub>A</sub> = +85 °C	20	—	—	year	*

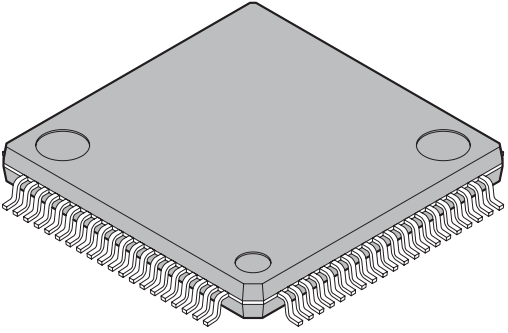
\* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

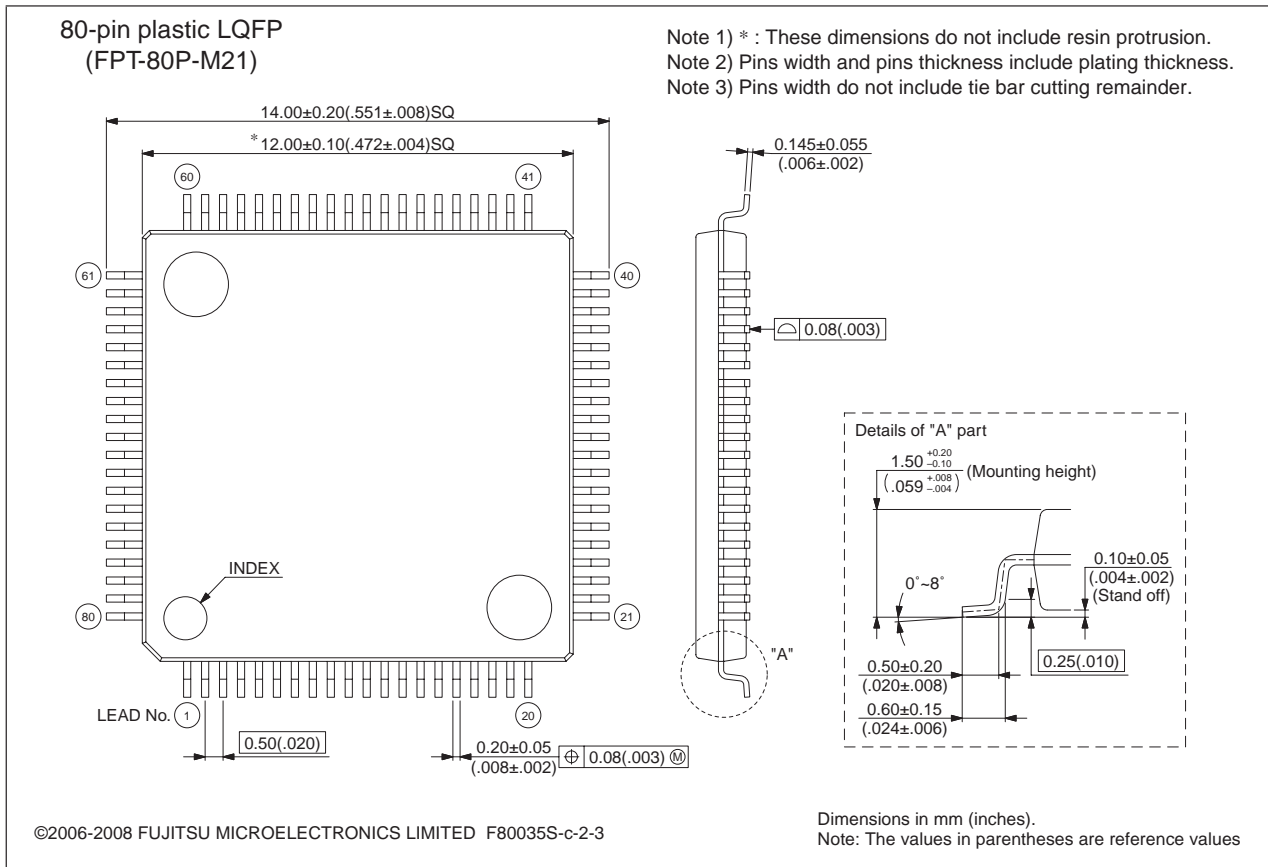
## ■ ORDERING INFORMATION

Part number	Package
MB90F823BPMC MB90F822BPMC MB90822BPMC MB90823BPMC MB90F828BPMC	80-pin plastic LQFP (FPT-80P-M21)
MB90F823BPMC1 MB90F822BPMC1 MB90822BPMC1 MB90823BPMC1 MB90F828BPMC1	80-pin plastic LQFP (FPT-80P-M22)
MB90F823BPF MB90F822BPF MB90822BPF MB90823BPF MB90F828BPF	80-pin plastic QFP (FPT-80P-M06)



## PACKAGE DIMENSIONS

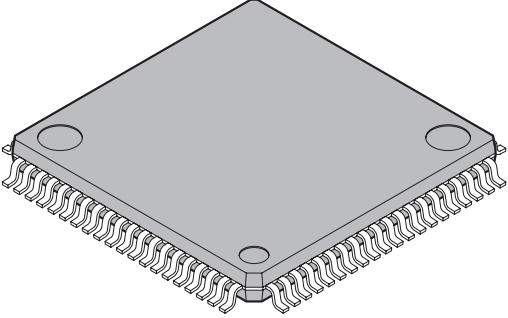
 <p>80-pin plastic LQFP</p> <p>(FPT-80P-M21)</p>	Lead pitch	0.50 mm
	Package width × package length	12 mm × 12 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.47 g
	Code (Reference)	P-LFQFP80-12×12-0.50

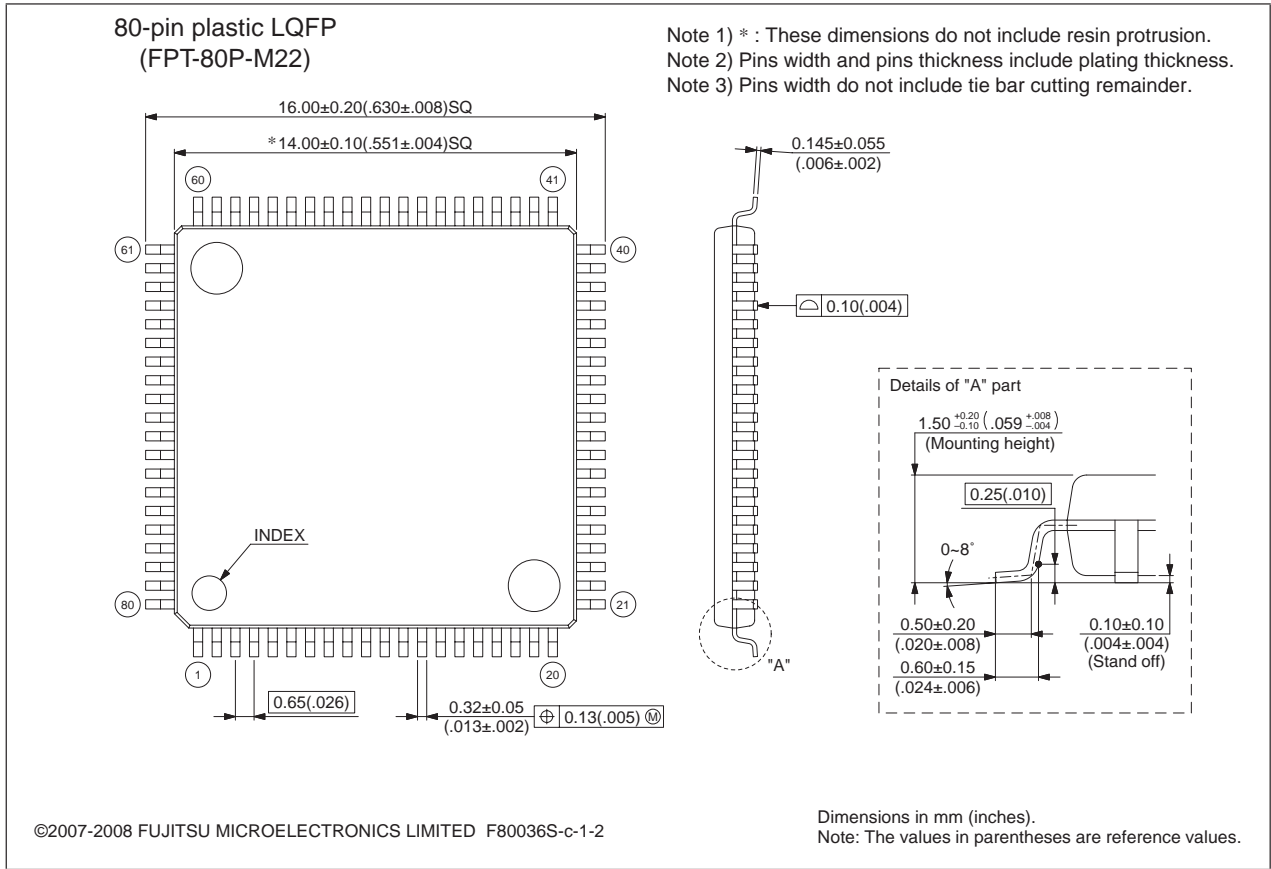


Please confirm the latest Package dimension by following URL.  
<http://edevic.fujitsu.com/package/en-search/>

(Continued)

# MB90820B Series

<p>80-pin plastic LQFP</p>  <p>(FPT-80P-M22)</p>	Lead pitch	0.65 mm
	Package width × package length	14.00 mm × 14.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.62 g
	Code (Reference)	P-LFQFP80-14×14-0.65

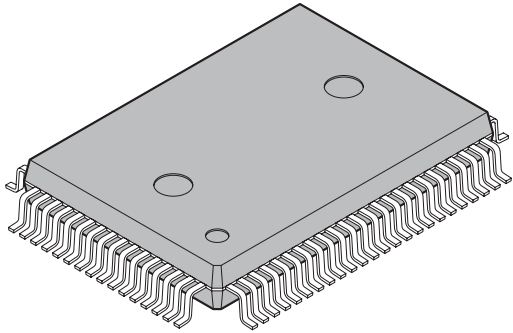


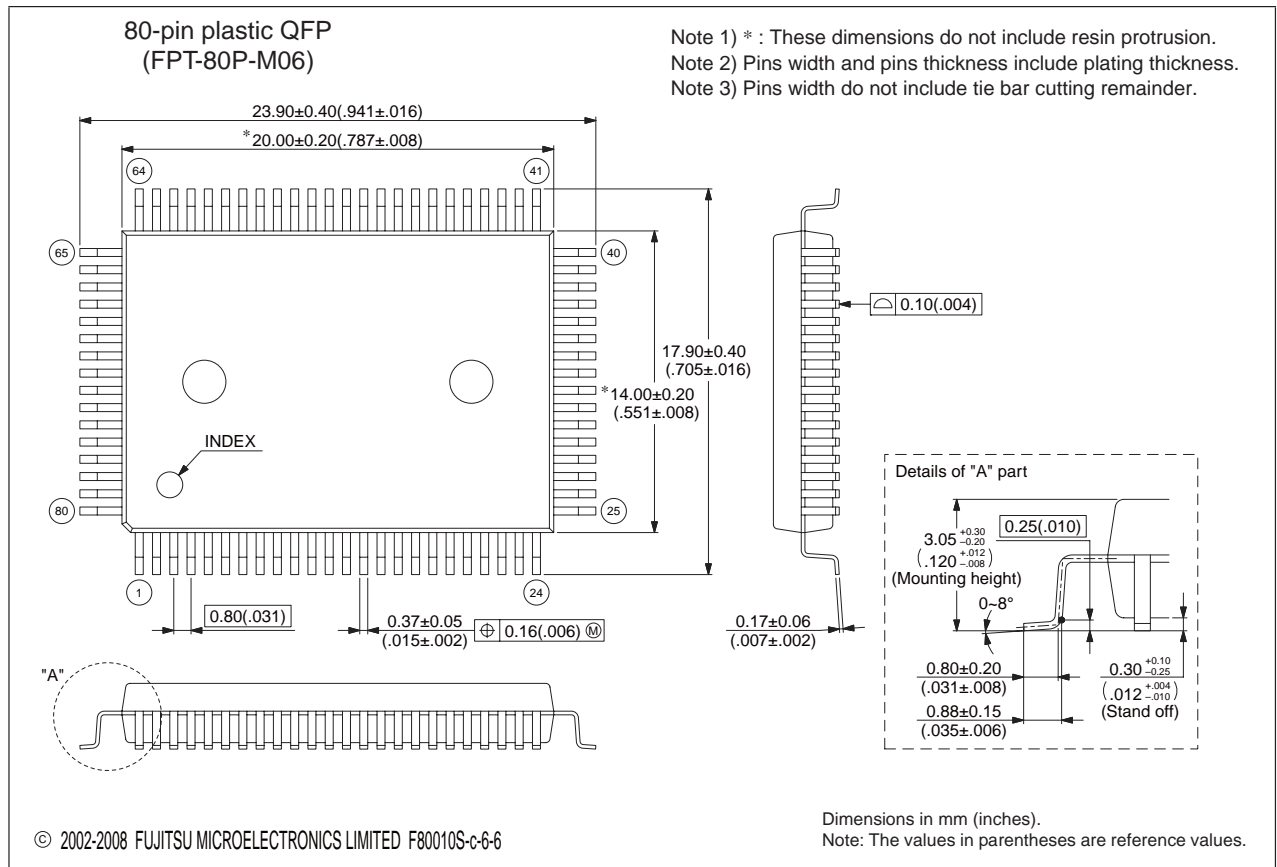
Please confirm the latest Package dimension by following URL.  
<http://edevic.fujitsu.com/package/en-search/>

(Continued)

# MB90820B Series

(Continued)

<p>80-pin plastic QFP</p>  <p>(FPT-80P-M06)</p>	Lead pitch	0.80 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP80-14×20-0.80



Please confirm the latest Package dimension by following URL.  
<http://edevice.fujitsu.com/package/en-search/>

# MB90820B Series

## ■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
4	■ PACKAGE AND CORRESPONDING PRODUCTS	Changed the MB90822B (FPT-80P-M21). X : Not available → ○ : Available
43	■ ELECTRICAL CHARACTERISTICS 5. A/D Converter Electrical Characteristics	Changed the unit of zero transition voltage and full-scale transition voltage. mV → V
48	■ ORDERING INFORMATION	Added the part number. MB90822BPMC MB90823BPMC

The vertical lines marked in the left side of the page show the changes.

**MEMO**

**MEMO**

**MEMO**

# MB90820B Series

## FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg. 7-1, Nishishinjuku 2-chome, Shinjuku-ku,  
Tokyo 163-0722, Japan Tel: +81-3-5322-3347 Fax: +81-3-5322-3387  
<http://jp.fujitsu.com/fml/en/>

*For further information please contact:*

### North and South America

FUJITSU MICROELECTRONICS AMERICA, INC.  
1250 E. Arques Avenue, M/S 333  
Sunnyvale, CA 94085-5401, U.S.A.  
Tel: +1-408-737-5600 Fax: +1-408-737-5999  
<http://www.fma.fujitsu.com/>

### Europe

FUJITSU MICROELECTRONICS EUROPE GmbH  
Pittlerstrasse 47, 63225 Langen,  
Germany  
Tel: +49-6103-690-0 Fax: +49-6103-690-122  
<http://emea.fujitsu.com/microelectronics/>

### Korea

FUJITSU MICROELECTRONICS KOREA LTD.  
206 KOSMO TOWER, 1002 Daechi-Dong,  
Kangnam-Gu, Seoul 135-280  
Korea  
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111  
<http://www.fmk.fujitsu.com/>

### Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LTD.  
151 Lorong Chuan, #05-08 New Tech Park,  
Singapore 556741  
Tel: +65-6281-0770 Fax: +65-6281-0220  
<http://www.fujitsu.com/sg/services/micro/semiconductor/>

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.  
Rm.3102, Bund Center, No.222 Yan An Road(E),  
Shanghai 200002, China  
Tel: +86-21-6335-1560 Fax: +86-21-6335-1605  
<http://cn.fujitsu.com/fmc/>

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.  
10/F., World Commerce Centre, 11 Canton Road  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: +852-2377-0226 Fax: +852-2376-3269  
<http://cn.fujitsu.com/fmc/tw>

All Rights Reserved.

The contents of this document are subject to change without notice.

Customers are advised to consult with sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of FUJITSU MICROELECTRONICS device; FUJITSU MICROELECTRONICS does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information.

FUJITSU MICROELECTRONICS assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of FUJITSU MICROELECTRONICS or any third party or does FUJITSU MICROELECTRONICS warrant non-infringement of any third-party's intellectual property right or other right by using such information. FUJITSU MICROELECTRONICS assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that FUJITSU MICROELECTRONICS will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.

The company names and brand names herein are the trademarks or registered trademarks of their respective owners.